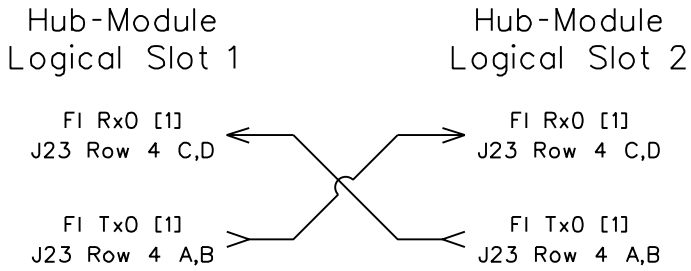
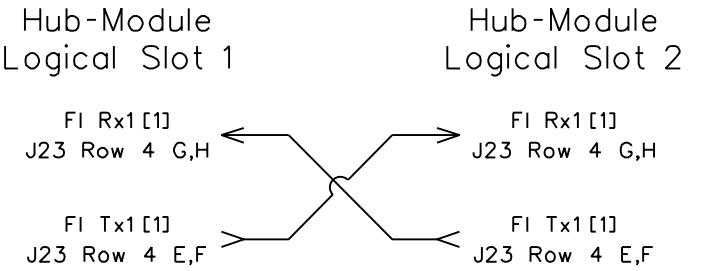
Hub-Module to Hub-Module Backplane Connections

40.08 MHz LHC Clock Links



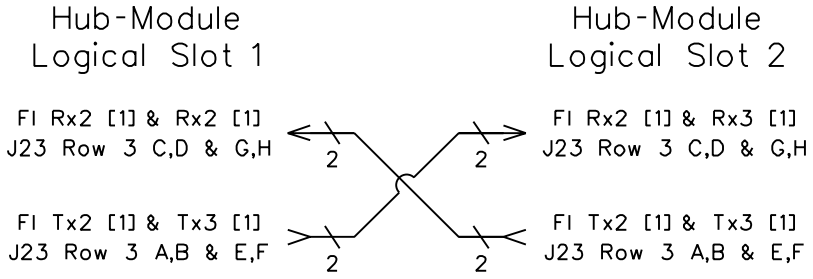
These links start in dedicated clock hardware.
These links end at an LVDS Select I/O input on FPGA.
The Hub-2 to Hub-1 link is typically not used.

Combined TTC + RO Control Links



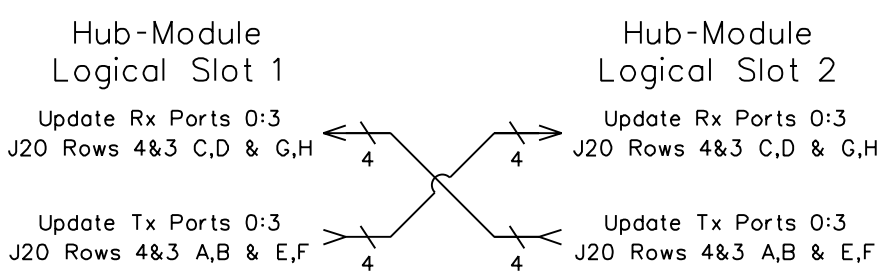
These links start and end in Virtex MGT Transceivers.
The Hub-2 to Hub-1 link typically carries only Hub-2
RO Control information back to Hub-1 for distribution.

Links that Carry the Hub's Readout Data



These links start from a Hub FPGA MGT Transmitter.
These links run to the Other Hub's FEX Data Fanout.

10/100/1000 Base-T Ethernet Links



All of these links start at the Hub's Ethernet Switch "B" Port 5
and end at the Hub's FPGA Phys Chip U21.
The normal Hub-to-Hub Base Interface Channel 2 is not used.

Hub-1 and Hub-2 PCBs are exactly the same. Hub-1 and Hub-2 do have some Firmware differences.