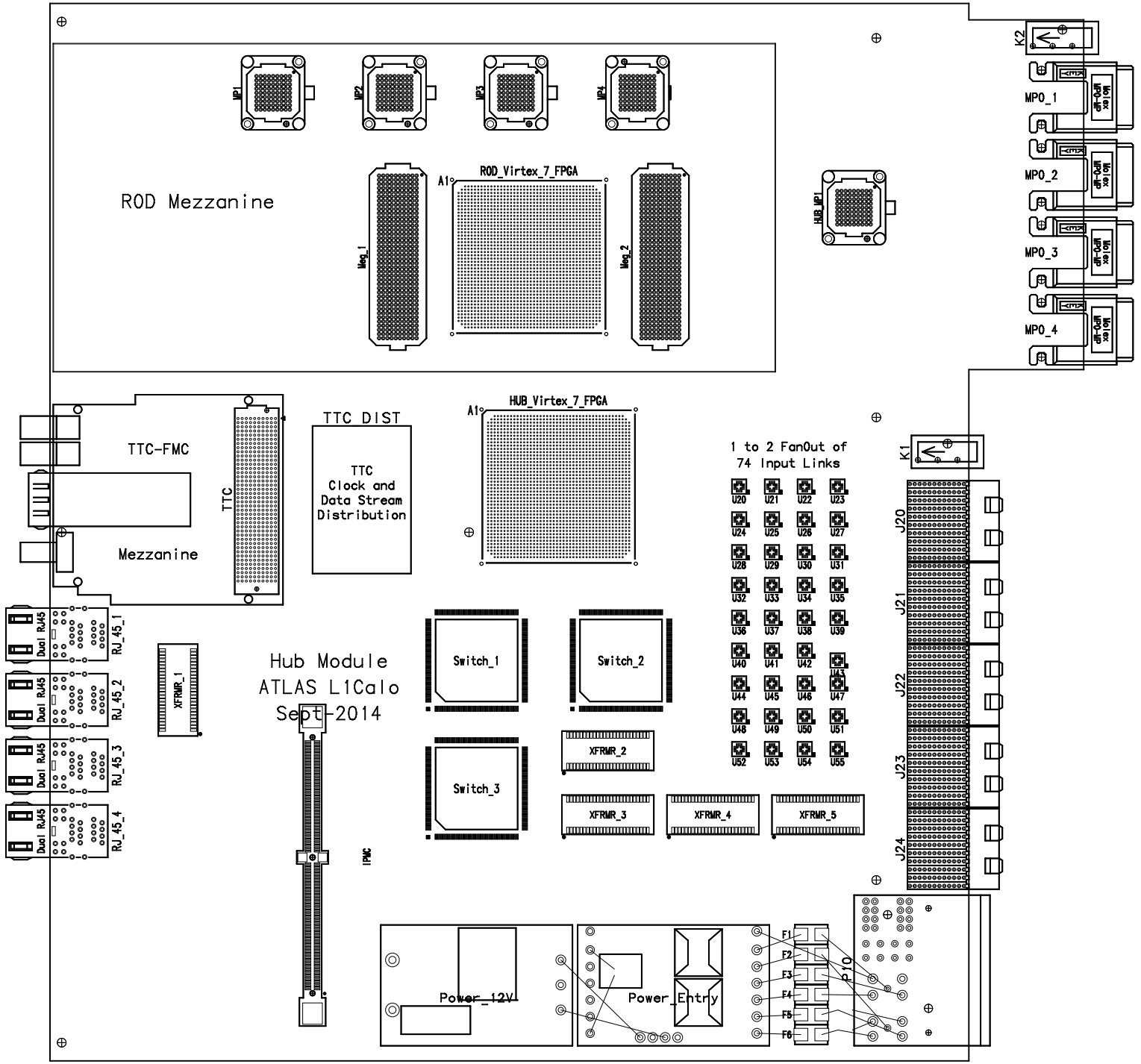
ROD Mezzanine
MP1
MP2
MP3
MP4
ROD_Virtex_7_FPGA
A1
Mez_1
Mez_2
HUB_MP1
K2
MPO_1
MPO_2
MPO_3
MPO_4
TTC-FMC
Mezzanine
TTC
TTC DIST
TTC
Clock and
Data Stream
Distribution
HUB_Virtex_7_FPGA
A1
1 to 2 FanOut of
74 Input Links
K1
J20
J21
J22
J23
J24
Dual RJ45
RJ_45_1
RJ_45_2
RJ_45_3
RJ_45_4
XFRMR_1
Hub Module
ATLAS L1Calo
Sept-2014
Switch_1
Switch_2
Switch_3
XFRMR_2
XFRMR_3
XFRMR_4
XFRMR_5
IPMC
Power_12V
Power_Entry
P10
F1
F2
F3
F4
F5
F6