



ROD Mezzanine

ROD_Virtex_7_FPGA

HUB_Virtex_7_FPGA

TTC DIST

TTC
Clock and
Data Stream
Distribution

TTC-FMC

Mezzanine

Hub Module
ATLAS L1Calo
Sept-2014

Switch_1

Switch_2

Switch_3

XFRMR_2

XFRMR_3

XFRMR_4

XFRMR_5

Power_12V

Power_Entry

1 to 2 FanOut of
74 Input Links

- U20 U21 U22 U23
- U24 U25 U26 U27
- U28 U29 U30 U31
- U32 U33 U34 U35
- U36 U37 U38 U39
- U40 U41 U42 U43
- U44 U45 U46 U47
- U48 U49 U50 U51
- U52 U53 U54 U55

XFRMR_1

- Dual RJ45 RJ_45_1
- Dual RJ45 RJ_45_2
- Dual RJ45 RJ_45_3
- Dual RJ45 RJ_45_4

- MPO_1
- MPO_2
- MPO_3
- MPO_4

- J20
- J21
- J22
- J23
- J24

- F1
- F2
- F3
- F4
- F5
- F6

HUB_IP1

K2

K1

Mezz_1

Mezz_2

A1

A1

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IPMC