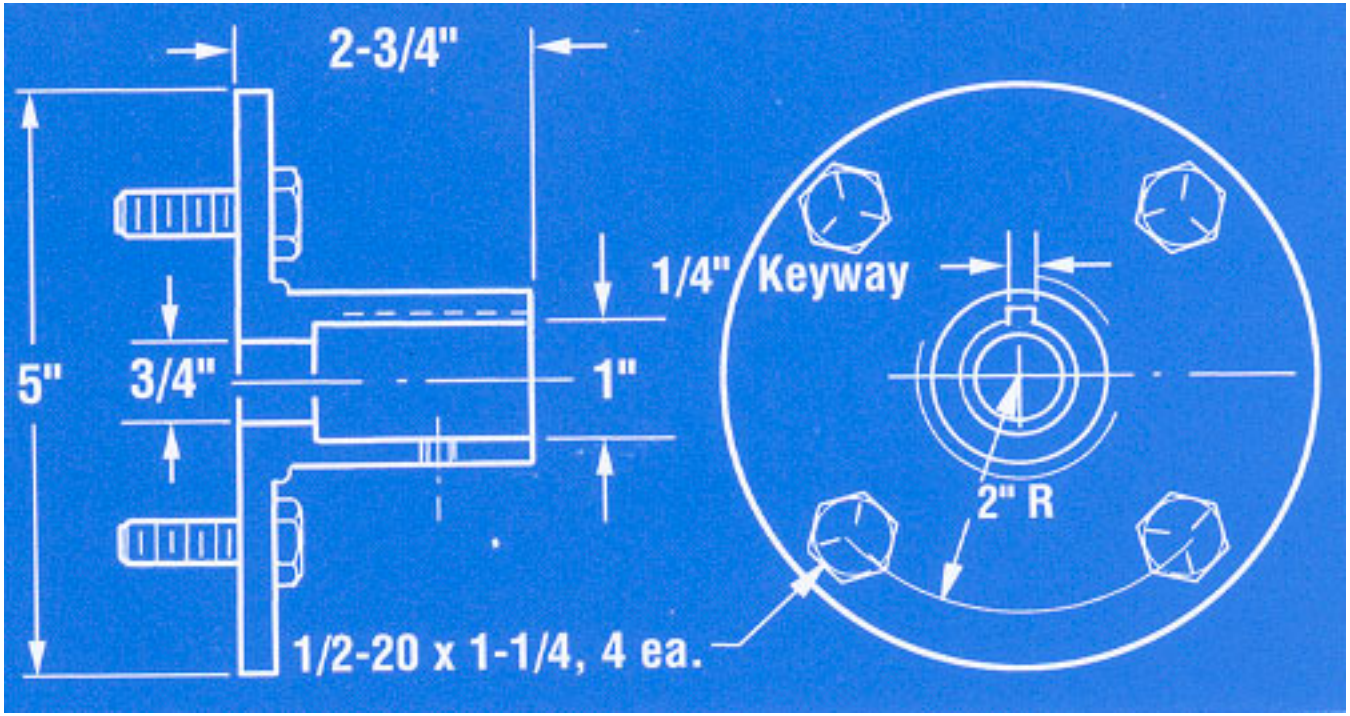
FEX Hub Module Update



Wade Fisher
for the MSU team

20 May 2014

MICHIGAN STATE UNIVERSITY

Outline

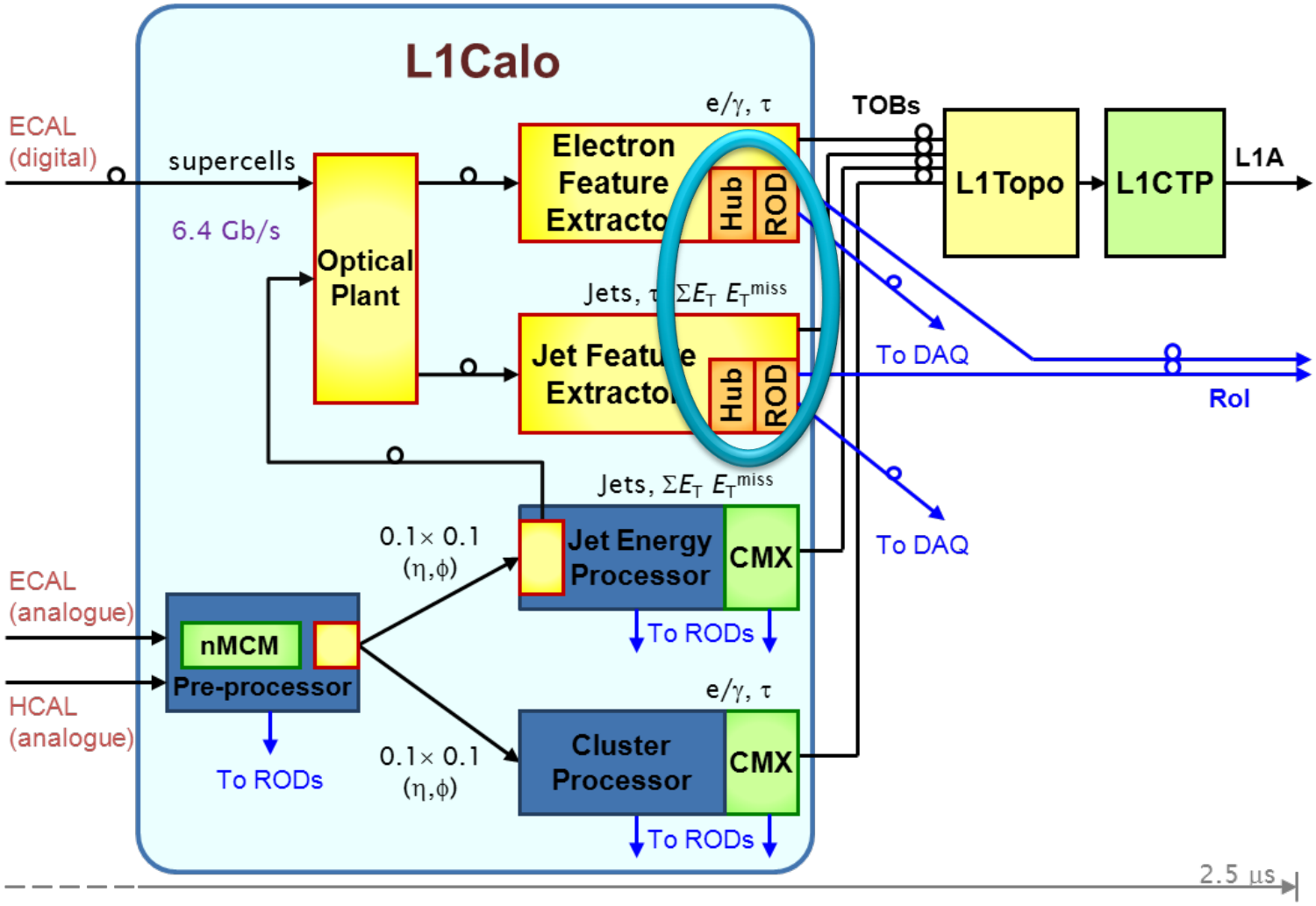
- Overview of FEX ATCA hub module project
- Hub module technical overview
  - Physical Interfaces: Rack space & ATCA shelf
  - Functional design of Hub module
- Areas of primary design challenge and/or questions
  - Interface to ROD Mezzanine
  - FEX->ROD data path & volume
  - Main FPGA choice and utilization
  - Ethernet implementation

Project Personnel

- Primary design team:
  - Dan Edmunds, Philippe Laurens, Yuri Ermoline
  - Much work/input from David Sankey
  - Maker of spreadsheets & powerpoints: Wade Fisher

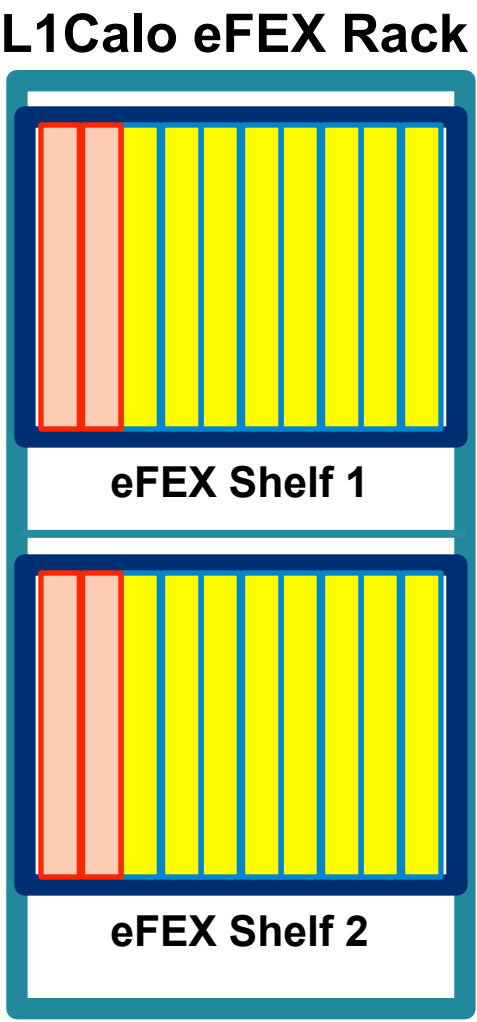
- Input from interfacing systems (so far)
  - eFEX: Ian Brawn and Weiming Qian
  - jFEX: Uli Schaefer
  - gFEX: Helio Takai
  - ROD: Maurice Goodrick
  - FTM: Richard Staley

Level 1 trigger in Phase 1



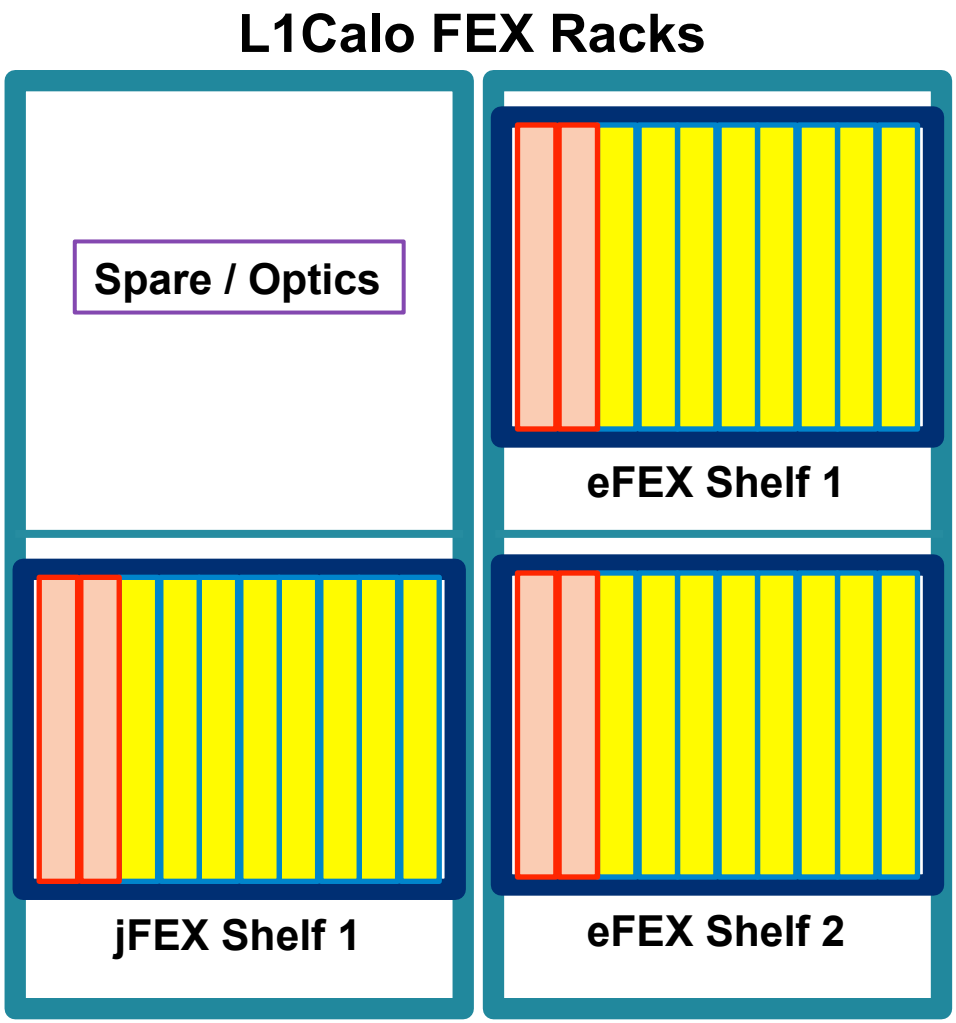
FEX ATCA Hub

- ATCA Hub is a core FEX system component
  - Supports common communication tasks: readout, TTC, networking, monitoring, DCS, busy aggregation, etc.
- Technical Motivations
  - Concentration of common functions on the Hub rather than on the FEX modules makes the FEX system:
    - Less costly
    - Simpler & more efficient
    - Easier to maintain
  - Phase-II upgrade could create single points of failure
    - Move all likely Phase-II targets off the FEX boards
    - Hub module provides a flexible platform to "future-proof" FEX system.

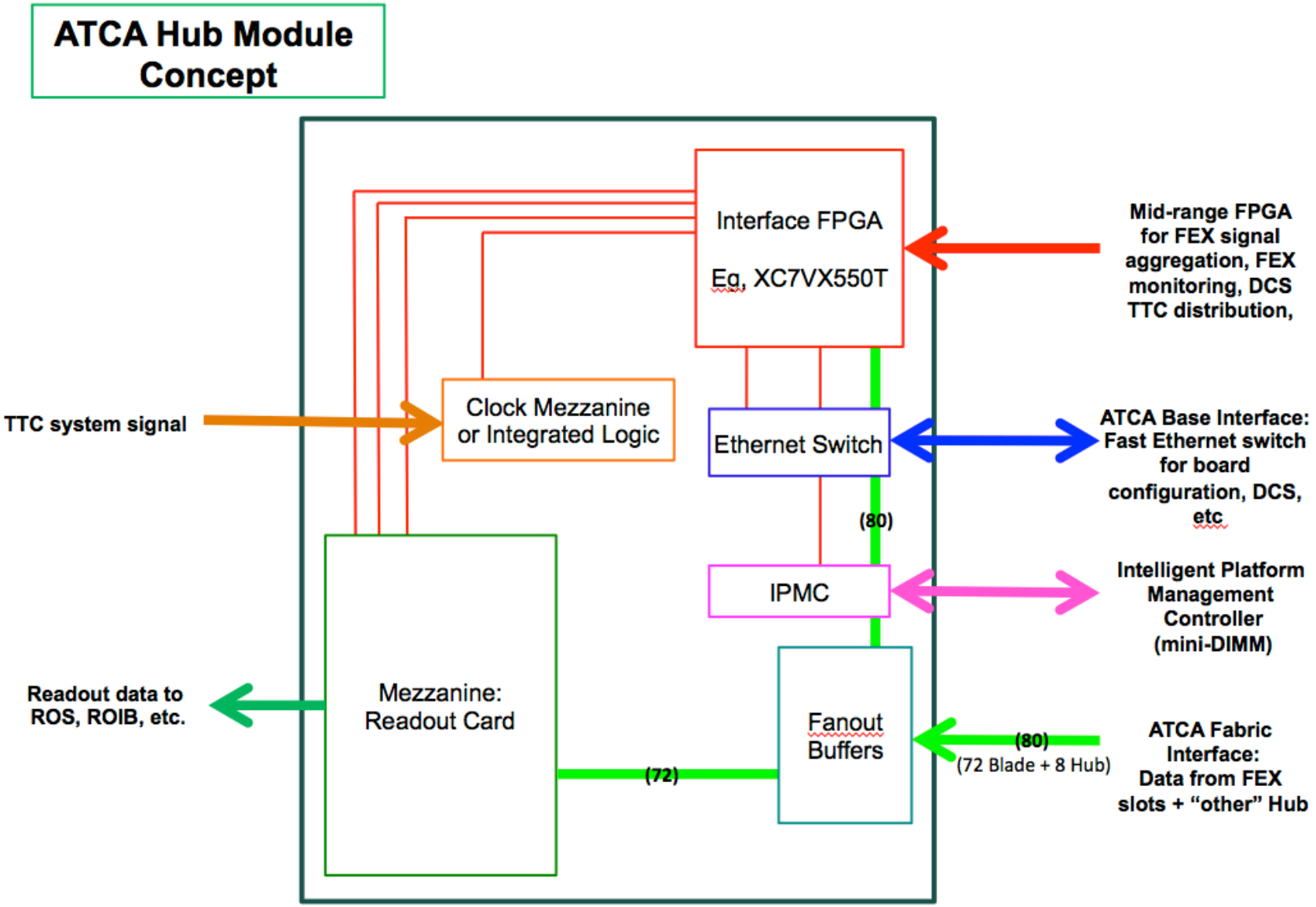


L1Calo Rack Layout

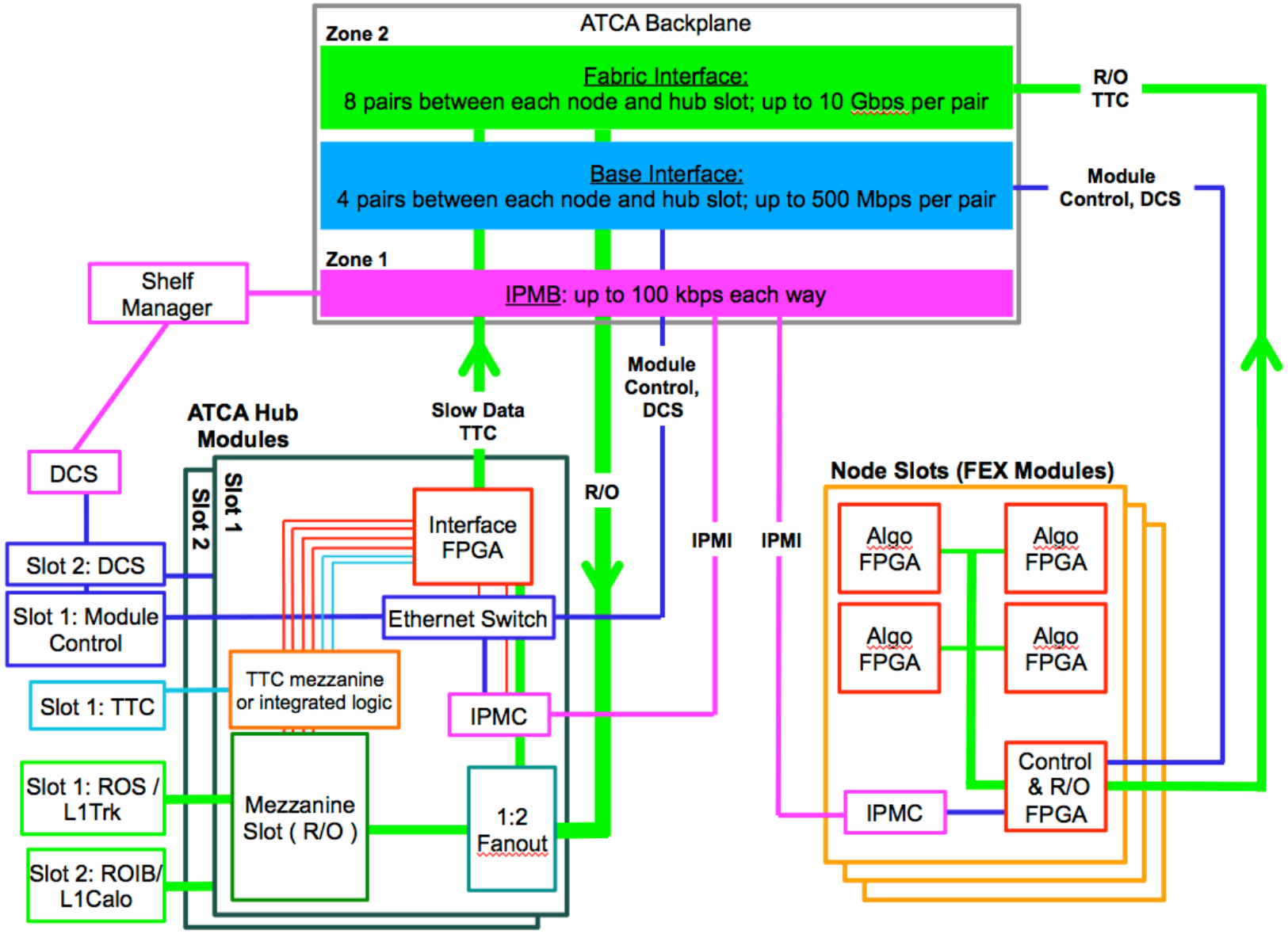
- There will be 3 ATCA shelves for the FEX system
- ~10 FEX boards per ATCA shelf
  - 7-8 for jFEX
  - 12 for eFEX (x2 shelves)
- ATCA shelf has two hub slots
  - L1Calo backplane is dual-star, so each Hub has point-to-point connections to all blades (and to the other Hub)



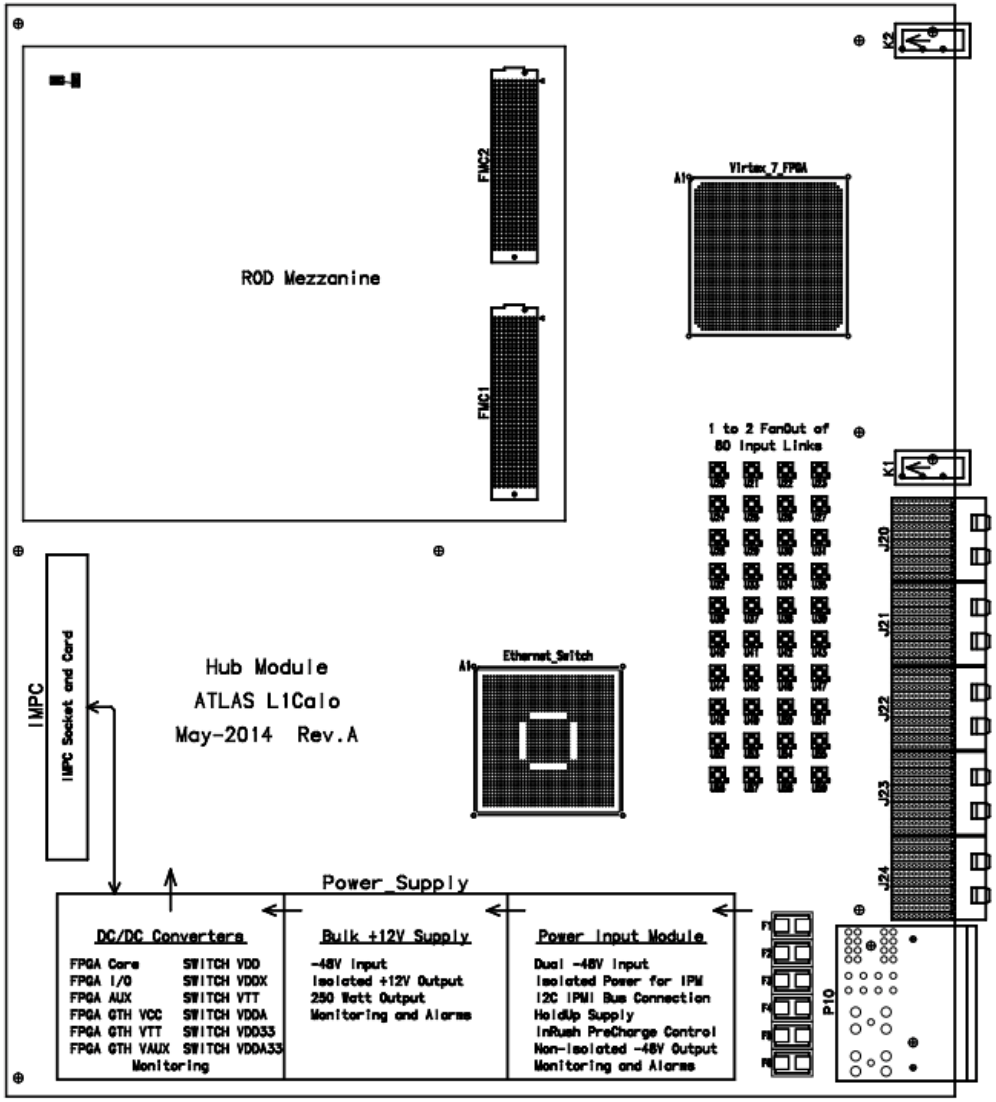
ATCA Hub Modular Design



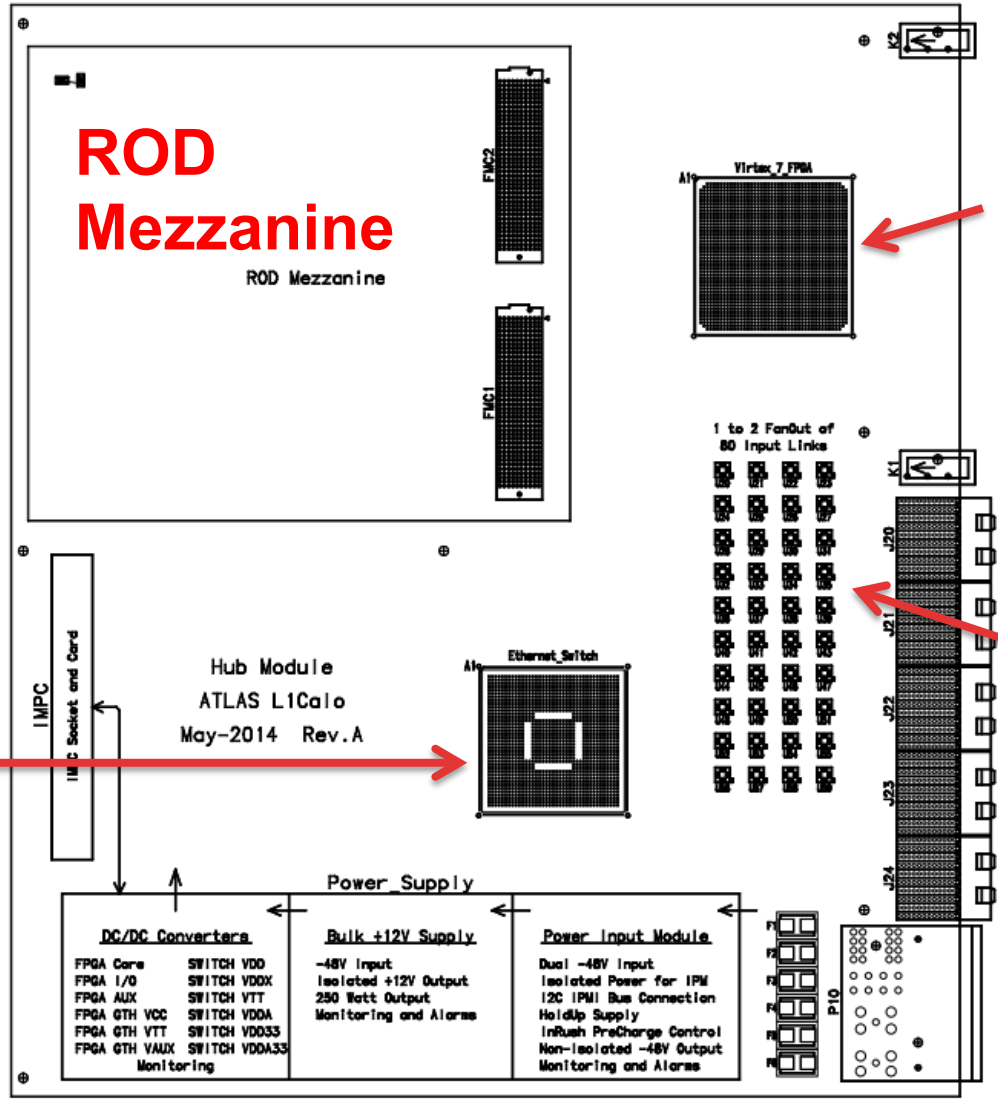
ATCA Hub Modular Design



ATCA Hub Preliminary Drawing



ATCA Hub Preliminary Drawing

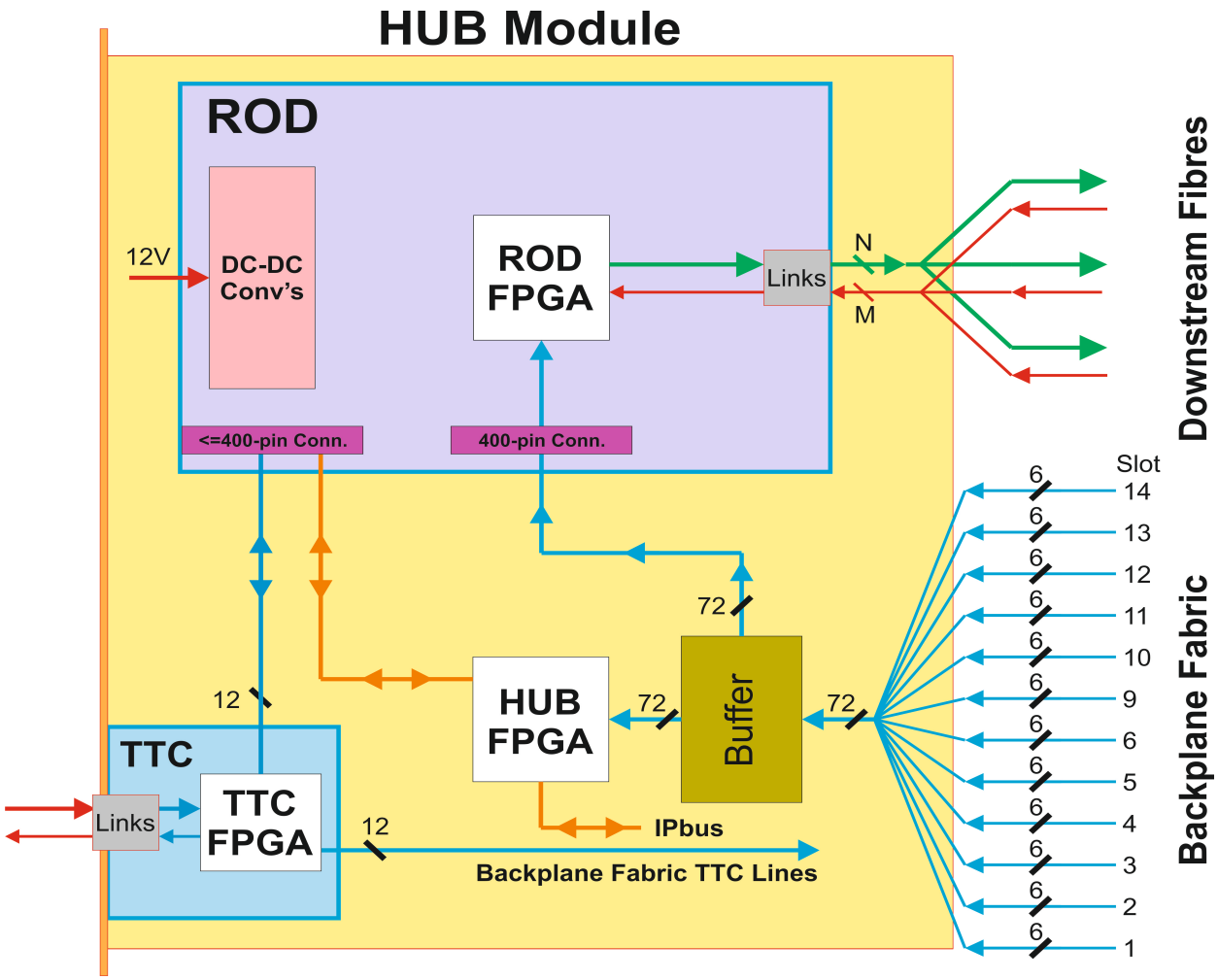


7-Series FPGA

Fabric Interface Fanout x2 (80 total)

Ethernet IC

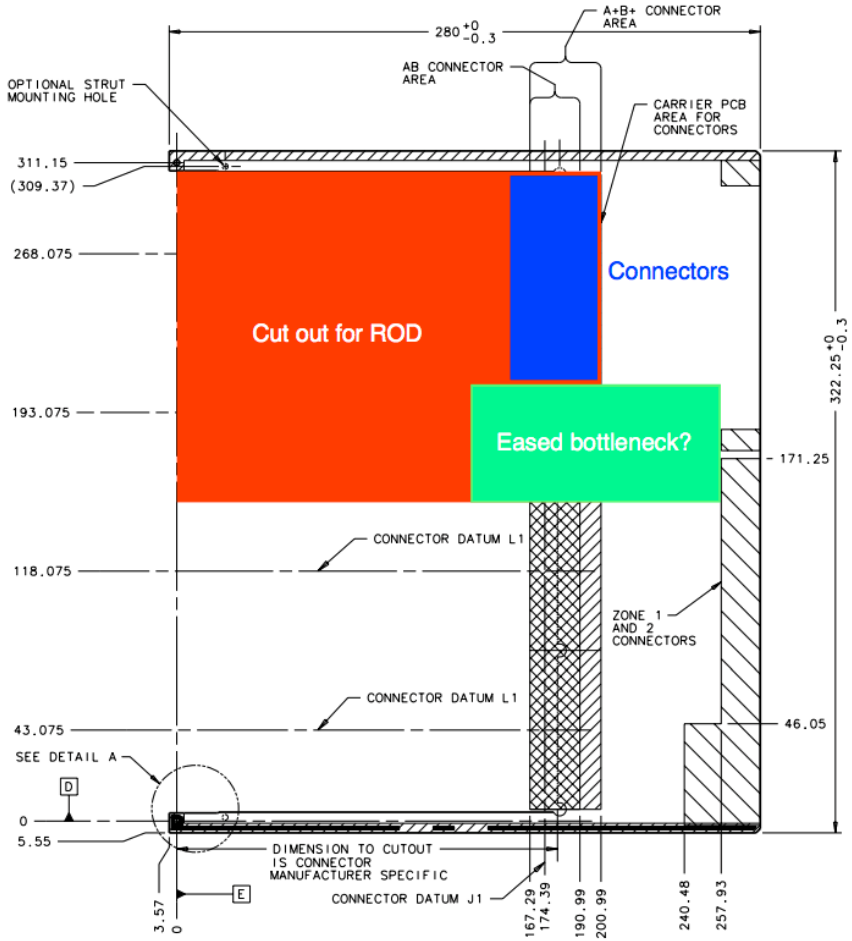
ROD Interface (1)



From the preliminary ROD specification

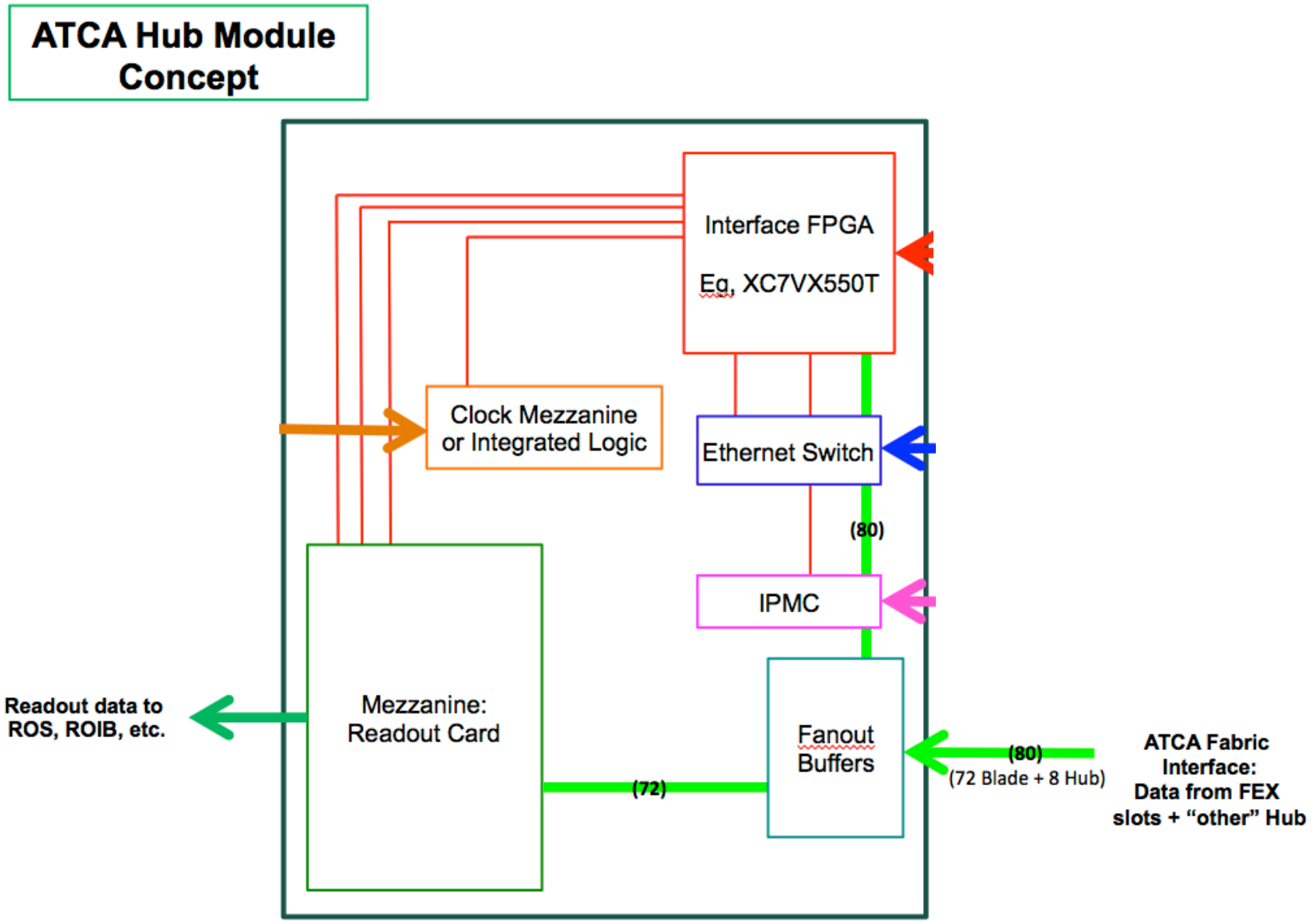
- Two 400 pin FMC connectors for data/power/etc

ROD Interface (2)



From David Sankey, using microTCA connectors

FEX-ROD Data Flow (1)



FEX-ROD Data Flow (2)

Data	No. Chan.	Bits / Chan. / BC (post 8b/10b)	BC / Event	Trigger Rate / KHz	Bandwidth / Gb/s
Input from ECAL	160	160	3	50	3.84
Input from HCAL	72	160	3	50	1.73
XTOBs	160	80	3	500	19.20
TOBs	2	160	3	500	0.48
Total					**25.25**

435 **Table 1. An estimate of the maximum readout bandwidth required for the eFEX. For**
436 **XTOBs, a channel equals an XTOB; for the other types of data, a channel equals a fibre.**

Extracted from the eFEX specification (*Ian says it's outlived its usefulness*)

- Calibrated to Run-4 at 500 kHz
- Assuming FEX input data is read out in 10% of events
- Translates to 6.3125 Gbps maximum rate
- 1 MHz trigger rate could be an issue

FEX-ROD Data Flow (3)

Requirements on differential fanout buffers

- Need 72 buffers for ROD data (Hub-only traffic doesn't need a copy)
- 10 Gbps max rate (ATCA backplane spec?)?
- Need to find an economical solution
  - Quick search for 10 Gbps: 1:2 ~$40/chip, 1:4 ~ $6/chip

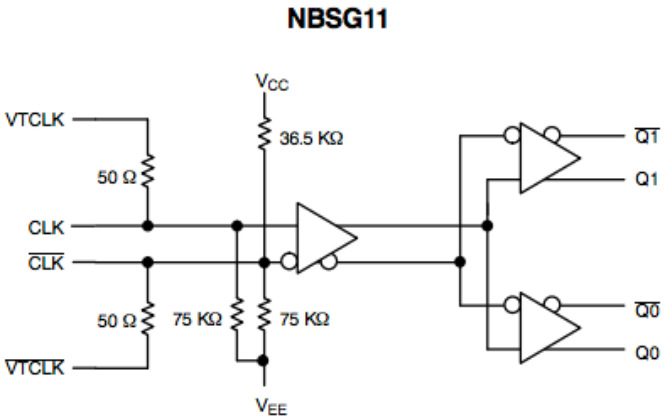


Figure 3. Logic Diagram

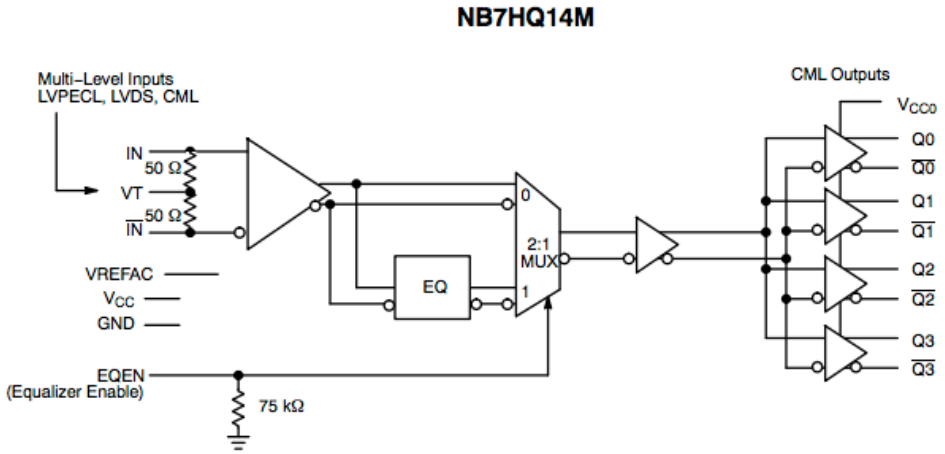


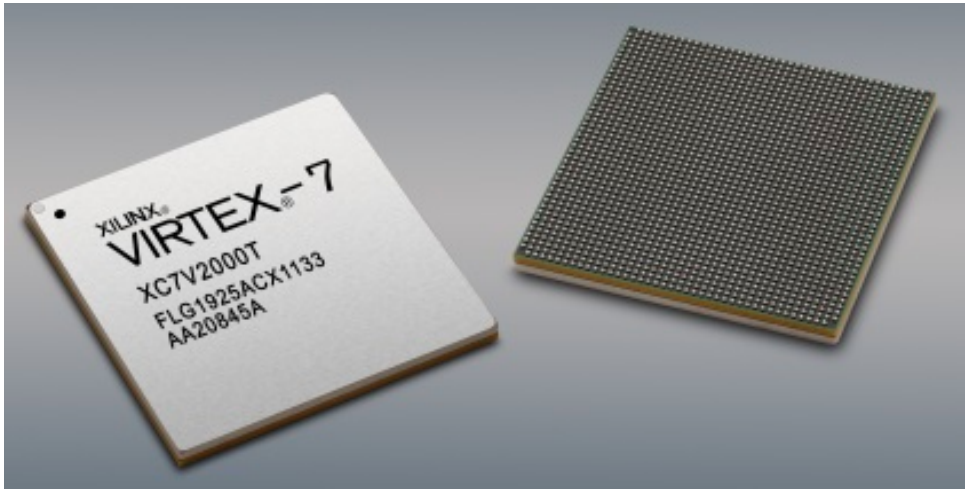
Figure 1. Detailed Block Diagram of NB7HQ14M

Main FPGA (1)

Requirements:

- 80 MGTs to allow a copy of 72 FEX data lines + up to 8 from the other hub slot
  - In the 7-series, this limits us to the XC7VX550T or XC7VX690T.

- Question: Are there sufficient resources to provide all board management?

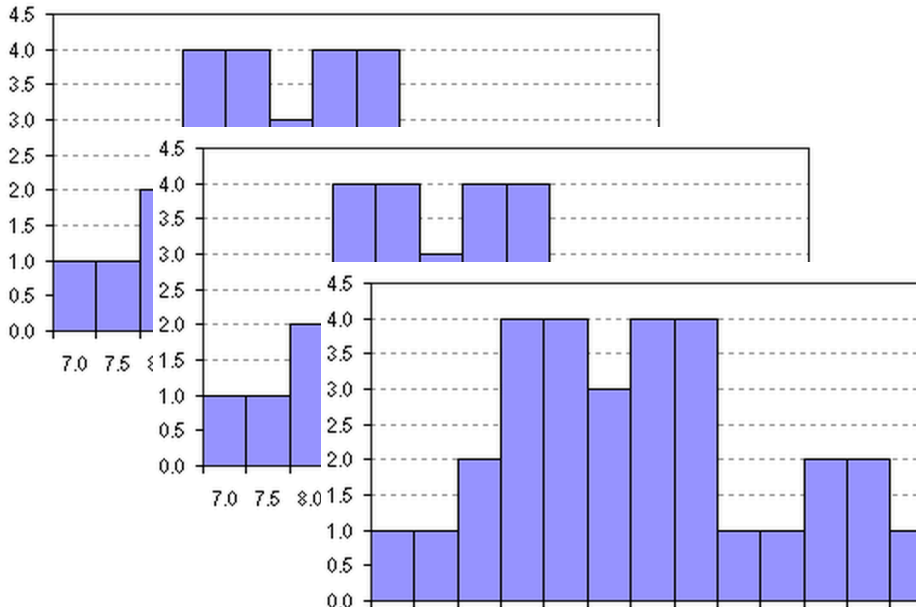


Main FPGA (2)

Thinking ahead a bit:

- We are planning to access ROD data after the fan-out
  - Nominal plan is to make some simple histograms or other monitoring feature.
  - Readout via Ethernet

- Is this readout path sufficient in the future?
  - Investigate adding lines to the ROD from the Hub FPGA



Ethernet

Requirements:

- 14 FEX + 1 Hub ports + 1 Shelf Manager = 16
  - +1 for each ROD = +2
  - +1 for each IPMC? = +2

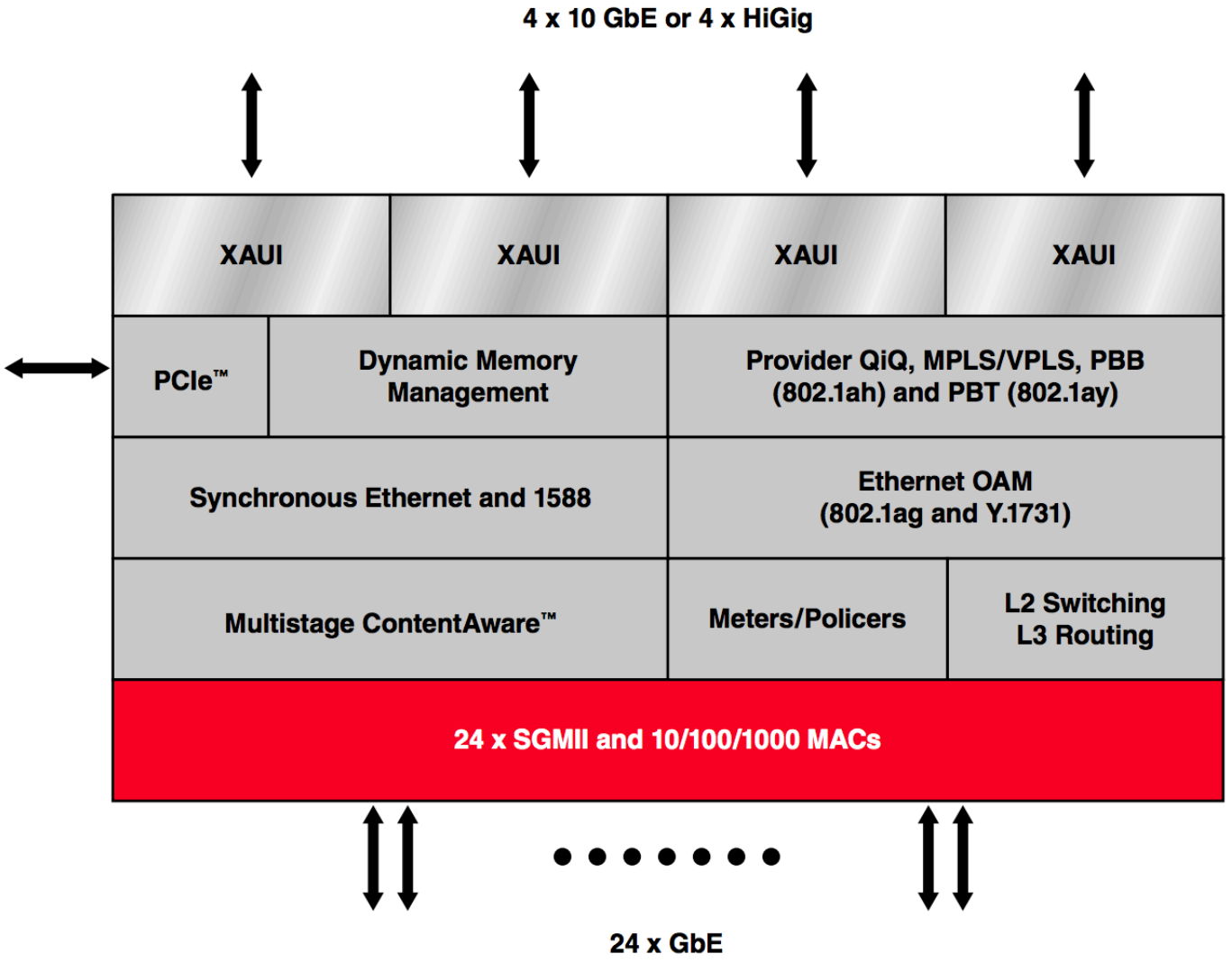
- Base Interface bandwidth = 1Gb

- Bandwidth to the outside world = 10Gb

Note: Connecting both RODs & IPMCs to each network may require some cleverness.

→ROD & IPMC on “second Hub” aren’t directly on the base interface.

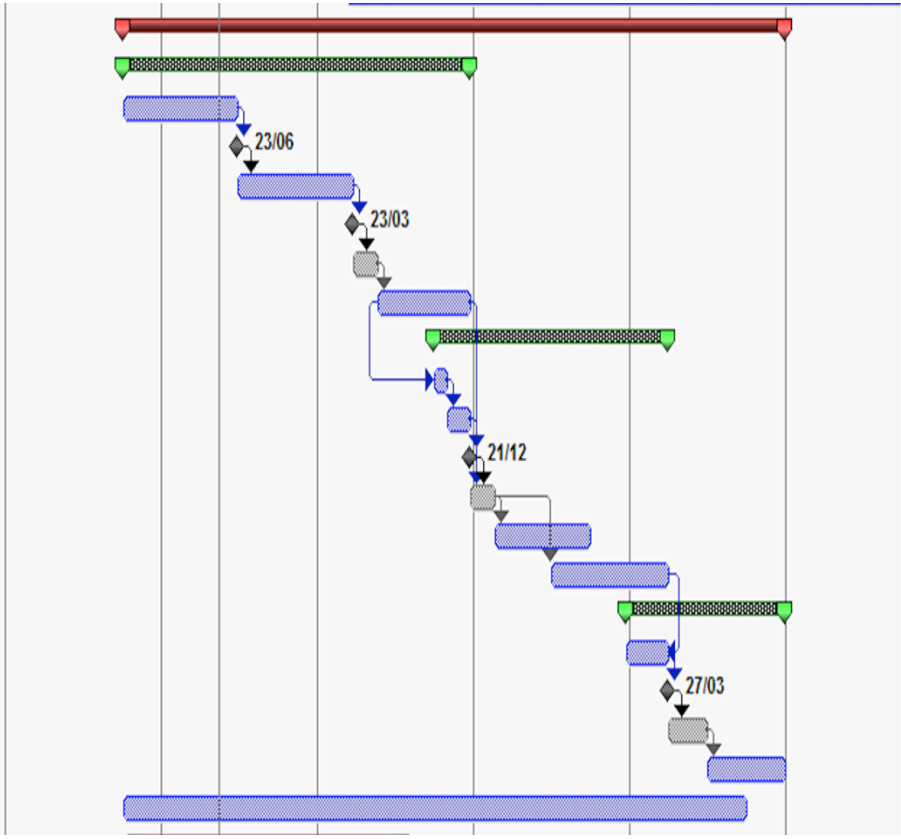
Example Architecture: BCM56330



BCM56330 Block Diagram

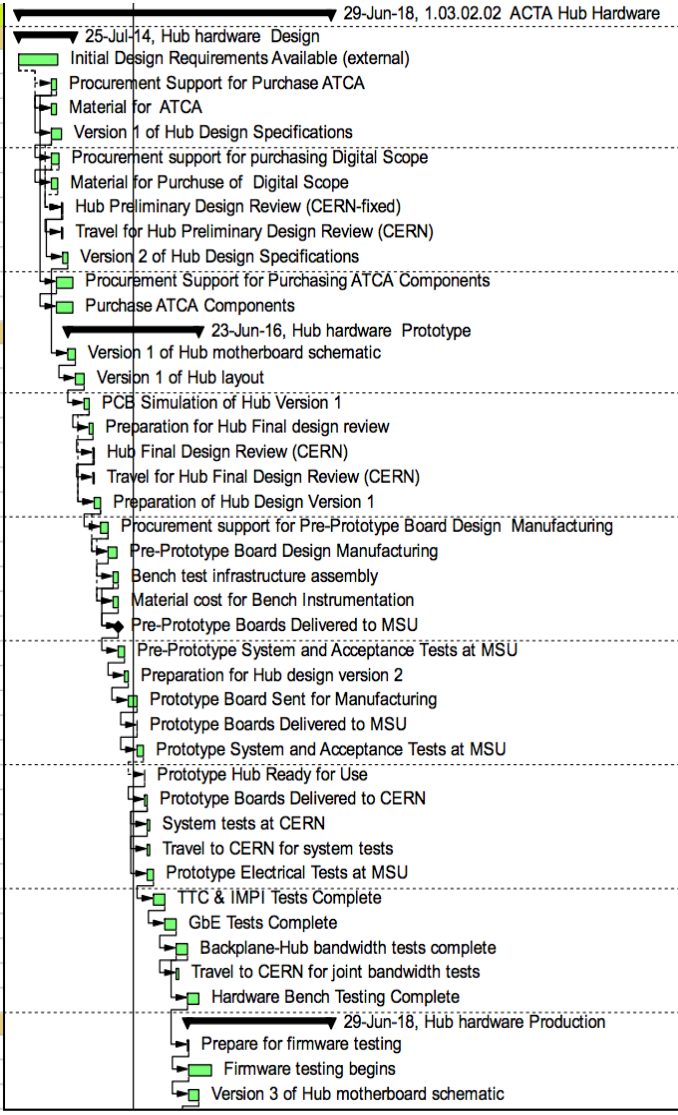
Schedule (Ian's Version)

137	FEX ATCA Hub	1105 days	Tue 01/10/13	Mon 25/12/17
138	Prototype	580 days	Tue 01/10/13	Mon 21/12/15
139	Engineering Specification	38 wks	Tue 01/10/13	Mon 23/06/14
140	Preliminary Design Review	0 days	Mon 23/06/14	Mon 23/06/14
141	Schematic Entry + Layout	39 wks	Tue 24/06/14	Mon 23/03/15
142	Interim Design Review 1	0 days	Mon 23/03/15	Mon 23/03/15
143	Manufacture	2 mons	Tue 24/03/15	Mon 18/05/15
144	Commissioning	31 wks	Tue 19/05/15	Mon 21/12/15
145	Pre-Production	390 days	Tue 29/09/15	Mon 27/03/17
146	Engineering Specification	1 mon	Tue 29/09/15	Mon 26/10/15
147	Schematic Entry + Layout	2 mons	Tue 27/10/15	Mon 21/12/15
148	Final Design Review	0 days	Mon 21/12/15	Mon 21/12/15
149	Manufacture	8 wks	Tue 22/12/15	Mon 15/02/16
150	Full Board Bench Testing	32 wks	Tue 16/02/16	Mon 26/09/16
151	Hardware/Firmware Testing	39 wks	Tue 28/06/16	Mon 27/03/17
152	Production	265 days	Tue 20/12/16	Mon 25/12/17
153	Schematic Entry + Layout	14 wks	Tue 20/12/16	Mon 27/03/17
154	Production Readiness Review	0 days	Mon 27/03/17	Mon 27/03/17
155	Manufacture	13 wks	Tue 28/03/17	Mon 26/06/17
156	Acceptance Tests	26 wks	Tue 27/06/17	Mon 25/12/17
157	Firmware	52 mons	Tue 01/10/13	Mon 25/09/17



Schedule (Funding Profile)

1.03.02.02 ACTA Hub Hardware			01-Oct-13	29-Jun-18	1211	318
Hub hardware Design			01-Oct-13	25-Jul-14	209	1320
1.03.02.02	HUB2000	Initial Design Requirements Available (external)	01-Oct-13*	01-May-14	150	137
1.03.02.02	HUB2010	Procurement Support for Purchase ATCA	01-Apr-14*	30-Apr-14	22	10
1.03.02.02	HUB2010M	Material for ATCA	01-Apr-14	30-Apr-14	22	1380
1.03.02.02	HUB2020	Version 1 of Hub Design Specifications	01-Apr-14	27-May-14	40	10
1.03.02.02	HUB2030	Procurement support for purchasing Digital Scope	01-Apr-14	12-May-14	30	10
1.03.02.02	HUB2030M	Material for Purchuse of Digital Scope	01-Apr-14	01-May-14	23	17
1.03.02.02	HUB2040EX	Hub Preliminary Design Review (CERN-fixed)	28-May-1	02-Jun-14	4	0
1.03.02.02	HUB2040T	Travel for Hub Preliminary Design Review (CERN)	28-May-14	02-Jun-14	4	1358
1.03.02.02	HUB2050	Version 2 of Hub Design Specifications	03-Jun-14	27-Jun-14	19	3
1.03.02.02	HUB2070	Procurement Support for Purchasing ATCA Components	01-May-14	25-Jul-14	60	1320
1.03.02.02	HUB2070M	Purchase ATCA Components	01-May-14	25-Jul-14	60	1320
Hub hardware Prototype			30-Jun-14	23-Jun-16	507	832
1.03.02.02	HUB2100	Version 1 of Hub motherboard schematic	30-Jun-14	13-Aug-14	32	3
1.03.02.02	HUB2110	Version 1 of Hub layout	14-Aug-14	01-Oct-14	34	3
1.03.02.02	HUB2120	PCB Simulation of Hub Version 1	02-Oct-14	28-Oct-14	19	3
1.03.02.02	HUB2130	Preparation for Hub Final design review	29-Oct-14	18-Nov-14	15	3
1.03.02.02	HUB2130EX	Hub Final Design Review (CERN)	19-Nov-14	25-Nov-14	5	3
1.03.02.02	HUB2130T	Travel for Hub Final Design Review (CERN)	19-Nov-14	25-Nov-14	5	1234
1.03.02.02	HUB2140	Preparation of Hub Design Version 1	26-Nov-14	29-Dec-14	22	3
1.03.02.02	HUB2150	Procurement support for Pre-Prototype Board Design Manufactu	30-Dec-14	11-Feb-15	31	3
1.03.02.02	HUB2150M	Pre-Prototype Board Design Manufacturing	12-Feb-15	01-Apr-15	35	3
1.03.02.02	HUB2160	Bench test infrastructure assembly	09-Mar-15	03-Apr-15	20	3
1.03.02.02	HUB2160M	Material cost for Bench Instrumentation	09-Mar-15	03-Apr-15	20	3
1.03.02.02	HUB2170	Pre-Prototype Boards Delivered to MSU		03-Apr-15	0	3
1.03.02.02	HUB2180	Pre-Prototype System and Acceptance Tests at MSU	06-Apr-15	08-May-15	25	3
1.03.02.02	HUB2185	Preparation for Hub design version 2	11-May-15	01-Jun-15	15	3
1.03.02.02	HUB2187	Prototype Board Sent for Manufacturing	02-Jun-15	21-Jul-15	35	3
1.03.02.02	HUB2190	Prototype Boards Delivered to MSU	22-Jul-15	22-Jul-15	1	3
1.03.02.02	HUB2195	Prototype System and Acceptance Tests at MSU	23-Jul-15	26-Aug-15	25	3
1.03.02.02	HUB2201EX	Prototype Hub Ready for Use	01-Sep-1	01-Sep-15	0	0
1.03.02.02	HUB2205	Prototype Boards Delivered to CERN	01-Sep-15	16-Sep-15	11	118
1.03.02.02	HUB2210	System tests at CERN	17-Sep-15	29-Sep-15	9	1020
1.03.02.02	HUB2210T	Travel to CERN for system tests	17-Sep-15	30-Sep-15	10	1019
1.03.02.02	HUB2220	Prototype Electrical Tests at MSU	17-Sep-15	16-Oct-15	22	118
1.03.02.02	HUB2230	TTC & IMPI Tests Complete	19-Oct-15	17-Dec-15	43	118
1.03.02.02	HUB2240	GbE Tests Complete	18-Dec-15	19-Feb-16	44	118
1.03.02.02	HUB2250	Backplane-Hub bandwidth tests complete	22-Feb-16	21-Apr-16	44	118
1.03.02.02	HUB2250T	Travel to CERN for joint bandwidth tests	22-Feb-16	07-Mar-16	11	909
1.03.02.02	HUB2260	Hardware Bench Testing Complete	22-Apr-16	23-Jun-16	44	118
Hub hardware Production			22-Apr-16	29-Jun-18	558	318
1.03.02.02	HUB2300	Prepare for firmware testing	22-Apr-16	29-Apr-16	6	118
1.03.02.02	HUB2310	Firmware testing begins	02-May-16	02-Sep-16	88	118
1.03.02.02	HUB2330	Version 3 of Hub motherboard schematic	02-May-16	24-Jun-16	39	118



Schedule Milestones

1. June 2014: Preliminary Design Review
2. March 2015: Interim Design Review

3. Sept 2015: Prototype Delivery to CERN

4. Dec 2015: Final Design Review
5. March 2017: Production Readiness Review

6. Jan 2018: Ready to install at CERN