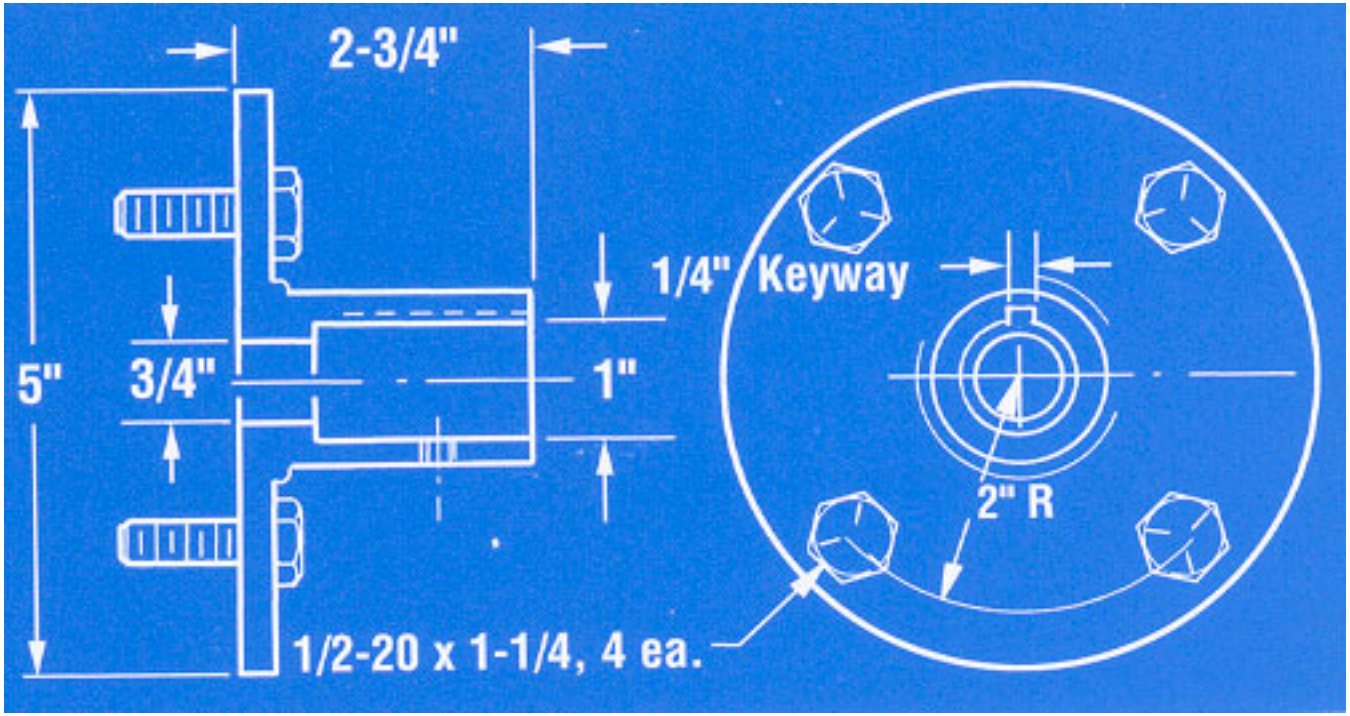
FEX Hub Module Update



Wade Fisher
for the MSU team

23 Sept 2014

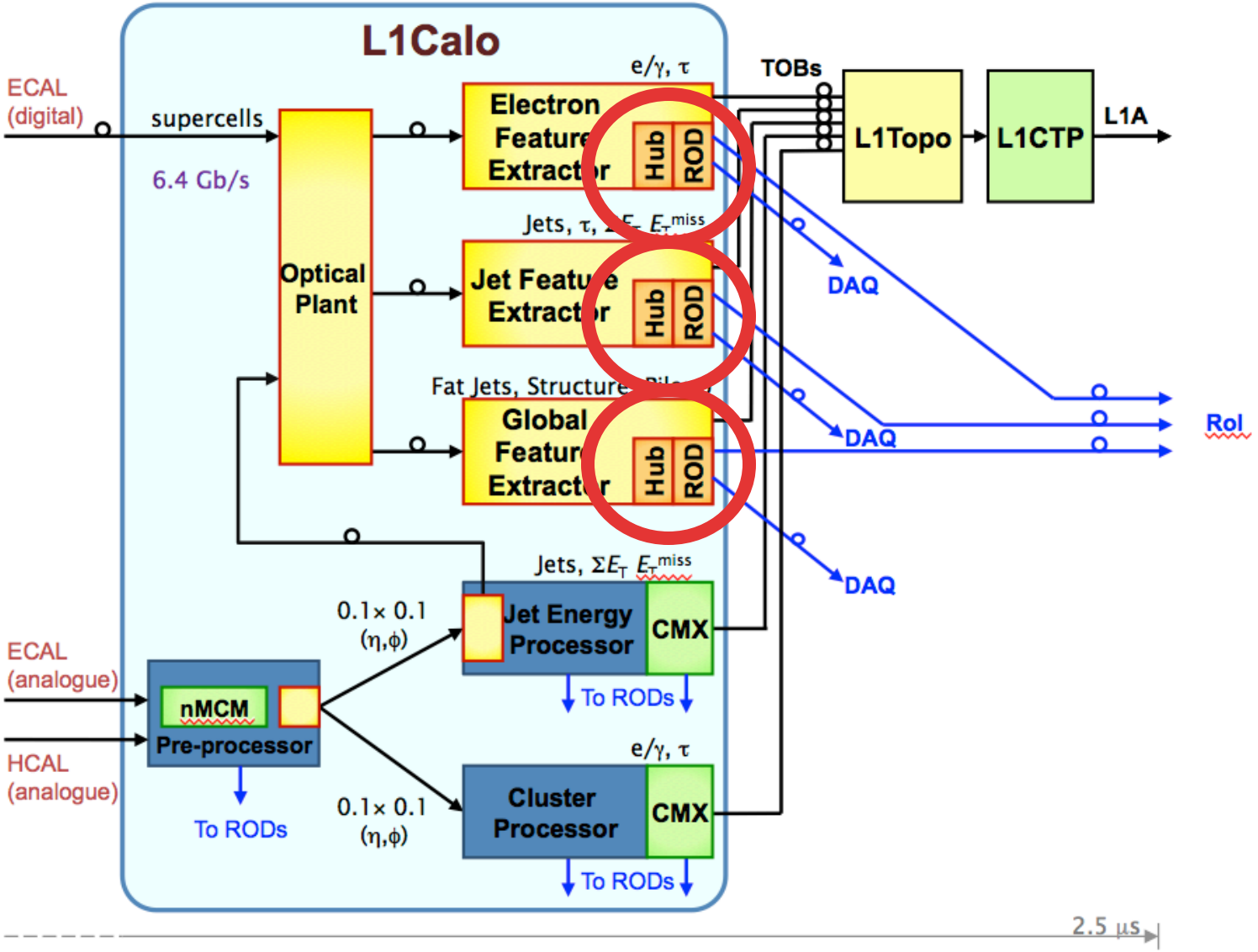
MICHIGAN STATE UNIVERSITY

Outline

- Overview of FEX ATCA hub module project
- Hub module technical overview
  - Physical Interfaces: Rack space & ATCA shelf
  - Functional design of Hub module
- Areas of primary design challenge and/or questions
  - Interface to ROD Mezzanine
  - FEX->ROD data path & volume
  - Main FPGA choice and utilization
  - Ethernet implementation
- Prototype Specification

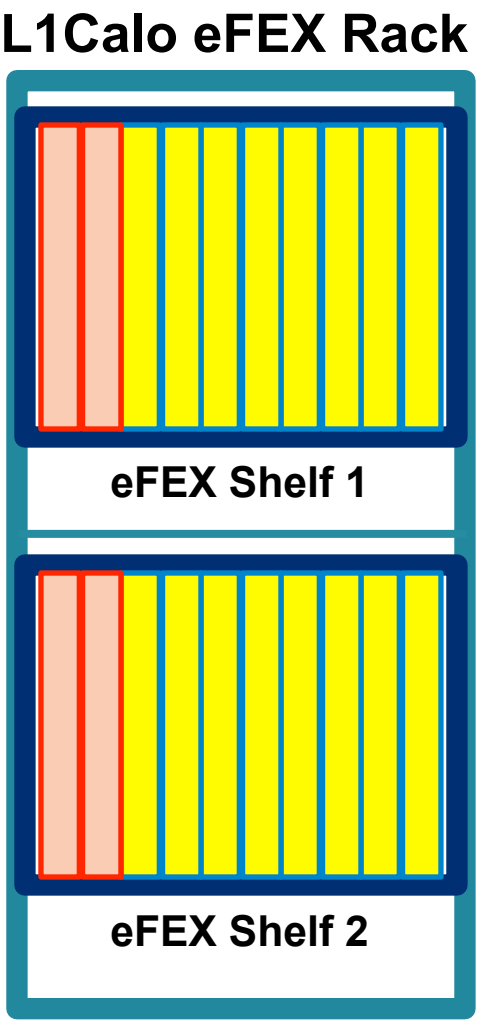
http://www.pa.msu.edu/~fisherw/ATLAS_Phase1/Hub_Spec_v0_3.pdf

Level 1 trigger in Phase 1

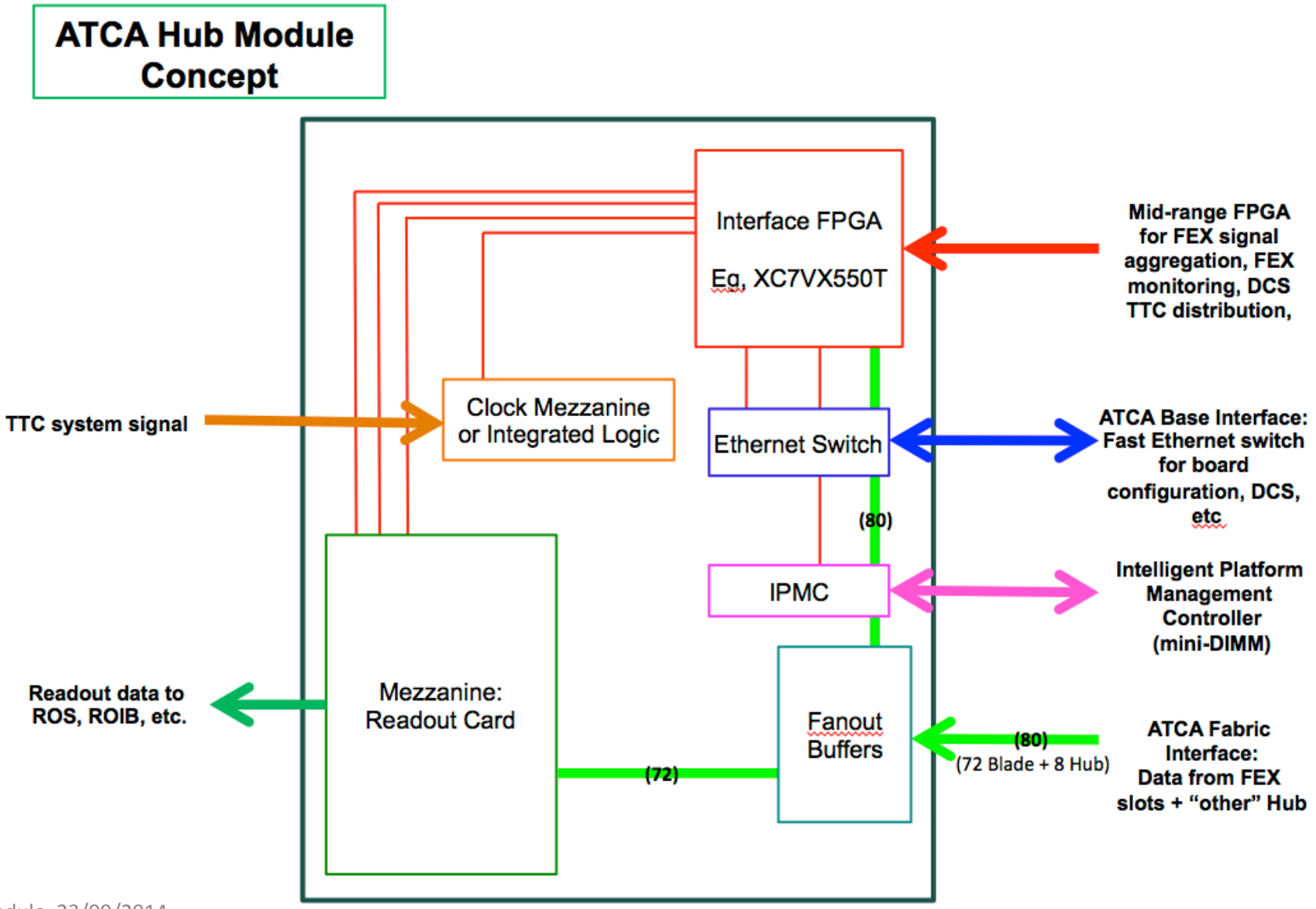


FEX ATCA Hub

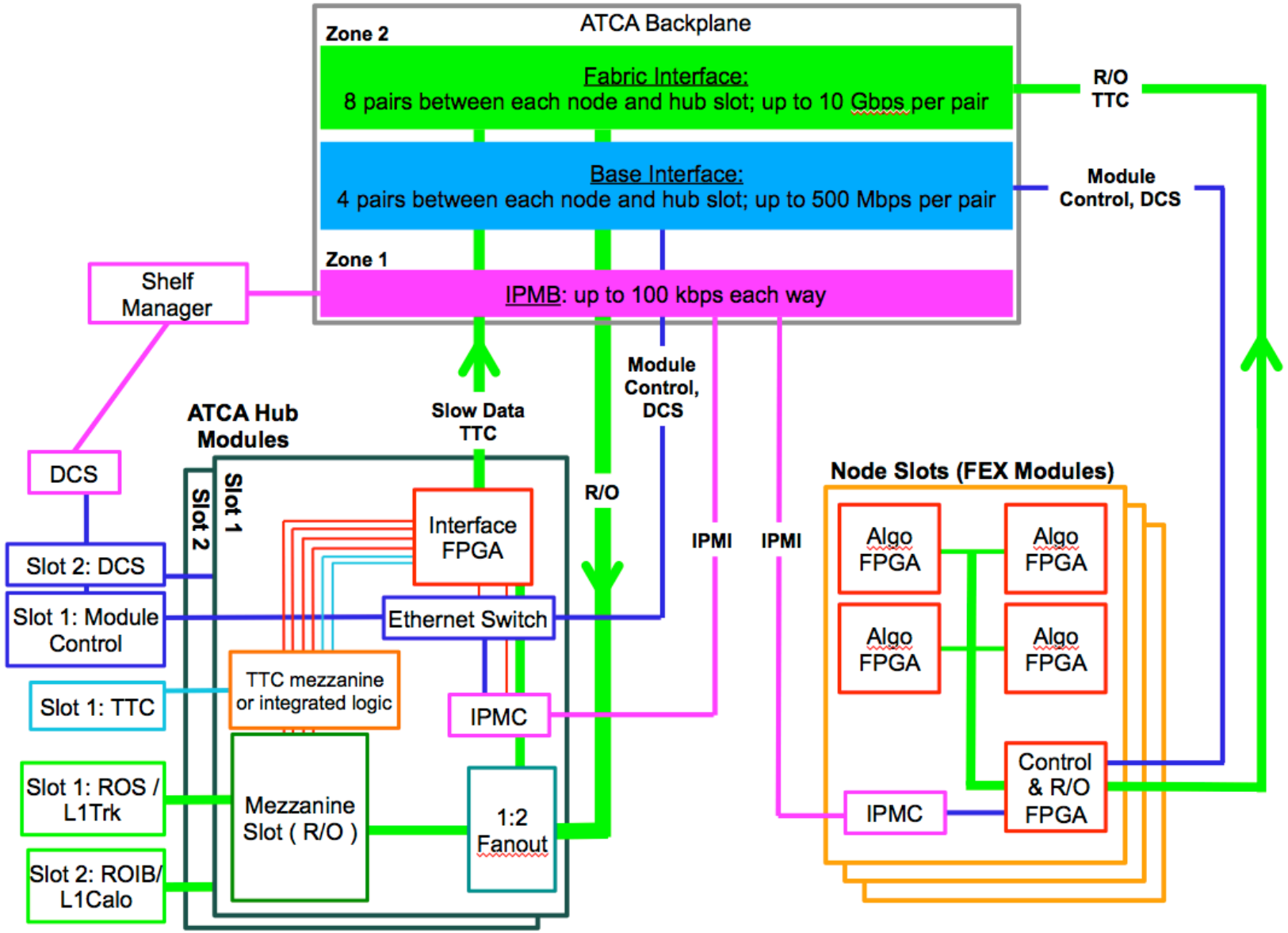
- ATCA Hub is a core FEX system component
  - Supports common communication tasks: readout, TTC, networking, monitoring, DCS, busy aggregation, etc.
- Technical Motivations
  - Concentration of common functions on the Hub rather than on the FEX modules makes the FEX system:
    - Less costly
    - Simpler & more efficient
    - Easier to maintain
  - Phase-II upgrade could create single points of failure
    - Move all likely Phase-II targets off the FEX boards
    - Hub module provides a flexible platform to "future-proof" FEX system.



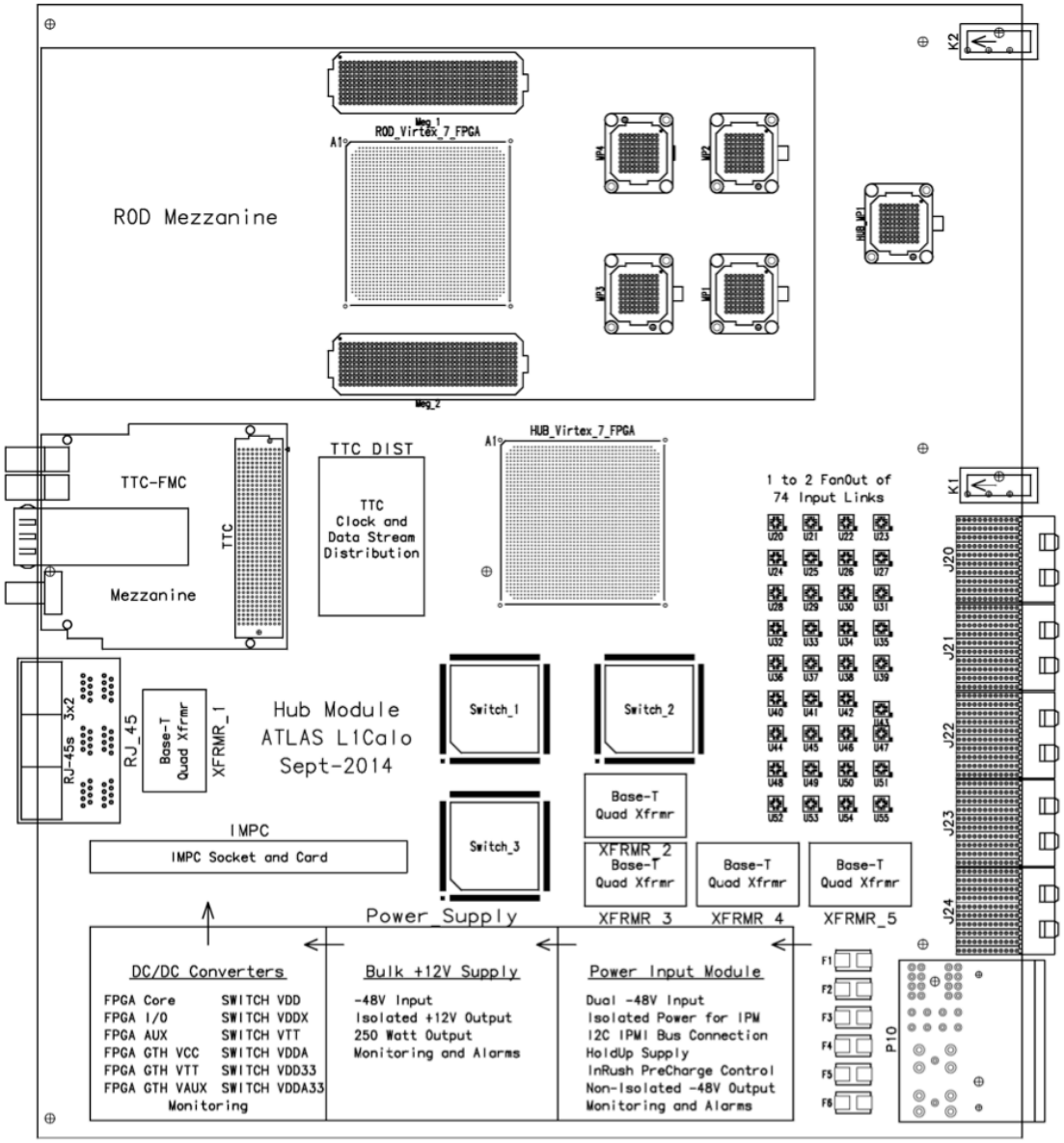
ATCA Hub Modular Design



ATCA Hub Modular Design

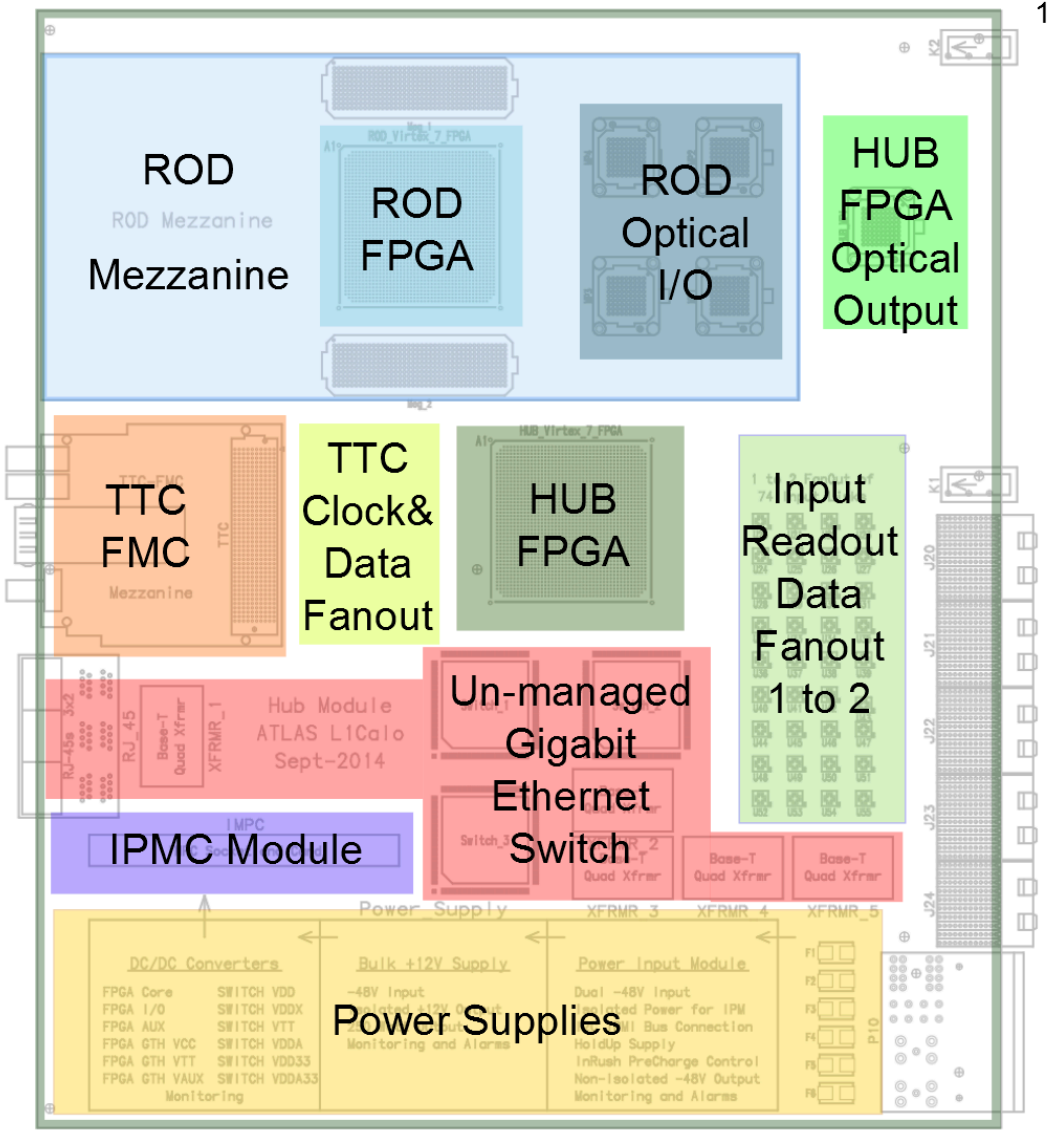


ATCA Hub Preliminary Drawing



ATCA Hub Preliminary Drawing

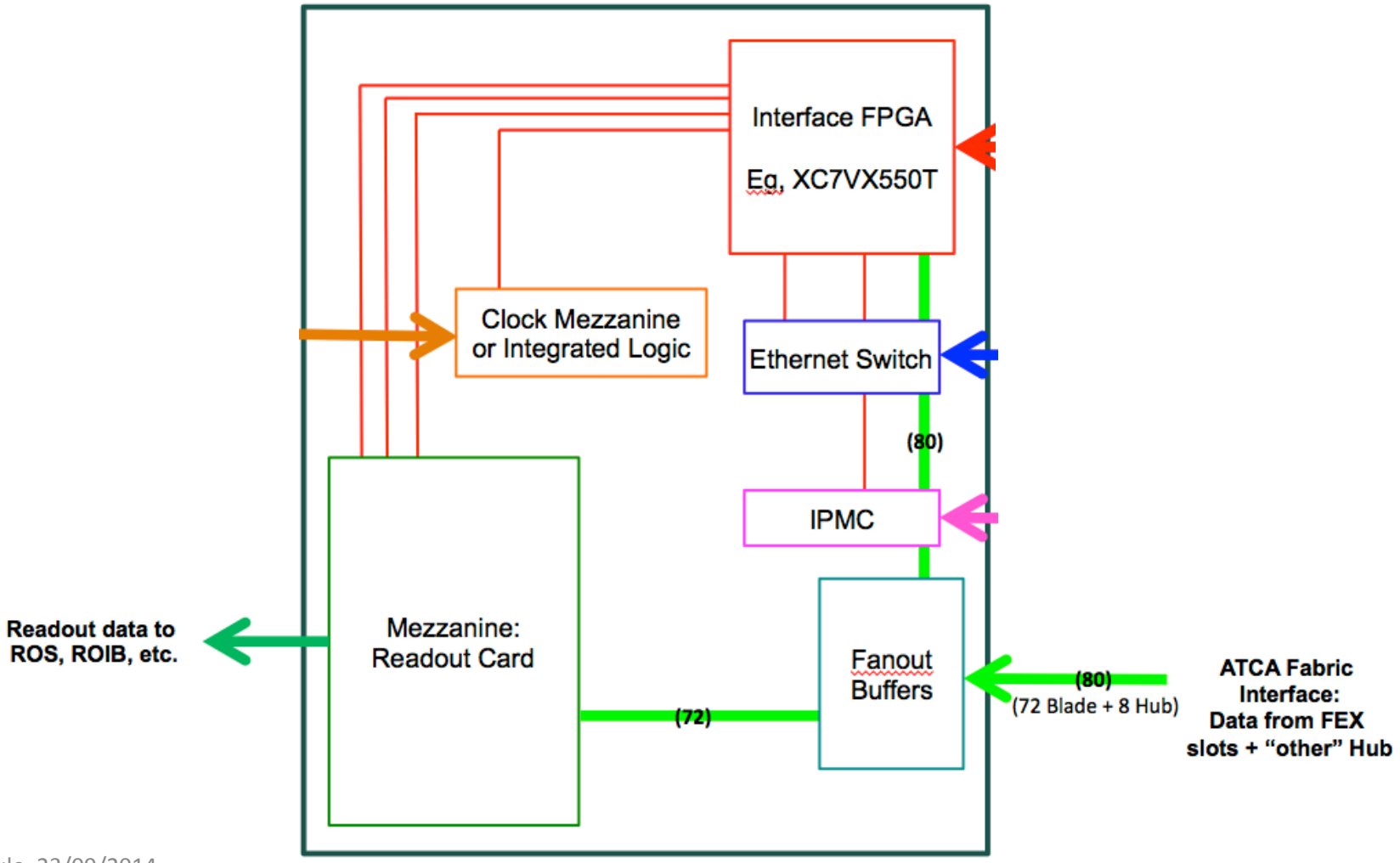
16-Sep-2014



L1Calo HUB Module

FEX-ROD Data Flow (2)

ATCA Hub Module Concept



FEX-ROD Data Flow (3)

ROD↔Hub Electrical Connections

- Two 400-pin MEG Array connectors
- Very low stack height to allow room for ROD Minipod
- Sufficient pin count for high-speed signals, power, spares.

Diagram from Maurice Goodrick

Note:

This has evolved since the ROD Spec was written.

http://www.fci.com/en/products/board-to-board-wire-to-board/high-speed-mezzanine/meg-array.html

Hub->ROD: Dual MEG Array 400: Proposed pin usage

Last Updated: 16-Sep-2014 SUBJECT TO CHANGE

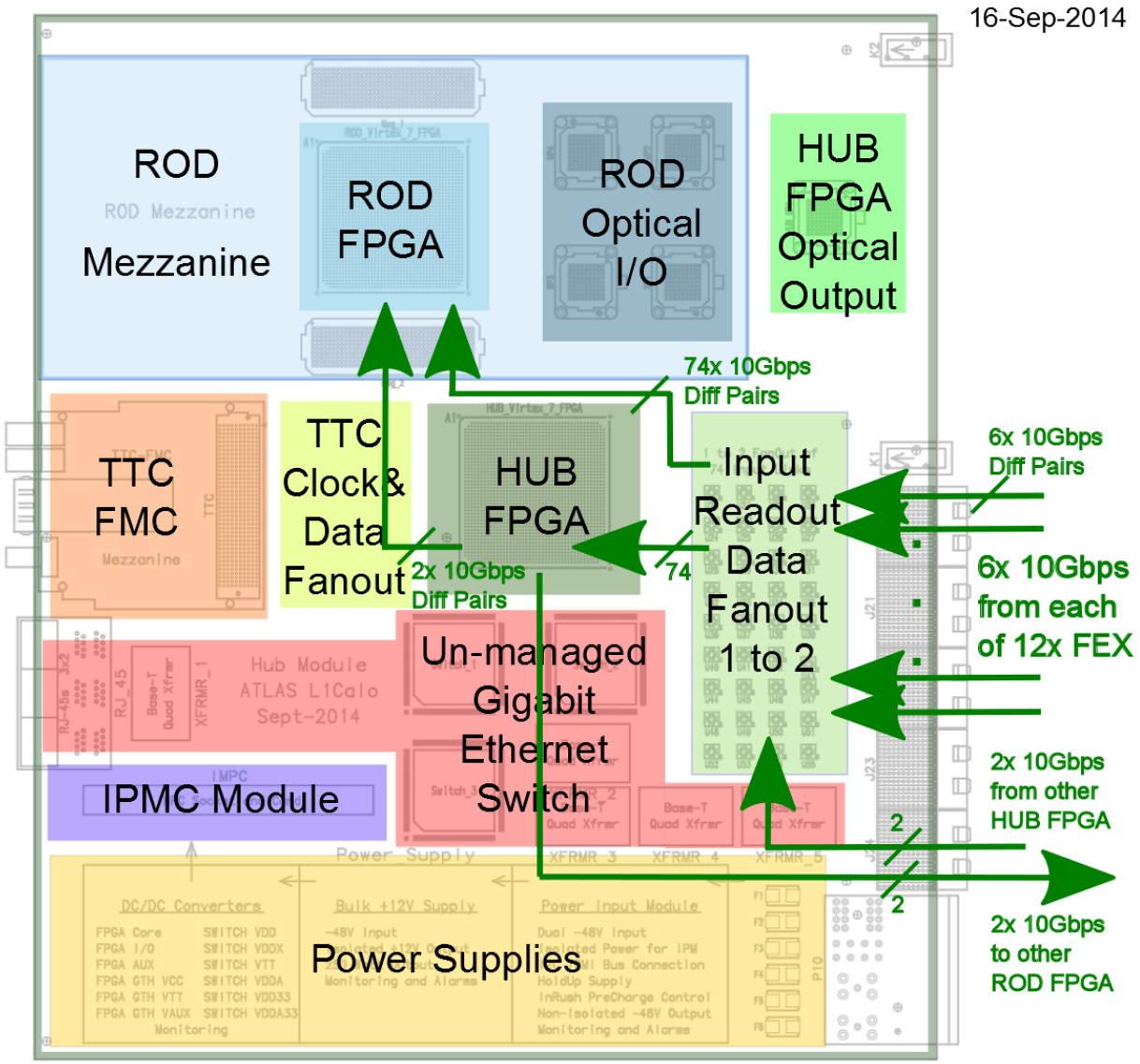
Col: / Row	A	B	C	D	E	F	G	H	I	J
1	T	G	T	V	V	V	V	V	S	S
2	G	+	G	V	V	V	V	V	S	S
3	G	-	G	T	G	T	S	S	S	S
4	T	G	+	G	+	G	S	S	S	S
5	T	G	-	G	-	G	S	S	S	S
6	G	+	G	+	G	T	S	S	S	S
7	G	-	G	-	G	T	S	S	S	S
8	T	G	+	G	+	G	S	S	S	S
9	T	G	-	G	-	G	S	S	S	S
10	G	+	G	+	G	T	S	S	S	S
11	G	-	G	-	G	T	S	S	S	S
12	T	G	+	G	+	G	S	S	S	S
13	T	G	-	G	-	G	S	S	S	S
14	G	+	G	+	G	T	S	S	S	S
15	G	-	G	-	G	T	S	S	S	S
16	T	G	+	G	+	G	S	S	S	S
17	T	G	-	G	-	G	S	S	S	S
18	G	+	G	+	G	T	S	S	S	S
19	G	-	G	-	G	T	S	S	S	S
20	T	G	+	G	+	G	S	S	S	S
21	T	G	-	G	-	G	S	S	S	S
22	G	+	G	+	G	T	S	S	S	S
23	G	-	G	-	G	T	S	S	S	S
24	T	G	+	G	+	G	S	S	S	S
25	T	G	-	G	-	G	S	S	S	S
26	G	+	G	+	G	T	S	S	S	S
27	G	-	G	-	G	T	S	S	S	S
28	T	G	+	G	+	G	S	S	S	S
29	T	G	-	G	-	G	S	S	S	S
30	G	+	G	+	G	T	S	S	S	S
31	G	-	G	-	G	T	S	S	S	S
32	T	G	+	G	+	G	S	S	S	S
33	T	G	-	G	-	G	S	S	S	S
34	G	+	G	+	G	T	S	S	S	S
35	G	-	G	-	G	T	S	S	S	S
36	T	G	+	G	+	G	S	S	S	S
37	T	G	-	G	-	G	S	S	S	S
38	G	+	G	T	G	T	S	S	S	S
39	G	-	G	V	V	V	V	V	S	S
40	T	G	T	V	V	V	V	V	S	S

Notes
(1)Differential Signal polarities are arbitrary: there may be a case for re-arranging them.
(2) Terminator pins have 50Ω to Ground: not fully established if better than Grounds
(3) The Signal pins are available for the other ROD-Hub signals
[4] Pins rated at 0.45 A/pin, so 20 OK for 9A: i.e. 108 W at 12V. All 12V on one connector?
[5] Mate/Un-Mate forces for 400 pins are 140/80N
[6] Only have to route Differential Pairs 4 columns back: simpler, less layers?

Signal Pairs	0	10	9	8	9	0	0	0	0	0
Grounds	20	20	20	18	18	18	0	0	0	0
Terminators	20	0	2	2	0	18	0	0	0	0
12V Power	0	0	0	4	4	4	4	4	0	0
Other Signals	0	0	0	0	0	0	36	36	40	40

Total Pins	
for Signal Pairs	72
Grounds	114
Terminators	42
12V Power	20
Other Signals	152
Total Totals	400

FEX-ROD Data Flow (4)



L1Calo HUB Module **ROD Readout path including HUB Data**

FEX Bandwidth (1)

Data	No. Chan.	Bits / Chan. / BC (post 8b/10b)	BC / Event	Trigger Rate / KHz	Bandwidth / Gb/s
Input from ECAL	160	160	3	50	3.84
Input from HCAL	72	160	3	50	1.73
XTOBs	160	80	3	500	19.20
TOBs	2	160	3	500	0.48
Total					**25.25**

435 **Table 1. An estimate of the maximum readout bandwidth required for the eFEX. For**
436 **XTOBs, a channel equals an XTOB; for the other types of data, a channel equals a fibre.**

Extracted from the eFEX specification

- Calibrated to Run-4 at 500 kHz
- Assuming FEX input data is read out in 10% of events
- Translates to 6.3125 Gbps maximum rate
- 1 MHz trigger rate could be an issue

FEX Bandwidth (2)

eFEX

Data	No. Chan.	Bits / Chan. / BC (post 8b/10b)	BC / Event	Trigger Rate / KHz	Bandwidth / Gb/s
Input from ECAL	160	160	3	50	3.84
Input from HCAL	72	160	3	50	1.73
XTOBs	160	80	3	500	19.20
TOBs	2	160	3	500	0.48
Total					**25.25**

4 pairs / eFEX
~6.44 Gbps

jFEX

Data	No. Chan.	Bits / Chan. / BC (post 8b/10b)	BC / Event	Trigger Rate / KHz	Bandwidth / Gb/s
Input data	416	320	3	50	19.97
XTOBs	96	80	3	500	11.52
TOBs	4	320	3	1000	3.84
Total					**35.33**

6 pairs / jFEX
~5.89 Gbps

gFEX

Data	Trigger Rate (kHz)	FPGA	bits/BC	BC/event	Bandwidth (Gb/s)	Total (Gb/s)
TOBs	1000	1	492	3	1.845	7.380
		2	492	3	1.845	
		3	492	3	1.845	
		4	492	3	1.845	
Calorimeter	100	1	7168	3	2.688	11.532
		2	7168	3	2.688	
		3	8208	3	3.078	
		4	8208	3	3.078	
Total						18.912

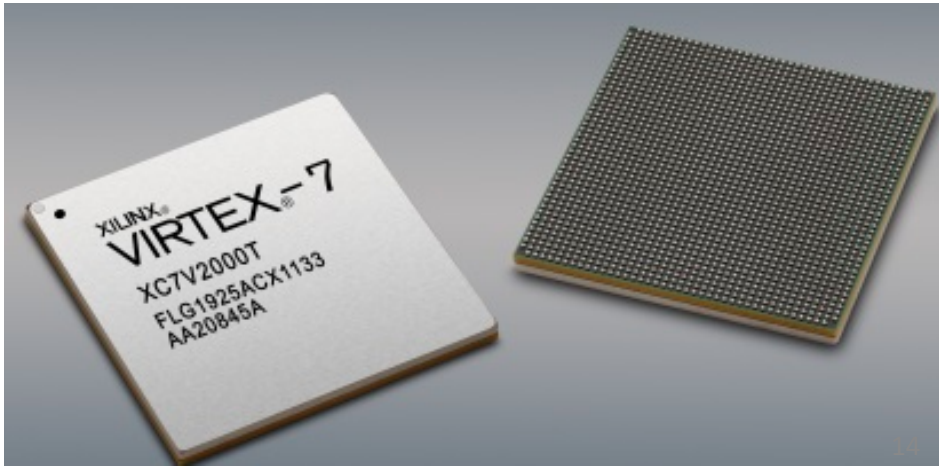
4 pairs / gFEX
~4.73 Gbps

Main FPGA (1)

Requirements:

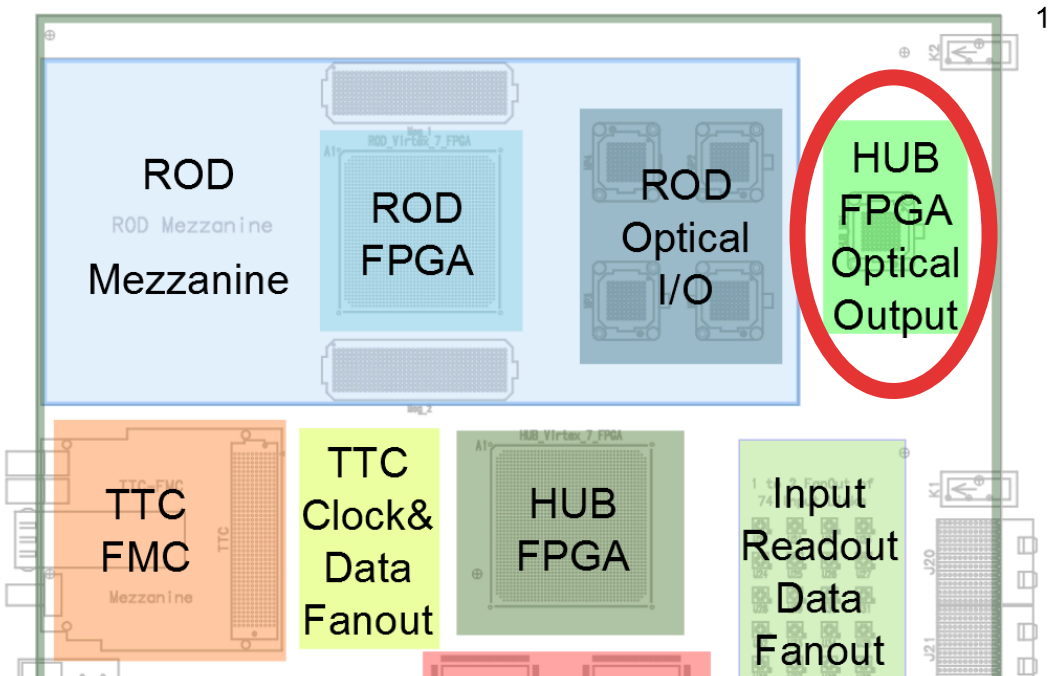
- 80 MGTs to allow a copy of 72 FEX data lines + 2 from the other hub slot
  - In the 7-series, this limits us to the XC7VX550T or XC7VX690T.

- Sufficient resources to provide all board management?
  - Firmware required to:
    - Merge TTC control signals with ROD back-pressure signals
    - Interface to Control and DCS networks
    - Communicate with ROD
    - Monitor data streams



Main FPGA (2)

- Hub main FPGA resources are plentiful
  - Core Hub functions will not utilize all FPGA resources
  - Future-proofing options are being considered
- The Hub sees all of the readout data to ROD + the “other” Hub FPGA
  - Potential lifeboat in case extra processing is required
  - Proposed Minipod on Hub in case it’s needed.



Ethernet (1)

Requirements:

- Ports: 12 FEX + 2 ROD + 2 Hub + 1 Shelf Manager + 1 external
- Base Interface Bandwidth = 1Gb/port?
- Bandwidth to the outside world? 1Gb? 10Gb?

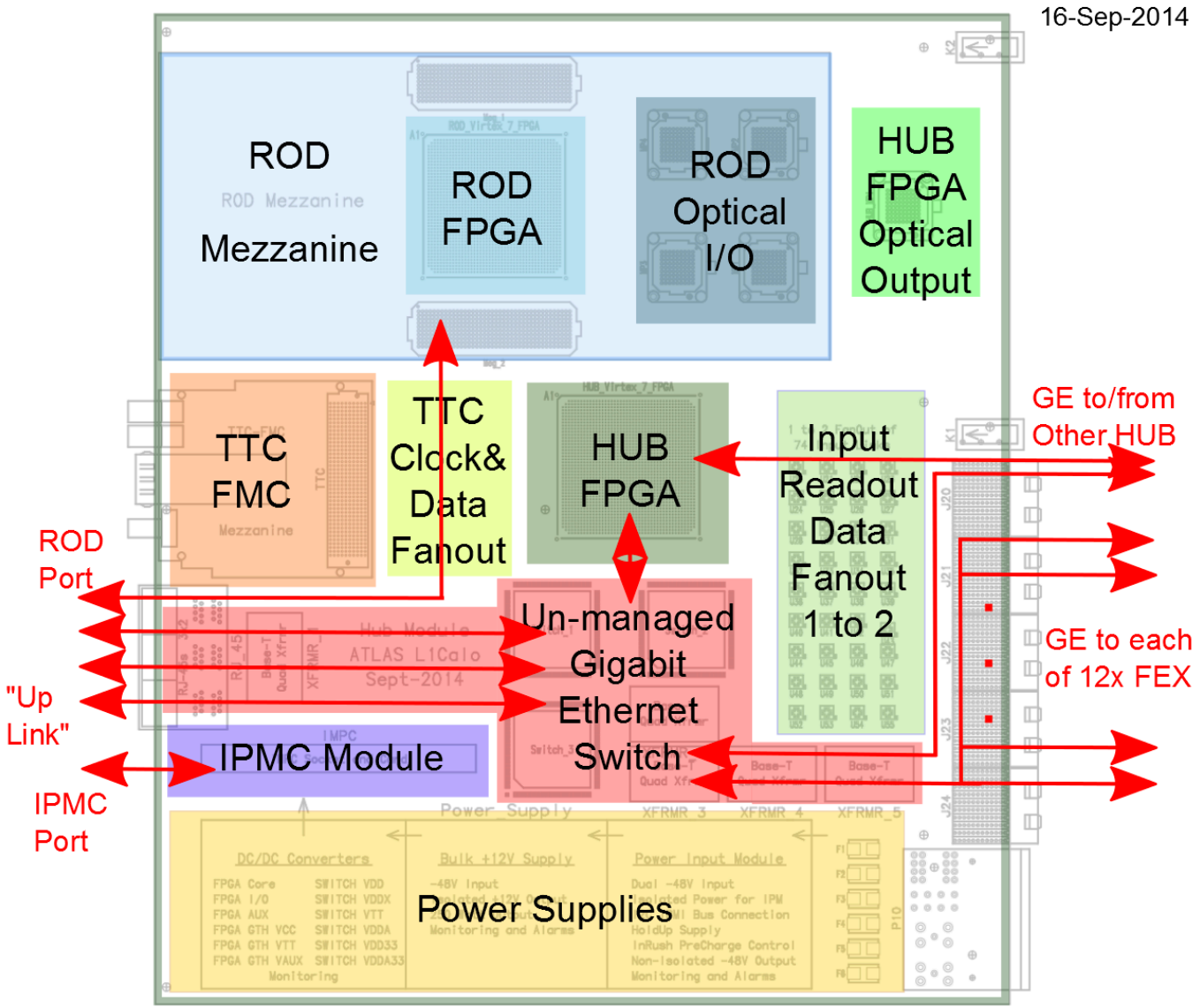
Note: Current Hub switch is implemented as a 1Gbps unmanaged switch using 3 Broadcom BCM53118 devices.

- Avoids the pain of a managed switch (& more reliable?)
- Limits outside uplink to 1 Gbps. Is that enough?

Hub-to-Hub interconnections proposed as front-panel patches.

- Satisfies “identical Hub layout” requirements
- Avoids the need for logic to select networks
- Frees up backplane lines in case they’re required

Ethernet (2)


16-Sep-2014
ROD
ROD Mezzanine
Mezzanine
ROD FPGA
ROD Optical I/O
HUB FPGA Optical Output
TTC FMC
Mezzanine
TTC Clock& Data Fanout
HUB FPGA
Input Readout Data Fanout 1 to 2
GE to/from Other HUB
ROD Port
"Up Link"
IPMC Port
Hub Module
ATLAS L1Calo
Sept-2014
Un-managed Gigabit Ethernet Switch
IPMC Module
GE to each of 12x FEX
Power Supply
XFRMR_3
XFRMR_4
XFRMR_5
DC/DC Converters
Bulk +12V Supply
Power Input Module
Power Supplies
L1Calo HUB Module
Gigabit Ethernet (GE) Connections

TTC / Clock

TTC/Clock source is a bit of a question mark

- Preliminary Hub design implements a FMC connection for “TTC”
- Long-term plan is to adopt FELIX/GBT input links (?)
  - But no details/specs available at this time
- Need to make a decision on what the Hub prototype will support
  - TTC-FMC?
  - GBT-FMC?
  - Both? (will pin-outs be compatible?)
  - Integrated functions on Hub PCB? (not very Phase-2 proof)
- To avoid two prototype runs, the 2015 design should address this

Current Status

- Preliminary Design Review Scheduled for Oct 1st
  - We have circulated v0.1 of the specification (Sept 16), v0.3 is also now available
    - http://www.pa.msu.edu/~fisherw/ATLAS_Phase1/Hub_Spec_v0_3.pdf
- Investigating various technical solutions for Hub functionality
  - Ongoing discussions on the ROD-Hub interface & ROD form factor
  - Decisions about Ethernet switch function and availability of Ics
  - Solutions for Hub-to-Hub network connections
  - Clock/Control input definitions: TTC and/or GBT
  - Questions about availability of IPMC software
  - And various other technical aspects
- Prototype production planned in accordance with 2015 integration test schedule