Joint L1Calo Meeting

Status of the FEX ATCA Hub Project

Wade Fisher, Dan Edmunds, Philippe Laurens, Yuri Ermoline

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MICHIGAN STATE UNIVERSITY

Outline

Today: Focus on recent evolution of the project

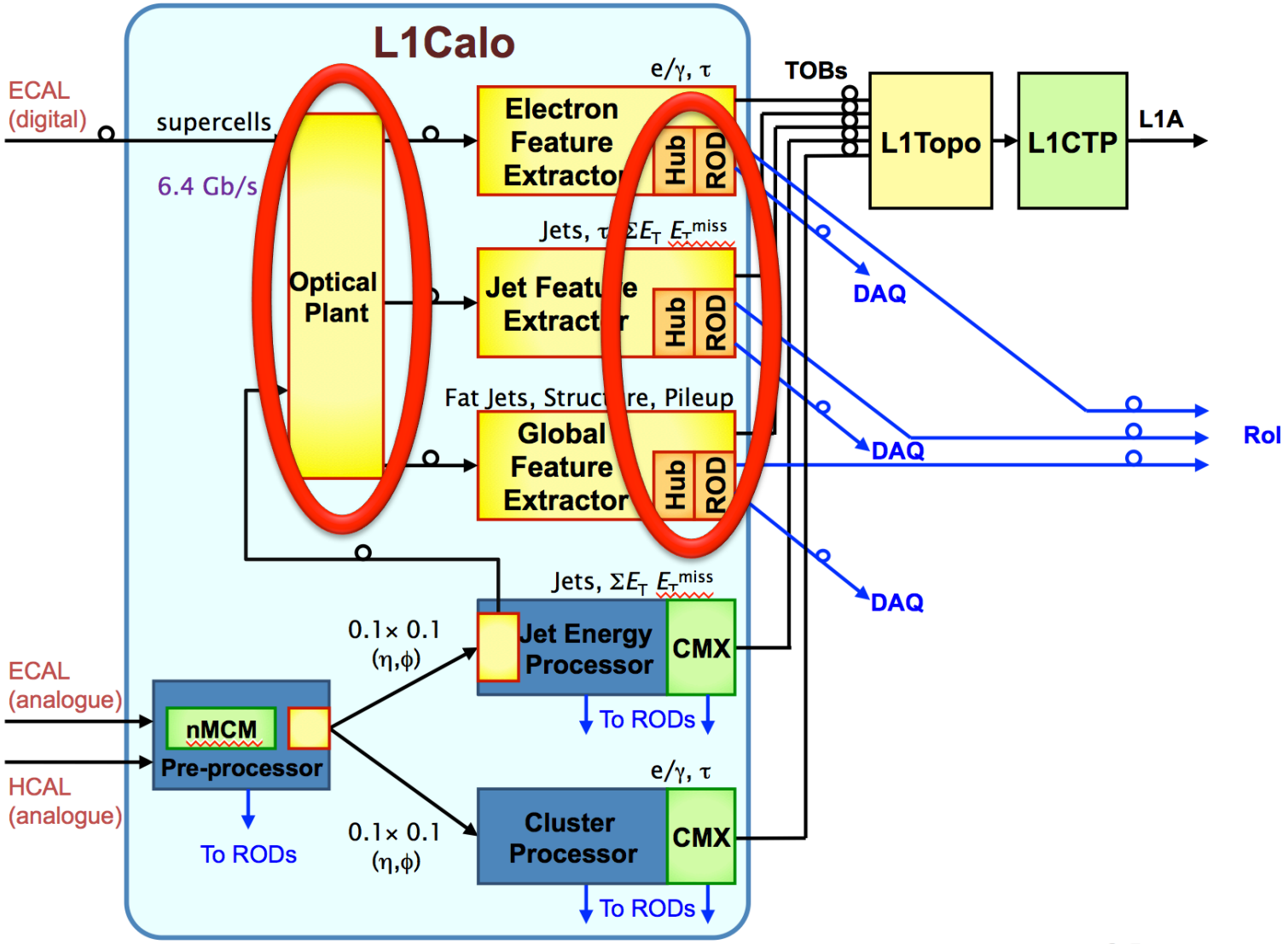
Action items from the Hub PDR

- TTC/Clock interface
- GbEthernet interface
- Signal integrity of fabric interface fan-out to ROD/Hub targets

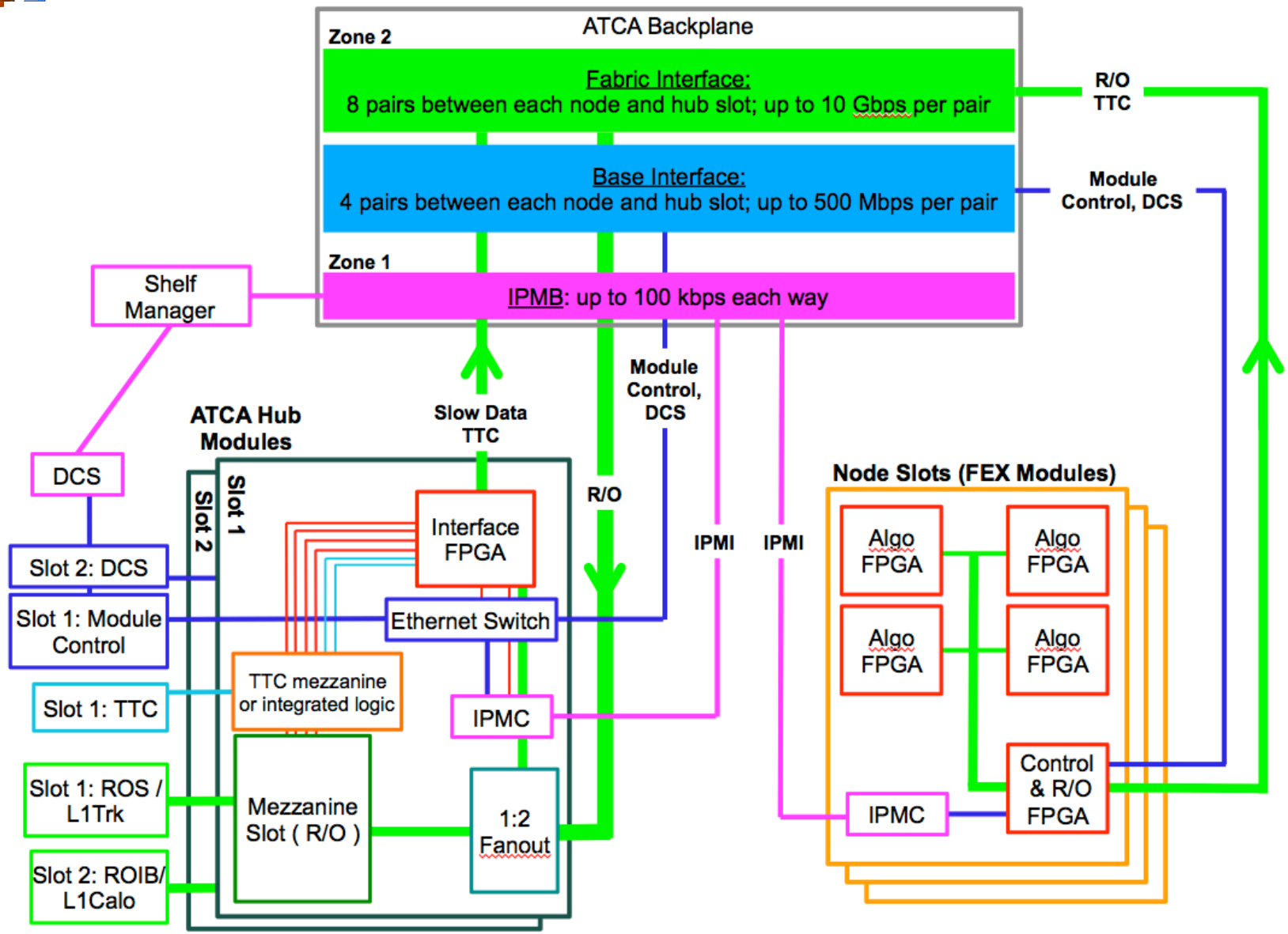
Planning for prototype Hub production

- Need to identify total number of prototypes
- General call for prototype requests

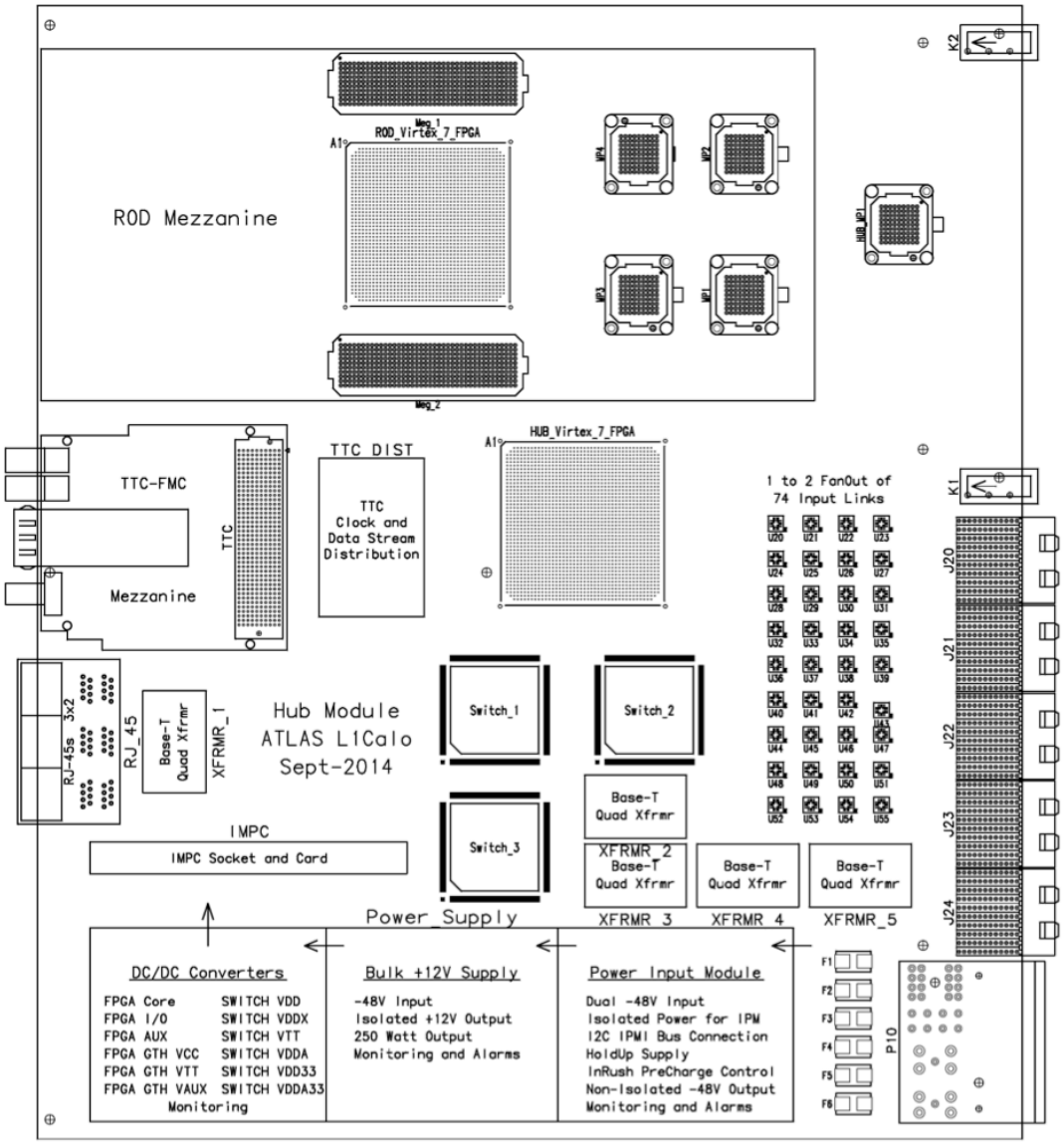
Level 1 trigger in Phase 1



FEX ATCA Hub


ATCA Backplane
Zone 2
Fabric Interface:
8 pairs between each node and hub slot; up to 10 Gbps per pair
Base Interface:
4 pairs between each node and hub slot; up to 500 Mbps per pair
Zone 1
IPMB: up to 100 kbps each way
R/O
TTC
Module
Control, DCS
Shelf
Manager
Slow Data
TTC
Module
Control,
DCS
ATCA Hub
Modules
Slot 1
Slot 2
DCS
Slot 2: DCS
Slot 1: Module
Control
Slot 1: TTC
Slot 1: ROS /
L1Trk
Slot 2: ROIB/
L1Calo
Interface
FPGA
Ethernet Switch
TTC mezzanine
or integrated logic
IPMC
Mezzanine
Slot (R/O)
1:2
Fanout
R/O
IPMI
IPMI
Node Slots (FEX Modules)
Algo
FPGA
Algo
FPGA
Algo
FPGA
Algo
FPGA
Control
& R/O
FPGA
IPMC

ATCA Hub Preliminary Drawing



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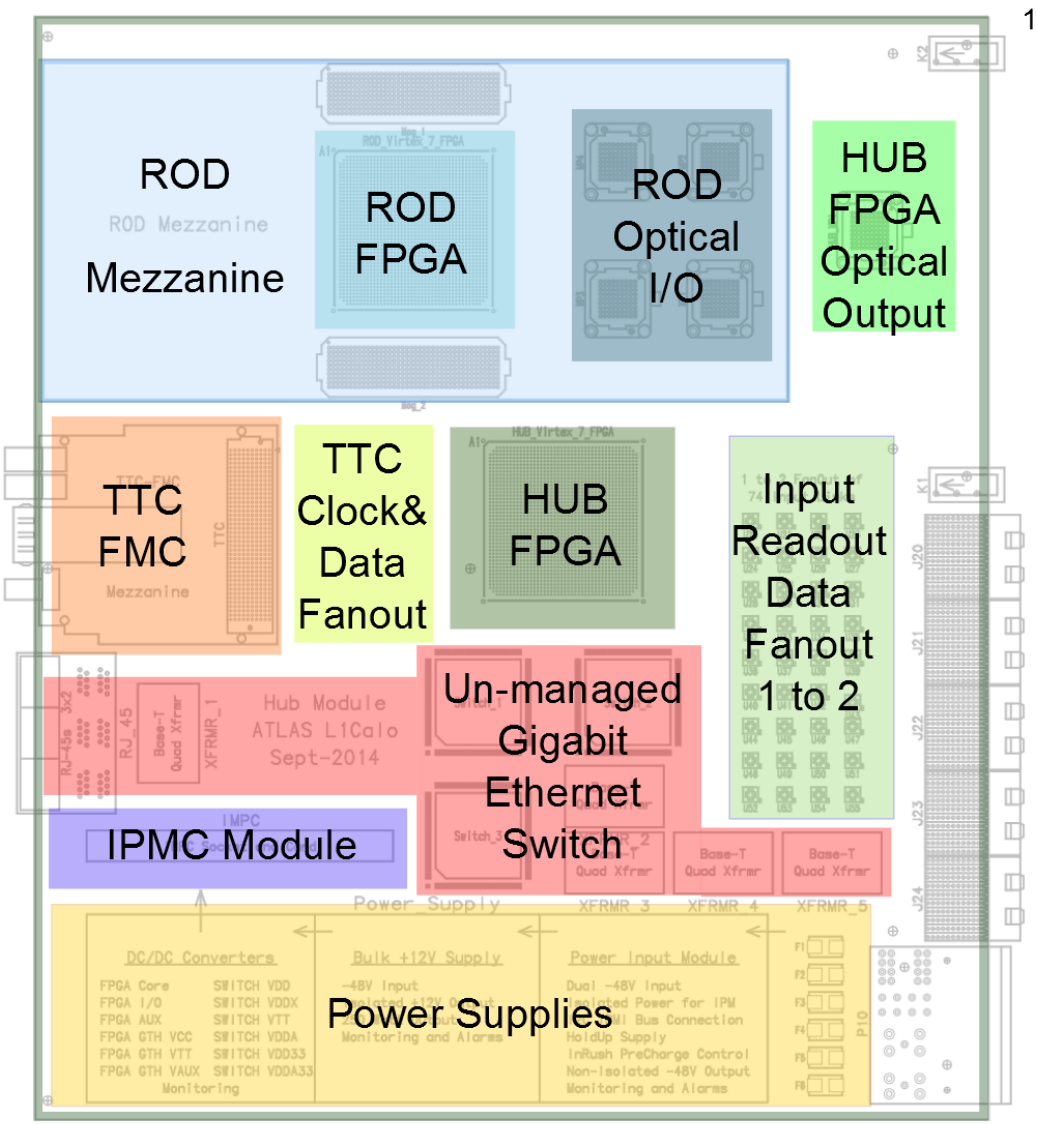


L1Calo HUB Module

Preliminary Design Review

Preliminary design review (PDR) for Hub took place Oct 1 2014

- Report available at https://edms.cern.ch/document/1415974/0.3
- Spec available at https://edms.cern.ch/nav/P:ATL-D:V0/P:ATL-0000010197:V0/TAB3

PDR was very positive, reflected good alignment of L1Calo group

- Reviewers present from all interfacing systems:
  - e/j/gFEX
  - ROD
  - TTC/FELIX
  - L1Calo/TDAQ/Physics

- The Hub design was approved, with action items
  - No show stoppers, but I will review the main points relevant to recent progress

Preliminary Design Review Actions

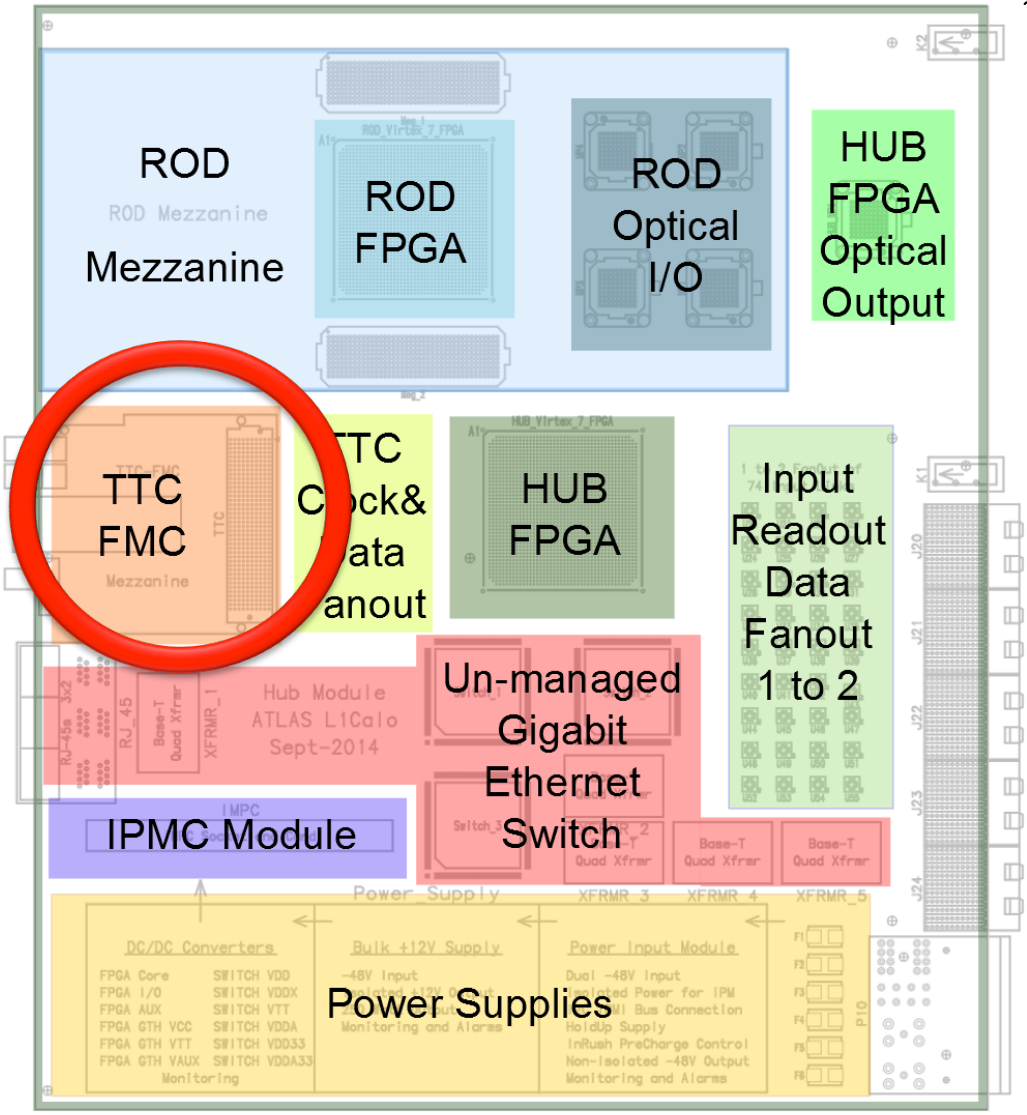
1) Investigate and finalize decision on clock/TTC interface
   - Original plan was to host a TTC-FMC mezzanine on the Hub
     - Pros: Relatively simple, know solution.
     - Cons: not future-proof; TTC-FMCs are scarce; eats a lot of space

ATCA Hub Preliminary Drawing

Since PDR, now plan to not include TTC FMC site on Hub PCB

- Frees up precious floor space for other constraints
  - Important as ROD form factor evolves
- We plan to implement a SFP interface to receive clock signals
  - Receive FELIX/GBT input in full system (& CERN integration test stand)
  - Receive GLIB+TTC FMC input in test stands requiring more than 2 shelves

Outstanding issue: still need to understand more about what we will receive & any related FW



L1Calo HUB Module

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   - Now planning on simple SFP or Mini-Pod receiver
     - Hopefully reduces (eliminates?) need for 2nd prototype run.

**MSU has 4 TTC-FMC cards available. They're scarce, so if you're looking for one just let us know.

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2) GbEthernet implementation should be streamlined & finalized
   - Larger worry about ability to get required data from manufacturers, potentially forcing us to a more complicated design.

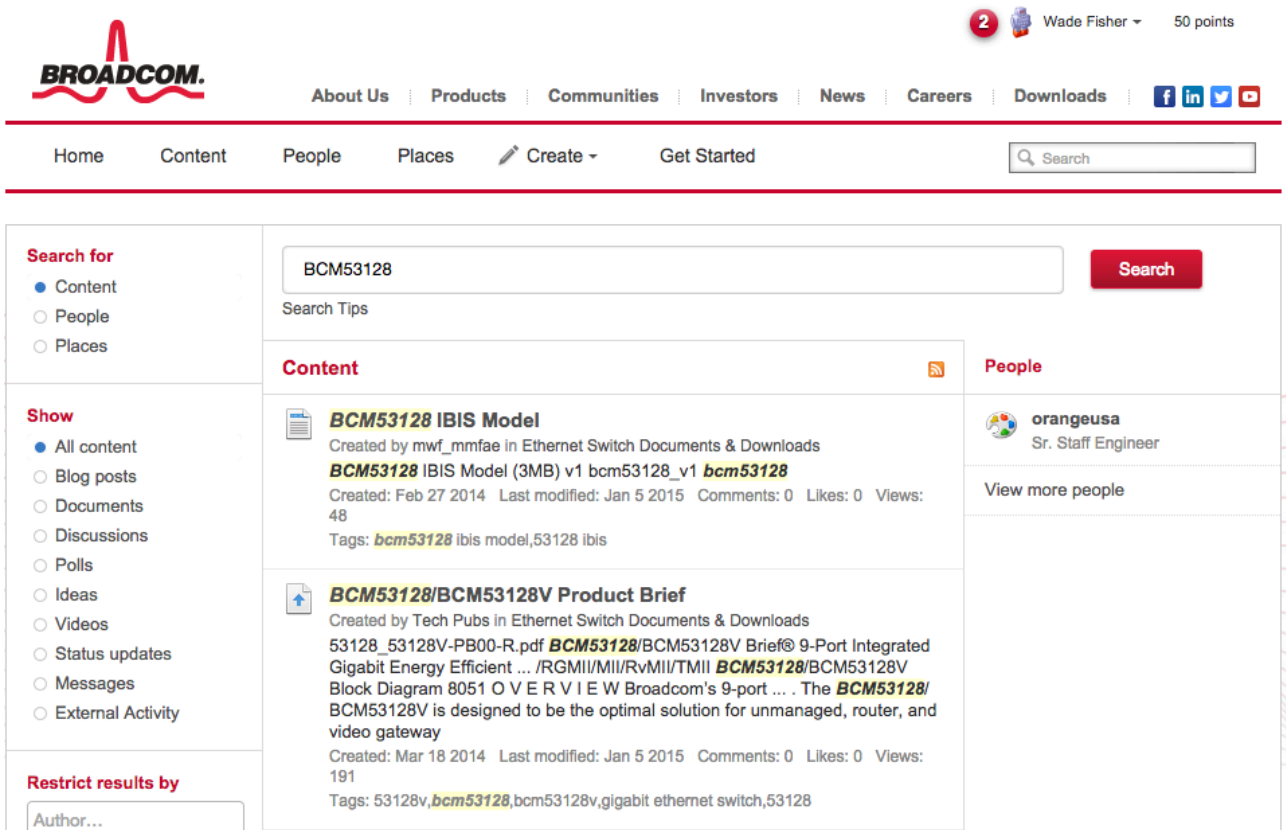
Ethernet Implementation

Implementation of Ethernet interfaces was a potential complication

- Ideally use cheap, unmanaged GbE switches for simplicity (Eg, BCM53128)
  - Detailed specs hidden by IP protections
  - MSU has made progress with Marvel and Broadcom
- Current plan: 3 8-port GbE swiches, with option to link switches

Major concern about access to GbE switch technical specs has been resolved for Broadcom switches.

* I'm happy to supply instructions for accessing to anyone who is interested.



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3) Careful studies of high-speed links in Hub-ROD data path should be finalized
   - Several worries here: ROD-Hub interface, FEX data fanout, backplane bandwidth

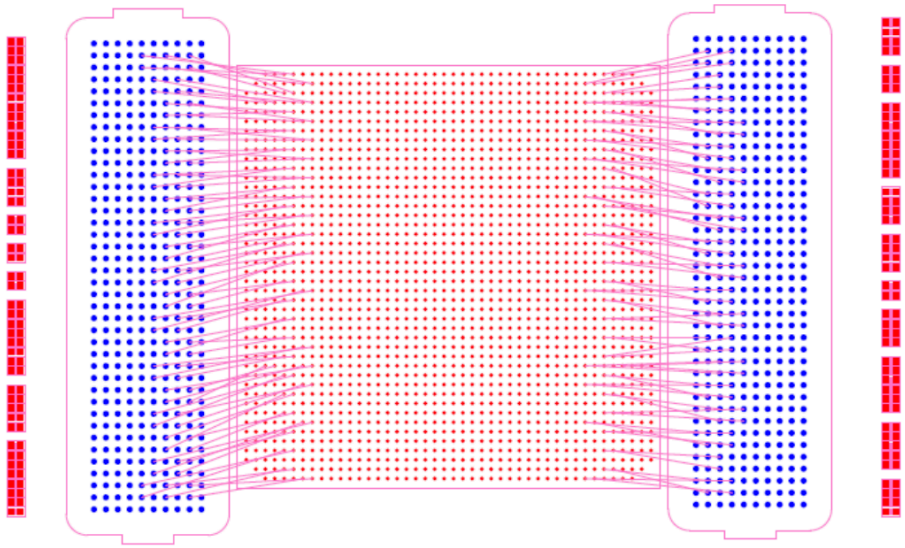
Hub-ROD Interface: Current Areas of Focus

- Signal Integrity for 10Gbps fabric interface
  - Requested to push for highest feasible backplane speed
    - Makes 74x high-speed link fanout hard
    - Potential cost impact
      - "Guaranteed success" fanout chip costs ~$300 ($24k / board!!)
      - We've agreed on a likely candidate to test: NB7VQ14M
        - » 1:4 fanout, with equalization
        - » Reasonably priced (~$8/chip)

- Signal Integrity for 10Gbps mezzanine structure
  - Considered to be a high risk aspect of the Hub-ROD architecture
  - Cadence "Sigrity" training in progress
  - Ed can say more about this in his talk

Studying Hub-ROD Signal Traces

Proposed MEG-Array to FPGA GBT Connections



- Traces are optimised as much as possible
- Does not follow the proposed scheme of having readout data on one connector
- Mapping of specific Quads to specific Readout Data (2 FEX Channels per 3 Quads) appears to be better done at Hub level
  - More degrees of freedom?

Stolen from Ed Flaherty

Studying Hub-ROD Signal Traces

Hub->ROD: Dual MEG Array 400: Proposed pin usage

Last Updated: 16-Sep-2014 **SUBJECT TO CHANGE**

Row	A	B	C	D	E	F	G	H	I	J
1	T	G	T	V	V	V	V	V	S	S
2	G	+	G	V	V	V	V	V	S	S
3	G	-	G	T	G	T	S	S	S	S
4	T	G	+	G	+	G	S	S	S	S
5	T	G	-	G	-	G	S	S	S	S
6	G	+	G	+	G	T	S	S	S	S
7	G	-	G	-	G	T	S	S	S	S
8	T	G	+	G	+	G	S	S	S	S
9	T	G	-	G	-	G	S	S	S	S
10	G	+	G	+	G	T	S	S	S	S
11	G	-	G	-	G	T	S	S	S	S
12	T	G	+	G	+	G	S	S	S	S
13	T	G	-	G	-	G	S	S	S	S
14	G	+	G	+	G	T	S	S	S	S
15	G	-	G	-	G	T	S	S	S	S
16	T	G	+	G	+	G	S	S	S	S
17	T	G	-	G	-	G	S	S	S	S
18	G	+	G	+	G	T	S	S	S	S
19	G	-	G	-	G	T	S	S	S	S
20	T	G	+	G	+	G	S	S	S	S
21	T	G	-	G	-	G	S	S	S	S
22	G	+	G	+	G	T	S	S	S	S
23	G	-	G	-	G	T	S	S	S	S
24	T	G	+	G	+	G	S	S	S	S
25	T	G	-	G	-	G	S	S	S	S
26	G	+	G	+	G	T	S	S	S	S
27	G	-	G	-	G	T	S	S	S	S
28	T	G	+	G	+	G	S	S	S	S
29	T	G	-	G	-	G	S	S	S	S
30	G	+	G	+	G	T	S	S	S	S
31	G	-	G	-	G	T	S	S	S	S
32	T	G	+	G	+	G	S	S	S	S
33	T	G	-	G	-	G	S	S	S	S
34	G	+	G	+	G	T	S	S	S	S
35	G	-	G	-	G	T	S	S	S	S
36	T	G	+	G	+	G	S	S	S	S
37	T	G	-	G	-	G	S	S	S	S
38	G	+	G	T	G	T	S	S	S	S
39	G	-	G	V	V	V	V	V	S	S
40	T	G	T	V	V	V	V	V	S	S

Notes
(1)Differential Signal polarities are arbitrary: there may be a case for re-arranging them.
(2) Terminator pins have 50Ω to Ground: not fully established if better than Grounds
(3) The Signal pins are available for the other ROD-Hub signals
[4] Pins rated at 0.45 A/pin, so 20 OK for 9A: i.e. 108 W at 12V. All 12V on one connector?
[5] Mate/Un-Mate forces for 400 pins are 140/80N
[6] Only have to route Differential Pairs 4 columns back: simpler, less layers?

Signal Pairs	0	10	9	8	9	0	0	0	0	0
Grounds	20	20	20	18	18	18	0	0	0	0
Terminators	20	0	2	2	0	18	0	0	0	0
12V Power	0	0	0	4	4	4	4	4	0	0
Other Signals	0	0	0	0	0	0	36	36	40	40

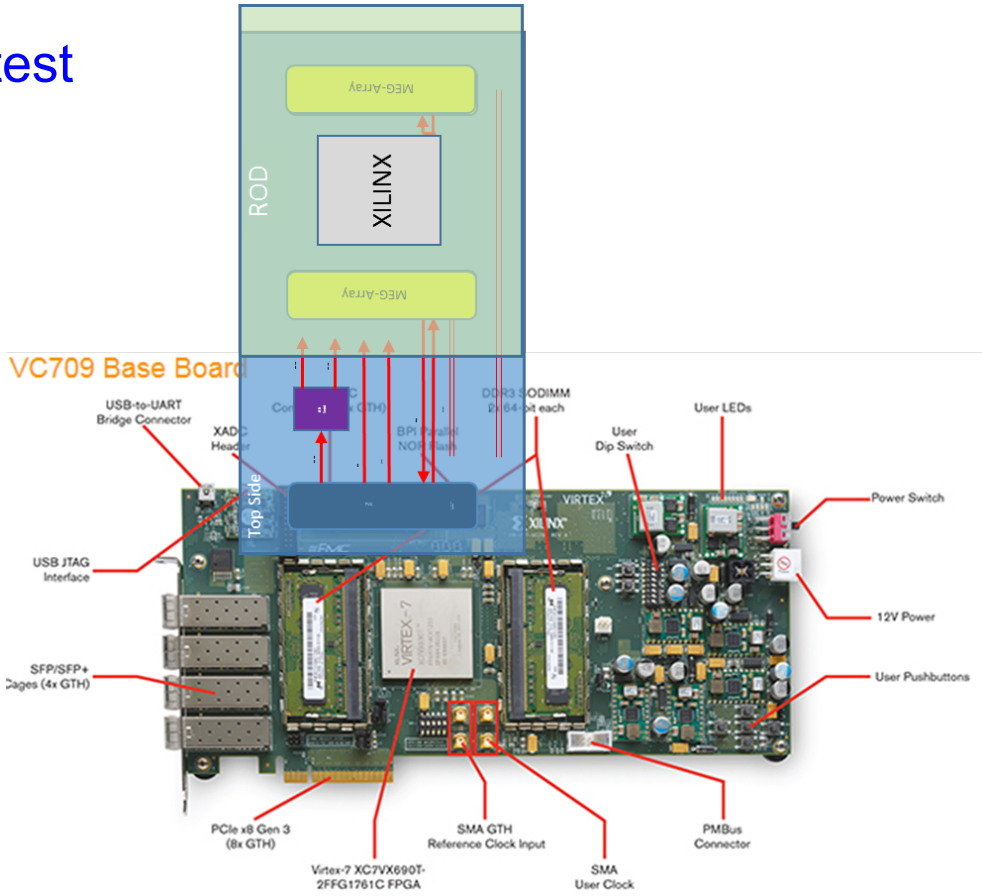
Total Pins	
for Signal Pairs	72
Grounds	114
Terminators	42
12V Power	20
Other Signals	152
Total Totals	400

Note: this diagram is in flux, this is not the current picture.

ROD Test/Host Platform

Test platform designed to interface with Xilinx test board (VC709)

- Provides a wide range of possible test capabilities
- Study signal link layout and signal splittings



Stolen from Ed Flaherty

Prototype Module Production

- MSU is hoping to begin purchasing components for prototype boards
  - And also production boards where it makes sense.
  - Need to know the total number of Hub prototypes

- Current Prototype Plans:
  - Full 2-Hub setups:
    - MSU, CERN (4 total)
  - Single-Hub setups:
    - Rutherford, Brookhaven, Birmingham/Cambridge (3 total)
    - Anyone else? Need to know soon.

- Outstanding question about who pays for test rig modules.
  - Should resolve this in the context of counting # prototypes.

Summary

- The ATCA FEX Hub project is coming along well
  - Several worries have been resolved, a few remain
    - Interactions with L1Calo community very positive, very productive
- PDR complete, design approved
  - Action items are not painful and we're on track addressing them
    - A few have potential impact on project, but nothing implying changes to budget/schedule
- We're continuing forward on prototype design, with the goal of delivery to CERN Sept 2015.