Joint L1Calo Meeting

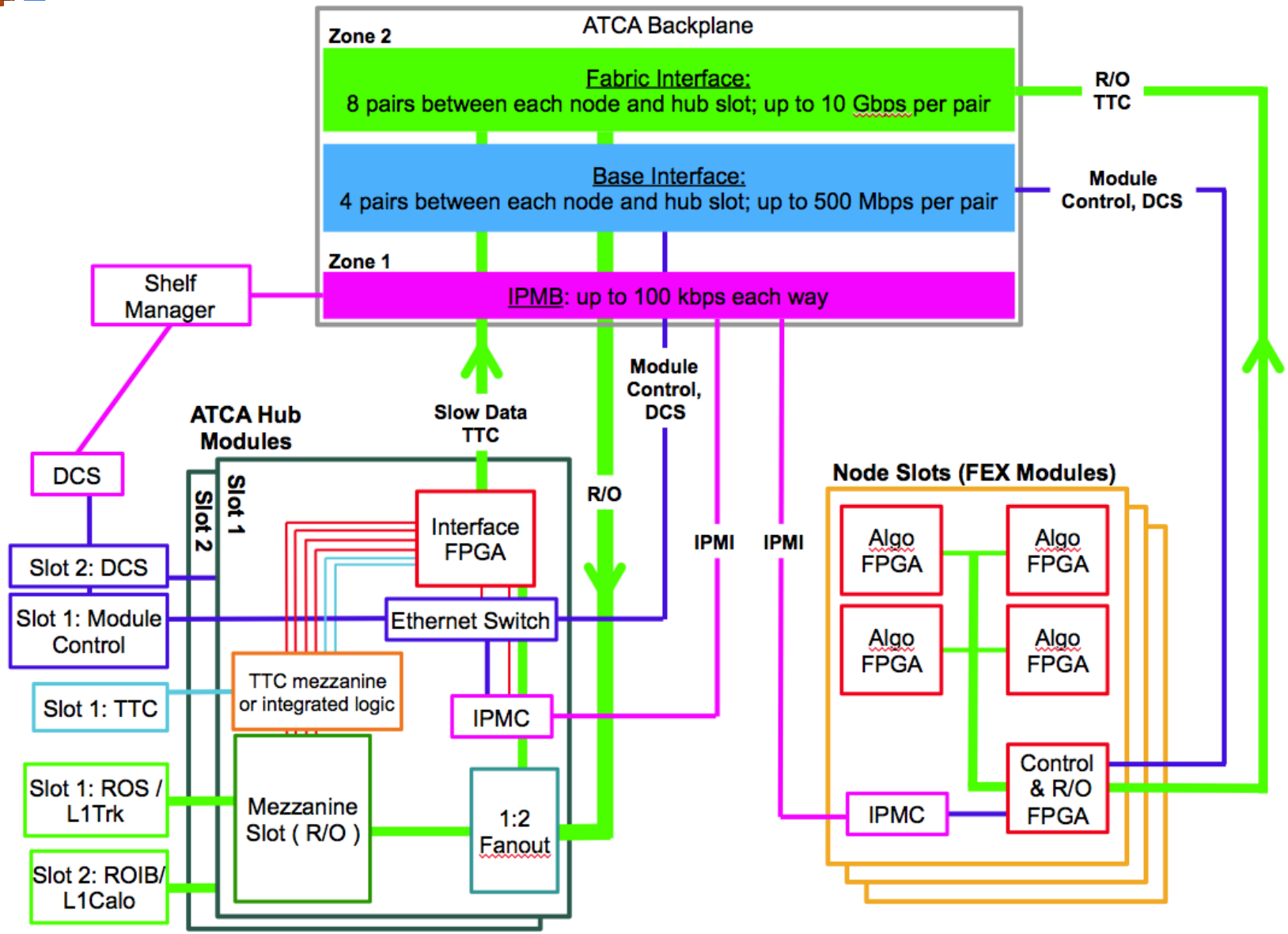
Status of the FEX ATCA Hub Project

Wade Fisher, Dan Edmunds, Philippe Laurens, Yuri Ermoline

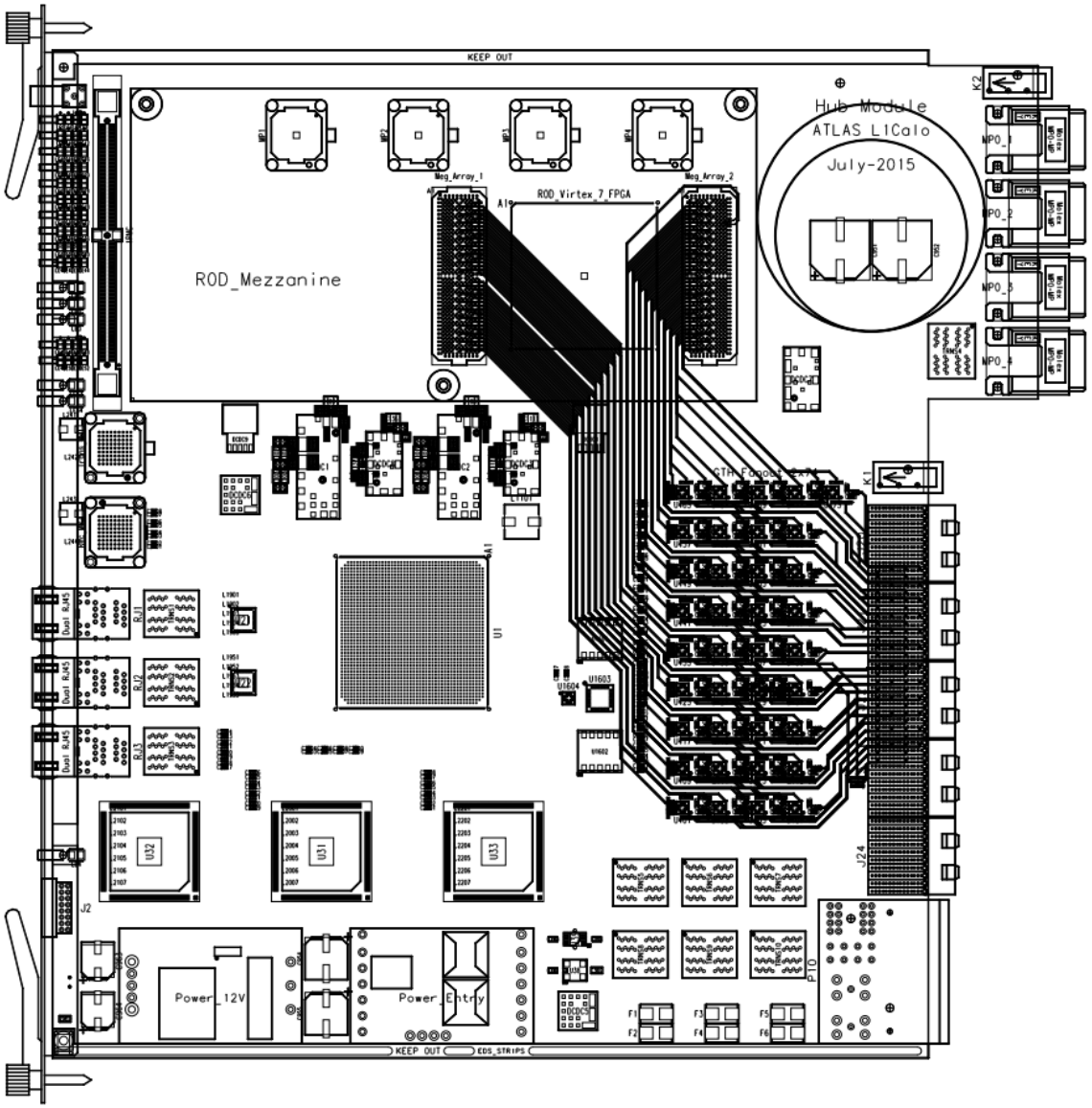
01 October 2015

MICHIGAN STATE UNIVERSITY

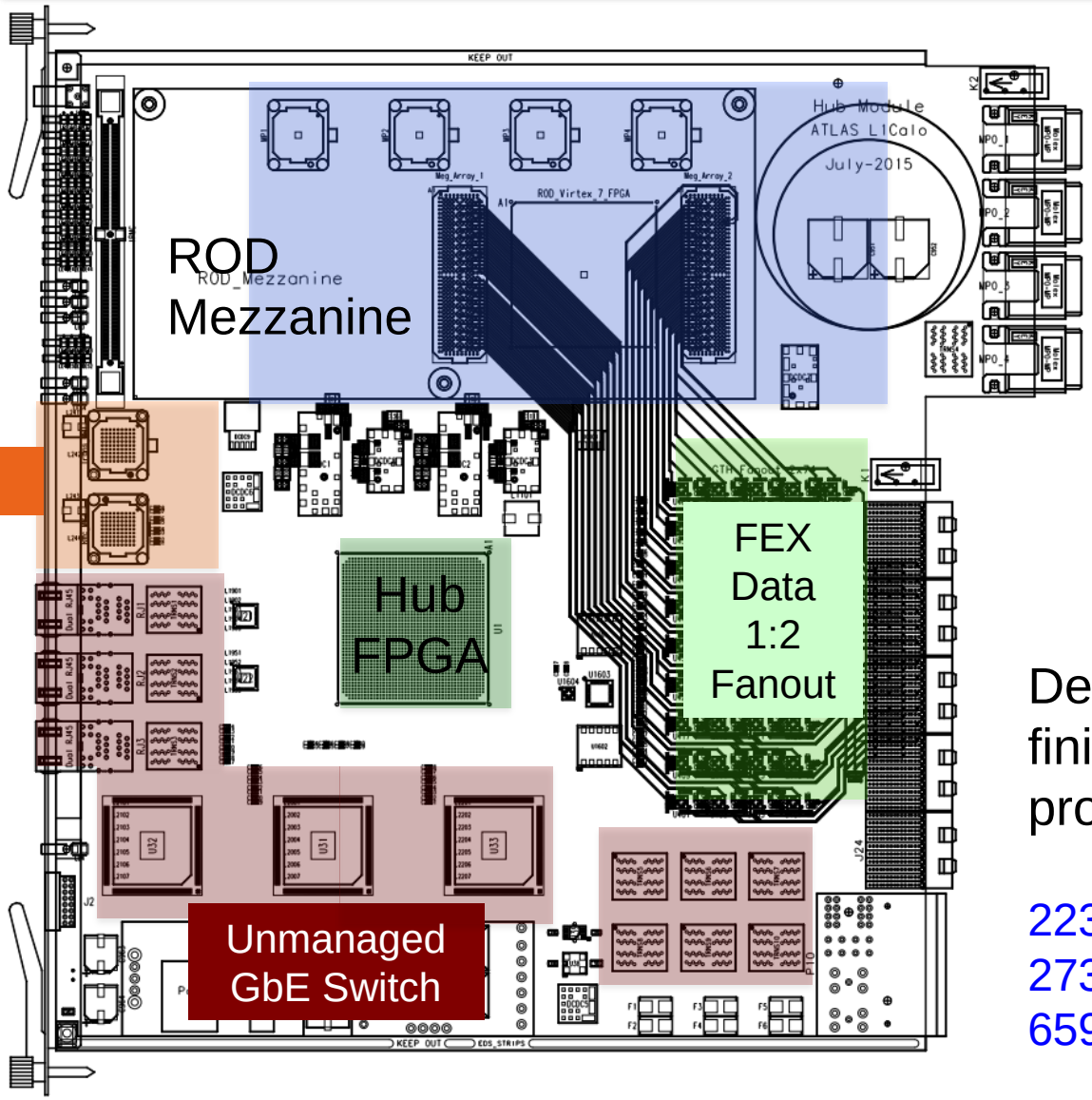
FEX ATCA Hub


ATCA Backplane
Zone 2
Fabric Interface:
8 pairs between each node and hub slot; up to 10 Gbps per pair
Base Interface:
4 pairs between each node and hub slot; up to 500 Mbps per pair
Zone 1
IPMB: up to 100 kbps each way
R/O
TTC
Module
Control, DCS
Shelf
Manager
Slow Data
TTC
Module
Control,
DCS
ATCA Hub
Modules
Slot 1
Slot 2
DCS
Slot 2: DCS
Slot 1: Module
Control
Slot 1: TTC
Slot 1: ROS /
L1Trk
Slot 2: ROIB/
L1Calo
Interface
FPGA
Ethernet Switch
TTC mezzanine
or integrated logic
IPMC
Mezzanine
Slot (R/O)
1:2
Fanout
R/O
IPMI
IPMI
Node Slots (FEX Modules)
Algo
FPGA
Algo
FPGA
Algo
FPGA
Algo
FPGA
Control
& R/O
FPGA
IPMC

ATCA Hub Current Drawing



ATCA Hub Current Drawing



Design essentially finished, routing in progress

2239 components,
2736 nets,
6594 connections

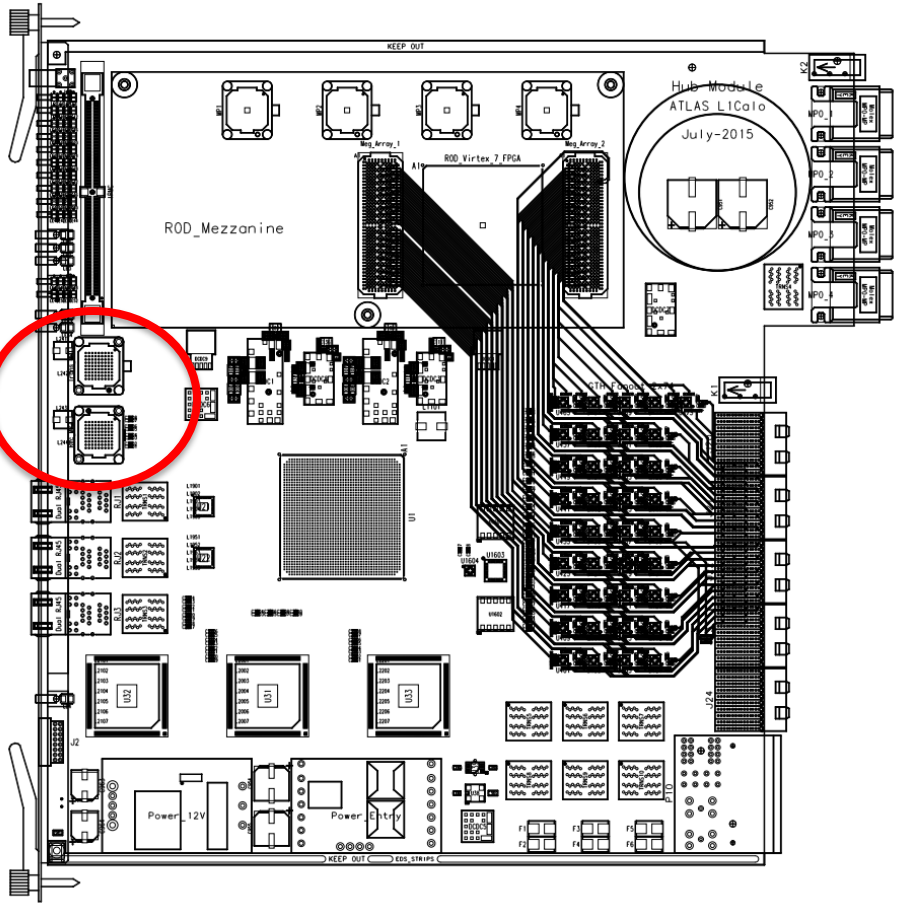
Design Changes: TTC/Clock

TTC/Clock interface

- Original design included a TTC FMC mezzanine card, swapped out for SFP+
- Current design removes SFP+, replace with spare MiniPod capacity

Anticipating future needs

- Tx/Rx MiniPods previously included to allow for potential for direct Hub/FELIX interface
- Removing SFP+ frees needed floor space
- Allows all optical interfaces to be located in RTM; plan for sharing of MTP connectors with ROD has been established



Design Changes: Backplane Speeds

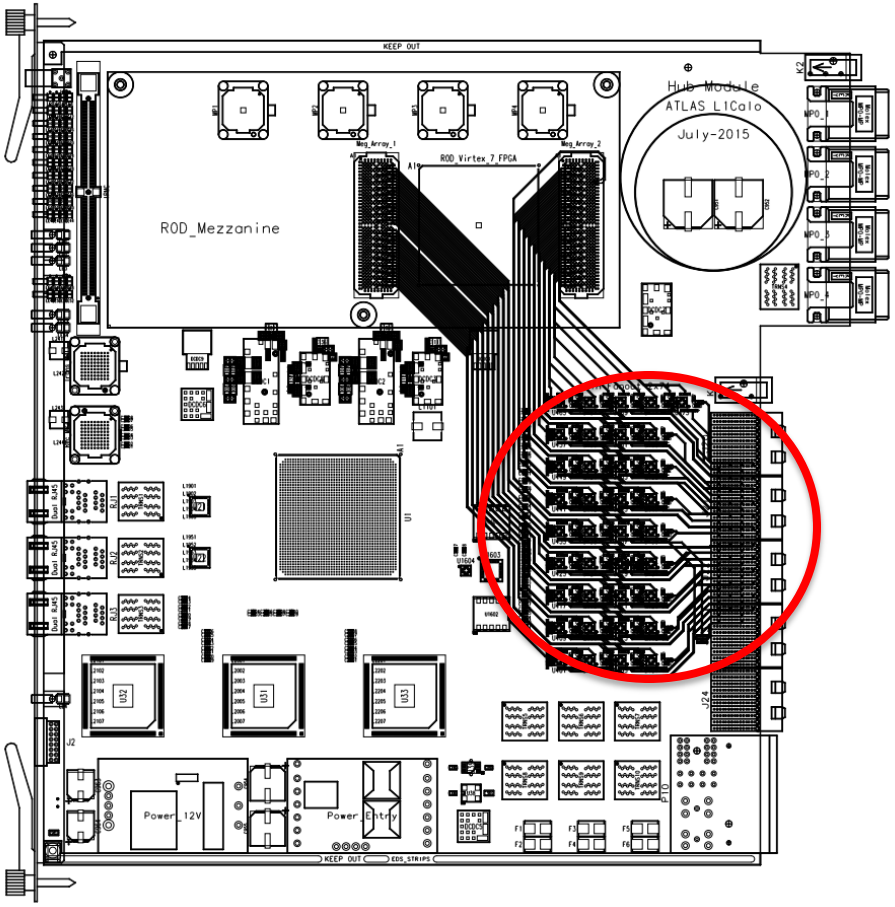
Backplane link speed options have been reduced

- July 2015: 10.26 Gbps option was eliminated
- Currently supported Hub speeds: 4.8, 6.4, 9.6 Gbps (3.2 gone?)

Zone 2 Fabric Traffic: potentially different link speeds

- FEX➔Hub➔ROD
- Clock➔ROD/FEX
- TTC➔ROD/FEX
- Hub1/2➔Hub2/1

Note: FELIX interface may change slightly in Phase-2, but Lorne has confirmed Phase-1 Tx speeds will be supported.



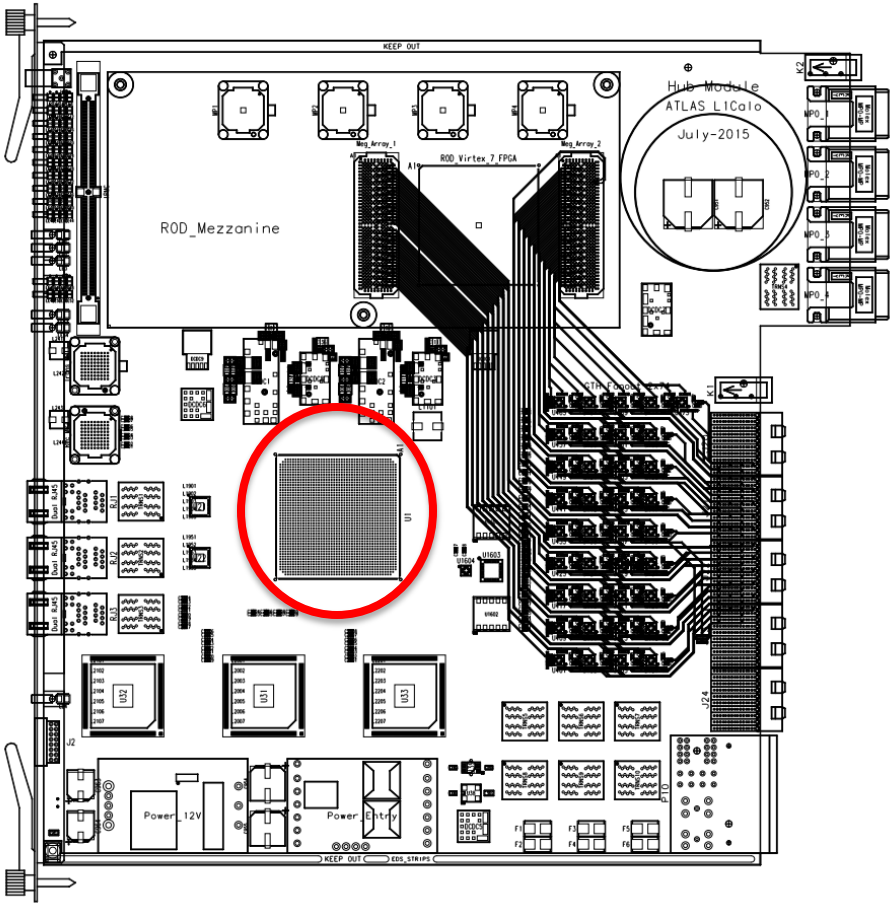
Design Changes: FPGA Choice

Serious study of pro/con for migration from Virtex-7 to Virtex-Ultrascale

- Previous FPGA choice: XC7VX550T/690T (80 MGTs)
- Ultrascale options: XCVU125/160 (80 / 104 MGTs)

Driving considerations

- Can design to the XCVU160
  - Pin compatible with XCVU125
  - Option to fully connect MiniPod channels
  - Cost-neutral with XC7VX1125T (smallest V7 with sufficient MGTs)
- XC7VX550 ➔ XCVU125: 3x in effective logic
  - Ensure option to emulate ROD-like functionality
  - Opens many doors at Phase-2
- Simplifies Hub routing
  - Ultrascale MGT quads have 2 QPLLs; V7 has 1 QPLL, 1 CPLL
- Long-term support more favorable



Design Changes: IPMC

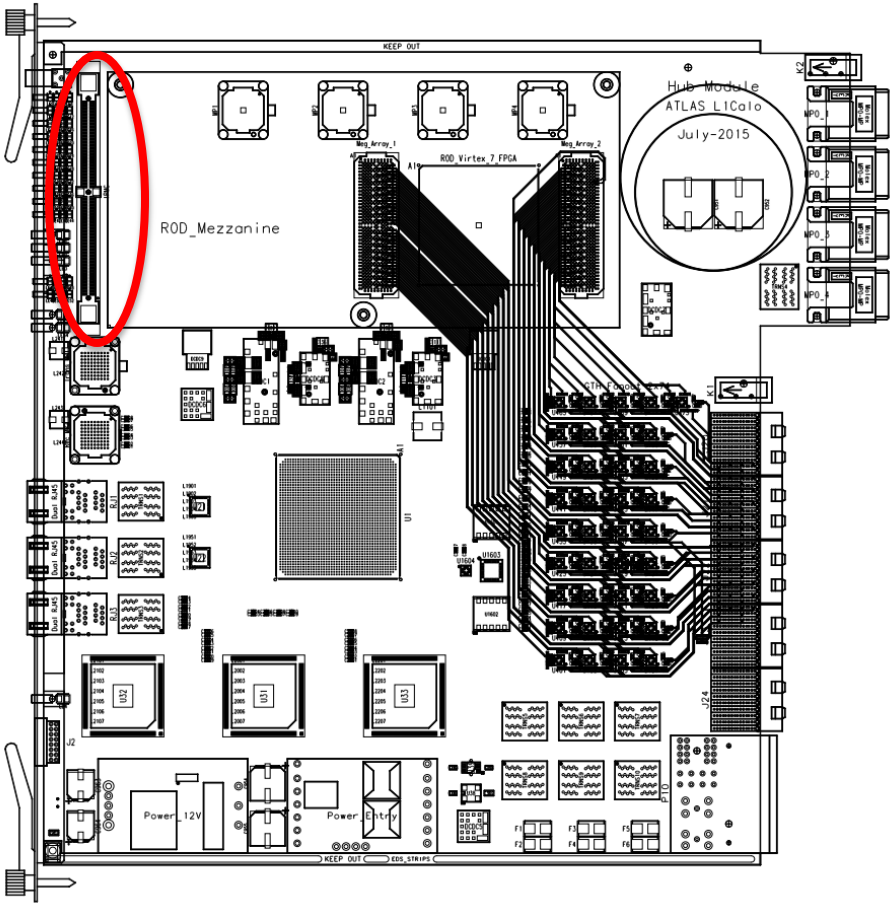
Not so much a design change as change in understanding

- We require that the IPMC provide geographical information
- Important: shelf number

This IPMC functionality was previously in question

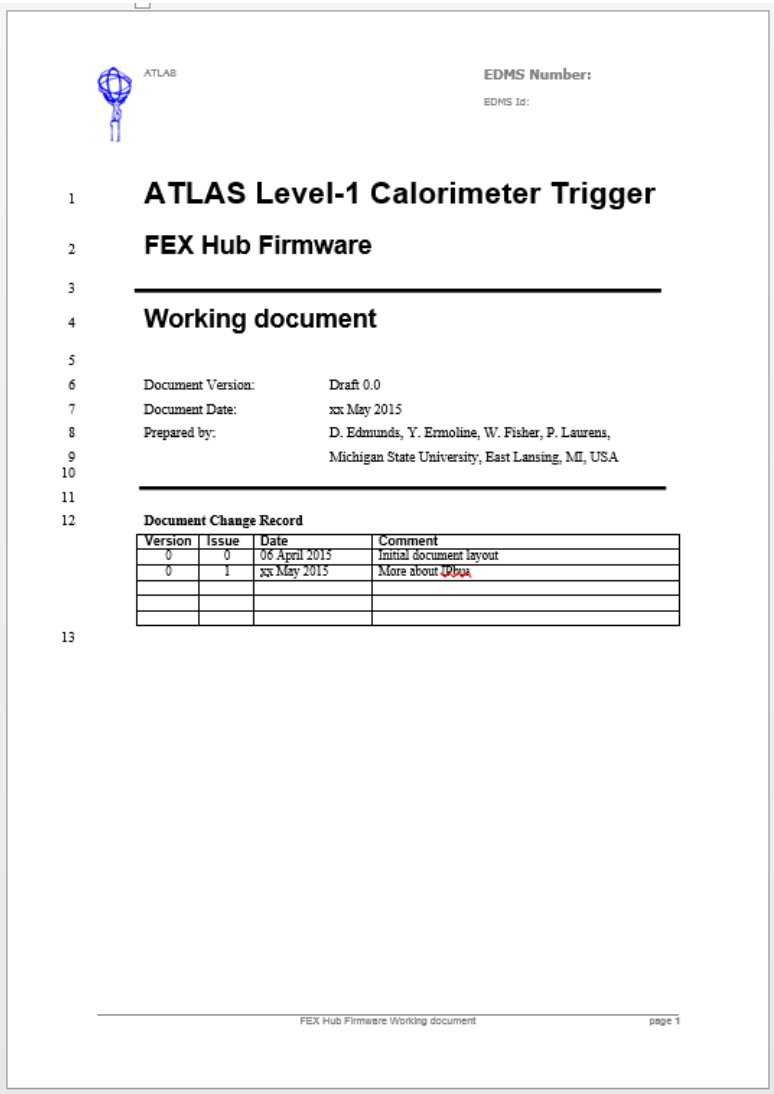
- This functionality would otherwise have to be established ad hoc

- Stony Brook LAr team has established IPMC-Shelf manager communications
  - Blade power and hot-swap functions appear to be capable
  - Currently no support for mezzanine communication / power management
  - We weren't counting on this in our ROD/Hub design



Hub Firmware

- HUB FW working document:
  - Interfaces to the HUB FPGA
    - FEX/ROD data
    - GBT interface
    - IPbus interface
    - Others (e.g. – MiniPOD)
- Start with the IPbus interface
  - CACTUS FW design examples
    - use as starting point
  - Use vc709 demo board
    - adapting kc705 example
  - Not exactly HUB HW
    - no PHY chip and copper Eth
  - Useful exercise (still not finished)
    - ISE14.7 and Vivado for V7
    - Need more RAM to run
    - VM, licences, board programming…



ATLAS

EDMS Number:

EDMS Id:

ATLAS Level-1 Calorimeter Trigger

FEX Hub Firmware

Working document

Document Version: Draft 0.0

Document Date: xx May 2015

Prepared by: D. Edmunds, Y. Ermoline, W. Fisher, P. Laurens, Michigan State University, East Lansing, MI, USA

Document Change Record

Version	Issue	Date	Comment
0	0	06 April 2015	Initial document layout
0	1	xx May 2015	More about IPbus

FEX Hub Firmware Working document page 1

Hub Schedule

- Layout/design essentially complete at this time
  - Routing in progress
    - Currently aiming at Ultrascale chip implementation
    - Xilinx delivery quote at 10 weeks puts assembly date in mid-December / early January
      - Represents a ~1 month delay on previous schedule

- Current plan
  - Fabricate blank board for electrical tests (2015)
  - Fab / Assemble test board without FPGA (1/2016)
    - Validate fab process / stack-up
  - Proceed to prototype construction (2/2016)
    - March 2016 commissioning date

Summary

- The ATCA FEX Hub project is coming along well
  - Several worries have been resolved, a few remain
    - Backplane link speed remains to be demonstrated
    - Move to Ultrascale introduces a delay, but not critical
- Firmware effort progressing in parallel
  - Nominal expectation that Ultrascale/V7 transition not disruptive
    - Indications so far are promising
- We're continuing forward on prototype design, with the goal of prototypes in Q1 2016.