# Joint L1Calo Meeting

# Status of the FEX ATCA Hub Project

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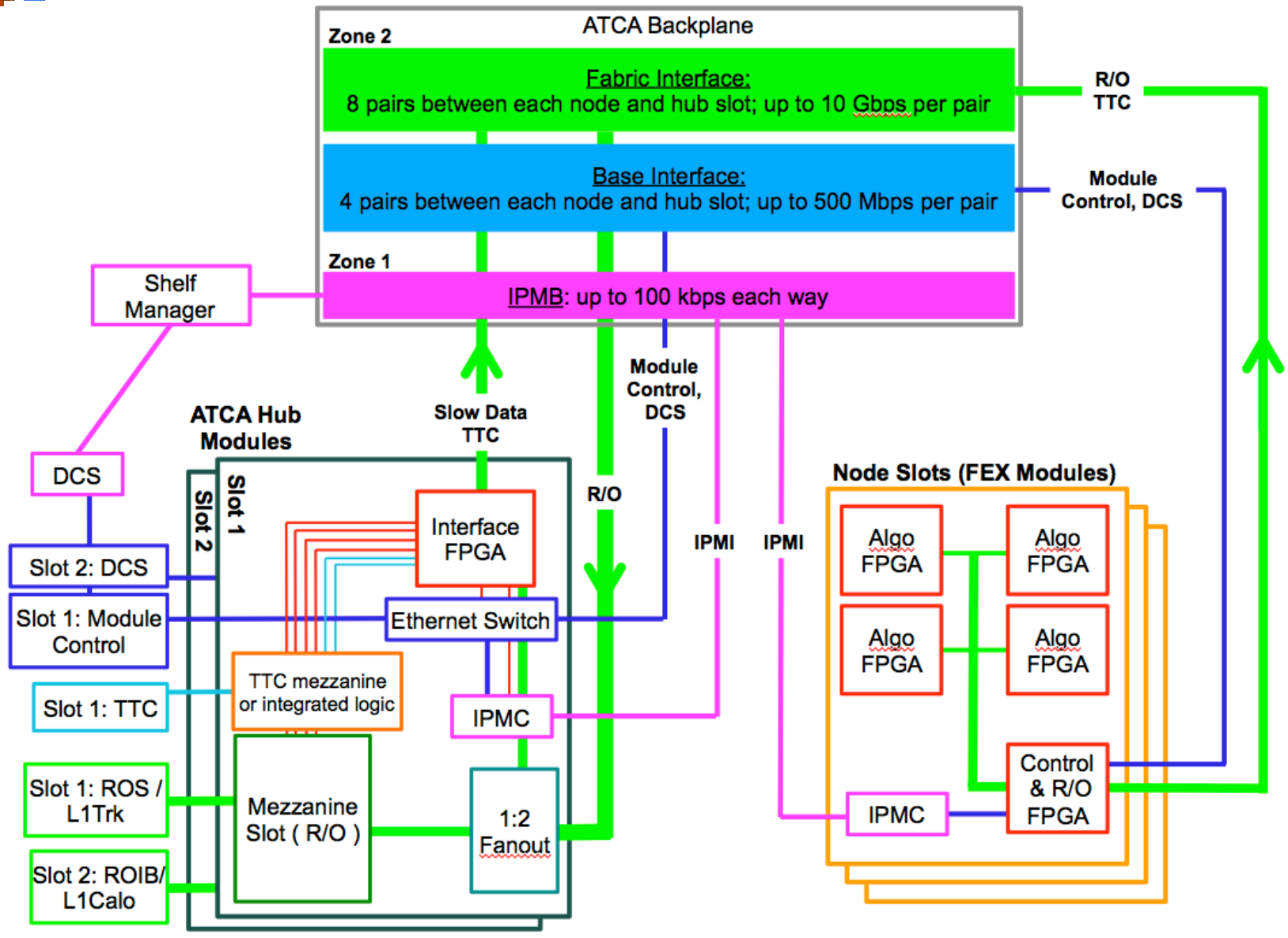
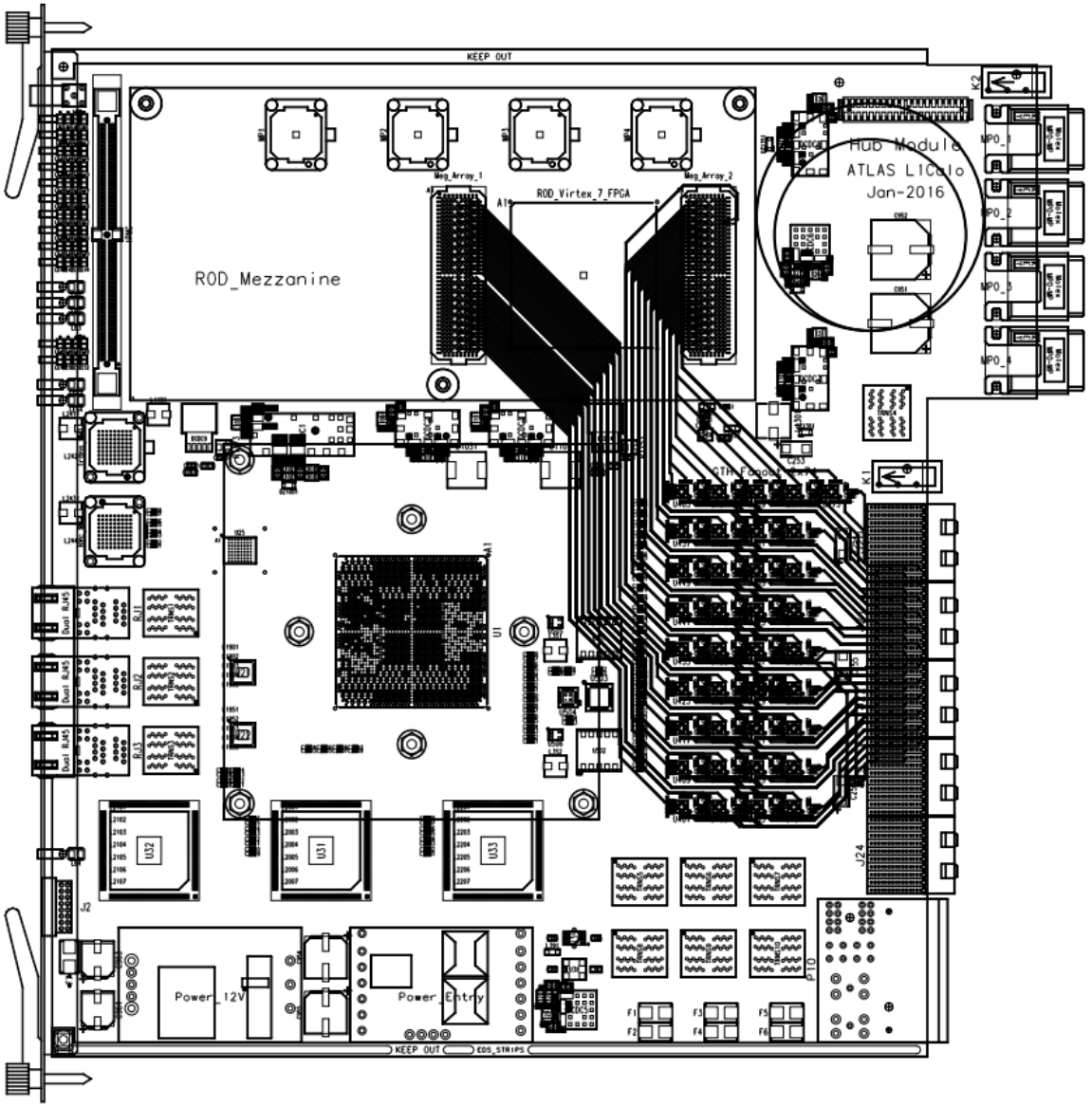
MICHIGAN STATE UNIVERSITY

# FEX ATCA Hub


ATCA Backplane
Zone 2
Fabric Interface:
8 pairs between each node and hub slot; up to 10 Gbps per pair
Base Interface:
4 pairs between each node and hub slot; up to 500 Mbps per pair
Zone 1
IPMB: up to 100 kbps each way
R/O
TTC
Module
Control, DCS
Shelf
Manager
Slow Data
TTC
Module
Control,
DCS
ATCA Hub
Modules
Slot 1
Slot 2
DCS
Slot 2: DCS
Slot 1: Module
Control
Slot 1: TTC
Slot 1: ROS /
L1Trk
Slot 2: ROIB/
L1Calo
Interface
FPGA
Ethernet Switch
TTC mezzanine
or integrated logic
IPMC
Mezzanine
Slot ( R/O )
1:2
Fanout
R/O
IPMI
IPMI
Node Slots (FEX Modules)
Algo
FPGA
Algo
FPGA
Algo
FPGA
Algo
FPGA
Control
& R/O
FPGA
IPMC

# ATCA Hub Current Drawing



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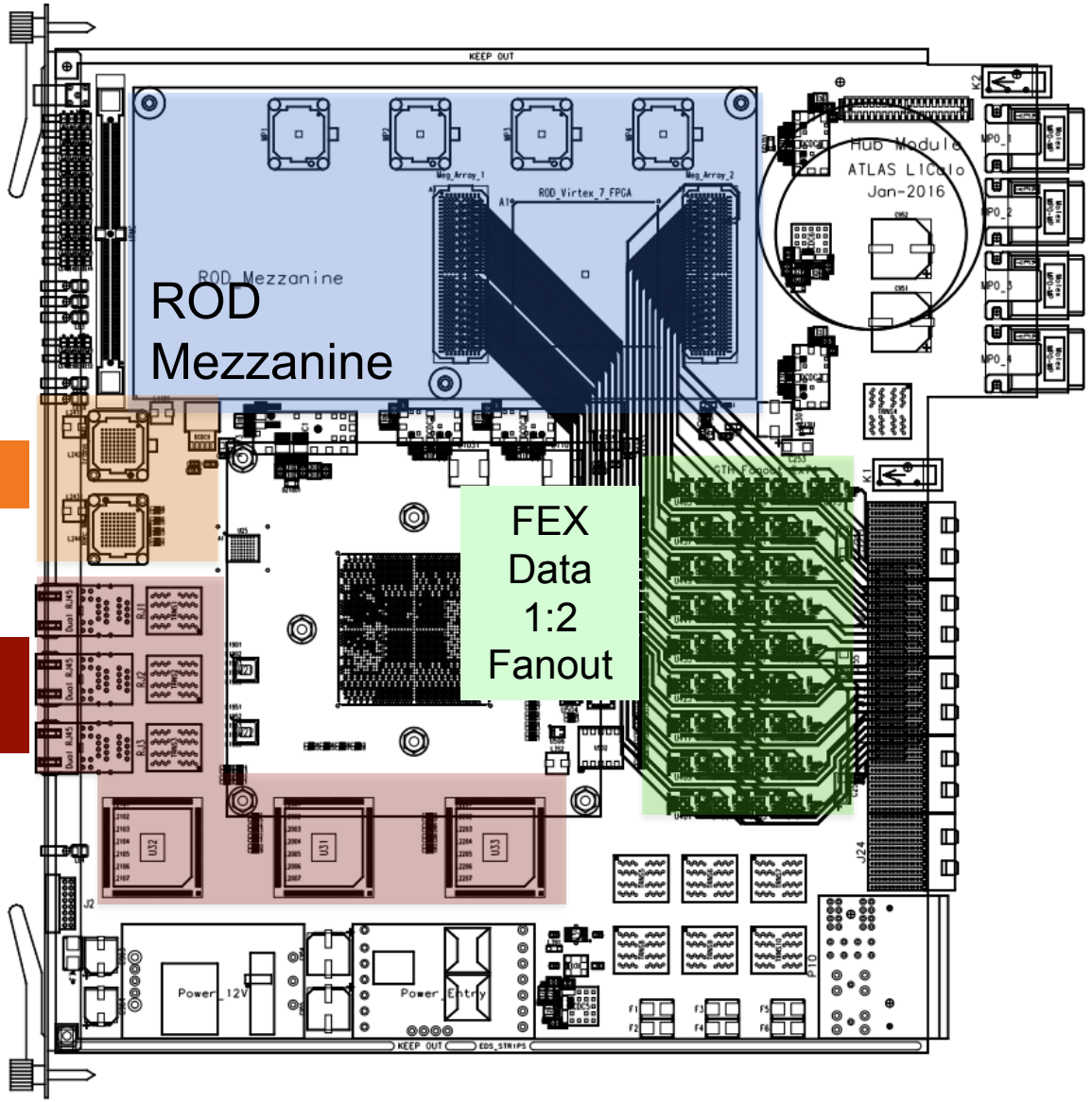


# Final Decision: Backplane Speeds

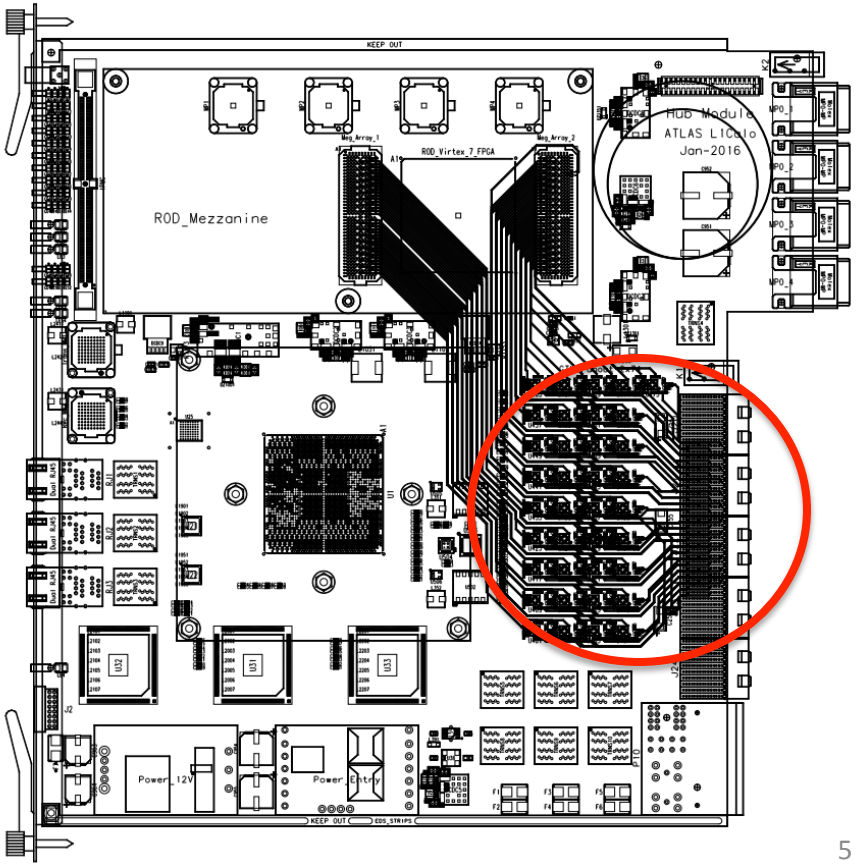
Backplane link speed options have been reduced

- July 2015: 10.26 Gbps option was eliminated.
- Oct 2015: No use case for 3.2 Gbps foreseen: eliminated.
- Currently supported Hub speeds: **4.8, 6.4, 9.6 Gbps**

Zone 2 Fabric Traffic: anticpate different link speeds

- FEX⇨Hub⇨ROD (9.6 Gbps)
- Clock/TTC⇨ROD/FEX (4.8 Gbps)
- Hub1/2⇨Hub2/1 (4.8 Gbps)

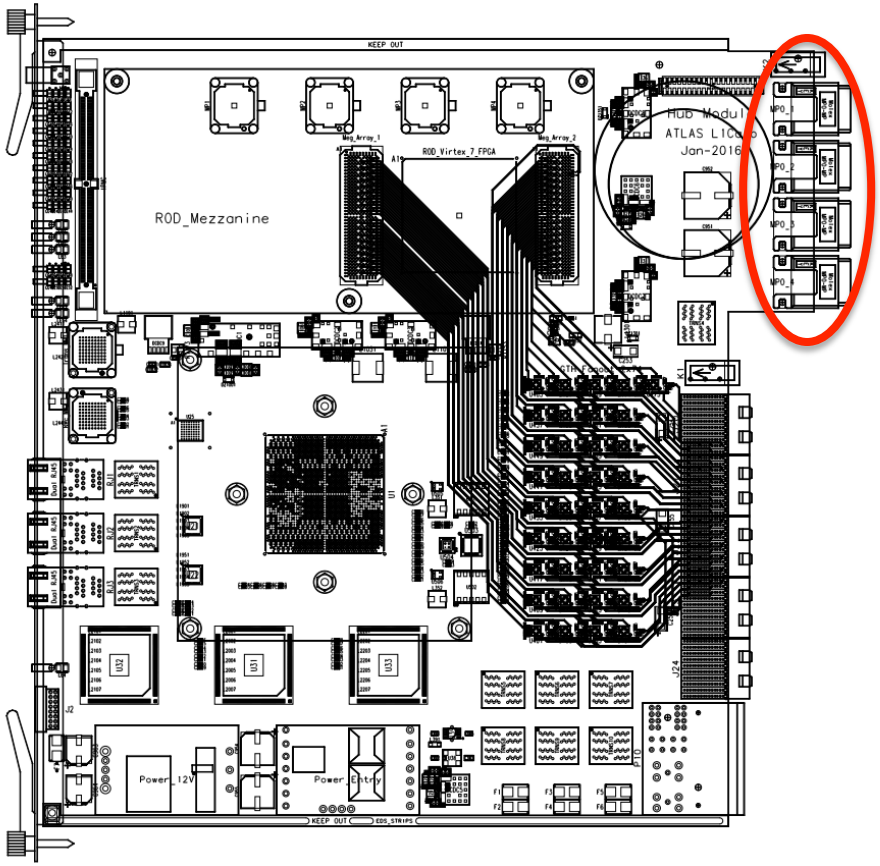
Note: FELIX interface may change slightly in Phase-2, but Lorne has confirmed Phase-1 Tx speeds will be supported.



# Final Decision: Optical Signal Routing

Given front-panel space limitations, current design plans to use RTM for optical signal feed-through

- Sharing agreement with ROD has been struck
- No apparent conflicts in the several use cases investigated



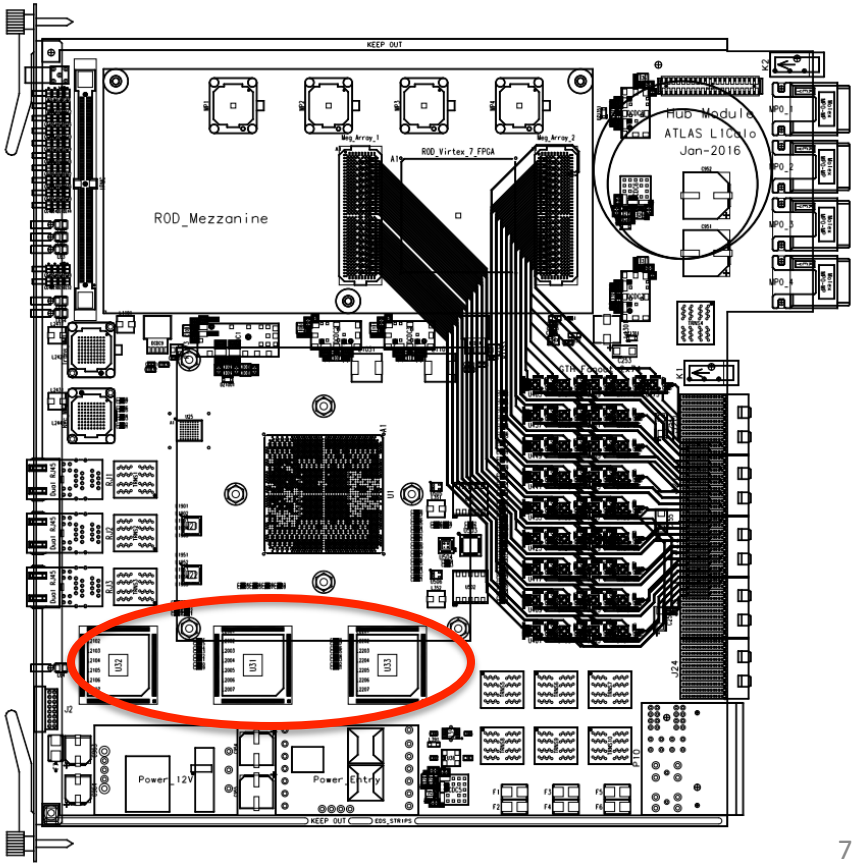
# Final Decision: GbE Interconnect

Multi-port gigabit Ethernet via bonded 8-channel chips

- Provides sufficient FEX, Hub and outside connections
- Independent networks on each hub maximize FEX Ethernet bandwidth

Design choices

- Front-panel jumpers in initial design retained
  - Choice maximizes board flexibility, see next slide
  - Test-bench/single-Hub usage improved with direct access to ROD, Hub and IPMC
- Option to split to three independent GbE networks per Hub may not be feasible
  - Prototype design has insufficient front-panel space to host extra ports
  - Exploring internal logic to switch between connection options.



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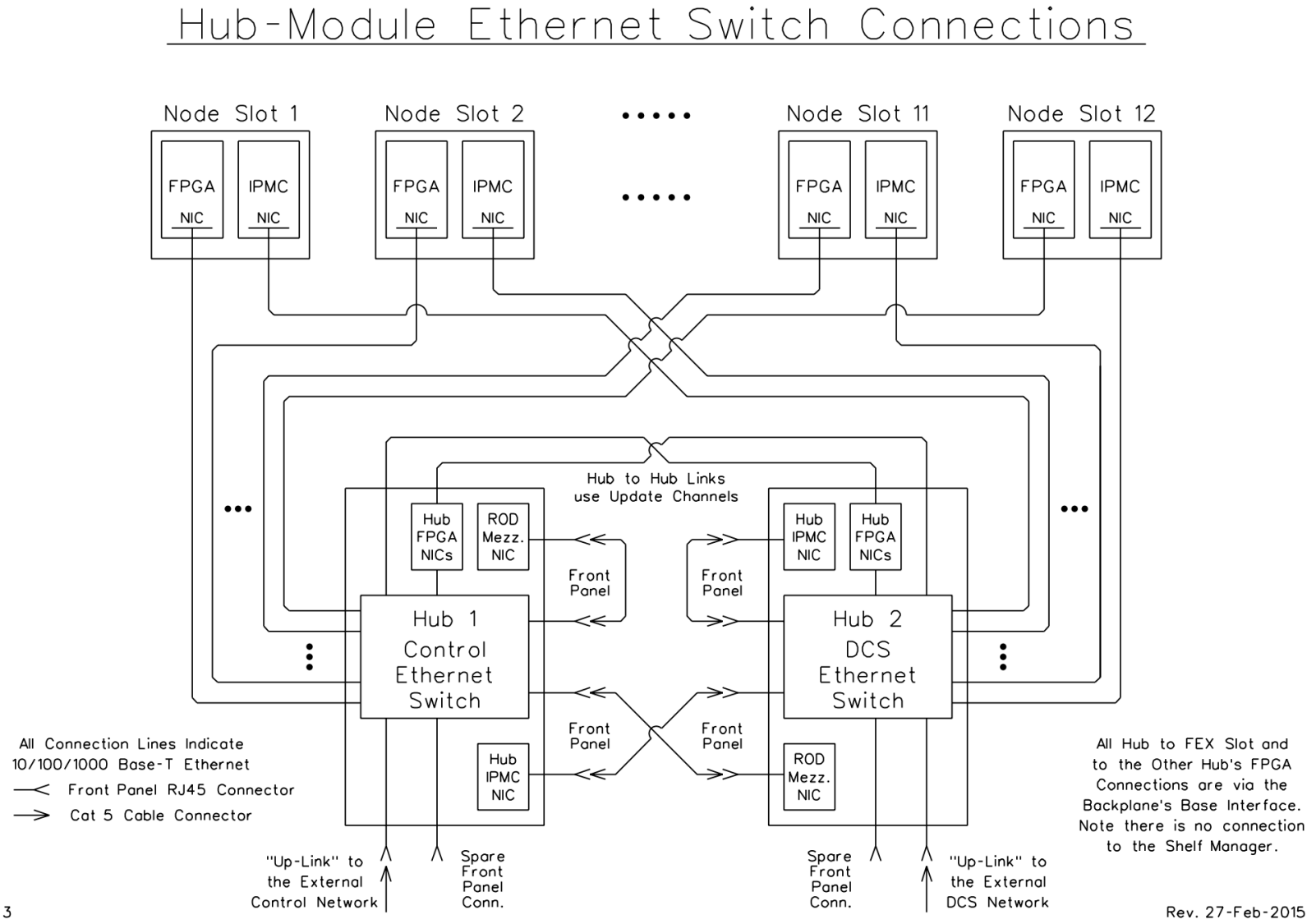


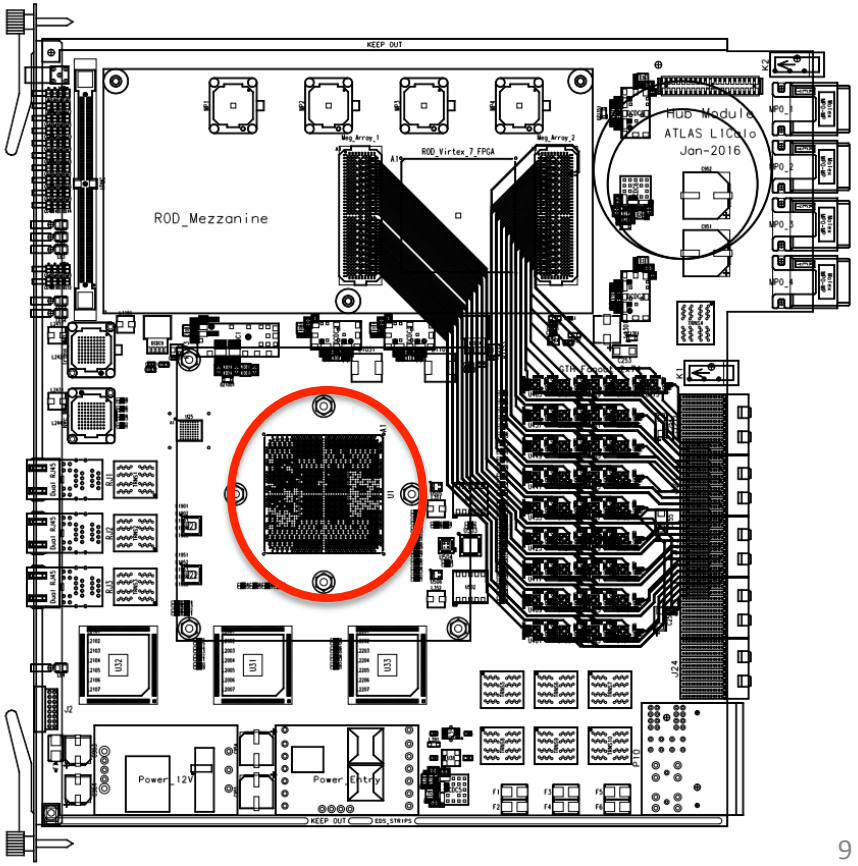
# FPGA Choice

Finalized decision to migrate from Virtex-7 to Virtex-Ultrascale

- Previous FPGA choice: XC7VX550T/690T (80 MGTs)
- Ultrascale options: XCVU125 (80 MGTs)

Driving considerations

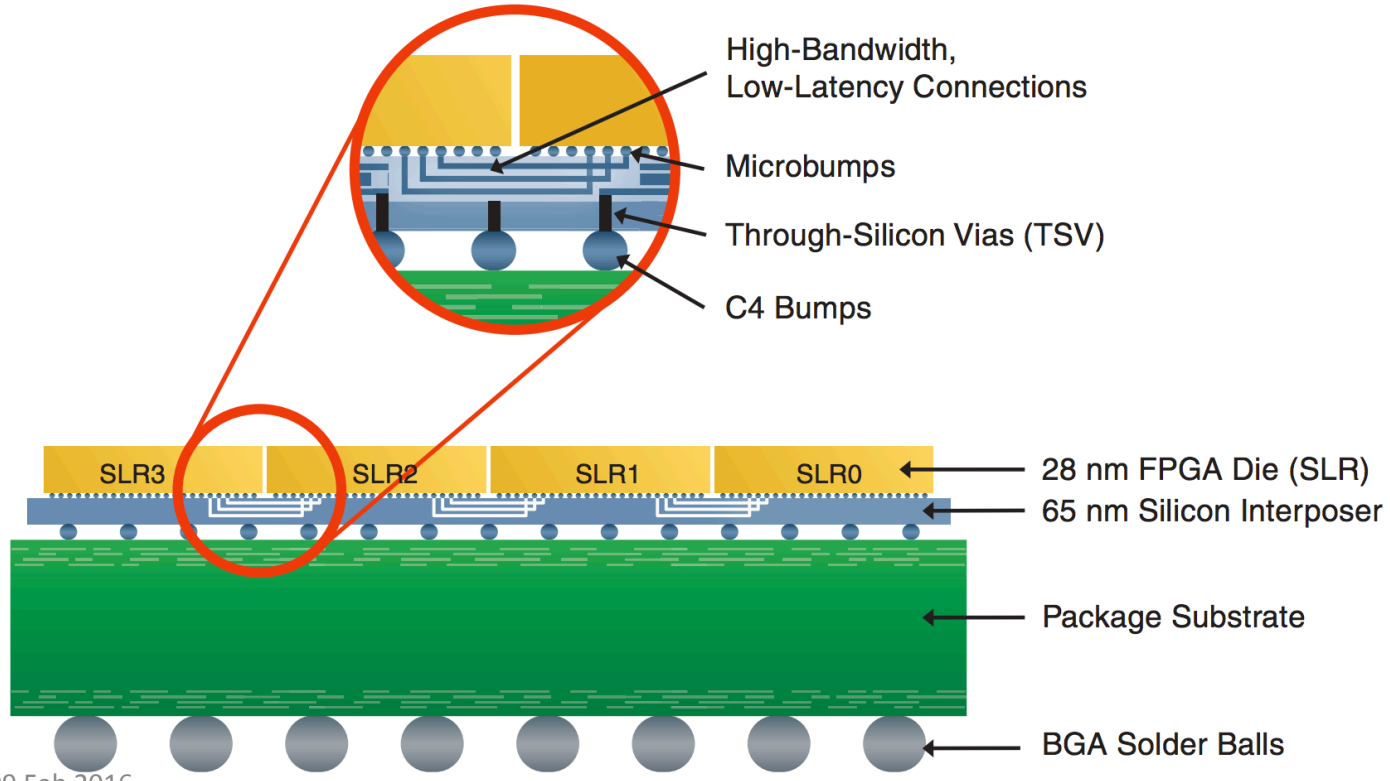
- Can design to the XCVU160
  - Pin compatible with XCVU125
  - Option to fully connect MiniPod channels
  - Cost-neutral with XC7VX1125T (smallest V7 with sufficient MGTs)
- XC7VX550 ⇨ XCVU125: 3x in effective logic
  - Ensure option to emulate ROD-like functionality
  - Opens many doors at Phase-2
- Simplifies Hub routing
  - Ultrascale MGT quads have 2 QPLLs; V7 has 1 QPLL, 1 CPLL
- Long-term support more favorable



# Ultrascale Nuances

Next-gen Xilinx chips host new “stacked silicon interconnect” design

- Multiple silicon die (Super Logic Regions, SLR) hosted on a single chip
  - Bonded with image sensor microbump tech, hosting “through-silicon vias”
- SSI chips behave somewhat differently than single-die chips
  - High bandwidth timing and I/O connections need careful consideration



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Range of best-practices to be found deep in Xilinx literature

- Place clock pin / MMCMs in same SLR as timing critical I/O interfaces (avoid driving timing critical I/O interfaces from a different SLR)
- Clock pin choices should be balanced across upper & lower SLR
- I/O interfaces should not span across SLRs
- Pay attention to data flow across SLRs

Table 14: UltraScale and UltraScale+ 3D IC SLR Count and Dimensions

| | Kintex UltraScale | | Virtex UltraScale | | | | Virtex UltraScale+ | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Device | KU085 | KU115 | VU125 | VU160 | VU190 | VU440 | VU5P | VU7P | VU9P | VU11P | VU13P |
| # SLRs | 2 | 2 | 2 | 3 | 3 | 3 | 2 | 2 | 3 | 3 | 4 |
| SLR Width (in regions) | 6 | 6 | 6 | 6 | 6 | 9 | 6 | 6 | 6 | 8 | 8 |
| SLR Height (in regions) | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 4 | 4 |

# Hub Schedule

Original schedule was for January prototype production run.

- Delay in procurement of Ultrascale FPGAs caused 1-2 month delay
  - FPGAs delivered early January
- Complications of Xilinx SSI design have set introduced further setback
  - Reworking of FPGA connections required
    - Aurora lanes cannot be bonded across SLRs
    - Clock-distribution needs to be balanced between SLRs to ensure high-speed timing constraints be met
    - HPIO lines should not be split over SLRs

Routing currently being reconfigured for SSI best-practices

- High-speed FEX data interfaces to Hub and ROD each need to be touched
  - Minor layout changes anticipated
- Expect prototype production to be delayed O(months)
  - Contingency-loaded schedule places prototype modules on summer timescale.

Firmware development continues in parallel

- Development on V-7 and Ultrascale dev boards providing good test beds
- Firmware schedule anticipates core and extended functions for Hub modules

# Summary

- The ATCA FEX Hub project is coming along well, but with delays
  - Several issues are being resolved, a few remain
    - Move to Ultrascale introduces a second delay, but not critical
    - Backplane link speed remains to be demonstrated
- Firmware effort progressing in parallel
  - Experience with both V-7/Ultrascale dev boards promising
    - Development of FW modules for prototype maturing
- Hub prototypes anticipated to be fully vetted with support firmware on timescale of Q3 2016
  - We expect steps to production Hub modules to be minor

# Design Changes: IPMC

Not so much a design change as change in understanding

- We require that the IPMC provide geographical information
  - Primary importance: shelf number

This IPMC functionality was previously in question

- This functionality would otherwise have to be established ad hoc

- Stony Brook LAr team has established IPMC-Shelf manager communications
  - Blade power and hot-swap functions appear to be capable
  - Currently no support for mezzanine communication / power management
  - We weren't counting on this in our ROD/Hub design