Joint L1Calo Meeting

Module Status & Firmware Plans: FEX ATCA Hub

Dan Edmunds, Yuri Ermoline
Brian Ferguson, Wade Fisher,
Philippe Laurens, Pawel Plucinski

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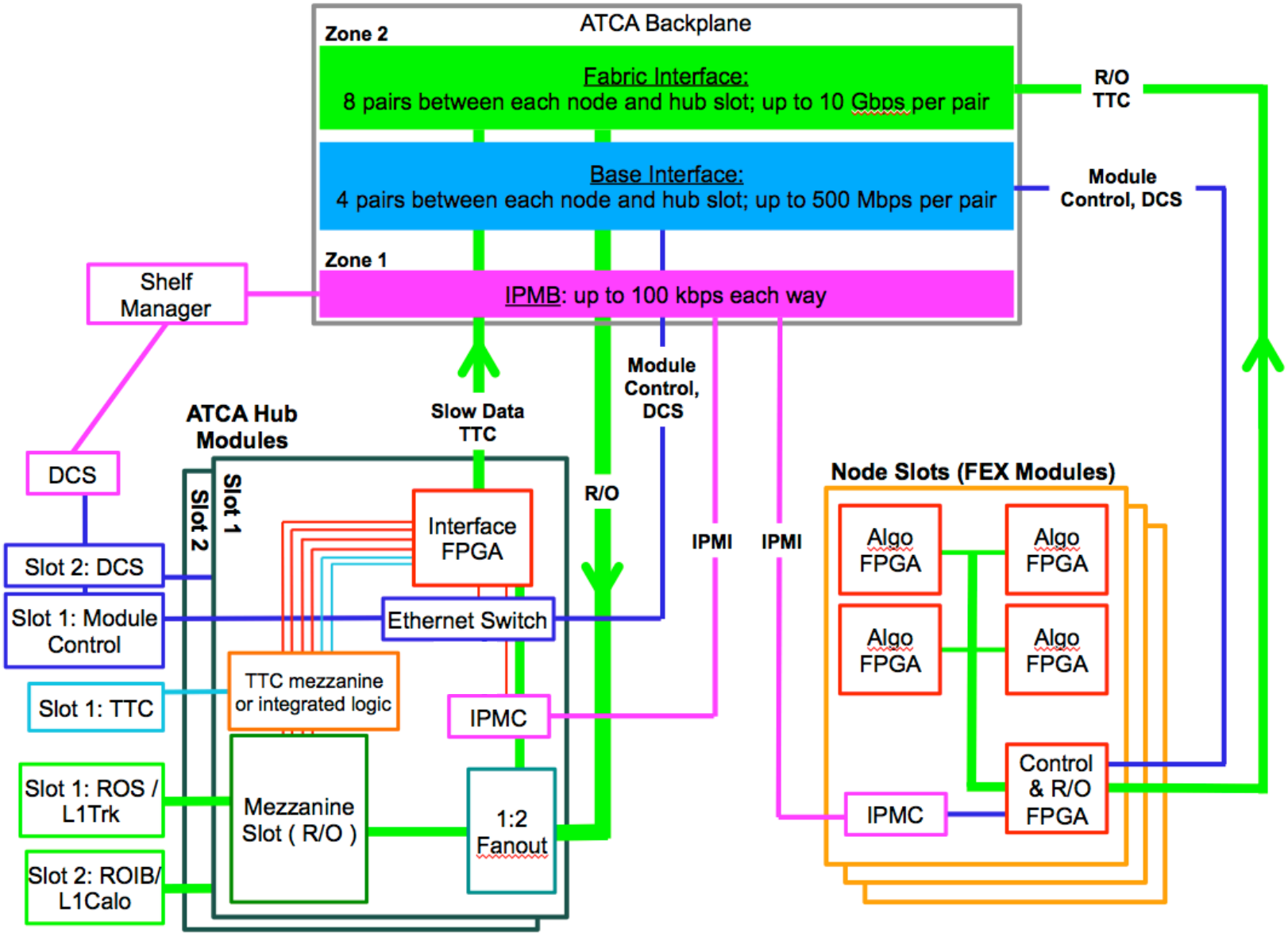
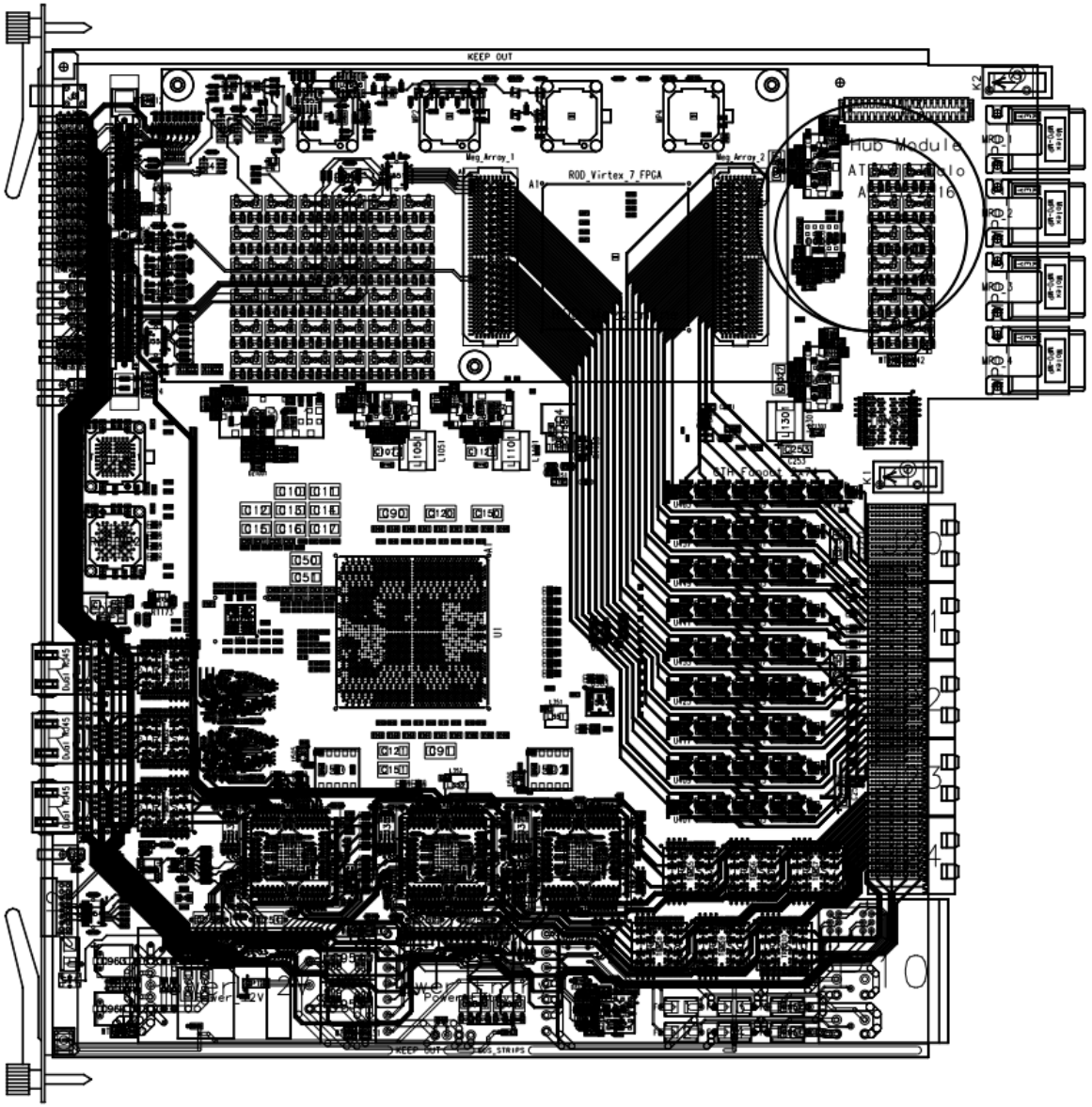
MICHIGAN STATE
UNIVERSITY

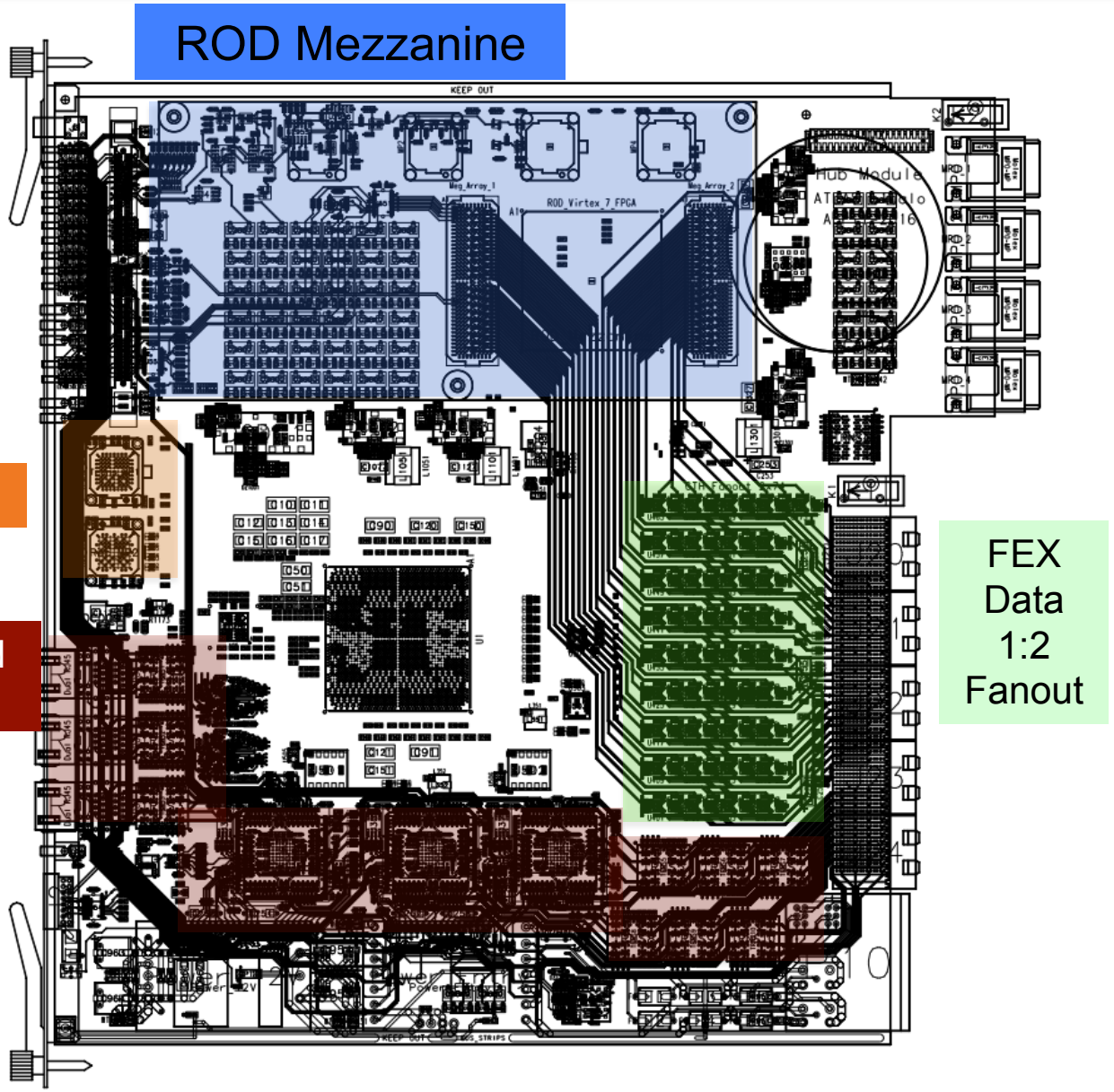
FEX ATCA Hub


ATCA Backplane
Zone 2
Fabric Interface:
8 pairs between each node and hub slot; up to 10 Gbps per pair
Base Interface:
4 pairs between each node and hub slot; up to 500 Mbps per pair
Zone 1
IPMB: up to 100 kbps each way
R/O
TTC
Module
Control, DCS
Shelf
Manager
Slow Data
TTC
Module
Control,
DCS
ATCA Hub
Modules
R/O
IPMI
IPMI
DCS
Slot 1
Slot 2
Slot 2: DCS
Slot 1: Module
Control
Slot 1: TTC
Slot 1: ROS /
L1Trk
Slot 2: ROIB/
L1Calo
Interface
FPGA
Ethernet Switch
TTC mezzanine
or integrated logic
IPMC
Mezzanine
Slot (R/O)
1:2
Fanout
Node Slots (FEX Modules)
Algo
FPGA
Algo
FPGA
Algo
FPGA
Algo
FPGA
Control
& R/O
FPGA
IPMC

ATCA Hub Current Drawing



ATCA Hub Current Drawing



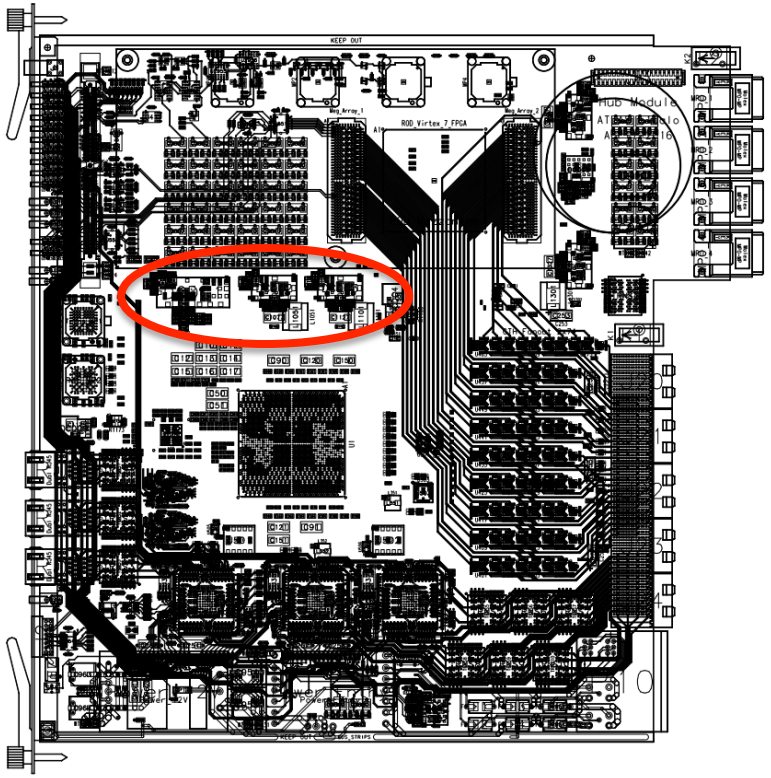
Current Status

Progress report

- Hub design is complete (one caveat, see below)
- Routing is nearly complete, waiting for the above caveat to be resolved
- Fabrication/assembly bid process is beginning
  - Two fully-qualified houses identified (including CMX manufacturer)

Resolved/Existing Issues:

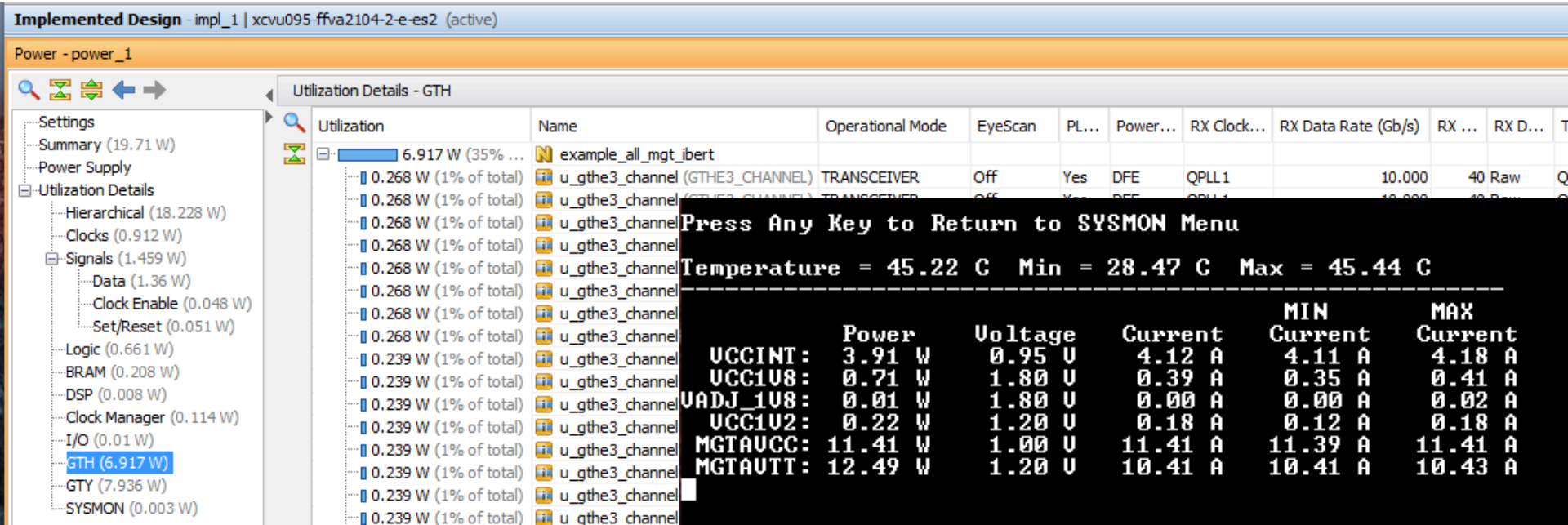
- Questions on dual-SLR FPGA architecture arose early 2016.
  - Delay injected to study Aurora bonding requirements, clocking, etc.
  - Partially resolved to the extent it's been documented by Xilinx. Some final cross checks to complete.
- eFEX experiences with XPE power predictions studied in the Hub context
  - Ongoing studies to understand if MGT DC/DC supply capacities are sufficient in current design. (* more on next page)
- Functionality of IPMC remains unclear
  - No delay planned here, but we need to understand more about this



FPGA Power Consumption

eFEX experience with XPE gave us pause

- We're also finding mixed signals between XPE, Vivado and SYSMON
  - Using VCU108 (XCVU095 chip), observe factors of 2x/0.5x in differences
  - Attempt to replicate Hub MGT usage to good approximation and extrapolate.
    - Studying RX-only, TX-only, RX+TX @ appropriate mixture of line rates
- In particular, we're concerned about MGT supply rails (MGTAVCC, MGTAVTT)
  - Planned DC/DC supplies @ 20A may be marginal.
  - Hoped to avoid 40A supplies to save precious high-frequency trace real estate
  - We are in a short holding pattern until this is sorted out.



IPMC Hardware Interface

Not so much a design change as change in understanding

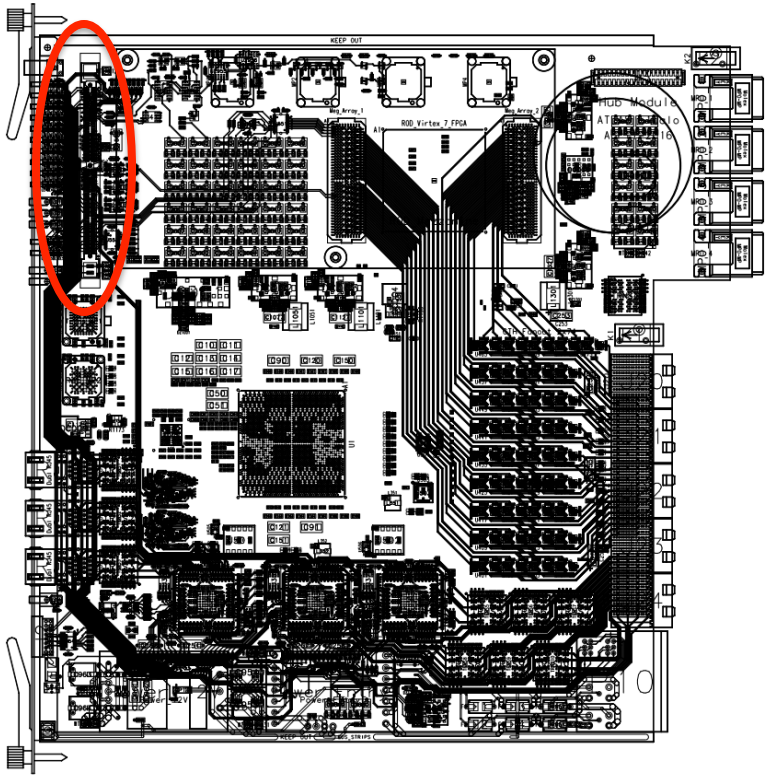
- We require that the IPMC provide geographical information
  - Primary missing piece: shelf number address (or even just assigned pins)
- Additionally, desire to have capability to suspend IPMC I2C bus cycles.
  - This allows the main FPGA I2C master to initiate bus cycles

This IPMC functionality remains in question (?)

- This functionality would otherwise have to be established in ad hoc fashion

Incomplete summary of potential needs:

- N (=8?) pins for shelf address (we have guesses laid out for now)
- 1 pin for confirmation that the shelf address is valid
- Scheme to generate Hub & ROD IP/Hardware addresses from shelf/slot numbers
- Means to communicate to the IPMC that the module will initiate and master Sensor_I2C bus cycles



Firmware Modules

ATLAS

EDMS Number:

EDMS Id:

ATLAS Level-1 Calorimeter Trigger

FEX Hub Firmware

Working document

Document Version:	Draft 0.0
Document Date:	06 April 2015
Prepared by:	D. Edmunds, Y. Ermoline, W. Fisher, P. Laurens,
	Michigan State University, East Lansing, MI, USA

Document Change Record

Version	Issue	Date	Comment

Firmware Modules

Note: this is a description of what's planned, not a prioritized list

- Short- / medium- / long-term milestones are identified and evolving.
- Matching prioritizations with Hub module status/needs with preliminary versions of FW is happening in parallel.

ATLAS

EDMS Number:

EDMS Id:

1 **ATLAS Level-1 Calorimeter Trigger**

2 **FEX Hub Firmware**

3 ---

4 **Working document**

5

6 Document Version: Draft 0.0

Firmware Modules: FEX/ROD Data

Several, inter-related FEX/ROD data signals to be handled

- FEX data to Hub, ROD data to Hub, Hub-1 data to Hub-2 (& vice versa)

- Lower priority in early efforts**, expect to have significant overlap with ROD firmware
  - ** Current focus on this area to understand Aurora channel bonding requirements, clocking limitations, etc. Though not required for early prototype tests, still being pushed. Also required to validate Hub PCB design.

Firmware Modules: GBT/TTC

Clock and Combined-Data distribution/processing

- Clock recovery and distribution to FEX/ROD modules
- Decode GBT "TTC" payload from FELIX and merge with ROD/Hub back-pressure, distribute to FEX modules

- Clock distribution in early system is essential.
  - Clock-source logic embedded (GBT vs crystal), so task is just distribution
  - Combined data protocol to be defined
  - Modifications of example designs produced/tested

Firmware Modules: IPBus/GbE

GbE network operation and Hub FPGA interface

- On-startup configuration/setup of GbE network is an early high priority
- Interfaces to Hub FPGA may be numerous, but include: nominal communications (as with any other module), network monitoring, configuration management.

- Early firmware work has focused on the GbE interface
  - Implementation, configuration, management
  - Not starting from scratch (examples exist) and maintaining contact with other L1Calo firmware engineers.

Firmware Modules: IPMC

Interface and communication with IPMC

- Access to core IPMC functionality: geographical addressing, etc
- Still-undefined communication options (see previous slide)
  - Eg: “Line-clear” signal for asserting I2C bus master status?

- Beyond what’s known now, not well defined
  - Beyond core functions, not much is required for early commissioning
  - We will need to get more sophisticated in our overall understanding of the IPMC functions

Firmware Modules: Other

Minipods, LEDs, front panel, etc

- Requirements for optical interfaces will evolve over time, but will optical communication will likely be useful in Hub commissioning
- Front panel/LED functions are a high priority

- To proceed as other core Hub functions are developed
  - These are well-defined and largely not novel or specific to the Hub module

Some Outstanding Questions

IPMC I2C monitoring

- We expect that the IPMC will gather monitoring information from targets on the various modules. How should this info be handled?
  - If there is a IPMC→Shelf Manager→DCS path, where will the data→engineering unit conversion occur? Stored in some database?
  - Or should the conversion somehow occur on the module itself?

External I2C management

- There may be targets on the I2C bus that require some degree of management. For example, power supplies with a PMBus interface
  - If there is an allowed path of IPBus→FPGA→I2CBus→Target, do we have a means to suspend the IPMC as I2CBus master?
  - Following the PMBus example, are we allowed to manage power supplies or are such configurations required to be "fixed". Eg, trimming of DC voltage levels.

Common IPBus/I2C firmware

- If we envision IPBus→FPGA→I2CBus communication, we should have common conversion firmware. Is this on the list of L1Calo common FW?

Summary: Ignore this for now

- The ATCA FEX Hub project is coming along well, but delayed relative to the original schedule
  - Several issues are being resolved, a few remain
    - Move to Ultrascale introduced a delay, but not critical
    - Questions about FPGA power estimates being addressed
    - Backplane link speed remains to be demonstrated

- Firmware tasks are defined and underway
  - Early efforts in areas that support hardware design
    - Prioritizations to evolve as we move towards commissioning
    - Will continue to work towards common FW solutions in areas of overlap with L1Calo groups