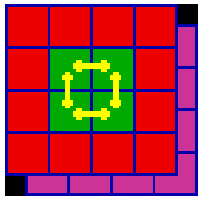

Barcelona TDAQ Week

Preparations for ROD-HUB tests

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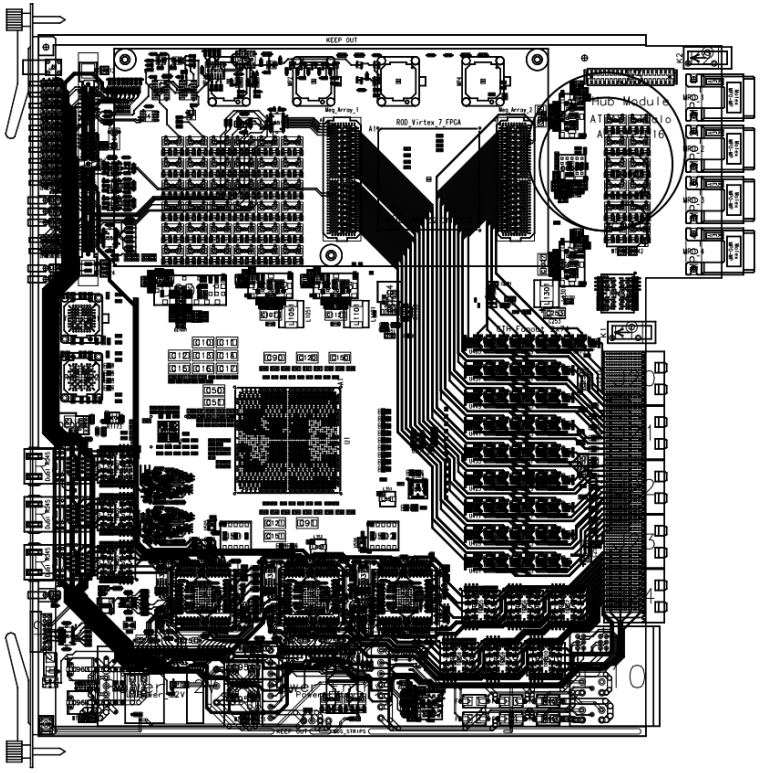
28 September 2016

UNIVERSITY OF CAMBRIDGE

MICHIGAN STATE UNIVERSITY

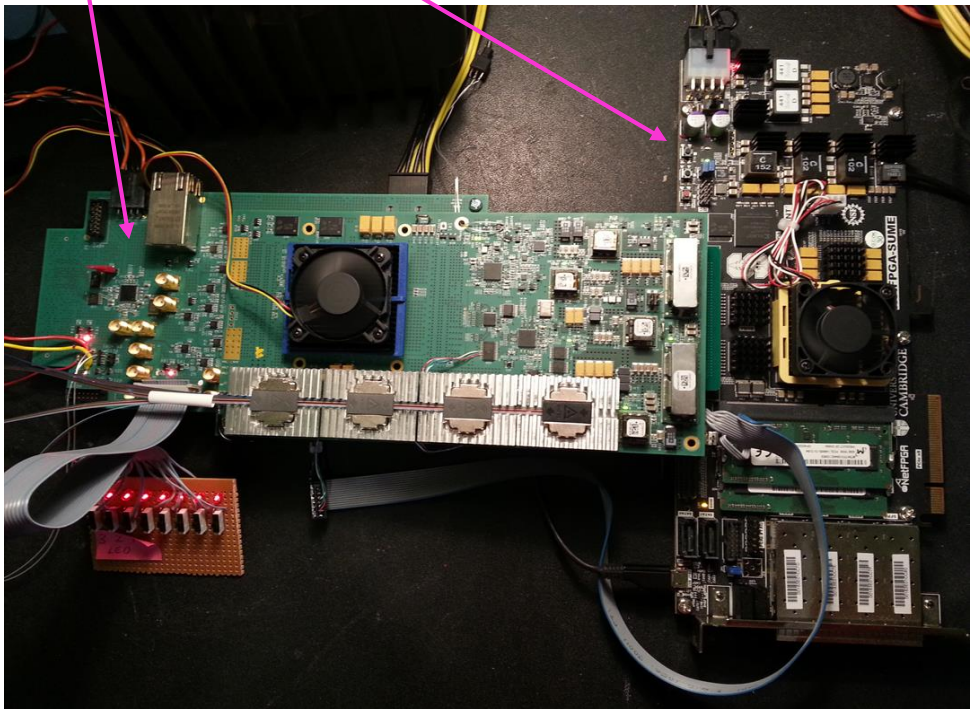
Outline

- Current status of development and MSU and Cambridge
- Initial HUB tests at MSU
- ROD tests at Cambridge
- ROB-HUB join tests preparation



ROD+Host Test Setup

Host Board + Development Board provide Hub functionality



HUB development at MSU

Hardware development

- Power distribution – the MGT rail supplies that were in question, sorted out, DC/DC supplies @ 20A
- The bulk of the PCB layout is done, with only few details remaining, some manufacturing choices to finalize, and more checking all around before the design can be released for manufacturing.

Firmware development

- Interface to FEX/ROD data – UltraScale specific tests ongoing with Aurora 8b10b over GTY
- GBT/TTC Interface - clock recovery, TTC decoding – on hold for now
- IPbus interface / Gb Ethernet switch control – moving to UltraScale
- IPMC Interface – to be understood
- Minipods I2C access, LEDs, front panel, etc.

Software development

- Low-level IPbus software on Linux PC to communicate with IPbus slaves
- Looking into basic test program implementation

Initial HUB tests at MSU

Preliminary work plan of tests at MSU is worked out:

- List of hardware test stages - not necessarily sequential
- Lower priority stuff (e.g. IPMI) and high priority topics (e.g. switch, MGT)

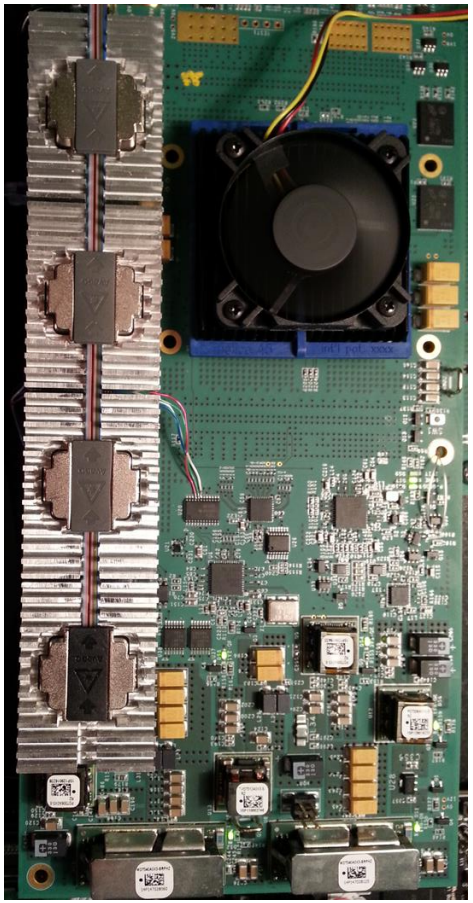
HUB-only tests (upon receipt of 1st Hub module):

- HUB SN00 (with no FPGA) on the bench upon assembly
  - Visual test, final assembly, power supplies, oscillators and PLLs, switch
- HUB SN01 - clock/power checkout, and basic FPGA configuration via JTAG
  - Initial clock from the PLL free-running at the LHC frequency
- IPbus testing – initially bypassing the Ethernet Switch
  - Access to internal (dummy) registers, (sysmon –V & T from both Logic Regions)
- Ethernet Switch Testing - configured from Switch Chips EEPROMs
  - Switch should work without Hub FPGA initial tests, then test IPbus again via switch
- IPMC
  - Ethernet to IPMC, I2C access from IPMC to FPGA, Shelf Address
- Optical and electrical data transmission tests
  - Only a few MGTs can be accessed using miniPODs, 4 RX + 12 TX, GTH channels
  - IBERT and user-data transmission planned: but would be best if we can practice with a protocol as close as possible to what we will use for FEX→ROD

ROD development at Cambridge

Hardware development

- Revision 1.0 ROD fully tested
  - Minor power supply issues found
- Revision 2.0 ROD in manufacture
  - 1st board expected mid October
- Host Revision 2.0
  - Testing complete



Firmware Development

- Working implementations in place for
  - I2C, SPI, GPIO
  - Flash Interface
  - HWICAP
  - IPBus
- Working prototypes for
  - Aurora 6-Lane
  - Serial Simplex links

Software Development

- Power supply modules read via IPBus + I2C/PMBus
- BPI Flash programming and verification via IPBus

ROD Test Firmware

Host Basic I/O Core (controlled through JTAG)

- SPI master for Host Clock Programming
- I2C master for access to ROD power supplies and clocks
- GPIO for several static controls

ROD Basic I/O Core (controlled through JTAG)

- SPI master for ROD clock programming
- I2C master for ROD clocks, power supplies, MiniPods
- GPIO for several static controls

ROD IBERT (optical)

- Tests speed of Felix Data looped into Felix Backpressure (10.2Gbps)
- Tests speed of S-Link output to return path (4.0Gbps)

ROD IBERT (FEX data)

- Tests link speed of 72 FEX-HUB-ROD data links (10.2Gbps)

HOST IBERT (Fex data)

- Works in conjunction with the ROD FEX data IBERT (10.2Gbps)

IPBus/RGMII core

- Confirms Ethernet phy functionality

ROD-HUB joint tests preparation

First meeting of ROD and HUB at Cambridge or MSU

- We assume we'll send a Hub (+Dan +Pawel) to Cambridge
- After that HUB stays at Cambridge and ROD comes to MSU

Hub+ROD Tests (Not likely before the holidays)

- ROD power up sequence
- IPbus to ROD – from front panel and via switch
- ROD JTAG - load ROD firmware
- MGTs can be tested using iBERT
- HPIO Lines can be tested using the basic I/O core + TCL scripts
  - GPIO, I2C
- ROD images may be reused from the ROD+Host tests
- Hub images may be ported from the Host
  - or easily generated using the Xilinx tools

If make good progress in the ROD/Hub mating step we could go to ROD+Hub+FEX/FTM tests at that time (at RAL, Cambridge?).

Further tests (preliminary)

Two HUB test (at MSU)

- MGT communication over backplane
  - 2 lane GTY to GTY readout to other Hub
  - 1 lane GTY to GTY combined data to other Hub

One HUB + one FEX or FTM (+ROD)

- MGT communication (IBERT, Aurora)
- Over backplane - 6 lane from FEX V7 GTH to HUB Ultrascale
  - GTH or GTY depending on FEX slot
- Walk FEX through 12 slots in full crate or 4 slots in mini crate

At CERN:

- CERN will likely be the only place where we can test TTC input and where the highest number of FTM and FEXs will come together in one single crate backplane
- one HUB + one FEX + GBT
- one or two HUB+ROD + many FEXs + GBT optional

Tests of FEX->HUB->ROD Bandwidth

Early tests

- Few FEX/FTM cards available to test backplane links.
- Suffice to test individual links (1slot=6 links at a time), moving source card slot-to-slot
- Borrow V1 FTM or prototype FEX for MSU-based tests

More Comprehensive tests

- We will require full tests of all 74 high-speed backplane links to fully qualify the prototype Hub modules
- Availability of FTM/eFEX/jFEX prototypes may limit this to <74 links
- Should plan on dedicated CERN-based tests for this

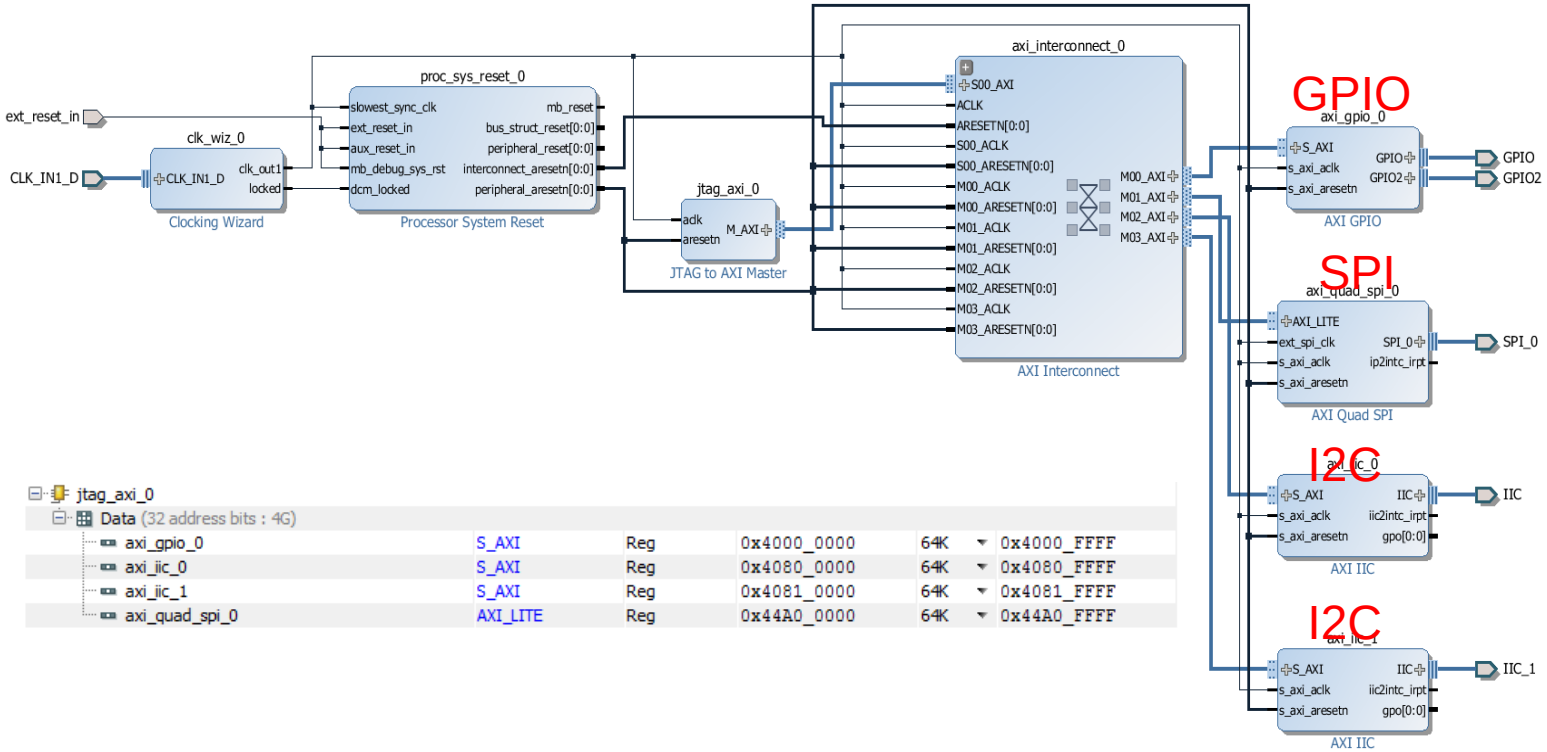
Test of production Hub modules

- Eventually, we will need to characterize/verify the bandwidth performance of all Hubs to be installed in USA15.
- Need to work out plans for 12-FEX/FTM test bench at CERN
- Bandwidth limitations / failures observed at this late date may jeopardize overall L1Calo performance, so this should be taken seriously.

Extra Details on ROD Firmware

ROD basic I/O core

- JTAG Master + Simple Peripherals
- Programmed via TCL script
- Can be placed in both the Hub and the ROD



jtag_axi_0

Data (32 address bits : 4G)

axi_gpio_0	S_AXI	Reg	0x4000_0000	64K	0x4000_FFFF
axi_iic_0	S_AXI	Reg	0x4080_0000	64K	0x4080_FFFF
axi_iic_1	S_AXI	Reg	0x4081_0000	64K	0x4081_FFFF
axi_quad_spi_0	AXI_LITE	Reg	0x44A0_0000	64K	0x44A0_FFFF