L1Calo Joint Meeting

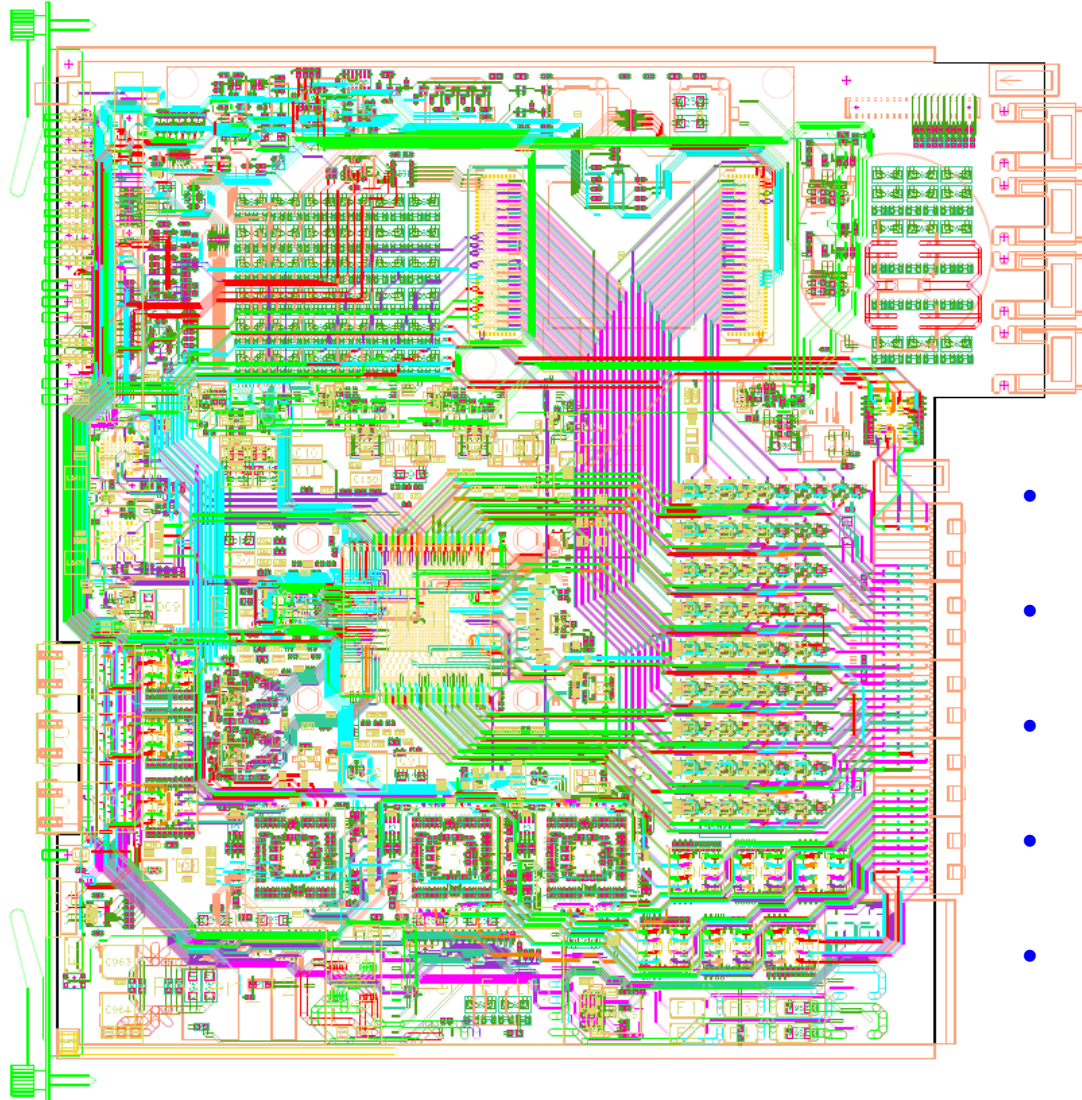# Hub Status & Plans

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MICHIGAN STATE
U N I V E R S I T Y

HUB HW – PCB development

HUB PCB is a 22 layer IPC* class 2 card, 3.05 mm thick.

IPC, the **Association Connecting Electronics Industries (**initial name: **Institute for Printed Circuits)**

- Selected same vendors that did CMX (assembly + PWB)
- 10 of the layers are 1/2 oz Ground planes
- 8 of the layers are 1/2 oz signal routing
- 2 of the layers are 1 oz mixed signal/power fills
- 2 of the layers are 1 oz power fills/routing

HUB HW – PCB development

ROD Mezzanine

Ultrascale FPGA

FEX Data Fanout

GbE Switch

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HUB PCB details

- There are 51 power fills in the card.

- There are about 8277 connections in the HUB PCB (w/out GND/Power)

- There are currently 2793 components on the HUB.

- Requiring high-speed differential pairs on all 10 routing layers is one of the "issues" with the HUB design. There are about 378 differential signal pairs used in the design, all of the high-speed FEX MGT signals are routed as strip-lines on the 8 internal signal layers – no vias.

- The Gbit Ethernet differential pairs are routed on all 10 layers and are kept physically separated from the high-speed MGT differential signals.

- The 74 channel FEX MGT Data Fan-out is located immediately adjacent to where the FEX signals enter the HUB Module from the Zone 2 backplane connectors. To achieve the required fan-out channel density the fan-out chips are located on both sides of the HUB PCB.

HUB FW/SW

Firmware development

- Interface to FEX/ROD data – UltraScale tests with Aurora 8b10b over GTY
  - Successes in using the Aurora 8b10b protocol using GTY - it was performed successfully and Xilinx seems have signed off on the implementation

- IPbus interface / Gb Ethernet switch control – moving to UltraScale
  - Exercise with the Xilinx vcu108 development board (not the same PHY chip and not the GMII interface, however provide design experience…)

SW:

- Low-level IPbus software on Linux PC to communicate with IPbus slaves
  - From Cactus project

- Looking into basic test program implementation
  - Setting up the SW environment at MSU

Preliminary work plan of tests at MSU is worked out:
- List of hardware test stages - not necessarily sequential
- Lower priority stuff (e.g. IPMI) and high priority topics (e.g. switch, MGT)

One HUB / Two HUB test (at MSU)
- Local tests will be limited by available interfaces
  - To do: work out schedule to obtain/borrow N FTM/FEX modules (N>1?)
- Hub-to-Hub communications & GbE tests can cover partial ground
  - To do: set up GBT demonstrator on VC709 dev board with GBT FW
  - To do: establish GbE test bench

Preparation for tests: @UK/CERN

First meeting of ROD and HUB at Cambridge or MSU
- We assume we'll send a Hub (+Dan +Pawel) to Cambridge
- After that HUB stays at Cambridge and ROD comes to MSU

If we make good progress in the ROD/Hub mating step we could go to ROD+Hub+FEX/FTM tests at that time (at RAL, Cambridge?).

At CERN:
- CERN will likely be where the highest number of FTM and FEXs will come together in one single crate backplane
  - To do: establish bandwidth spec for @CERN shelf (>10 Gbps?)
  - To do: establish # available FEX/FTMs and work out bandwidth test strategy
- HUB + one FEX + GBT
- one or two HUB+ROD + many FEXs + GBT optional

Full bandwidth test

Early tests
- Few FEX/FTM cards available to test backplane links.
  - Borrow V1 FTM or prototype FEX for MSU-based tests
- Sufficient to test individual links (1slot=6 links at a time)
  - Moving source card slot-to-slot

More Comprehensive tests
- We will require full tests of all 74 high-speed backplane links to fully qualify the prototype Hub modules
- FDR and PRR requirements for such tests need to be decided soon.
  - "Proceeding to preproduction without comprehensive tests represents a significant risk."

Test of production Hub modules
- Eventually, we will need to characterize/verify the bandwidth performance of all Hubs to be installed in USA15.
- Need to work out plans for 12-FEX/FTM test bench at CERN

Hub Test Options

We have identified a potential problem with the test plan for the prototype Hub modules. To fully qualify (and quantify) the Hub design, we will need a shelf with 12 blades capable of populating 6 transmit lanes of the zone-2 fabric interface.

Thus we need to identify potential solutions.

- Option 1: Identify commercial ATCA cards that have the non-standard zone-2 interface that we are using.
    - Pro: Simple (?)
    - Con: Unlikely to find COTS card with custom Zone-2 interface.

- Option 2: Negotiate with the FEX/FTM community to build sufficient modules on the timescale of the tests that we need.
    - Pro: Closest to actual implementation, best tests bandwidth limitations
    - Con: Potentially costly and may not fit partner's available person-power/schedule.

- Option 3: Design our own simple "FEX lookalike" that closely emulates how a FEX transmitter/receiver would appear over the backplane.
    - Pro: Could be cheaper in HW costs (though not in engineering time)
    - Con: Differences WRT real FEX could be significant; large impact to schedule