ATLAS Level-1 Calorimeter Trigger Phase-I Upgrade

High-Speed Demonstrator (HSD)

Project Report

Version: 1.02

Date: 27 Jan 2014

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Contents

Document History ... 4
1 Introduction ... 5
1.1 Motivation ... 5
1.2 Design method ... 5
1.3 PCB simulation ... 6
1.4 Test/Measurement tools ... 7
1.5 HSD Overview ... 7
1.6 HSD PCB material and construction ... 8
1.7 Relevant standards ... 10
2 Measurements and Simulation ... 10
2.1 PCB material test ... 10
2.2 Power supply ... 12
2.2.1 Learning points ... 12
2.3 Differential skew ... 13
2.4 Clock jitter ... 15
2.5 Crosstalk ... 17
2.6 Time Domain Reflectometry (TDR) ... 19
2.6.1 Corrective actions ... 19
2.6.2 Effect of AC coupling capacitor ... 20
2.6.3 Routing under BGA ... 20
2.7 Time Domain Transmission (TDT) ... 21
2.8 3D structure modelling ... 23
2.8.1 PCB via ... 23
2.8.2 SMA connector ... 24
2.9 Channel simulation ... 26
2.9.1 Xilinx Virtex-6 [8] GTX at 5Gb/s ... 27
2.9.2 Xilinx Virtex-6 GTH at 10Gb/s ... 28
2.10 BER test ... 29
2.10.1 Xilinx Virtex-6 GTX ... 30
2.10.2 Xilinx Virtex-6 GTH ... 30
2.11 Eye diagram compliance test ... 31
2.11.1 HSD TP1 eye diagram measurement ... 31
2.11.2 HSD TP2 eye diagram measurement ... 32
2.11.3 HSD TP4 eye diagram measurement ... 33
2.12 Data sharing ... 34

2.12.1 High-speed buffer 34
2.12.2 Far-end PMA loopback 35
2.12.3 Passive Optical splitter 36
3 Joint BNL/RAL 10Gb/s link tests 38
3.1 IBERT scan with Virtex-7 + MicroPOD 38
3.2 Optical splitter test with Virtex-7 + MicroPOD 39
3.3 Optical power measurement of MicroPOD 39
3.4 Far-end PMA loopback test with Virtex-7 + MicroPOD 39
3.5 Eye diagram measurement with Virtex-7 + MicroPOD 40
3.5.1 Virtex-7 (TP1) 40
3.5.2 MicroPOD Rx (TP4) 41
3.5.3 MicroPOD Rx + high-speed electrical buffer (TP4) 42
3.5.4 Far-end PMA loopback (TP4) 43
4 Conclusions 44
5 Acknowledgement 45
References 45

Figure 1. High-speed PCB design method 6
Figure 2. Typical high-speed link channel 7
Figure 3. HSD overview 8
Figure 4. HSD Layer stackup 9
Figure 5. PCB material loss simulation 9
Figure 6. HSD Impedance specification 10
Figure 7. HSD signal speed measurement 11
Figure 8. PCB S-parameter simulation and measurement 12
Figure 9. HSD Xilinx GTH power supply noise 13
Figure 10. Cause of differential skew 13
Figure 11. Differential skew control 14
Figure 12. HSD differential skew measurement 14
Figure 13. Jitter decomposition 15
Figure 14. Illustration of the mask of the sinusoidal component of jitter tolerance 16
Figure 15. Clock TIE jitter (>100KHz) 16
Figure 16. Clock TIE jitter (>100KHz) 16
Figure 17. Clock TIE jitter (>100KHz) 17
Figure 18. CDCE62005 output synchronization 17
Figure 19. Crosstalk Overview 18
Figure 20. Correlation of crosstalk simulation (right) to measurement (left) 18
Figure 21. HSD PCB differential crosstalk simulations 18
Figure 22. TDR differential impedance measurement and microsection on HSD v1 19
Figure 23. Left: TDR differential impedance measurement and microsection on HSD v2 19
Figure 24. TDR measurement on AC coupling capacitor 20
Figure 25. Routing under BGA 21

Figure 26. Differential impedance under BGA 21
Figure 27. HSD PCB TDT test. Red curve: real measurement, Yellow curve: simulation. 22
Figure 28. Example of SFI Host Recommended Channel 22
Figure 29. Modelling of PCB vias on HSD 23
Figure 30. Dangling via TDR measurement and 3D simulation 24
Figure 31.TDR of SMA on HSD v1 24
Figure 32. 3D model of SMA in HFSS 25
Figure 33. 3D SMA simulation 25
Figure 34. TDR of SMA on HSD v2 26
Figure 35. SMA centre signal pin assembly on HSD v1 26
Figure 36. MGTTXP1_114 channel layout and modelling (HyperLynx) on HSD 27
Figure 37. Xilinx V6 GTX channel simulation @ 5Gb/s on HSD 28
Figure 38. MGTTXP2_108 channel layout and modelling (HyperLynx) on HSD 29
Figure 39. Xilinx V6 GTH channel simulation @ 10Gb/s on HSD 29
Figure 40. HSD GTX optical link test topology 30
Figure 41. HSD GTH optical link test topology 30
Figure 42. HSD GTH optical link IBERT bathtub curves at 10Gb/s 30
Figure 43. Optical link model for 40 and 100 Gigabit Ethernet 31
Figure 44. HSD TP1 eye diagram measurement 32
Figure 45. HSD TP2 eye diagram measurement 33
Figure 46. HSD TP4 eye diagram measurement 34
Figure 47. Topology for buffer test on GTH channel 34
Figure 48 HSD PPOD Rx eye diagram measurement after buffer 35
Figure 49. Topologies for Far-end PMA loopback tests on HSD 36
Figure 50. Virtex-6 GTH PMA loopback test 36
Figure 51. Passive 1-to-2 optical splitter measurement 37
Figure 52 Optical eye definitions 37
Figure 53. PPOD Transmitter optical power measurement on HSD 38
Figure 54. IBERT scan tests with Virtex-7 + MicroPOD 38
Figure 55. Passive optical splitter test with MicroPOD 39
Figure 56. Output optical power of MicroPOD transmitter 39
Figure 57. Far-end PMA loopback with Virtex-7 and MicroPOD 40
Figure 58. TP1 eye diagram measurement at Virtex-7 41
Figure 59. TP4 eye diagram measurement at MicroPOD Rx 42
Figure 60. TP4 eye diagram after buffer 43
Figure 61. TP4 eye diagram after Far-end PMA loopback 44

Document History

1 Introduction

1.1 Motivation

The Phase-1 Upgrade [1][2] of ATLAS [3] Level-1 Calorimeter Trigger [4] will employ new Feature Extractors running on much finer granularity information from calorimeters. Enormous data volume (~50Tbit/s) needs to be transported between new trigger subsystems, which necessitate multi-Gb/s high-speed high-density PCB design to keep the new subsystems reasonably compact. Signal Integrity (SI) is a big challenge in multi-Gb/s PCB design, which concerns the following areas:

1) Impedance control
2) High frequency attenuation
3) Crosstalk
4) Clock jitter
5) Differential skew
6) Power distribution system

Given such big challenge and limited experience in these areas, a relatively simple High Speed Demonstrator (HSD) has been designed to explore these new technologies. This report focuses on the SI aspect of multi-Gb/s PCB simulation/design/measurement on HSD. It does not cover the protocol aspect of multi-Gb/s high-speed link design.

1.2 Design method

A new systematic PCB design method as shown in Figure 1 has been pioneered in the HSD design. This new design method adds a series of incremental Quality Assurance (QA) procedures (shown as diamond boxes) to the traditional PCB design flow. The core and most challenging parts of this flow are the PCB simulation and correlation. The biggest aim of HSD project is to learn the PCB simulation in multi-Gb/s speed regime and correlate the PCB simulation to real measurement so that PCB simulation can be used to guide next much more complex PCB design of Feature Extractors.

The pre-layout simulation is used to formulate a set of routing constraints for critical PCB signals. It is also used to check critical signal topology and termination. When the PCB layout is finished, the post-layout simulation is performed to verify the PCB layout quality of critical signals.

When the PCB is manufactured, the bare PCB undergoes a time-domain reflectometry (TDR) test before assembly. This test reveals any impedance errors or discontinuities in the PCB signal paths. With advance TDR tools, the electrical model of a whole signal path can also be extracted and fed into a simulation tool for further simulation, which can then be compared with the post-layout simulation.

Once the TDR test results are fully understood and satisfactory, the PCB is assembled. Then, an eye diagram test and a bit error rate test can be performed, the results of which can then be compared to that of PCB channel simulation.

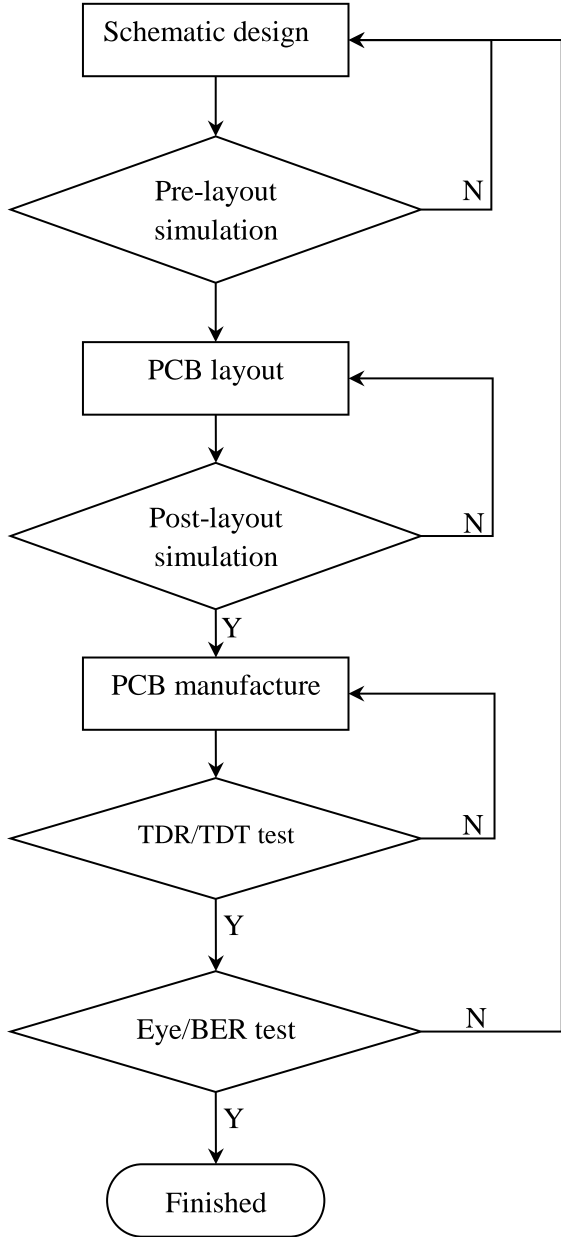


Figure 1. High-speed PCB design method

1.3 PCB simulation

PCB simulation becomes increasingly important as signal speeds approach 5 Gb/s and over. Figure 2 shows a simplified high-speed link channel. To simulate this channel, models are needed for transmitter, receiver and interconnects (PCB tracks, connectors, cables and etc.).

For HSD, Xilinx Virtex-6 GTX/GTH is used for multi-Gb/s transceivers, their models are downloaded from Xilinx website. The models for the PCB tracks are extracted by the PCB simulation software, HyperLynx 8.2 from Mentor graphics. The models for connectors (e.g. SMA) are extracted by 3D EM solver, HFSS from Ansys. The models for cables can be measured directly using TDR oscilloscope.

Different types of simulation models have different simulation speed, accuracy and limitation. The choice of models needs to fit for the purpose. For example, SPICE model is very accurate but extremely slow (~100bit/hour), so it can be used in crosstalk simulation where not many bits are needed. IBIS-AMI model is reasonably accurate and fast (~10^6 bits/minute), and it can be used in EYE diagram/BER simulation. The speed of IBIS model is between SPICE and IBIS-AMI, but it cannot model complex analogue circuit such as equalization and Clock Data Recovery (CDR) circuit. IBIS model can be used for example in simulations of reference clock coupling and termination.

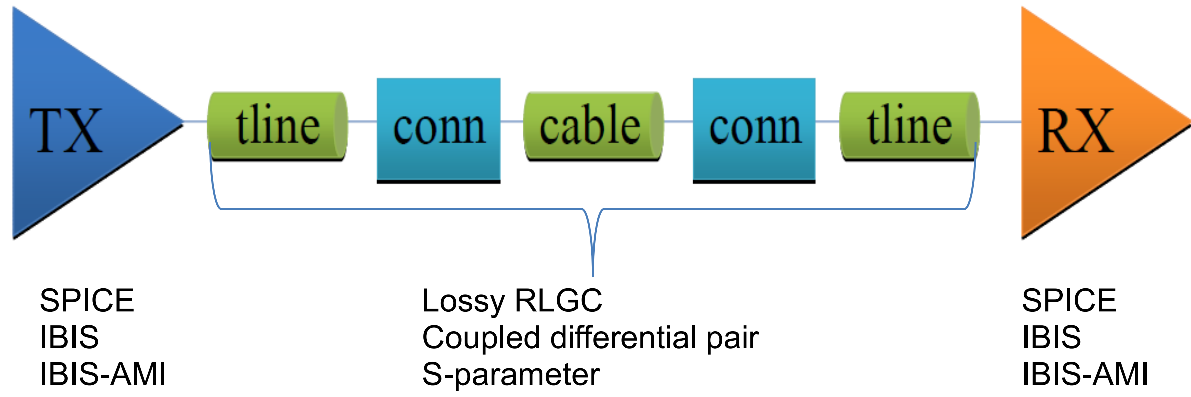


Figure 2. Typical high-speed link channel

1.4 Test/Measurement tools

The following equipments are used to test and measure HSD.

Agilent 86100C Infiniium DCA-J Wideband Oscilloscope Mainframe with following plug-in modules:

- 86105C, optical(9GHz)/electrical(20GHz) sampling module
- 83496A, optical/electrical clock recovery module, 50Mb/s – 13.5Gb/s
- 86112A, dual channel electrical sampling module, 20GHz
- 54754A, differential TDR module, 18GHz
- N1021B, differential TDR/TDT probe kit, 18GHz
- N1024B, TDR calibration kit

Tektronix MSO72004C, 20GHz/100Gs.

Tektronix TDS 5104, 1GHz/5GS.

FIS OV-PM F18513HR optical power meter.

1.5 HSD Overview

Figure 3 shows the function block diagram of the HSD on the left and the real hardware on the right. The HSD uses a Xilinx Virtex-6 FPGA (XC6VHX255T) as the multi-Gb/s data sink/source. It has 24 GTX running at 5 Gb/s and 24 GTH running at 10 Gb/s. Many new technologies are prototyped on the HSD to be tested, including:

- Clock jitter-cleaning circuitry
- Multi-Gb/s fan-out circuitry
- 12-way parallel optical transmitters and receivers PPOD
- Blind via PCB technology

The lengths of PCB tracks for high-speed links on HSD range from a few centimetres up to 50 centimetres, so that the high-frequency PCB loss can be accurately characterised and link performance limits can be explored.

A variety of serial links on the HSD are terminated at SMA connectors, facilitating easy connections to oscilloscope for measurements. More importantly, those SMA connectors enable various link topologies to be easily formed and tested. For example, the performance of GTX/GTH/PPOD can be easily characterised via SMA connectors. Optical links and electrical links can also be concatenated together via SMA connectors to explore performance limits. Links over a backplane can also be tested using two HSD modules.

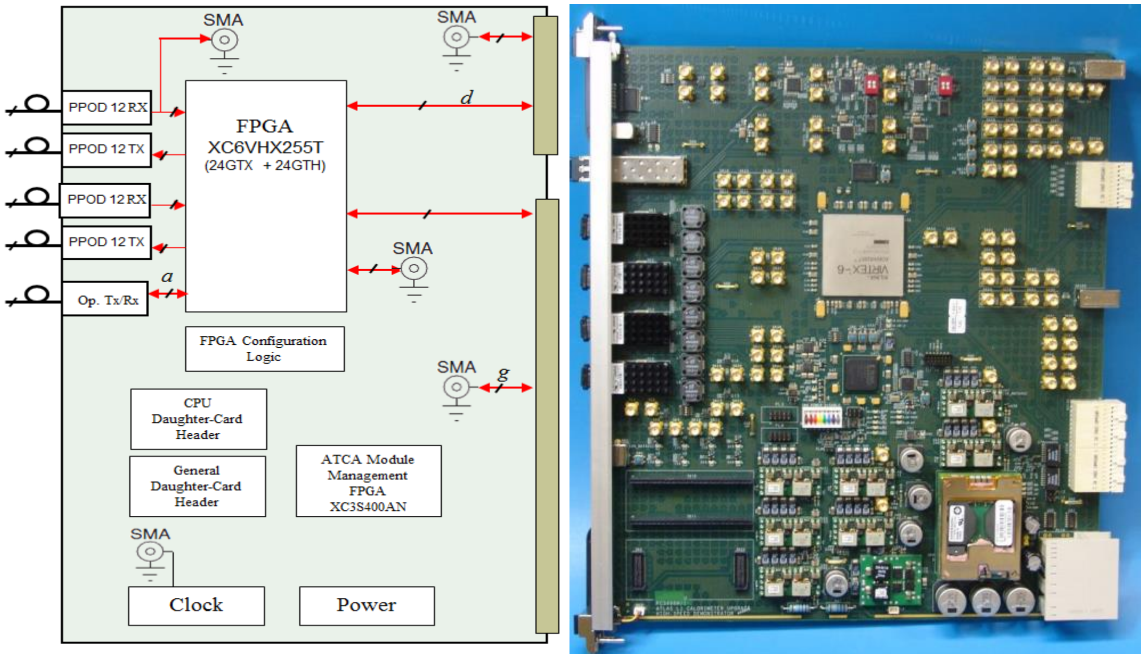
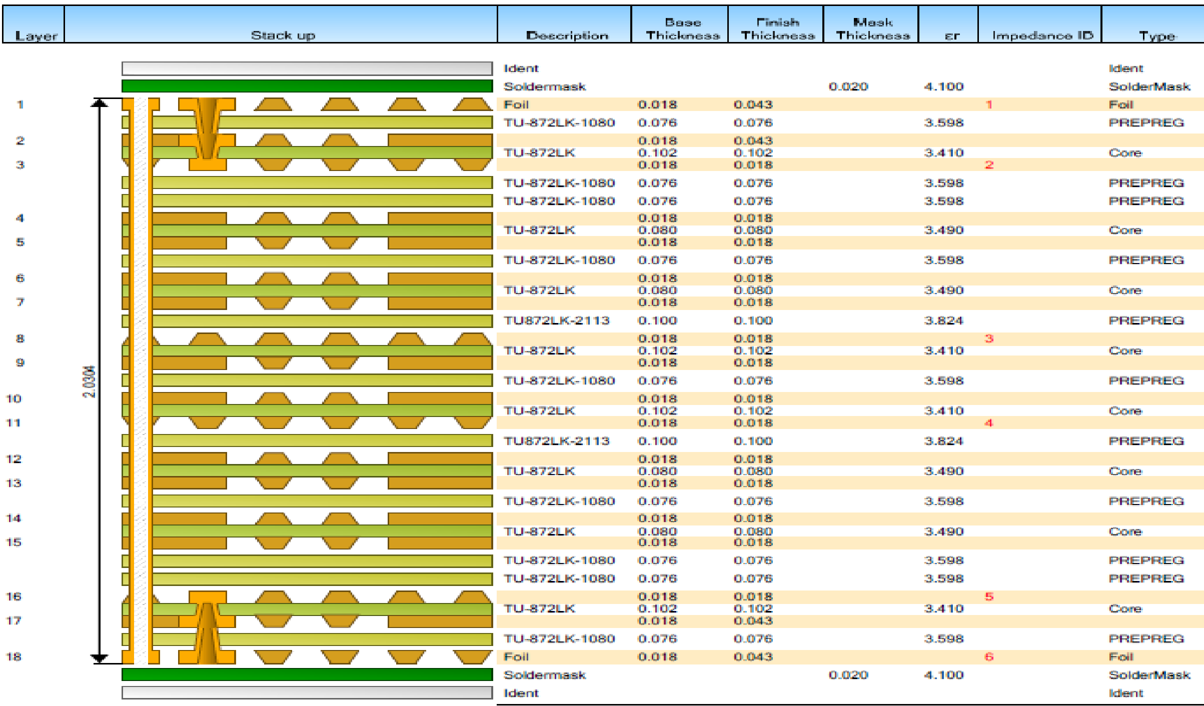


Figure 3. HSD overview

1.6 HSD PCB material and construction

Most modern large FPGAs have 1500 to 2000 pins in a single BGA package, which needs many PCB layers to breakout signals. They also need about 10 different power rails, which require many layers for power distribution. PCB impedance control and crosstalk also needs extra ground planes. All together, the total number of PCB layers required can easily reach 20. Figure 4 shows the HSD PCB layer stackup with 6 signal layers and 12 power/ground layers.



Layer	Description	Base Thickness	Finish Thickness	Mask Thickness	εr	Impedance ID	Type
	Ident						Ident
	Soldermask			0.020	4.100		SolderMask
1	Foil	0.018	0.043			1	Foil
	TU-872LK-1080	0.076	0.076		3.598		PREPREG
2 3	TU-872LK	0.018 0.102 0.018	0.043 0.102 0.018		3.410	2	Core
	TU-872LK-1080	0.076	0.076		3.598		PREPREG
	TU-872LK-1080	0.076	0.076		3.598		PREPREG
4 5	TU-872LK	0.018 0.080 0.018	0.018 0.080 0.018		3.490		Core
	TU-872LK-1080	0.076	0.076		3.598		PREPREG
6 7	TU-872LK	0.018 0.080 0.018	0.018 0.080 0.018		3.490		Core
	TU872LK-2113	0.100	0.100		3.824		PREPREG
8 9	TU-872LK	0.018 0.102 0.018	0.018 0.102 0.018		3.410	3	Core
	TU-872LK-1080	0.076	0.076		3.598		PREPREG
10 11	TU-872LK	0.018 0.102 0.018	0.018 0.102 0.018		3.410	4	Core
	TU872LK-2113	0.100	0.100		3.824		PREPREG
12 13	TU-872LK	0.018 0.080 0.018	0.018 0.080 0.018		3.490		Core
	TU-872LK-1080	0.076	0.076		3.598		PREPREG
14 15	TU-872LK	0.018 0.080 0.018	0.018 0.080 0.018		3.490		Core
	TU-872LK-1080	0.076	0.076		3.598		PREPREG
	TU-872LK-1080	0.076	0.076		3.598		PREPREG
16 17	TU-872LK	0.018 0.102 0.018	0.018 0.102 0.043		3.410	5	Core
	TU-872LK-1080	0.076	0.076		3.598		PREPREG
18	Foil	0.018	0.043			6	Foil
	Soldermask			0.020	4.100		SolderMask
	Ident						Ident

Figure 4. HSD Layer stackup

The PCB board thickness is limited by ATCA [5] standard to ~2mm; hence the average dielectric layer thickness is only about 0.1mm. Given the 100Ω differential or 50Ω single-ended impedance requirement, the PCB trace width of high speed signals is also driven down to about 0.1mm. This limit on the PCB signal trace width will in turn set the minimum resistive loss on a PCB channel. The pre-layout simulation was used in PCB material selection. An example is shown in Figure 5, in which the signal loss was simulated for two PCB materials. For the standard PCB material FR4, with loss tangent of 0.035 (left graph), the loss is dominated by dielectric loss above 1 GHz. Using a modified FR4 with a loss tangent of 0.01 (right graph), the PCB dielectric loss is brought down under the PCB resistive loss up to 10 GHz. From this simulation, it was concluded that a PCB material with loss tangent of 0.01 would be adequate for the HSD. Any PCB material with even smaller loss tangent would increase the cost significantly without much improvement in the overall PCB lost performance. As a result, the PCB material TU-872LK from Taiwan was chosen for HSD, which has a loss tangent of 0.009.

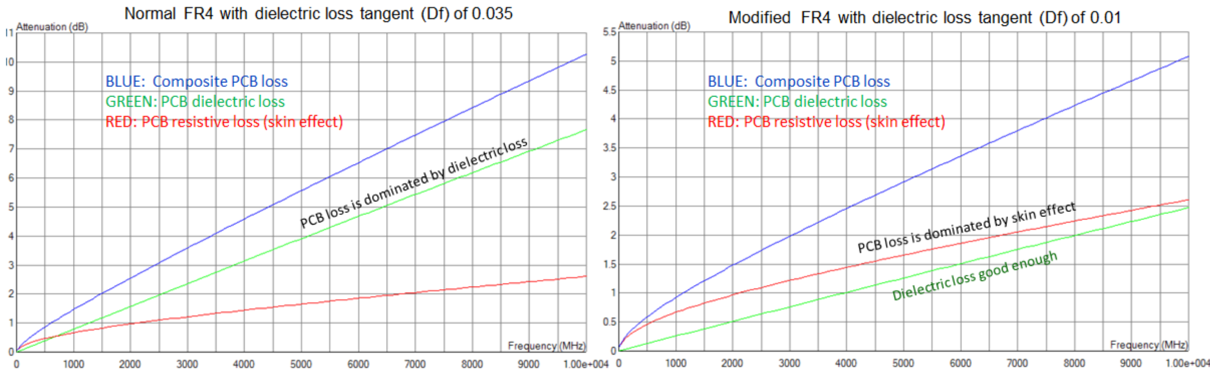


Figure 5. PCB material loss simulation

High-speed transceivers are utilising differential architecture with 100Ω termination. The HSD PCB differential impedance is specified at 100Ω to match the termination inside high-speed components. It is not uncommon now to specify impedance tolerance of ±5% in telecom industry for multi-Gb/s PCB design. However, the chosen PCB manufacturer couldn't make it due to the complexity of HSD. Hence the impedance tolerance for HSD is still set to ±10%.

Impedance ID	Structure Image	Structure Name	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width	Trace Separation	Ground Strip Separation	Broadside 2nd Layer	Calculated Impedance	Target Impedance	Tol (+/- %)
1		Edge Coupled Coated Microstrip 1B	1	2	0	0.102	0.140	0.000	0	97.880	100.000	10.000
2		Edge Coupled Offset Stripline 1B1A	3	2	4	0.121	0.235	0.000	0	98.240	100.000	10.000
3		Edge Coupled Offset Stripline 1B1A	8	7	9	0.102	0.254	0.000	0	97.570	100.000	10.000
4		Edge Coupled Offset Stripline 1B1A	11	10	12	0.102	0.254	0.000	0	97.570	100.000	10.000
5		Edge Coupled Offset Stripline 1B1A	16	15	17	0.121	0.235	0.000	0	98.240	100.000	10.000
6		Edge Coupled Coated Microstrip 1B	18	17	0	0.102	0.140	0.000	0	97.880	100.000	10.000

Figure 6. HSD Impedance specification

PCB vias have a significant effect on multi-Gb/s signals. The single most important factor of vias is the stub length. On HSD, blind via/micro-via technology is used as shown in Figure 4, which connects traces from layer 1 to 3 and from layer 16 to 18. The performance of blind vias will be compared to that of through-hole vias.

1.7 Relevant standards

Following relevant industry standards are referenced during HSD development and test.

SFF-8431, Specification for enhanced small form factor pluggable module SFP+ [6]

IEEE 802.3ba, 40 and 100 Gigabit Ethernet Architecture [7]

2 Measurements and Simulation

2.1 PCB material test

Two electrical parameters, dielectric constant (Dk or ε_r) and loss tangent (Df), of PCB dielectric material are very important to the multi-Gb/s PCB simulation and need to be verified on HSD.

The dielectric constant can be calculated using equation

$$v = \frac{c}{\sqrt{\varepsilon_r}}$$

where c is the speed of light in vacuum and v is the signal speed on HSD PCB. To measure signal speed accurately, two small copper pads are placed 5 cm apart on a signal track on layer 3. The TDR (see more in 2.6) measurement on this signal track is shown in Figure 7. HSD signal speed measurement

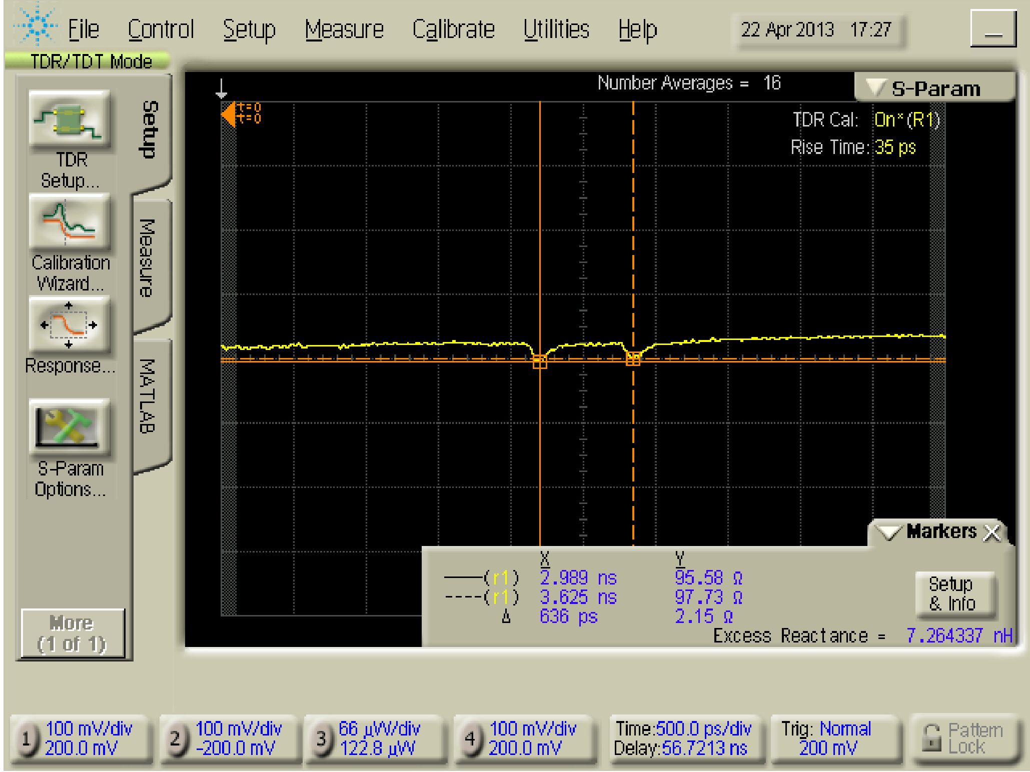


Figure 7. HSD signal speed measurement

The two small negative bumps are reflections due to the small capacitive copper pads on the signal track. The time difference between the two reflections is 636ps, which is the round-trip propagation delay between the two copper pads. Hence the signal propagation speed on HSD layer 3 is

$$v = \frac{2 \times 5cm}{636ps} = 1.572327 \times 10^8 m/s$$

Given $c = 2.997924 \times 10^8 m/s$,

$$\varepsilon_r = \left(\frac{c}{v}\right)^2 = 3.635$$

So the measured HSD PCB dielectric constant is 3.635. The dielectric constant from material datasheet (see Figure 4) is 3.598, which is very close to the real measurement.

The PCB dielectric loss tangent cannot be easily measured directly with a TDR scope. A TDR scope can measure the overall PCB loss, including dielectric loss, resistive loss and reflection loss, but it is hard to isolate the individual components.

The verification method used here is to model a PCB signal channel and extract its composite S-parameters with a PCB simulation tool. Then compare it to the S-parameter measurement on the TDR scope. In Figure 8, the composite PCB loss over a 50cm differential PCB channel on HSD is simulated with a loss tangent of 0.01 (shown in green line). The red line shows the TDR scope measurement. It can be seen that simulation agrees with measurement very good up to about 6GHz. This verifies that the real PCB material dielectric loss tangent closely matches its datasheet parameter 0.009. Beyond 6 GHz, the simulation and measurement begin to diverge, which is due to limitations on TDR scope noise floor and PCB channel model accuracy.

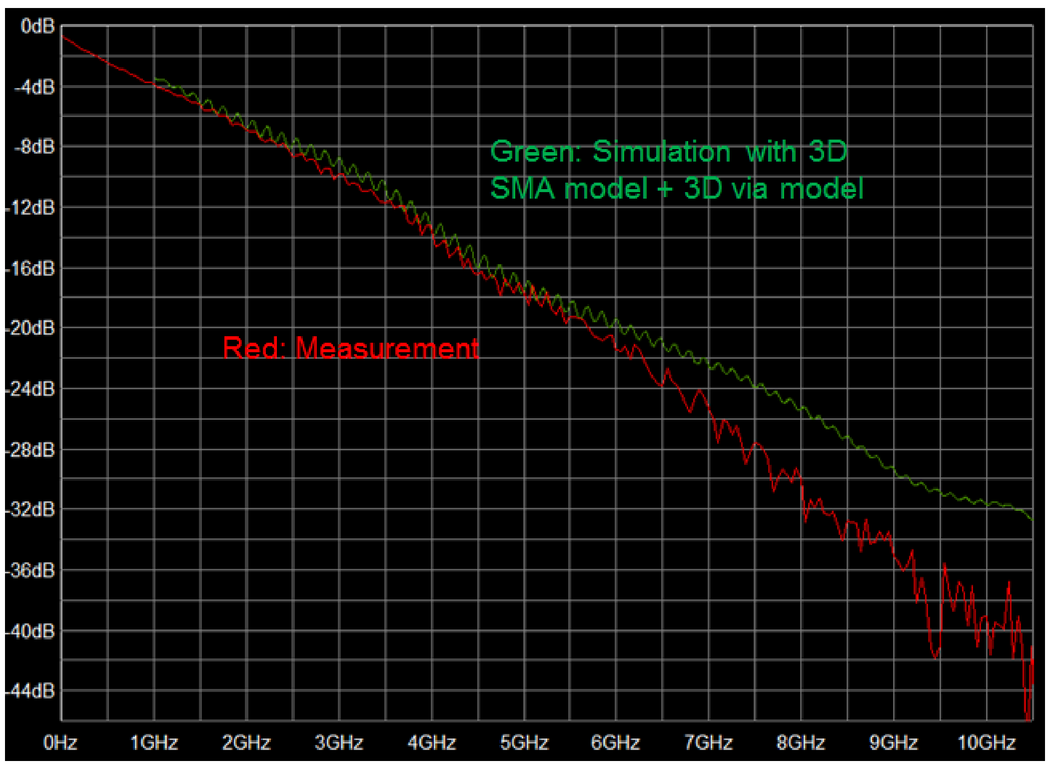


Figure 8. PCB S-parameter simulation and measurement

2.2 Power supply

Xilinx GTX/GTH transceiver requires the total peak-to-peak noise at its power pins to be less 10mV. This is a very stringent requirement. The HSD is designed as an ATCA module. The power input for ATCA module is 48V DC. An on-board main DC-DC convertor first steps down 48V to 12V. Xilinx GTX/GTH needs power supplies at around 1V. Linear regulators are usually the best means to provide voltage regulation for GTX/GTH transceiver. However the efficiency of linear regulators depends on the voltage difference between input and output. In case of HSD, the input is 12V and output is about 1V, the efficiency of linear regulator would be less than 10%. Given the high current needed for the whole HSD module, 10% efficiency is not acceptable.

To avoid this efficiency problem of linear regulators, a two-stage regulation could be used. First, DC-DC switching regulators step down 12V to somewhere slightly higher than the required voltages. Second, linear regulators provide final regulations. This scheme would work best for GTX/GTH transceivers. However, Xilinx high-end FPGA needs about 10 differential power supplies, a two-stage regulation scheme would need significant more PCB estate than available on the future eFEX module.

On HSD, a low noise single-stage DC-DC switching power module from TI (PTH08T210W) was chosen for power regulation for GTX/GTH transceivers. Figure 9 shows the power supply noise measurements of this power module with different output voltages. With output voltage at 1V, only 3.2 mV Pk-Pk noise was measured. With output voltage at 1.8V, 4.8 mV Pk-Pk noise was measured. Both noise amplitudes are well within the 10mV requirement of Xilinx GTH transceivers.

2.2.1 Learning points

A few problems related to the PCB layout for power modules were discovered in HSD v1 and were corrected in HSD v2.

The TI power module PTH08T210W used on HSD is a surface mount component. Its two output pins are connected to corresponding power plane with 8 small vias in HSD v1. Given the maximum output current capacity of 30A, each small via would need to carry a maximum of nearly 4A current. The rule of thumb is 1~3A/via. So for the eFEX design, a through-hole version of power module should be used or more vias should be used to connect output pins to power plane.

The voltage sensing wires of PTH08T210W were also connected to local power/ground planes using vias on HSD v1, which effectively disabled the power supply voltage sensing function. There is a very noticeable voltage drop of as high as 30 mV (3%) in HSD v1 test when all GTH or GTX transceivers are activated.

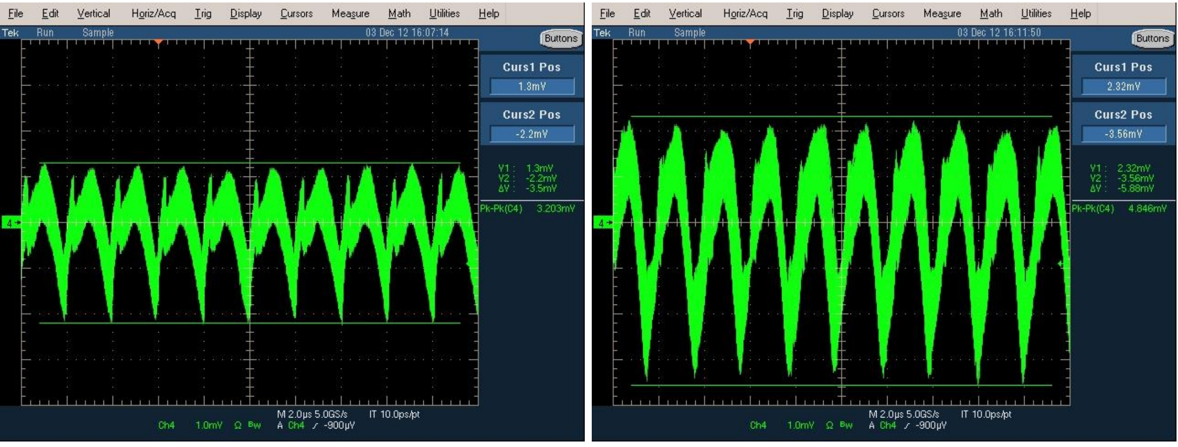


Figure 9. HSD Xilinx GTH power supply noise
(Left, 3.2mV pk-pk on 1.0V MGTAVCC; right 4.8mV pk-pk on 1.8V MGTAVCCPLL)

2.3 Differential skew

The cause of the differential skew is illustrated in Figure 10. FR4 PCB material is made of fibre glass and epoxy resin. The fibre glass in FR4 material is orthogonally woven. The fibre glass has a lower dielectric constant than epoxy resin. The trace sitting directly on a fibre strand (+ side of differential pair in Figure 10) sees a lower composite dielectric constant than the trace sitting in the gap between fibre strands (- side of differential pair in Figure 10). So signal propagation speed is different for the two traces of a differential pair, which causes differential skew. Without control, the differential skew was measured as high as 40 ps for a 15 cm long differential pair on a PCB module for another experiment, which was a disaster for 10 Gb/s signal.

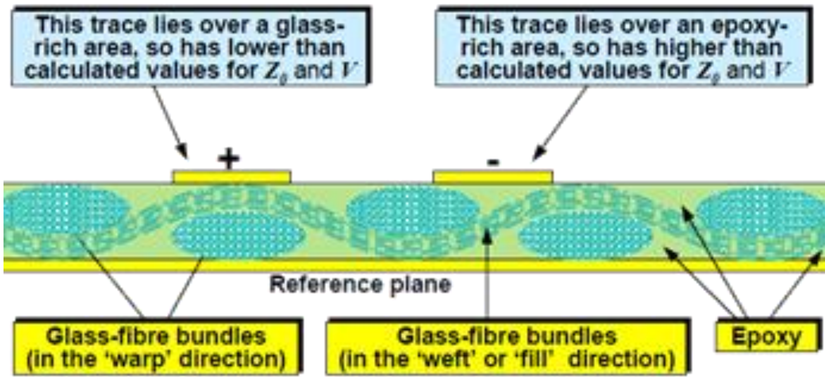


Figure 10. Cause of differential skew

In order not to cause significant degradation effect, the differential skew should be controlled to less than 10% of a signal bit period, that is 10 ps for a 10 Gb/s signal. The method used on HSD for differential skew control is to rotate HSD module 22 degree with reference to the PCB panel as shown in Figure 11. In this way, no pcb trace is running in parallel to fibre glass strand in FR4, hence averaging out the difference of dielectric constants between fibre glass and epoxy resin.

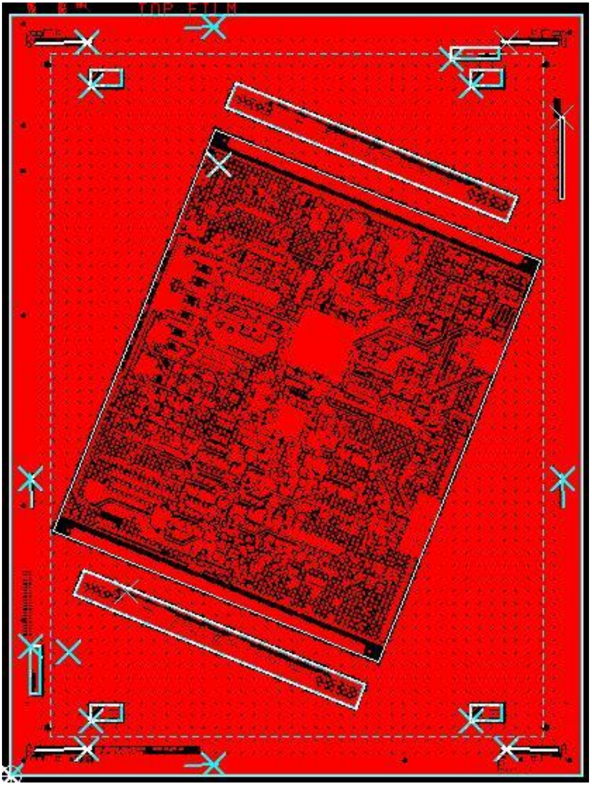


Figure 11. Differential skew control

Figure 12 shows the differential skew measurement of ~4 ps on a 13 cm channel on HSD, which is a very good result.

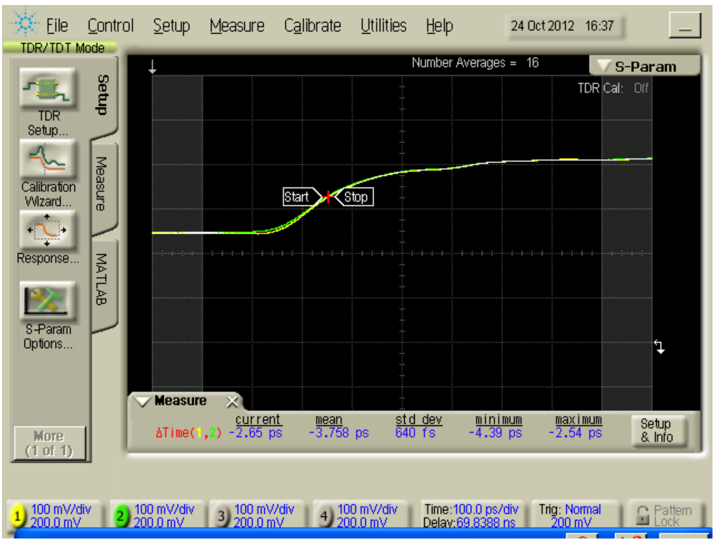


Figure 12. HSD differential skew measurement

2.4 Clock jitter

Jitter can be measured in time domain in many different ways, such as cycle-to-cycle jitter, period jitter and Time Interval Error (TIE) jitter. Cycle-to-cycle jitter measures the short-term variation in the clock period between adjacent clock cycles and only contains the highest frequency components of jitter. Period jitter measures variation in the clock period over all measured clock cycles and contains relatively high frequency components of jitter. TIE jitter measures the actual deviation from the ideal clock (golden PLL) and includes all the jitter frequency components within the bandwidth of the sampled data.

Jitter can also be measured in frequency domain as spectrum noise and phase noise. A FFT post-processing on TIE jitter measurement can also give equivalent frequency domain information on the jitter source.

Jitter analysis normally involves jitter decomposition as shown in Figure 13, which is a very good diagnostic tool to find the root cause of jitter-related problem. Random jitter is caused by accumulation of a large number of uncorrelated processes that have small magnitude such as thermal noise, shot noise, pink noise, etc. Random jitter is typically represented as a Gaussian distribution and quantified by the standard deviation. Deterministic jitter is caused by power supply noise, ground bounce, crosstalk, dispersion, impedance mismatch, inter symbol interference, duty-cycle distortion, etc. Deterministic jitter is typically detected as deviation of the PDF from Gaussian distribution and quantified by the peak-to-peak value.

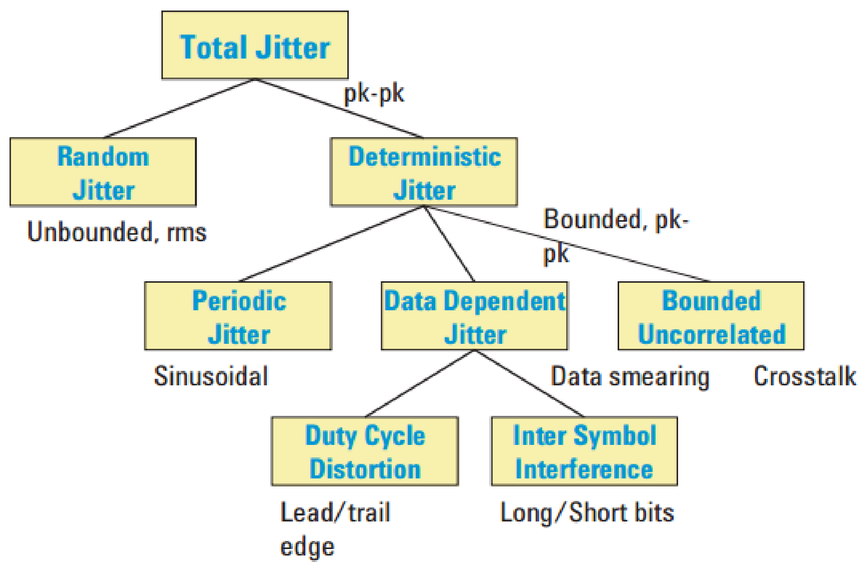


Figure 13. Jitter decomposition

Multi-Gb/s high-speed links require high-quality low jitter reference clock. The TIE jitter is the most relevant and important parameter for the reference clock quality of high-speed link. As far as clock jitter is concerned, there is no data dependent jitter component. IEEE 802.3ba defines the mask of the sinusoidal component of jitter tolerance for the receiver tests in Figure 14, which means a compliant receiver should be able to tolerate much bigger jitter at lower frequency than at higher frequency. Therefore, a number of clock sources are evaluated according to their clock TIE jitter with bandwidth over 100 KHz.

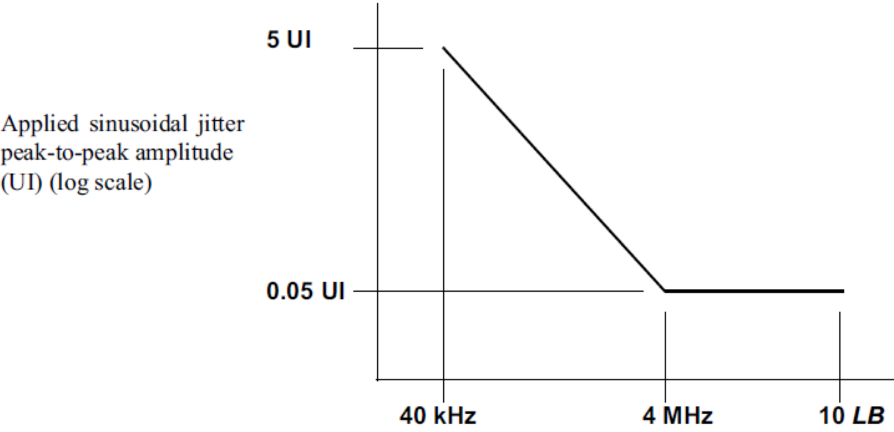


Figure 14. Illustration of the mask of the sinusoidal component of jitter tolerance

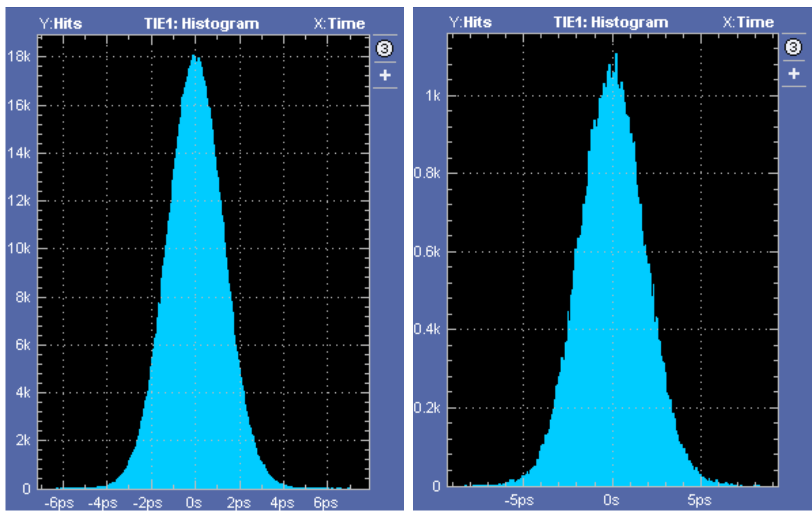


Figure 15. Clock TIE jitter (>100KHz)
Left: CDCE62005 1.3ps RMS. Right: ECL Crystal on HSD 1.8ps RMS

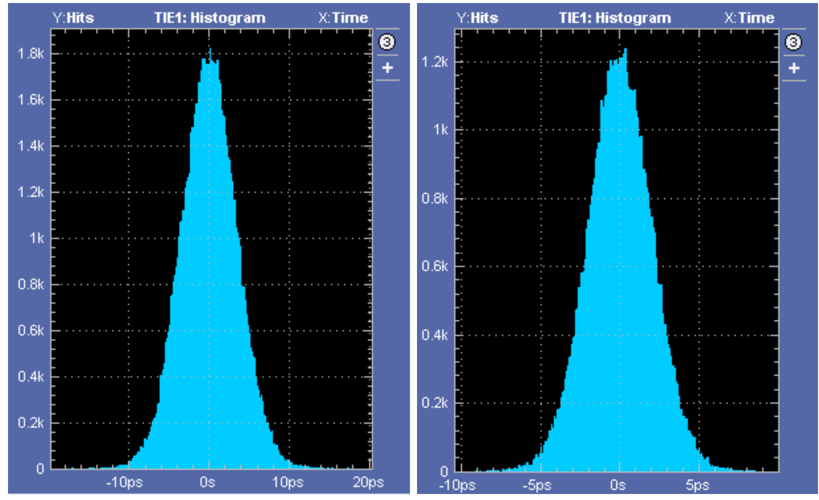


Figure 16. Clock TIE jitter (>100KHz)
Left: LMK0482xEVAL 3.5ps RMS. Right: LMK03200EVAL 2.0ps RMS

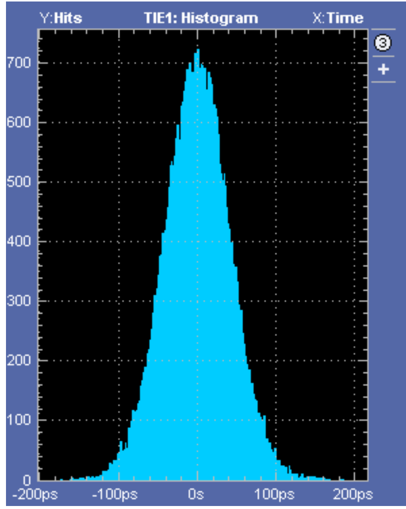


Figure 17. Clock TIE jitter (>100KHz)
TTC clock NIM output from TTC VI, 42ps RMS

As shown in figure 15-17, the TI CDCE62005 PLL, which is already used on HSD, provides the best quality reference clock with only 1.3ps RMS jitter. The current TTC clock has a really bad jitter performance with 42ps RMS jitter.

A nice feature of CDCE62005 is that it has a sync input pin (Figure 18), which can be used to guarantee the fixed phase relationship between its reference input and output clocks. Metastability could happen with the output divider reset. This has been tested and could cause up to 1ns phase difference between reference input and output clocks during power cycle.

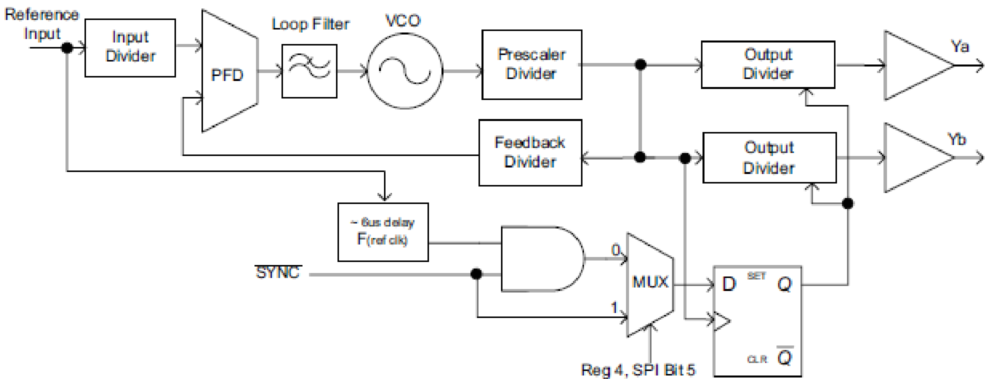


Figure 18. CDCE62005 output synchronization

2.5 Crosstalk

Crosstalk is the coupling of energy from one line to another via mutual capacitance (electric field) and mutual inductance (magnetic field). As shown in Figure 19, crosstalk is highly directional, and near end crosstalk (NEXT) and far end crosstalk (FEXT) have very different behaviour.

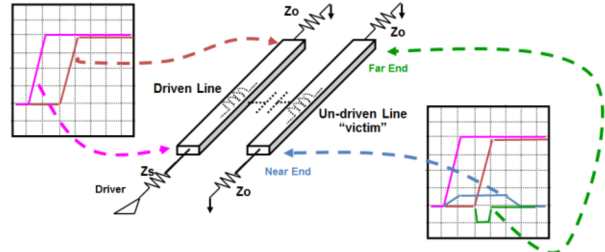


Figure 19. Crosstalk Overview

HyperLynx has been used to simulate the crosstalk and derive the design rule for crosstalk control. Figure 20 shows very good correlation achieved between HyperLynx simulation and real measurement.

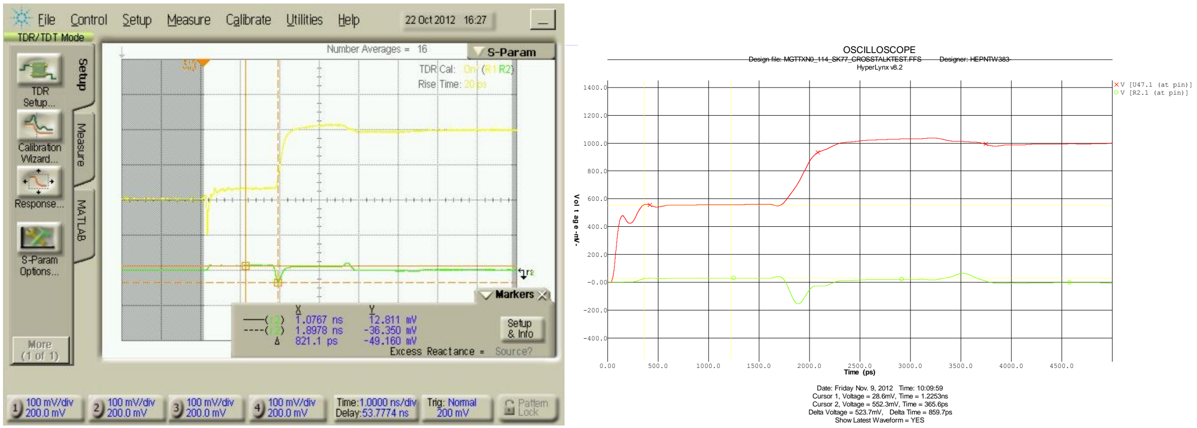
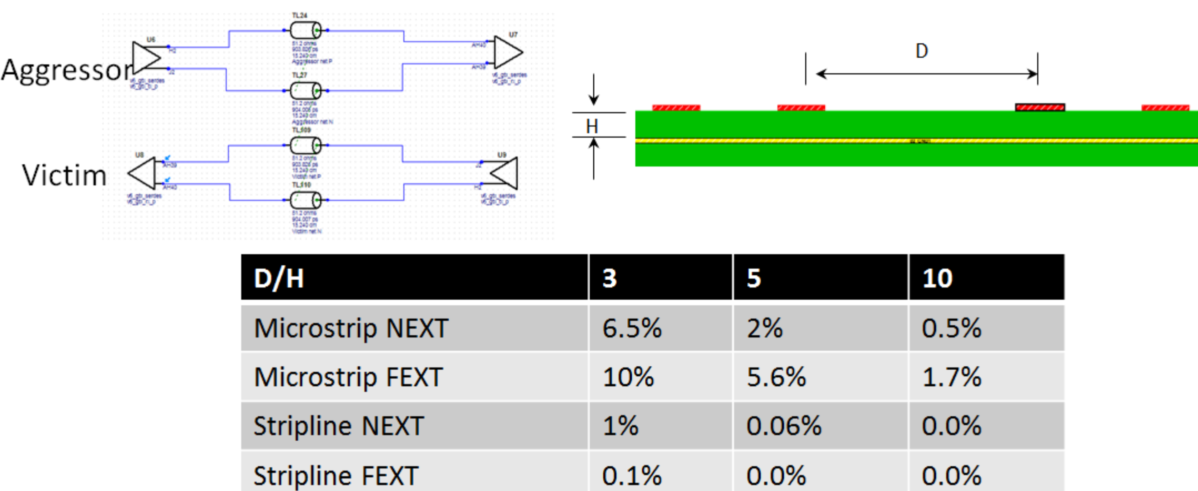


Figure 20. Correlation of crosstalk simulation (right) to measurement (left)

In multi-Gb/s high-speed design, the inductive crosstalk is much bigger than the capacitive crosstalk. Hence, the best control of crosstalk is the ratio between trace separation (D) and the height (H) of traces from its ground plane. A series of simulations have been done with results shown in Figure 21.



D/H	3	5	10
Microstrip NEXT	6.5%	2%	0.5%
Microstrip FEXT	10%	5.6%	1.7%
Stripline NEXT	1%	0.06%	0.0%
Stripline FEXT	0.1%	0.0%	0.0%

Figure 21. HSD PCB differential crosstalk simulations

The simulation results show that microstrip traces on top/bottom layers have much worse crosstalk performance than stripline traces on inner layers. To achieve about 1% crosstalk between adjacent differential pairs, the D/H ratio have to be more than 10 for top/bottom layers.

2.6 Time Domain Reflectometry (TDR)

PCB impedance control is very important in multi-Gb/s high-speed PCB design. Impedance mismatches in a PCB channel would cause multiple reflections to degrade signal eye opening. The PCB impedance control includes the PCB traces, vias, AC coupling capacitors and connectors.

TDR has been used to verify the HSD PCB impedance. Figure 22 shows the measured impedance of 123Ω on one differential channel on HSD v1, which is out of tolerance specification. The microsection on HSD v1 shows that some layers are of wrong thickness. As a result, the HSD v2 was manufactured.

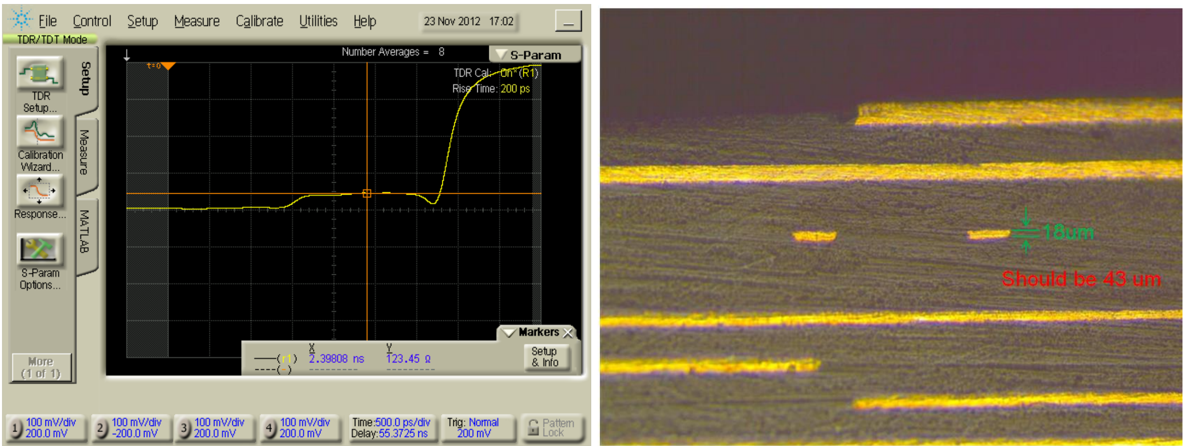


Figure 22. TDR differential impedance measurement and microsection on HSD v1

The TDR tests on HSD v2 shows very good impedance control for all the inner layers. However, the differential impedance on top/bottom layers is still out of specification. Figure 23 shows the measured impedance of 119Ω on top layer of HSD v2 test coupon and its microsection. The microsection has revealed overplating (up to 40%) on top layer, which led to overetching (up to 25%).

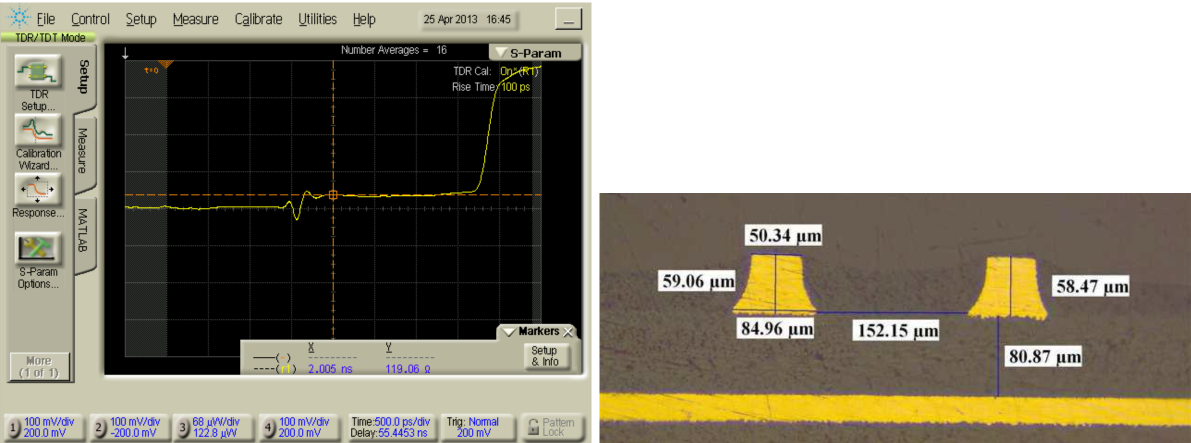


Figure 23. Left: TDR differential impedance measurement and microsection on HSD v2

2.6.1 Corrective actions

Given the problems encountered in the PCB production, following actions are recommended for next multi-Gb/s high-speed PCB job.

In design phase:

1. Recommend to completely flood the outer layers with copper.
2. Coplanar waveguide structure (with advice from PCB manufacturer) for controlled impedance tracks.
3. Move high-speed traces to inner layers if possible.

In manufacturing phase:

1. Review the plating parameters and control the copper deposition for a better distribution.
2. Microsections to be done after panel plating.
3. Measure the copper weight prior to etching.
4. First off to be checked on AOI (Automatic Optical Inspection) and validated prior to processing the rest of the job.

2.6.2 Effect of AC coupling capacitor

The Xilinx FPGA multi-Gb/s transceiver GTX/GTH needs AC coupling on the receiver side. In order to minimise the impedance discontinuity due to these capacitors, an extremely small type capacitor, 0201, has been used on HSD. Figure 24 shows the TDR measurement on a channel with AC coupling capacitors. The reflection of capacitor is determined by the distance of it from the probe. There is a very minor negative reflection, which is due to the body capacitance between capacitor body and underneath ground plane. Given the negligible amplitude, there is no need to cut a void, as suggested by Xilinx user guide, on the underlying ground plane to further reduce the body capacitance of this small capacitor.

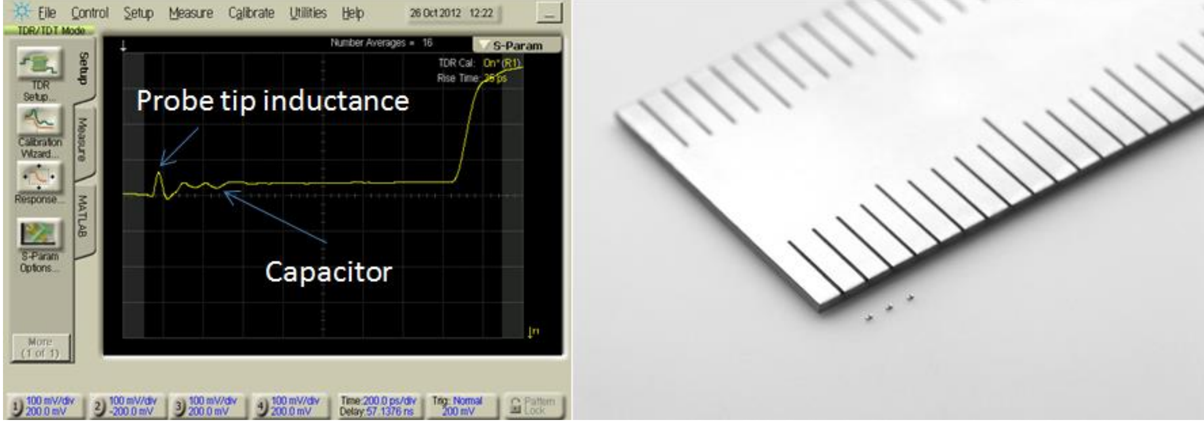


Figure 24. TDR measurement on AC coupling capacitor

2.6.3 Routing under BGA

Figure 25 shows the layout of HSD under FPGA BGA area. There are many differential pairs running significant length (up to 5cm) under the BGA area. The differential pair configuration as recommended by PCB manufacturer in Figure 6 cannot be followed due to the constraints of via grid. With the aid of HyperLynx simulation, the differential pair is shrinked and squeezed to fit between via grid. Figure 26 shows the TDR test on such a differential channel and the impedance discontinuity is very pronounced with differential impedance under BGA area rising to 125Ω.

This TDR test shows that HyperLynx 2D solver is not good enough, that is because HyperLynx 2D solver assumes a rectangle cross section of PCB traces and does not take into account practicalities of manufacturing process such as plating, etching, etc. The HSD PCB manufacturer has agreed to provide recommendations for differential pair impedance configuration under BGA area based on their more advance solver software.

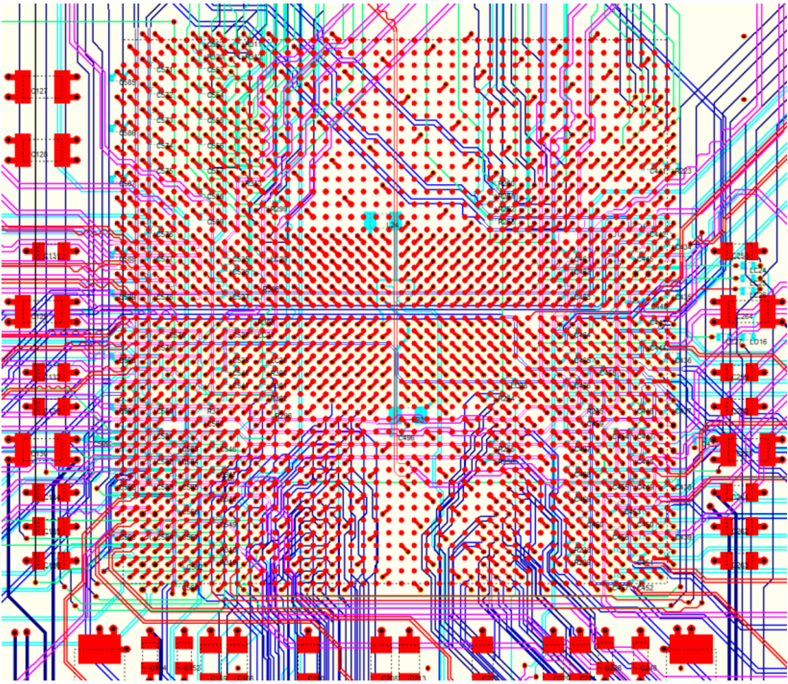


Figure 25. Routing under BGA

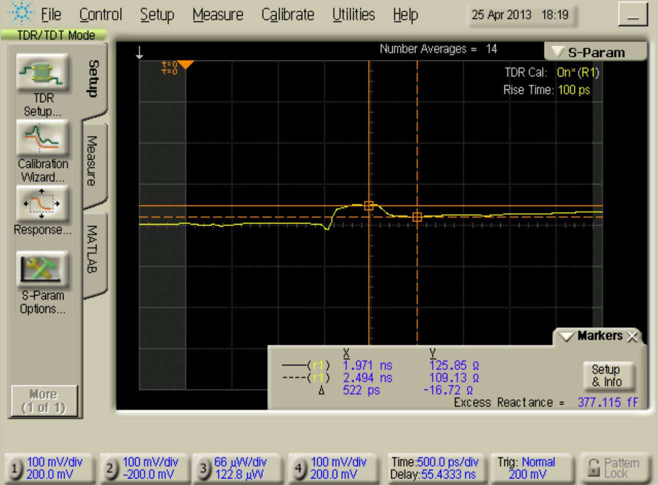


Figure 26. Differential impedance under BGA

2.7 Time Domain Transmission (TDT)

The TDT measurement has been mention in section 2.1, where it is used to verify the PCB material dielectric loss tangent. Figure 27 below shows more TDT measurements on HSD v2, which, in general, match corresponding PCB S-parameter simulations very well up to 6 GHz.

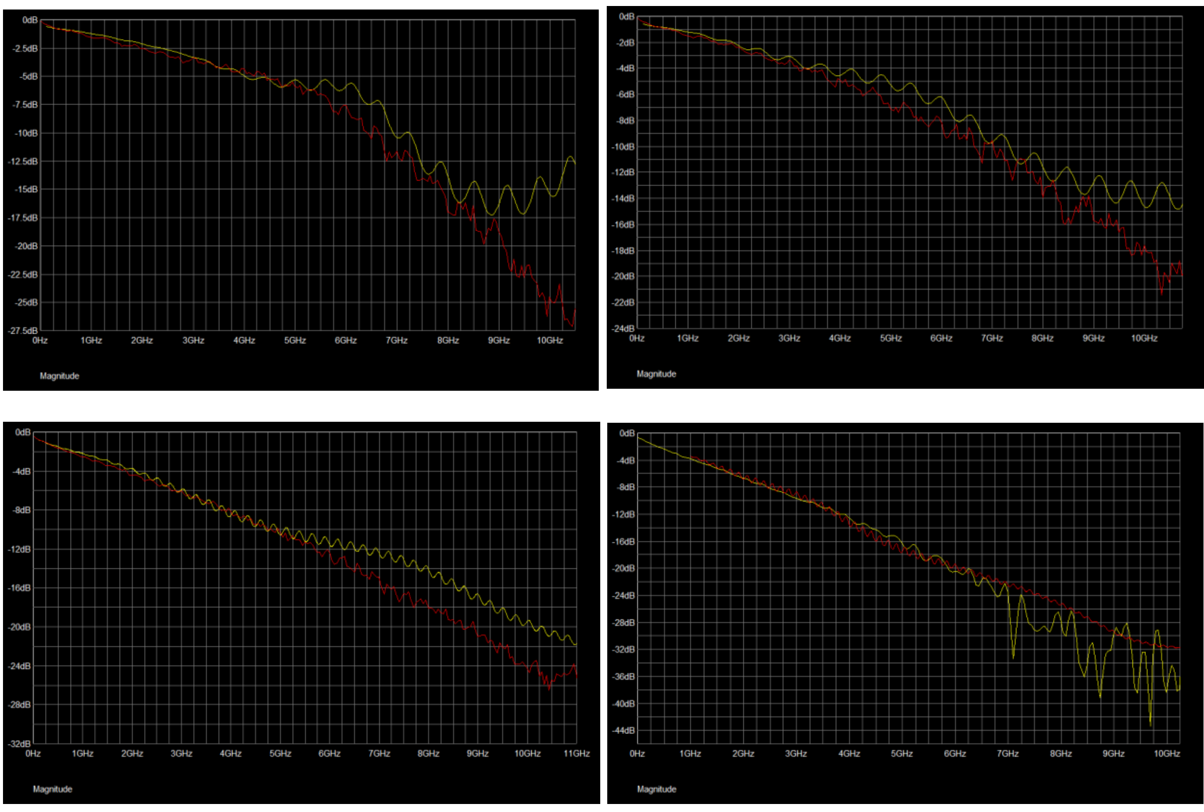


Figure 27. HSD PCB TDT test. Red curve: real measurement, Yellow curve: simulation.

Another way of using this TDT measurement is to check the compliance of PCB design against relevant industry standards. The SFF-8431 defines the high-speed electrical interface specifications for 10 Gb/s SFP+ optical transceivers and hosts. In particular, it gives the recommended SFI host channel S-parameter (SDD21) mask as shown in Figure 28. This can be used to guide the future design of PCB channel between optical transceivers and FPGA MGTs.

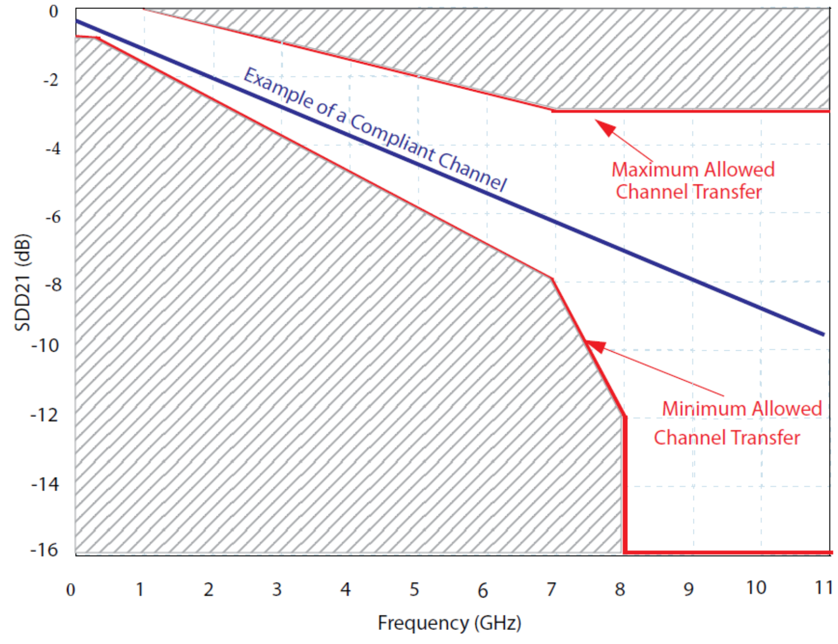


Figure 28. Example of SFI Host Recommended Channel

2.8 3D structure modelling

HyperLynx is good at 2D transmission line simulation. However, for 3D structure like PCB via and connector, HyperLynx is running out of steam. Accurate modelling of PCB via and connector is very important for PCB simulation and design at multi-Gb/s speed range. ANSYS HFSS has been used to model the PCB vias and connectors on HSD.

2.8.1 PCB via

Figure 29 shows the PCB via modelling in HFSS. The right side plot gives a series of via impedance simulations with different via anti-pad sizes. To achieve best performance, the differential via impedance should closely match the differential trace impedance 100Ω. The strategy for PCB via design is to use the smallest via diameter and fine tune the anti-pad size with 3D simulation. The smallest via diameter is limited by aspect ratio of PCB via diameter to PCB thickness due to the PCB plating process. For through-hole vias, the aspect ratio is about 1:10. For blind vias, the aspect ratio is about 1:1.

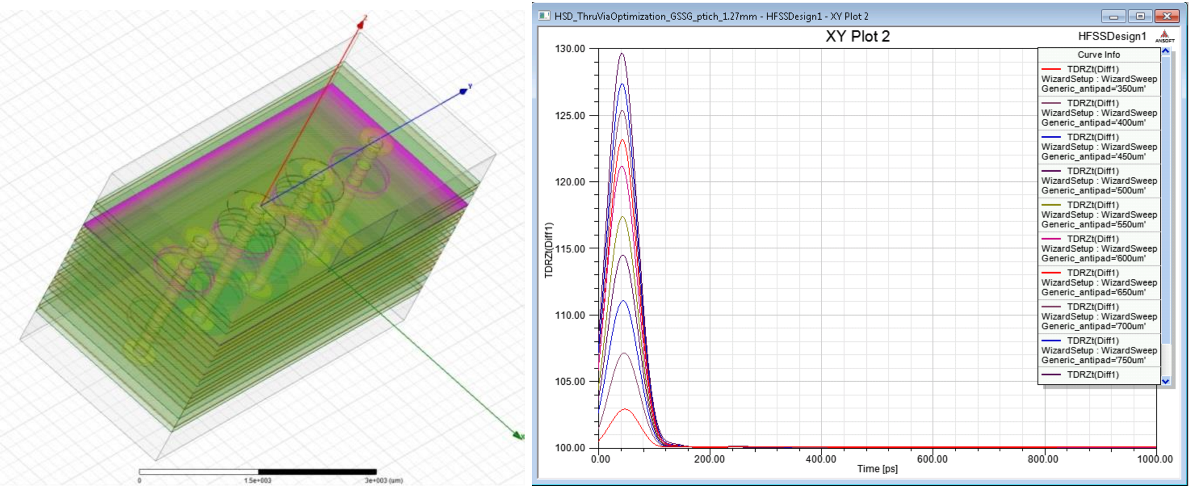
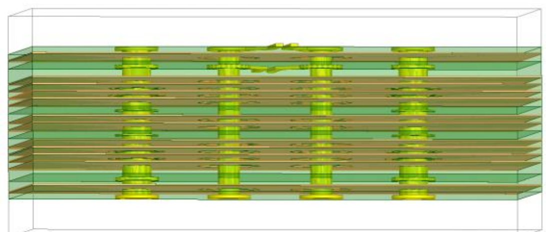


Figure 29. Modelling of PCB vias on HSD

The biggest issue with through-hole vias is the stub length, the longer stub length the more problematic. The top of Figure 30 shows a HFSS model of differential dangling vias connecting signals between top layer and inner layer 1. The lower left scope shot is the TDR measurement (72Ω) of these differential vias. The positive bump is due to the TDR probe tip. The negative reflection is due to the dangling vias. The lower right plot is the HFSS simulation result (71Ω), which closely match the TDR measurement.



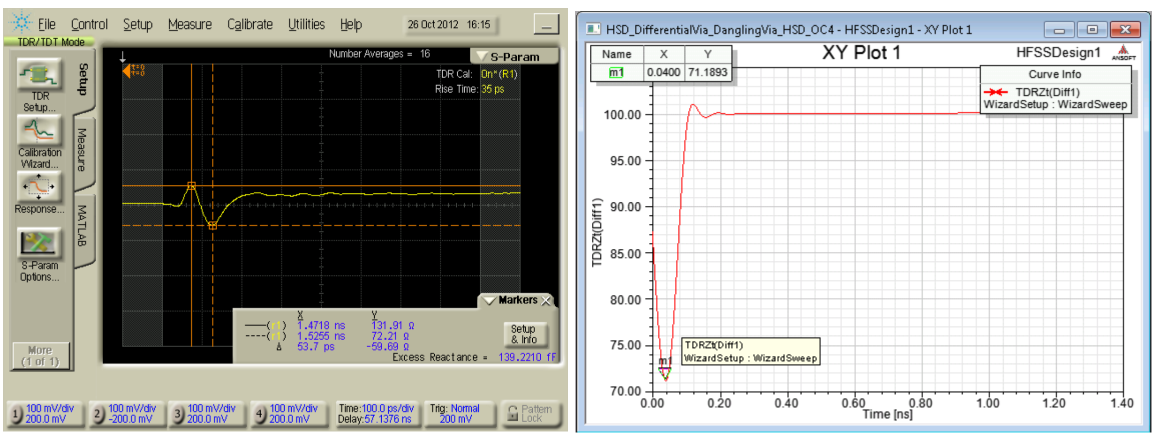


Figure 30. Dangling via TDR measurement and 3D simulation

2.8.2 SMA connector

SMA connectors are used on HSD to facilitate scope probe connection and various channel topologies. In designing HSD v1, a SMA footprint from its datasheet was used and no 3D simulation was performed on SMA connector. A simple TDR test (Figure 31) on HSD v1 reveals the problem, a huge negative reflection, with this “standard” SMA launch design, which has as low as only 20Ω impedance as opposed to it nominal 50Ω.

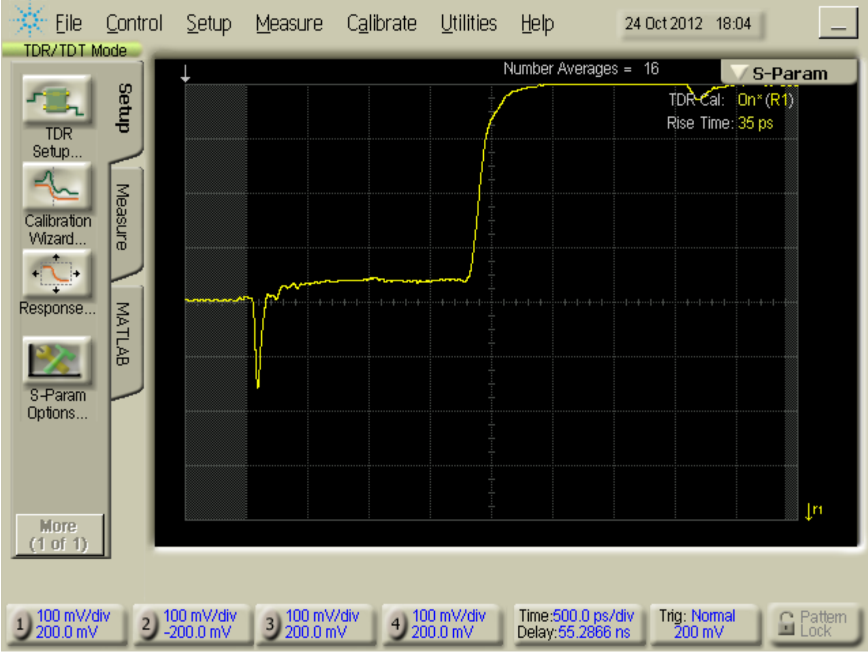


Figure 31.TDR of SMA on HSD v1

Given this problem, SMA connector was modelled in HFSS as shown in Figure 32. To compensate the huge negative reflection, a round void cut was done on the underlying power/ground planes, which would reduce the parasitic capacitance between SMA centre signal pin and power/ground planes.

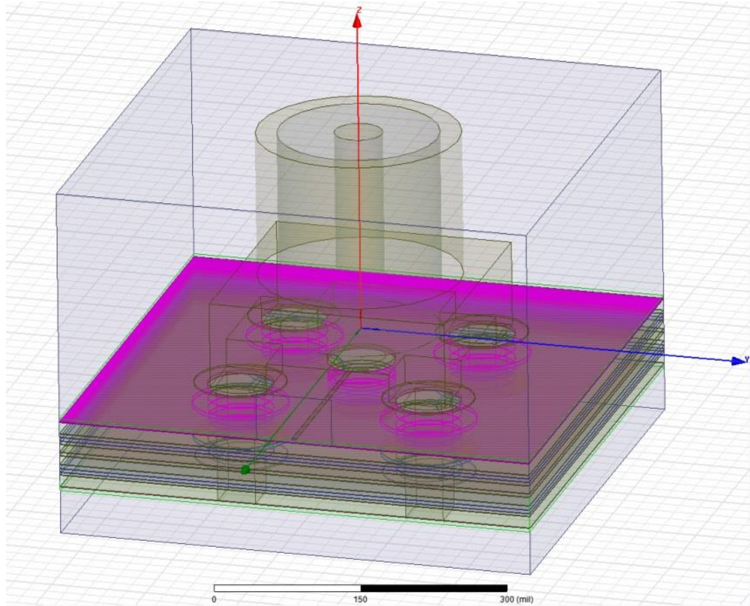


Figure 32. 3D model of SMA in HFSS

Figure 33 shows the simulation results of a series of diameters of the round void cut. When the round void cut diameter is 0, meaning no cut, the simulated SMA impedance is 24Ω, very close to the measurement on HSD v1. Base on this simulation, an optimal void cut was chosen for HSD v2.

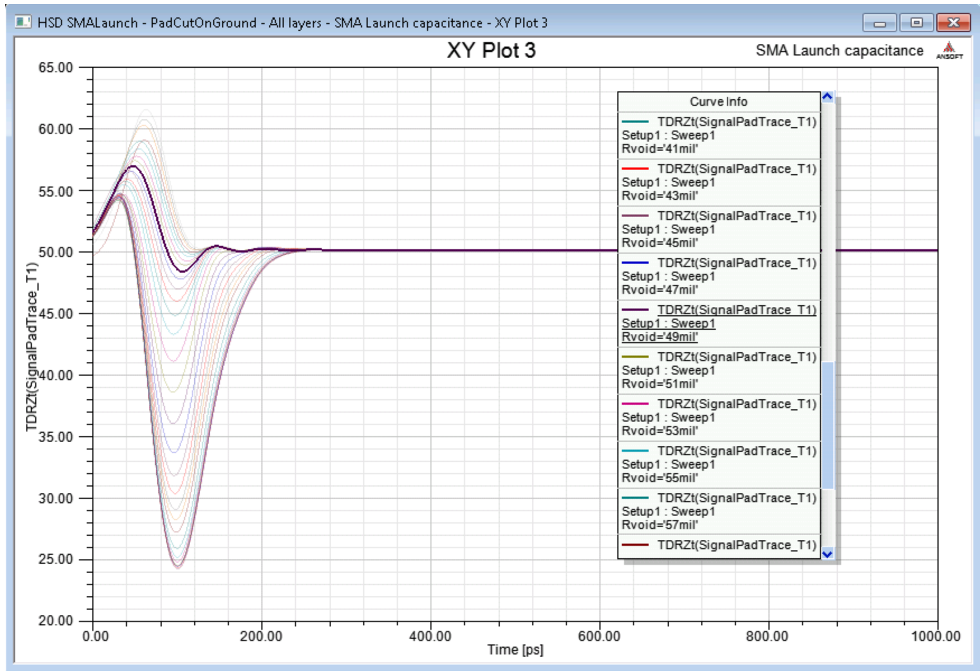


Figure 33. 3D SMA simulation

Figure 34 shows the differential TDR test on a pair of SMA connectors on HSD v2. The measured impedance is 133.8/2=66.9Ω, which is slightly higher than simulation (57Ω). This minor difference is partly due to the over etching on HSD v2 in PCB production process.

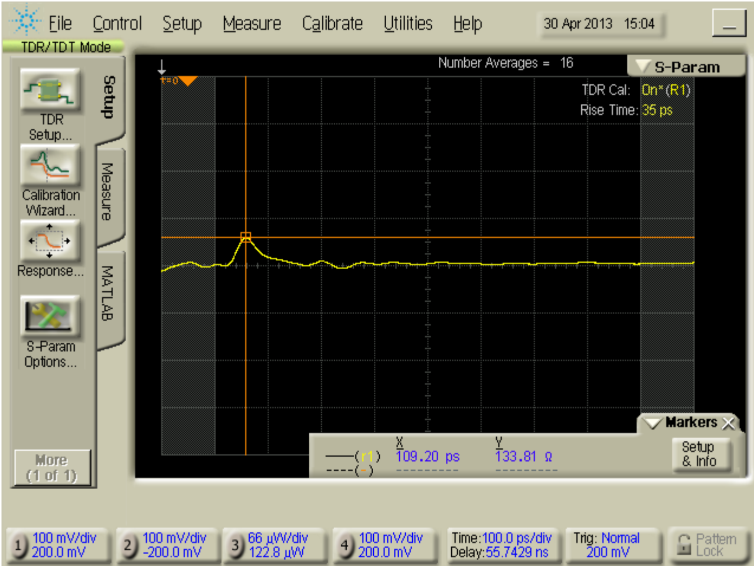


Figure 34. TDR of SMA on HSD v2

2.8.2.1 Learning points

The SMA connectors were not correctly assembled on HSD v1, which led to a bad connection on SMA central signal pin. Figure 35 shows the problem in assembly, where no solder paste was applied on the central signal pad on HSD v1. While the four ground pins on this SMA connector are through-hole pins, the central signal pin is a surface mount pin. The layout engineer had done the layout correctly with this SMA connector. However, the PCB manufacturer removed the solder paste on the SMA central pad on HSD v1.

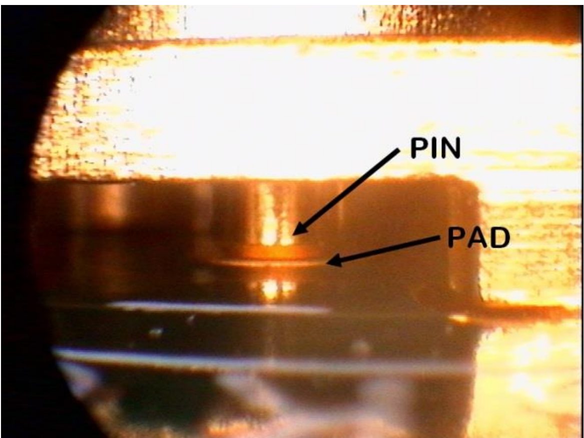


Figure 35. SMA centre signal pin assembly on HSD v1

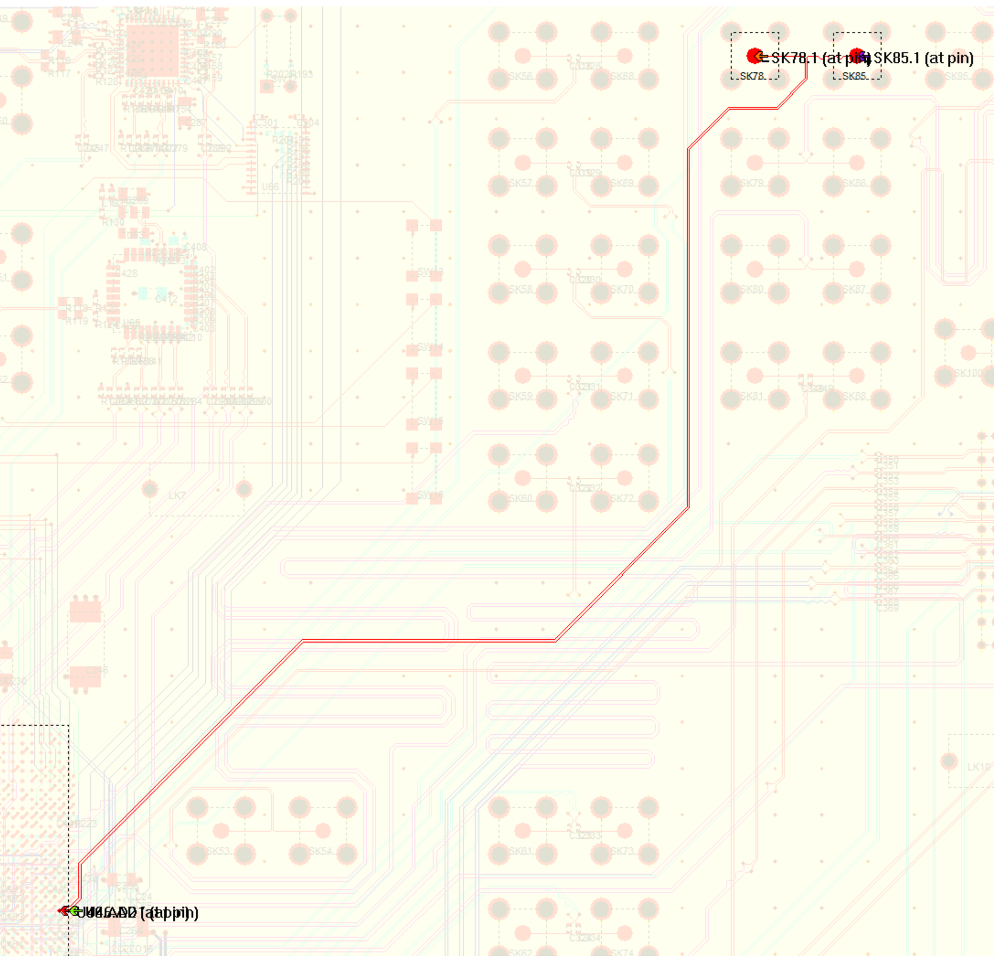
2.9 Channel simulation

In previous sections, the loss versus frequency has been discussed in detail for PCB traces, PCB materials and 3D structures, which are all important in understanding how to design effective interconnect channel. The ultimate constraints of the overall channel insertion loss depend on the timing and voltage margin measured in the Tx and Rx eye diagrams. Channel simulation provides a way to simulate the eye diagrams (and BER with statistical method) and optimize Tx/Rx equalization settings, hence provides guidance for the overall PCB channel design. Simulation itself would be meaningless unless it could be validated with real measurement. This section gives the examples of validation of PCB channel simulation on HSD.

2.9.1 Xilinx Virtex-6 [8] GTX at 5Gb/s

Upper part of Figure 36 shows a highlighted differential channel (MGTTXP1_114, GTX) on HSD PCB layout. This channel starts from a Xilinx Virtex-6 GTX and is routed on top layer and terminated at a pair of SMA connectors. The whole channel length is 15cm. The lower part shows the simulation model for this channel, which also includes the probing SMA cables and oscilloscope internal terminations towards right end. The probing cable is about 1 meter long and it has significant effect on signal eye diagram, hence cannot be ignored. The probing cable was first measured on TDR scope and its S-parameter was extracted and imported into this channel model.

The left part of Figure 37 shows the eye diagram @5Gb/s measured on oscilloscope for channel MGTTXP1_114 as shown in Figure 36. The right part shows a simulated eye diagram overlaid on the scope eye measurement. There is very good correlation between simulation and real measurement. The eye opening of scope eye measurement is slightly less than the simulated eye diagram. That is partly due to the overetching on HSD, which led to narrower PCB traces and more resistive loss. Unfortunately, HyperLynx v8.1 cannot easily account for this PCB process variation.



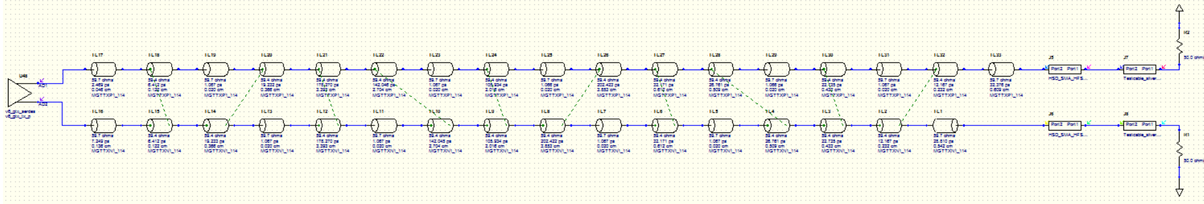


Figure 36. MGTTXP1_114 channel layout and modelling (HyperLynx) on HSD

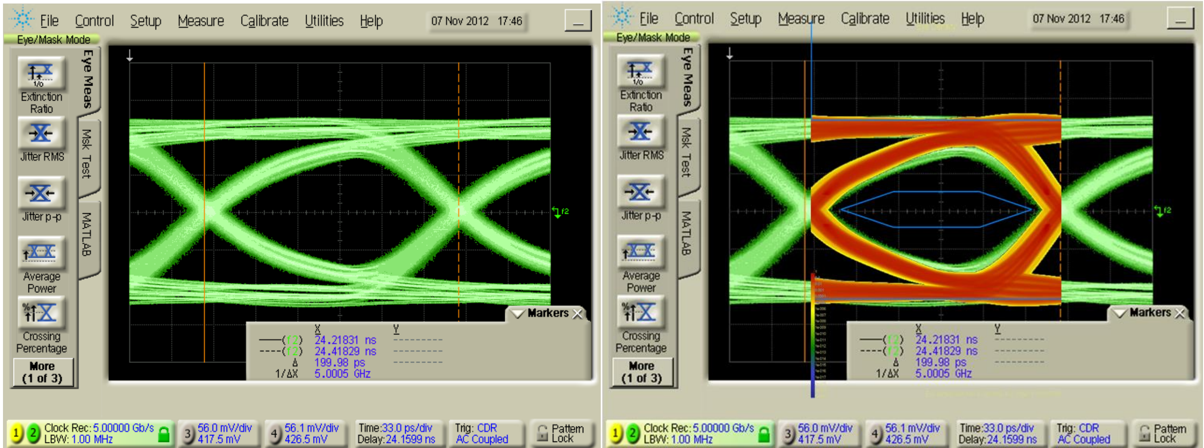
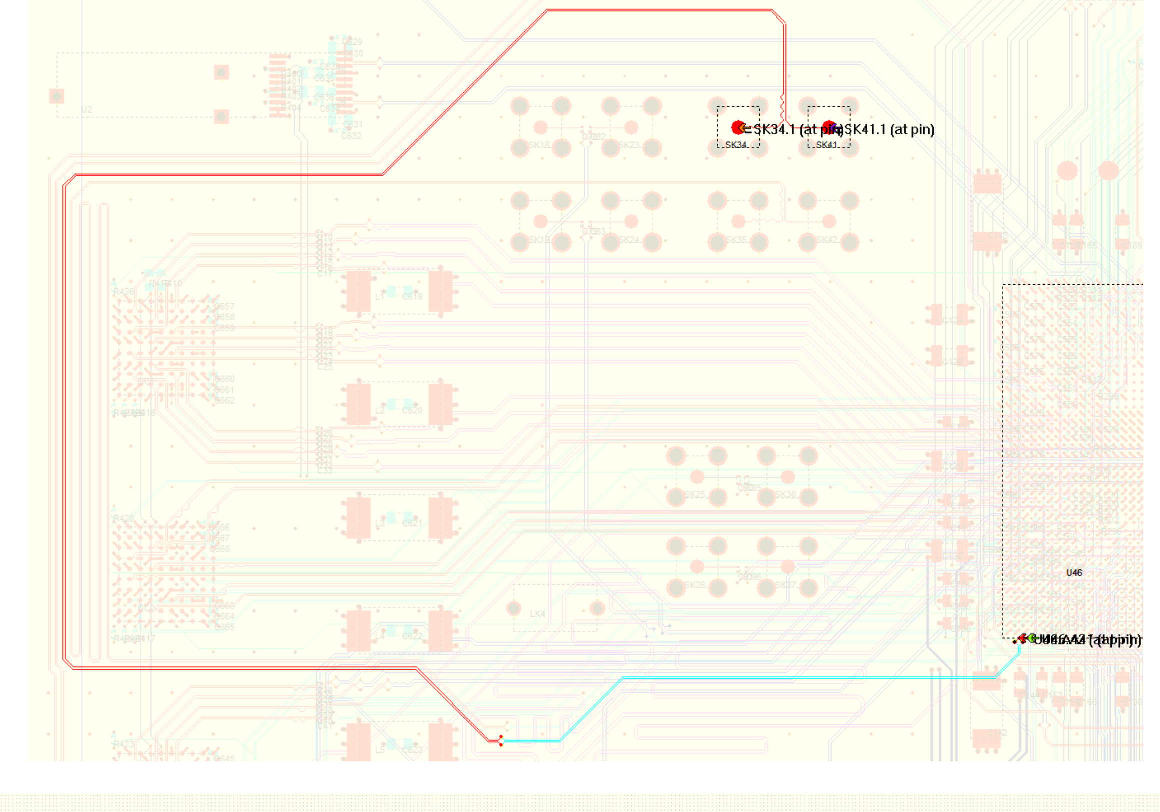


Figure 37. Xilinx V6 GTX channel simulation @ 5Gb/s on HSD

2.9.2 Xilinx Virtex-6 GTH at 10Gb/s

Upper part of Figure 38 shows a highlighted differential channel (MGTTXP2_108, GTH) on HSD PCB layout. This channel starts from a Xilinx Virtex-6 GTH and is routed on bottom layer first and then on top layer and finally terminated at a pair of SMA connectors. The whole channel length is 30cm. The lower part shows the simulation model for this channel, which also includes the probing SMA cables and oscilloscope internal terminations towards right end. The probing cable is about 1 meter long and it has significant effect on signal eye diagram, hence cannot be ignored. The probing cable was first measured on TDR scope and its S-parameter was extracted and imported into this channel model. As the signal routing changes layer twice, there are two differential vias included in the channel model.

The left part of Figure 39 shows the eye diagram @10Gb/s measured on oscilloscope for channel MGTTXP2_108 as shown in Figure 38. The right part shows a simulated eye diagram overlaid on the scope eye measurement. There is extremely good correlation between simulation and real measurement. At 10Gb/s, the PCB dielectric loss takes over the resistive loss, so the PCB overetching effect (more resistive loss) is not as pronounced as that at 5Gb/s.



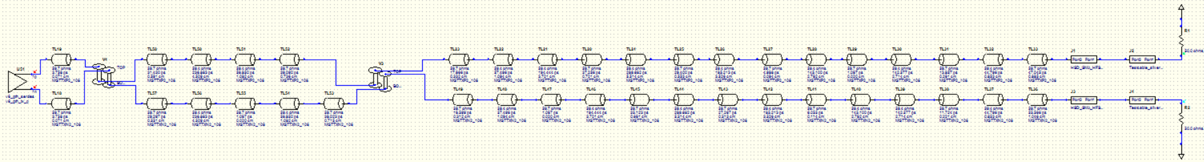


Figure 38. MGTTXP2_108 channel layout and modelling (HyperLynx) on HSD

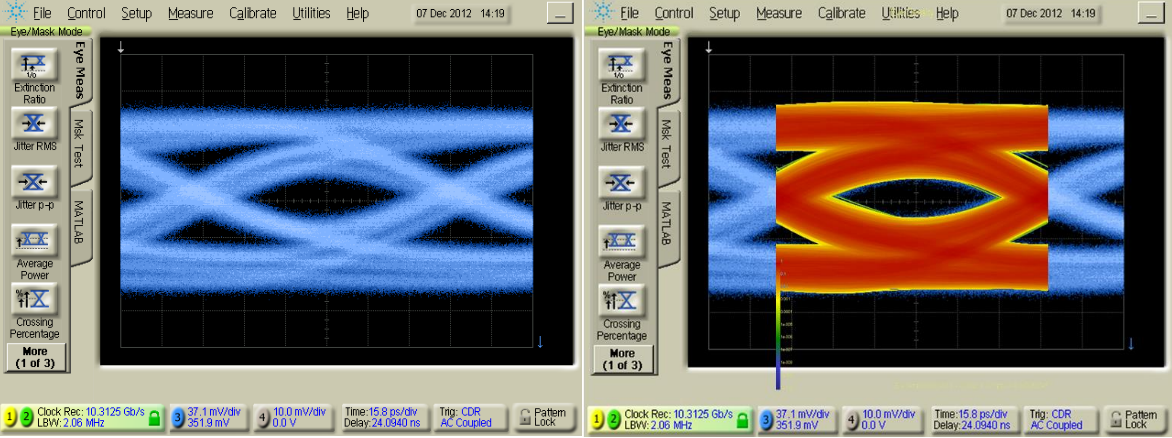


Figure 39. Xilinx V6 GTH channel simulation @ 10Gb/s on HSD

2.10 BER test

Xilinx IP core IBERT together with Chipscope software was used to perform following bit error rate tests with various channels.

2.10.1 Xilinx Virtex-6 GTX

HSD has 12 GTX optical links intended for data source/sink. These links were tested with the topology shown in Figure 40. PPOD is the 12-way parallel optical transmitter or receiver. The IBERT tests at 5Gb/s achieved over 40% margin at BER of 10^{-12} consistently. This is very good result.

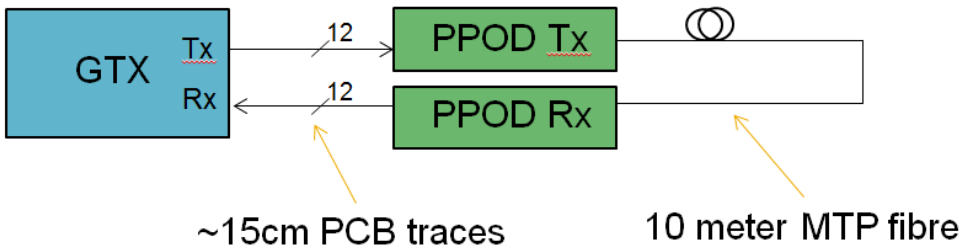


Figure 40. HSD GTX optical link test topology

2.10.2 Xilinx Virtex-6 GTH

HSD has a few GTH optical links for test purpose. These links were tested with the topology shown in Figure 41. The IBERT test results at 10 Gb/s is shown in Figure 42. Compared to GTX running at 5 Gb/s, GTH running at 10Gb/s has much smaller margin. Further, repeating IBERT scan test on the same channel under the same conditions can give big variation. Overall, the GTH optical links on HSD have a ~20±10% margin.

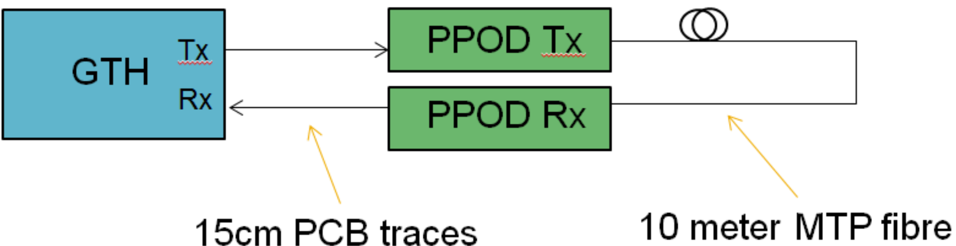


Figure 41. HSD GTH optical link test topology

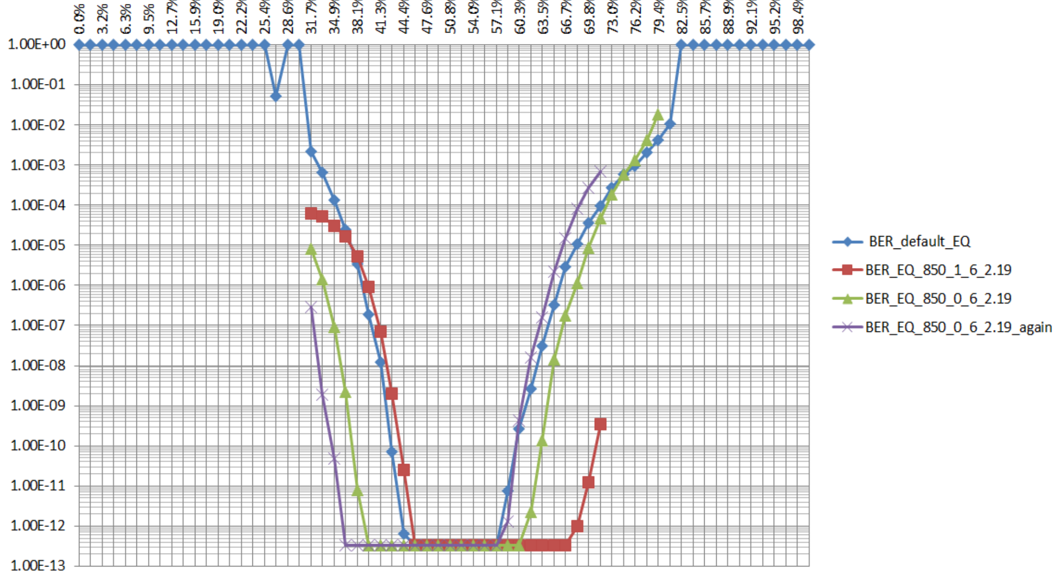


Figure 42. HSD GTH optical link IBERT bathtub curves at 10Gb/s

2.11 Eye diagram compliance test

Eye diagram measurement has been discussed in section 2.9 for the validation of channel simulation. This section discusses the eye diagram compliance test to relevant industry standard. The IEEE STD 802.3ba-2010 (40 and 100 Gigabit Ethernet Architecture) was chosen for this purpose. It is very important to follow an established standard so that the link interface between different subsystems can be clearly defined.

The upper part of Figure 43 gives the test points definition of optical link for 40/100 Gigabit Ethernet. Three test points (TP1, TP2 and TP4) were chosen for the compliance tests here. The lower part of Figure 43 shows the eye mask definition for TP1, TP2 and TP4. Hit Ratio is defined as the ratio between the number of samples hitting the mask and the total samples collected on oscilloscope. The hit ratio limit (5×10^{-5}) has been chosen to avoid misleading results due to signal and oscilloscope noise.

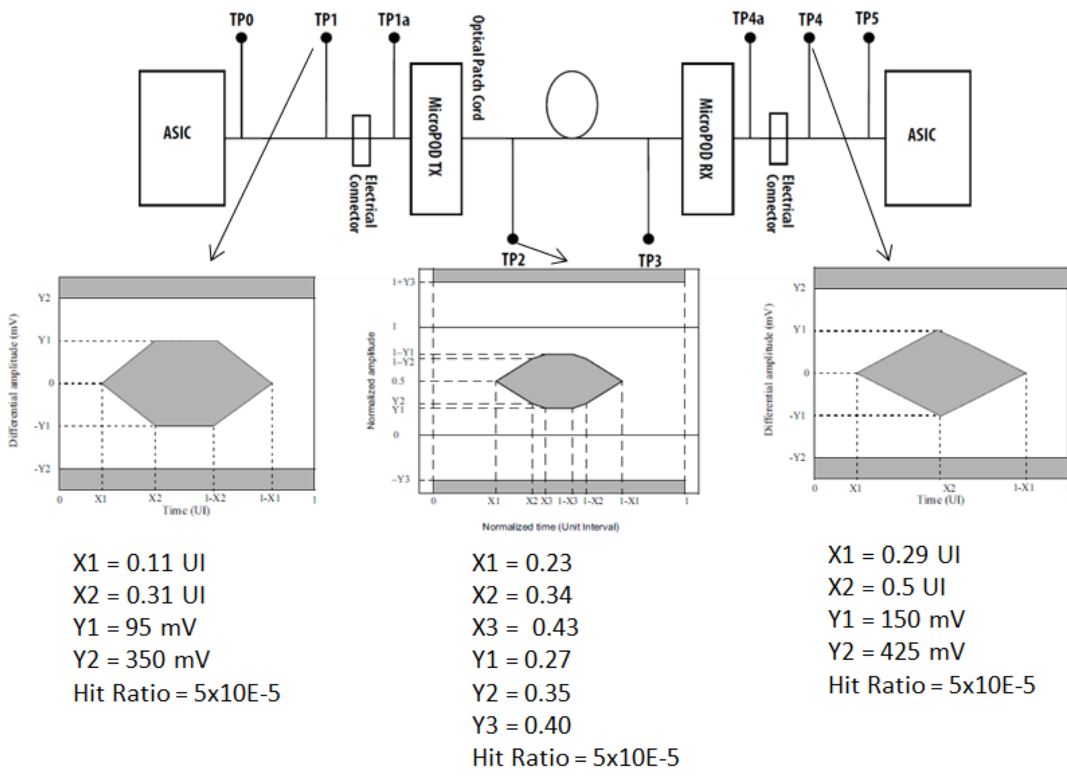
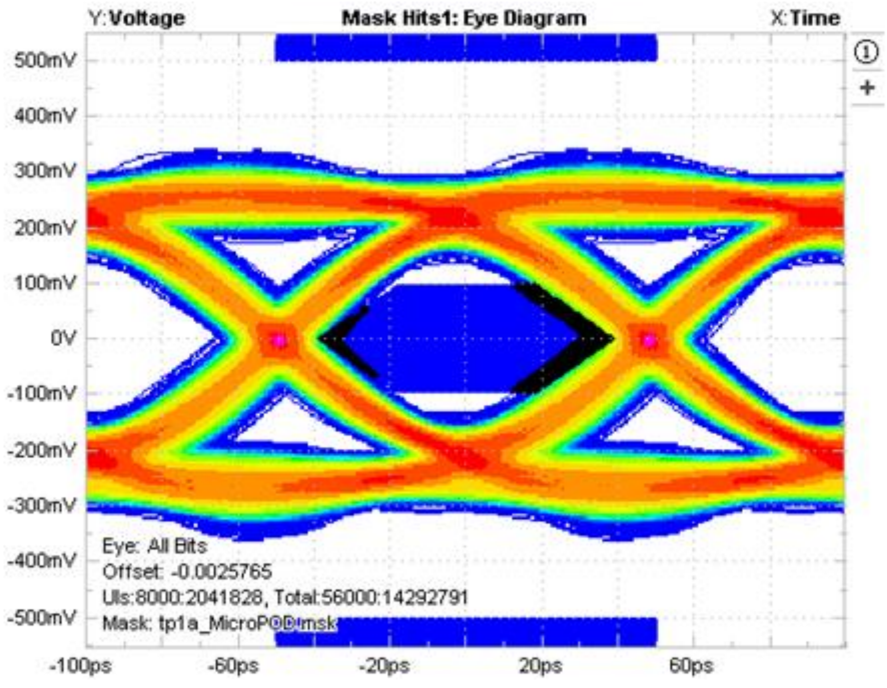


Figure 43. Optical link model for 40 and 100 Gigabit Ethernet

2.11.1 HSD TP1 eye diagram measurement

Figure 44 shows the TP1 eye diagram measurement on HSD Virtex-6 GTH QUAD118_2 running at 10Gb/s. The blue hexagon in the middle of eye opening is the eye mask defined for TP1 as shown in Figure 43. The black areas on the edges of the blue hexagon eye mask show where signals hit the mask. From the measurement data below the eye diagram, the hit ratio for this eye diagram can be calculated as $628 \div (14.293 \times 10^{6}) = 4.4 \times 10^{-5}$, which is less than the eye mask hit ratio limit.



Description	Mean	Std Dev	Max	Min	p-p	Population	Max-cc	Min-cc
Mask Hits1, Math1	628.00		108.00	74.000		14.293M		
Hits In Segment 1	0.0000		0.0000	0.0000		14.293M		
Hits In Segment 2	628.00		108.00	74.000		14.293M		
Hits In Segment 3	0.0000		0.0000	0.0000		14.293M		
TIE1, Math1	-506.31fs	4.5524ps	15.050ps	-18.623ps	33.672ps	7.1450M	21.133ps	-29.758ps
Current Acquisition	-490.09fs	4.5553ps	14.654ps	-18.623ps	33.276ps	1.0196M	20.605ps	-29.176ps
TJ@BER1, Math1	63.166ps	124.29fs	63.312ps	62.993ps	318.66fs	7	0.0000s	0.0000s
Current Acquisition	63.264ps	0.0000s	63.264ps	63.264ps	0.0000s	1	0.0000s	0.0000s
RJ1, Math1	4.5023ps	8.2620fs	4.5112ps	4.4900ps	21.118fs	7	0.0000s	0.0000s
Current Acquisition	4.5075ps	0.0000s	4.5075ps	4.5075ps	0.0000s	1	0.0000s	0.0000s
DJ1, Math1	5.1774ps	129.03fs	5.3298ps	4.9154ps	414.47fs	7	0.0000s	0.0000s
Current Acquisition	5.3298ps	0.0000s	5.3298ps	5.3298ps	0.0000s	1	0.0000s	0.0000s
PJ1, Math1	5.0962ps	126.67fs	5.2482ps	4.8400ps	408.22fs	7	0.0000s	0.0000s
Current Acquisition	5.2482ps	0.0000s	5.2482ps	5.2482ps	0.0000s	1	0.0000s	0.0000s
DDJ1, Math1	0.0000s	0.0000s	0.0000s	0.0000s	0.0000s	7	0.0000s	0.0000s
Current Acquisition	0.0000s	0.0000s	0.0000s	0.0000s	0.0000s	1	0.0000s	0.0000s
DCD1, Math1	81.169fs	3.0793fs	84.173fs	75.388fs	8.7849fs	7	0.0000s	0.0000s
Current Acquisition	81.642fs	0.0000s	81.642fs	81.642fs	0.0000s	1	0.0000s	0.0000s

Figure 44. HSD TP1 eye diagram measurement

2.11.2 HSD TP2 eye diagram measurement

Figure 45 shows the TP2 eye diagram measurement on HSD PPOD Tx channel 12. This is an optical eye diagram measured with optical module on Agilent sampling scope. The eye mask definition, shown in grey, for TP2 is normalised to the measured optical eye diagram. As can be seen, there is no signal sample hitting the eye mask and there is still decent margin between optical eye diagram and eye mask.

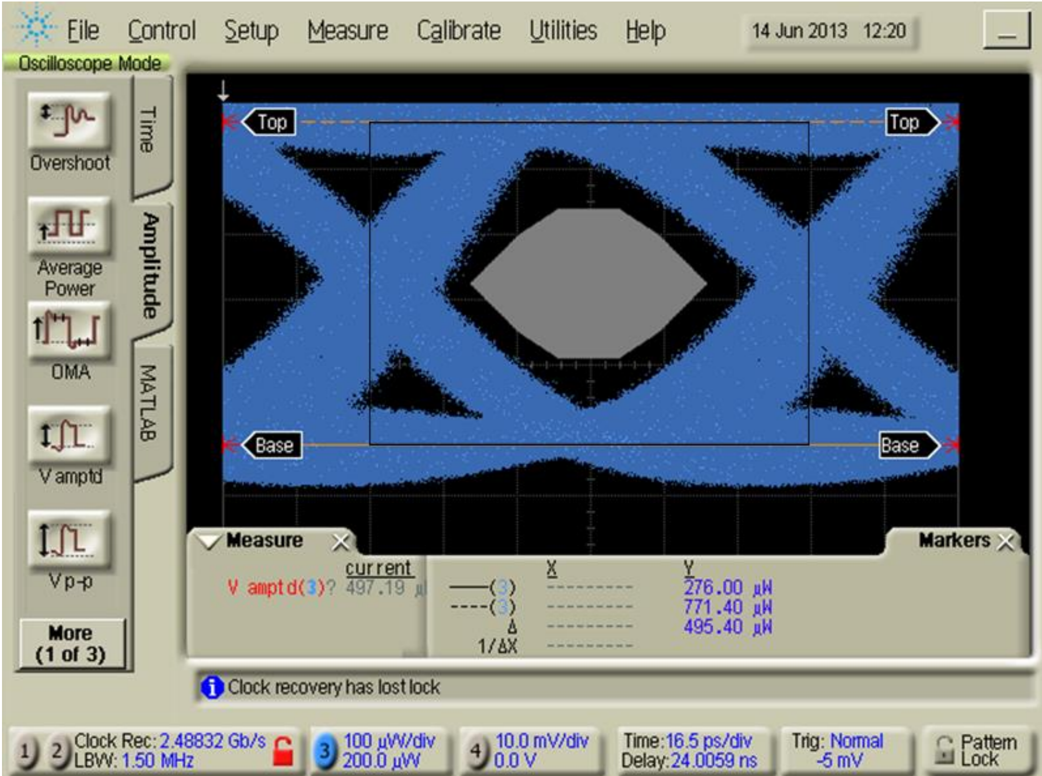
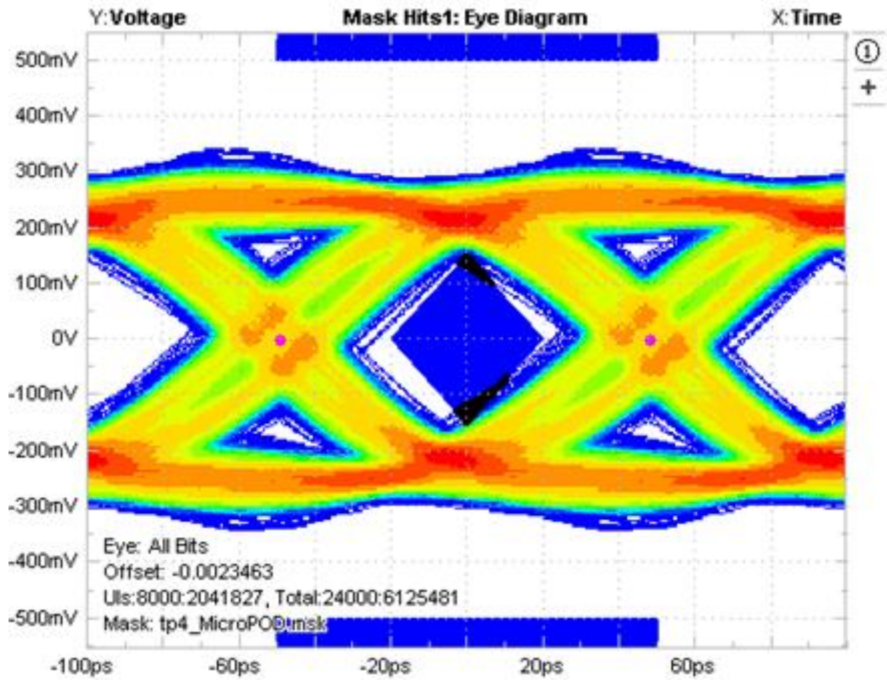


Figure 45. HSD TP2 eye diagram measurement

2.11.3 HSD TP4 eye diagram measurement

Figure 46 shows the TP4 eye diagram measurement on HSD PPOD Rx channel 5 running at 10Gb/s. The PPOD Rx electrical output differential amplitude was set to maximum. The blue hexagon in the middle of eye opening is the eye mask defined for TP4 as shown in Figure 43. The black areas on the edges of the blue hexagon eye mask show where signals hit the mask. From the measurement data below the eye diagram, the hit ratio for this eye diagram can be calculated as $30 \div (6.1255 \times 10^{6}) = 4.9 \times 10^{-6}$, which is much less than the eye mask hit ratio limit.



Description	Mean	Std Dev	Max	Min	p-p	Population	Max-cc	Min-cc
Mask Hits1, Math1	30.000		14.000	4.0000		6.1255M		
Hits In Segment 1	0.0000		0.0000	0.0000		6.1255M		
Hits In Segment 2	30.000		14.000	4.0000		6.1255M		
Hits In Segment 3	0.0000		0.0000	0.0000		6.1255M		
TIE1, Math1	-487.45fs	8.5882ps	24.168ps	-26.597ps	50.765ps	3.0630M	36.522ps	-40.351ps
Current Acquisition	-481.05fs	8.5919ps	24.002ps	-26.233ps	50.235ps	1.0215M	33.879ps	-40.351ps
TJ@BER1, Math1	119.72ps	354.49fs	119.97ps	119.22ps	751.97fs	4	0.0000s	0.0000s
Current Acquisition	119.71ps	0.0000s	119.71ps	119.71ps	0.0000s	1	0.0000s	0.0000s
RJ1, Math1	8.5793ps	28.324fs	8.6005ps	8.5407ps	59.830fs	4	0.0000s	0.0000s
Current Acquisition	8.5754ps	0.0000s	8.5754ps	8.5754ps	0.0000s	1	0.0000s	0.0000s
DJ1, Math1	7.1828ps	444.08fs	7.7670ps	6.8372ps	929.79fs	4	0.0000s	0.0000s
Current Acquisition	7.7670ps	0.0000s	7.7670ps	7.7670ps	0.0000s	1	0.0000s	0.0000s
PJ1, Math1	7.1679ps	453.92fs	7.7670ps	6.8157ps	951.31fs	4	0.0000s	0.0000s
Current Acquisition	7.7670ps	0.0000s	7.7670ps	7.7670ps	0.0000s	1	0.0000s	0.0000s
DDJ1, Math1	0.0000s	0.0000s	0.0000s	0.0000s	0.0000s	4	0.0000s	0.0000s
Current Acquisition	0.0000s	0.0000s	0.0000s	0.0000s	0.0000s	1	0.0000s	0.0000s
DCD1, Math1	14.918fs	10.210fs	21.524fs	0.0000s	21.524fs	4	0.0000s	0.0000s
Current Acquisition	0.0000s	0.0000s	0.0000s	0.0000s	0.0000s	1	0.0000s	0.0000s

Figure 46. HSD TP4 eye diagram measurement

2.12 Data sharing

The eFEX will still run sliding-window based algorithms, which need significant data-sharing between adjacent FPGAs. The eFEX subsystem needs input data-sharing at three levels: between crates, between modules within the same crate and between FPGAs within the same module. Data-sharing at multi-Gb/s speed range is very challenging. In addition, there is a very strong constraint on latency for the whole ATLAS Level-1 trigger system and the extra delay introduced by data-sharing must be kept minimum (i.e. no more than 1 LHC clock tick).

On HSD, the following three data-sharing methods have been investigated.

2.12.1 High-speed buffer

A 7GHz 1-to-4 fanout buffer (NB7HQ14M) from ON Semiconductor was put on HSD for test (shown in Figure 47). Figure 48 shows the eye diagram measurement after the buffer on HSD PPOD Rx channel 5 running at 10Gb/s. Compared to Figure 46, the horizontal eye opening is slightly reduced, which means the buffer introduces small extra jitter. However, the vertical eye height is much improved. The overall result is very good with no signal sample hitting the eye mask. The propagation delay of this buffer is 0.225 ns, which is negligible.

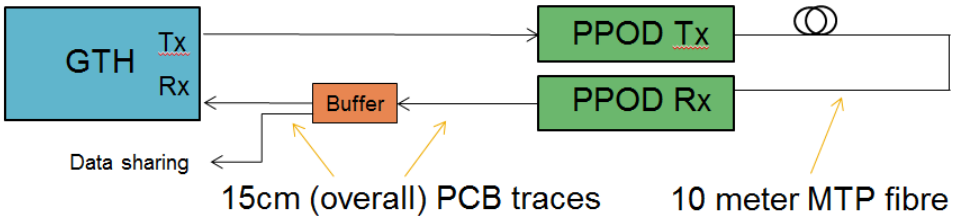
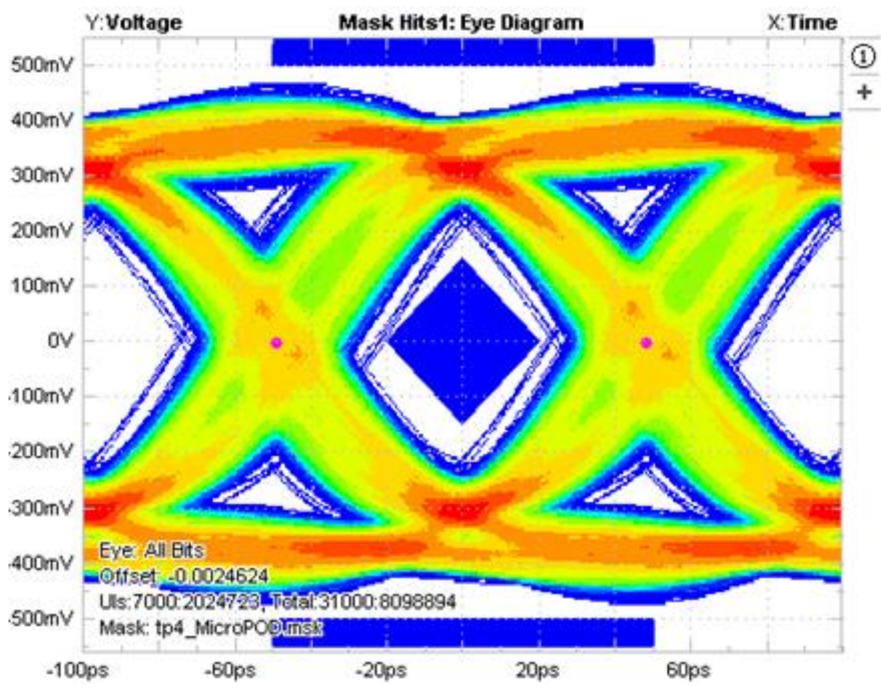


Figure 47. Topology for buffer test on GTH channel

Further IBERT test for above link topology gives more than 30% margin, which is a much improved result compared to Figure 41.



Description	Mean	Std Dev	Max	Min	p-p	Population	Max-cc	Min-cc
Mask Hits1, Math1	0.0000		0.0000	0.0000		8.0989M		
Hits In Segment 1	0.0000		0.0000	0.0000		8.0989M		
Hits In Segment 2	0.0000		0.0000	0.0000		8.0989M		
Hits In Segment 3	0.0000		0.0000	0.0000		8.0989M		
TIE1, Math1	-511.91fs	8.4881ps	27.559ps	-27.478ps	55.037ps	4.0507M	36.313ps	-43.195ps
Current Acquisition	-580.78fs	8.5208ps	25.964ps	-27.478ps	53.443ps	1.0132M	36.313ps	-42.750ps
TJ@BER1, Math1	118.90ps	597.85fs	119.50ps	117.92ps	1.5725ps	5	0.0000s	0.0000s
Current Acquisition	119.50ps	0.0000s	119.50ps	119.50ps	0.0000s	1	0.0000s	0.0000s
RJ1, Math1	8.5262ps	42.094fs	8.5704ps	8.4592ps	111.12fs	5	0.0000s	0.0000s
Current Acquisition	8.5704ps	0.0000s	8.5704ps	8.5704ps	0.0000s	1	0.0000s	0.0000s
DJ1, Math1	6.8299ps	214.98fs	7.0586ps	6.6119ps	446.77fs	5	0.0000s	0.0000s
Current Acquisition	6.6119ps	0.0000s	6.6119ps	6.6119ps	0.0000s	1	0.0000s	0.0000s
PJ1, Math1	6.8299ps	214.98fs	7.0586ps	6.6119ps	446.77fs	5	0.0000s	0.0000s
Current Acquisition	6.6119ps	0.0000s	6.6119ps	6.6119ps	0.0000s	1	0.0000s	0.0000s
DDJ1, Math1	0.0000s	0.0000s	0.0000s	0.0000s	0.0000s	5	0.0000s	0.0000s
Current Acquisition	0.0000s	0.0000s	0.0000s	0.0000s	0.0000s	1	0.0000s	0.0000s
DCD1, Math1	0.0000s	0.0000s	0.0000s	0.0000s	0.0000s	5	0.0000s	0.0000s
Current Acquisition	0.0000s	0.0000s	0.0000s	0.0000s	0.0000s	1	0.0000s	0.0000s

Figure 48 HSD PPOD Rx eye diagram measurement after buffer

2.12.2 Far-end PMA loopback

The Far-end PMA loopback has been tested with both GTX at 5Gb/s and GTH at 10Gb/s on HSD. The test topology is shown in Figure 49.

It works very well with GTX at 5Gb/s with slightly reduced margin at GTX3 (e.g. 37%) compared to GTX2 (e.g. 42%). The penalty of the Far-end PMA loopback is its associated latency of ~1 LHC clock tick.

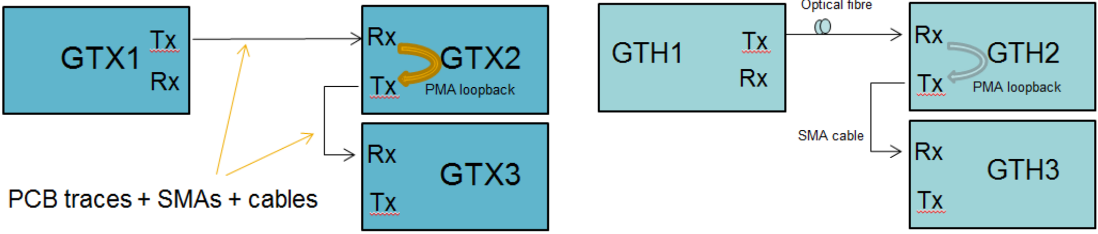


Figure 49. Topologies for Far-end PMA loopback tests on HSD

The Xilinx Virtex-6 Far-end PMA loopback test results on HSD is shown Figure 50. The blue curve is the IBERT scan result at GTH2 with 17% margin, and the red curve is the IBERT scan result at GTH3 with 14% margin. So the Far-end PMA loopback still works with Virtex-6 GTH at 10Gb/s, however, the margin is alarmingly low.

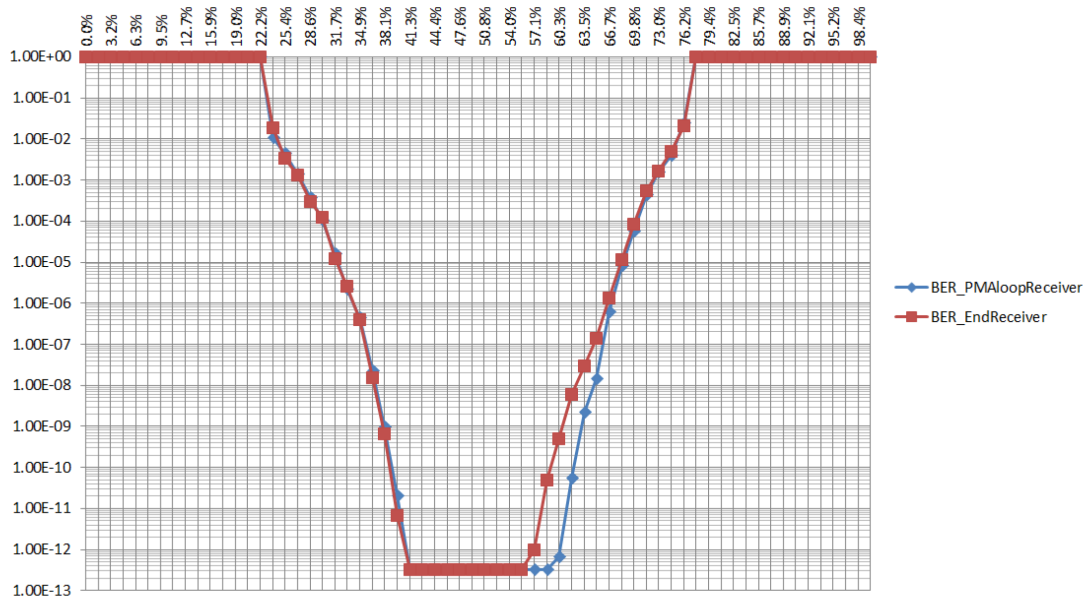


Figure 50. Virtex-6 GTH PMA loopback test

2.12.3 Passive Optical splitter

Avago PPOD Transmitter output optical power is -5.7dBm (minimum), and Avago PPOD Receiver input optical power sensitivity is -13.85dBm. So the overall optical power budget for PPOD optical links is 8.15dB. The optical insertion loss for a good optical 1-to-2 splitter should be less than 4dB. With well-designed optical patch panel with ~5 connections, it is possible to use passive 1-to-2 optical splitter for data sharing between crates and modules.

Figure 51 shows the 10Gb/s optical signal measurement on a passive 1-to-2 optical splitter with Agilent optical module and sampling oscilloscope. The left screen shot shows the optical signal before splitter with optical power 500µW (-3dBm). The right screen shot shows the optical signal after the passive 1-to-2 optical splitter with optical power 252µW (-6dBm). Comparing the two screen shots, the optical splitter is very linear.

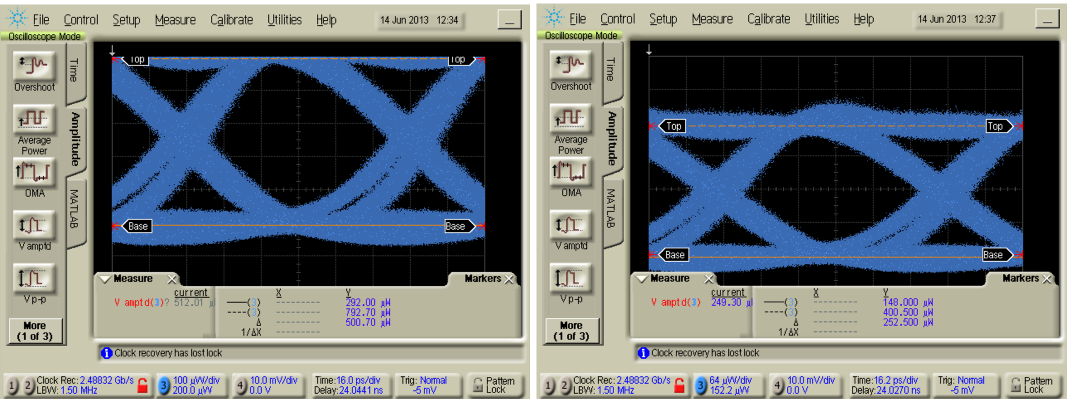


Figure 51. Passive 1-to-2 optical splitter measurement

Further IBERT scan tests show no apparent effect of the passive 1-to-2 optical splitter on the overall link margin.

Handheld optical power meter was also used to measure the PPOD Transmitter output optical power. Some definitions of optical eye are shown in Figure 52. Handheld optical power meter can only measure the average optical power $P_{ave} = (P_1+P_0)/2$. The extinction ration $ER = P_1/P_0$ is ~2.5. So the optical transmitter output Optical Modulation Amplitude (OMA) can be calculated as:

$$OMA = P_1 - P_0 = P_{ave} - 0.67dB$$

Figure 53 gives the average optical power measurement and calculated OMA for two PPOD transmitters used on HSD. These measurements were done at 10Gb/s and only six channels of PPOD can be activated on HSD. The two PPOD transmitters used on HSD have OMA at least 1dB higher than the minimum specification.

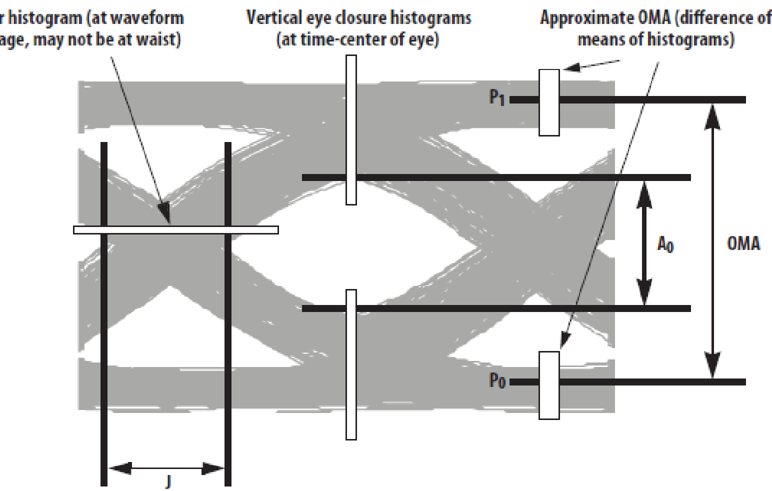


Figure 52 Optical eye definitions

Channel no.	PPOD SerNo AB220142 Pave (dBm)	PPOD SerNo AB220142 OMA (dBm) Calc'ed at ER=2.5	PPOD SerNo AB220138 Pave (dBm)	PPOD SerNo AB220138 OMA (dBm) Calc'ed at ER=2.5
1	-3.68	-4.35	-3.39	-4.06
2	-		-	
3	-		-	
4	-		-	
5	-3.56	-4.23	-3.66	-4.33
6	-4.01	-4.68	-3.13	-3.8
7	-3.89	-4.56	-3.46	-4.13
8	-		-	
9	-3.84	-4.51	-3.34	-4.01
10	-		-	
11	-3.7	-4.37	-3.61	-4.28
12	-		-	

Figure 53. PPOD Transmitter optical power measurement on HSD

3 Joint BNL/RAL 10Gb/s link tests

A joint BNL/RAL test was held in June 2013 at BNL with the focus on 10Gb/s link test based on Xilinx Virtex-7 [9] FPGA and Avago MicroPOD [10] optical transmitter/receiver. The test methods used were the same as those for HSD test in section 2, including IBERT scan, eye diagram, optical power and clock jitter. Several test results on HSD in section 2 were actually collected during the joint test week at BNL. This section records the test results with Xilinx Virtex-7 FPGA and Avago MicroPOD.

3.1 IBERT scan with Virtex-7 + MicroPOD

Figure 54 shows the IBERT scan tests on 10Gb/s links based on Xilinx Virtex-7 evaluation board and Avago MicroPOD. Four links shown all have very large margin (~50%) with small variation between them.

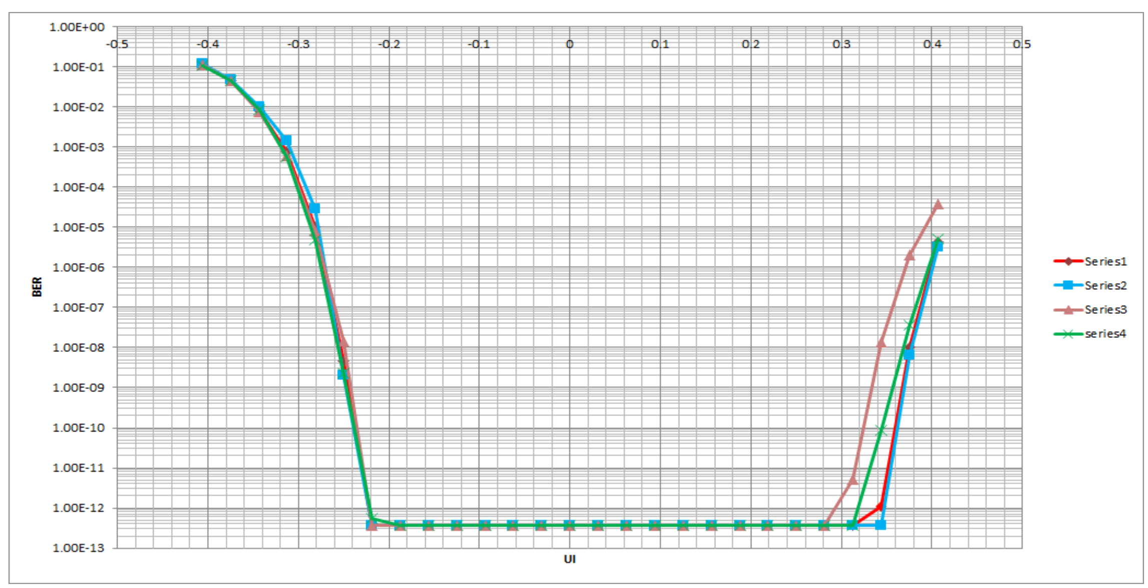


Figure 54. IBERT scan tests with Virtex-7 + MicroPOD

3.2 Optical splitter test with Virtex-7 + MicroPOD

A series of passive optical splitting tests have been done with MicroPOD as shown in Figure 55. Interestingly, the 10Gb/s optical link still works well with 28% margin (shown in right plot) after 3 stages of passive 1-to-2 optical splitters, which indicates that MicroPOD has a much bigger optical power budget.

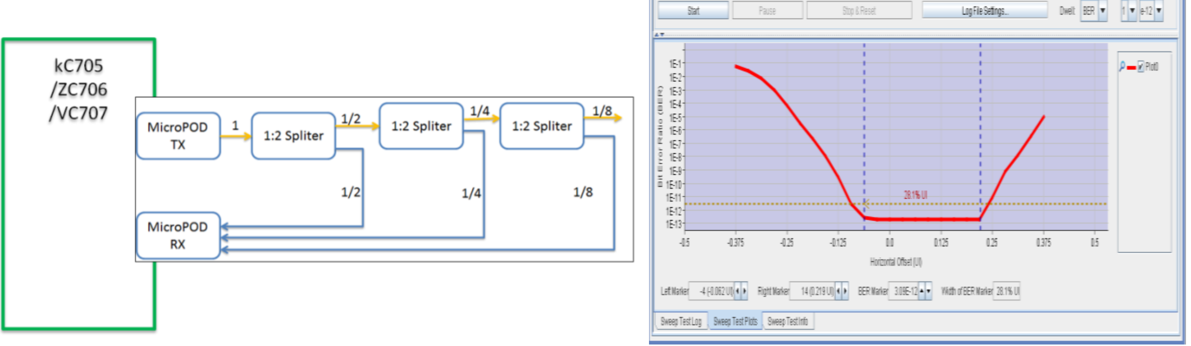


Figure 55. Passive optical splitter test with MicroPOD

3.3 Optical power measurement of MicroPOD

The output optical power was measured for two MicroPOD transmitters at BNL with handheld optical power meter. The result is shown in Figure 56. The MicroPOD datasheet specifies the Tx OMA minimum at -5.6dBm. The real measurement here is at least 4dB higher than the specification, which partly explains the exceptional results in section 3.2.

Channel no.	MicroPOD1 Pave (dBm)	MicroPOD1 OMA (dBm) Calc'ed at ER=2.5	MicroPOD2 Pave (dBm)	MicroPOD2 OMA (dBm) Calc'ed at ER=2.5
1	-0.35	-1.02	0.01	-0.66
2	-0.17	-0.84	-0.3	-0.97
3	-0.52	-1.19	-0.69	-1.36
4	-0.6	-1.27	0.43	-0.24
5	-0.45	-1.12	0.6	-0.07
6	-0.43	-1.1	0.5	-0.17
7	-0.77	-1.44	0.16	-0.51
8	-0.85	-1.52	-0.19	-0.86
9	-0.3	-0.97	-0.5	-1.17
10	-0.76	-1.43	-0.15	-0.82
11	-0.55	-1.22	-0.08	-0.75
12	-0.68	-1.35	-0.01	-0.68

Figure 56. Output optical power of MicroPOD transmitter

3.4 Far-end PMA loopback test with Virtex-7 + MicroPOD

Far-end PMA loopback test was also performed with Virtex-7 and MicroPOD using the same GTH topology as shown in Figure 49. Topologies for Far-end PMA loopback tests on HSDThe IBERT scan at GTH3 is shown in Figure 57 with a margin ~30%, which is a good result.

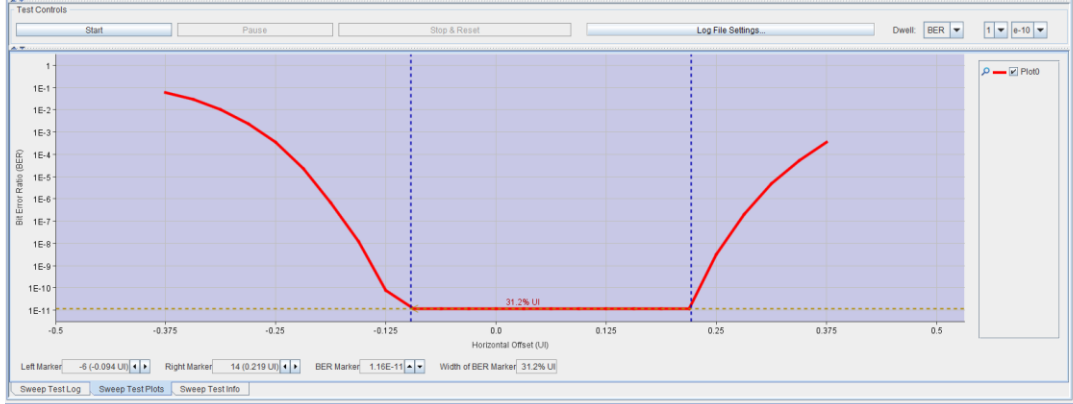


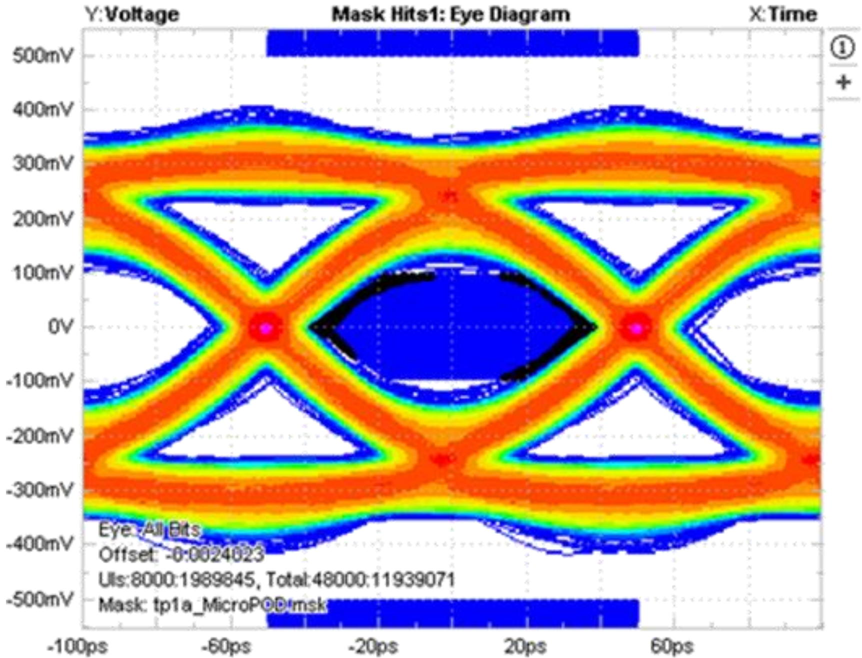
Figure 57. Far-end PMA loopback with Virtex-7 and MicroPOD

3.5 Eye diagram measurement with Virtex-7 + MicroPOD

Eye diagram compliance tests were performed at various test points with several link topologies.

3.5.1 Virtex-7 (TP1)

Figure 58 shows the eye diagram measurement at Virtex-7 evaluation board VC707 FMC1 Tx channel 1, which is TP1 according to link model in Figure 43. The PCB trance length between the Virtex-7 GTH and SMA connectors at TP1 is 5.15 inches. The calculated eye mask hit ratio is 7.7×10^{-6}, which is lower than the limit.

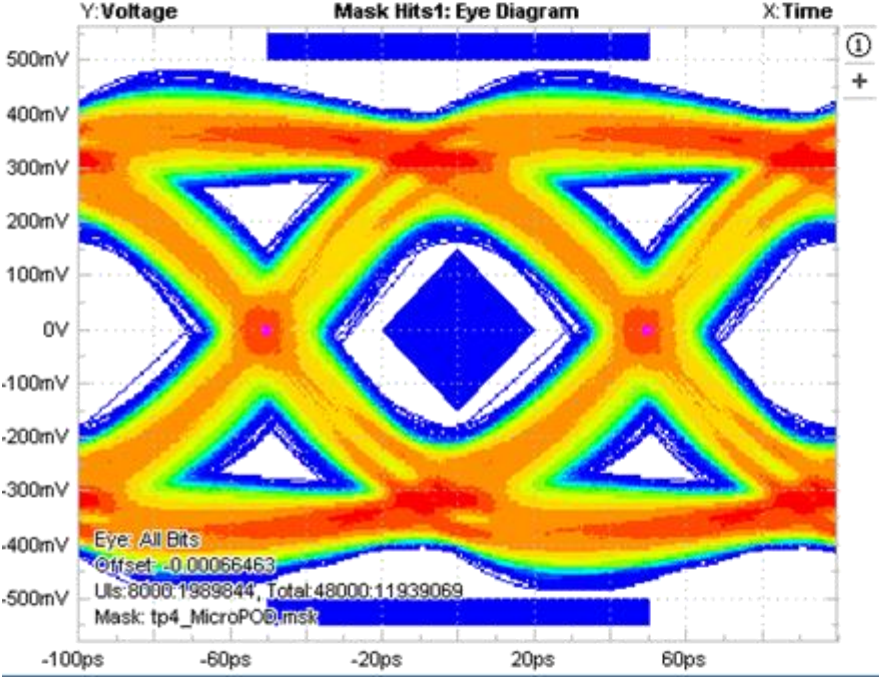


Description	Mean	Std Dev	Max	Min	p-p	Population
Mask Hits1, Math1	92.000		23.000	10.000		11.939M
Hits In Segment 1	0.0000		0.0000	0.0000		11.939M
Hits In Segment 2	92.000		23.000	10.000		11.939M
Hits In Segment 3	0.0000		0.0000	0.0000		11.939M
TIE1, Math1	-353.29fs	4.5335ps	16.454ps	-16.814ps	33.268ps	5.9724M
Current Acquisition	-353.24fs	4.5352ps	16.122ps	-16.814ps	32.936ps	994993
TJ@BER1, Math1	62.610ps	62.361fs	62.706ps	62.541ps	164.39fs	6
Current Acquisition	62.661ps	0.0000s	62.661ps	62.661ps	0.0000s	1
RJ1, Math1	4.4851ps	5.4274fs	4.4916ps	4.4769ps	14.683fs	6
Current Acquisition	4.4905ps	0.0000s	4.4905ps	4.4905ps	0.0000s	1
DJ1, Math1	3.7723ps	151.76fs	4.0244ps	3.5829ps	441.52fs	6
Current Acquisition	3.6703ps	0.0000s	3.6703ps	3.6703ps	0.0000s	1
PJ1, Math1	3.4299ps	156.80fs	3.6926ps	3.2237ps	468.95fs	6
Current Acquisition	3.3437ps	0.0000s	3.3437ps	3.3437ps	0.0000s	1
DDJ1, Math1	0.0000s	0.0000s	0.0000s	0.0000s	0.0000s	6
Current Acquisition	0.0000s	0.0000s	0.0000s	0.0000s	0.0000s	1
DCD1, Math1	342.36fs	12.276fs	359.20fs	326.61fs	32.593fs	6
Current Acquisition	326.61fs	0.0000s	326.61fs	326.61fs	0.0000s	1

Figure 58. TP1 eye diagram measurement at Virtex-7

3.5.2 MicroPOD Rx (TP4)

Figure 59 shows the eye diagram measurement at MicroPOD Rx channel 4, which is TP4 according to link model in Figure 43. The PCB trace length between MicroPOD Rx and SMA connectors is 1.4 inches. MicroPOD Rx electrical differential output amplitude was set to the maximum of 800mV. This a very good eye diagram with 0 mask hit ratio.

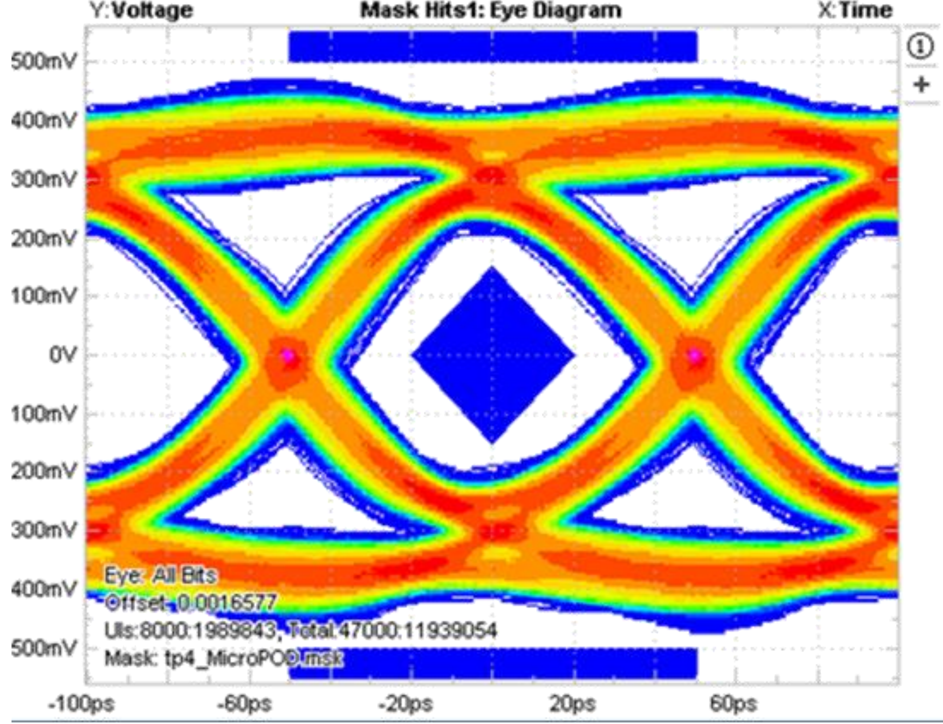


Description	Mean	Std Dev	Max	Min	p-p	Population
Mask Hits1, Math1	0.0000		0.0000	0.0000		11.939M
Hits In Segment 1	0.0000		0.0000	0.0000		11.939M
Hits In Segment 2	0.0000		0.0000	0.0000		11.939M
Hits In Segment 3	0.0000		0.0000	0.0000		11.939M
TIE1, Math1	-718.61fs	5.9572ps	22.339ps	-21.755ps	44.094ps	5.9703M
Current Acquisition	-573.51fs	5.9736ps	21.246ps	-21.755ps	43.001ps	995441
TJ@BER1, Math1	85.699ps	538.75fs	86.320ps	85.128ps	1.1921ps	7
Current Acquisition	86.222ps	0.0000s	86.222ps	86.222ps	0.0000s	1
RJ1, Math1	6.0769ps	33.109fs	6.1186ps	6.0445ps	74.053fs	7
Current Acquisition	6.1006ps	0.0000s	6.1006ps	6.1006ps	0.0000s	1
DJ1, Math1	7.1375ps	481.34fs	7.8949ps	6.7392ps	1.1557ps	7
Current Acquisition	7.3968ps	0.0000s	7.3968ps	7.3968ps	0.0000s	1
PJ1, Math1	7.1090ps	482.90fs	7.8751ps	6.7219ps	1.1532ps	7
Current Acquisition	7.3474ps	0.0000s	7.3474ps	7.3474ps	0.0000s	1
DDJ1, Math1	0.0000s	0.0000s	0.0000s	0.0000s	0.0000s	7
Current Acquisition	0.0000s	0.0000s	0.0000s	0.0000s	0.0000s	1
DCD1, Math1	28.468fs	14.487fs	49.399fs	13.729fs	35.670fs	7
Current Acquisition	49.399fs	0.0000s	49.399fs	49.399fs	0.0000s	1

Figure 59. TP4 eye diagram measurement at MicroPOD Rx

3.5.3 MicroPOD Rx + high-speed electrical buffer (TP4)

Figure 60 shows the eye diagram measurement at the output of a high-speed electrical buffer (NB7HQ14M) immediately after MicroPOD Rx channel 4, which is equivalent to TP4 according to link model in Figure 43. This is an excellent eye diagram with big margin.

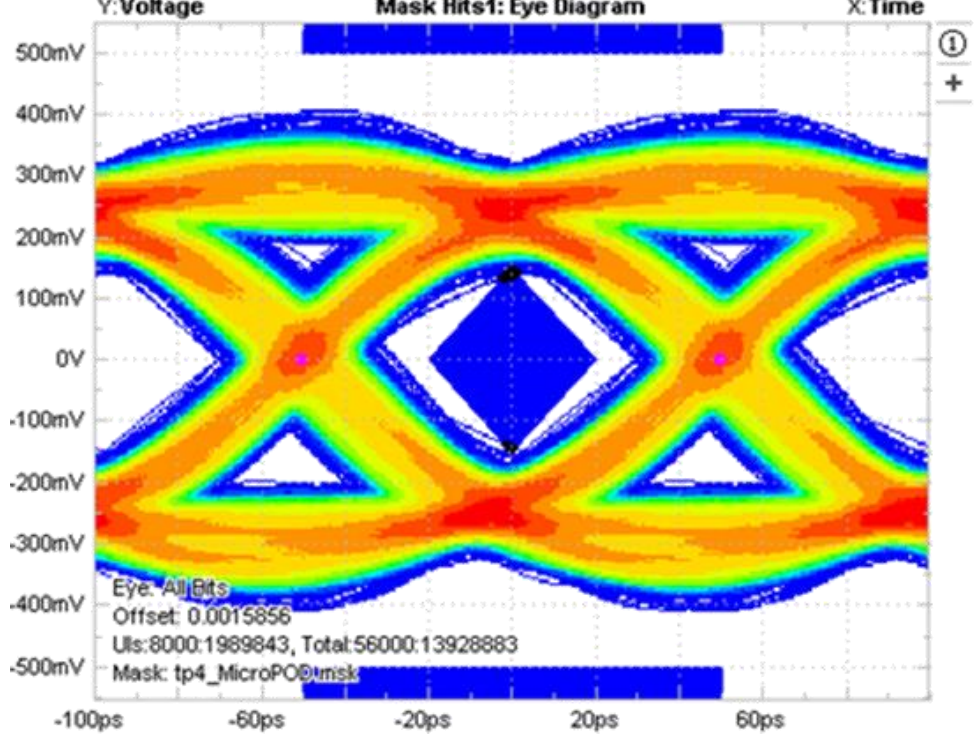


Description	Mean	Std Dev	Max	Min	p-p	Population
Mask Hits1, Math1	0.0000		0.0000	0.0000		11.939M
Hits In Segment 1	0.0000		0.0000	0.0000		11.939M
Hits In Segment 2	0.0000		0.0000	0.0000		11.939M
Hits In Segment 3	0.0000		0.0000	0.0000		11.939M
TIE1, Math1	-589.49fs	4.6383ps	17.593ps	-15.992ps	33.585ps	5.9686M
Current Acquisition	-599.14fs	4.6866ps	16.232ps	-15.858ps	32.090ps	994442
TJ@BER1, Math1	64.003ps	427.19fs	64.848ps	63.627ps	1.2206ps	7
Current Acquisition	64.282ps	0.0000s	64.282ps	64.282ps	0.0000s	1
RJ1, Math1	4.5642ps	30.892fs	4.6263ps	4.5388ps	87.567fs	7
Current Acquisition	4.5820ps	0.0000s	4.5820ps	4.5820ps	0.0000s	1
DJ1, Math1	4.7141ps	212.01fs	5.0766ps	4.4543ps	622.30fs	7
Current Acquisition	5.0766ps	0.0000s	5.0766ps	5.0766ps	0.0000s	1
PJ1, Math1	4.5844ps	206.68fs	4.9354ps	4.3266ps	608.82fs	7
Current Acquisition	4.9354ps	0.0000s	4.9354ps	4.9354ps	0.0000s	1
DDJ1, Math1	0.0000s	0.0000s	0.0000s	0.0000s	0.0000s	7
Current Acquisition	0.0000s	0.0000s	0.0000s	0.0000s	0.0000s	1
DCD1, Math1	129.74fs	6.5522fs	141.17fs	120.96fs	20.211fs	7
Current Acquisition	141.17fs	0.0000s	141.17fs	141.17fs	0.0000s	1

Figure 60. TP4 eye diagram after buffer

3.5.4 Far-end PMA loopback (TP4)

Figure 61 shows the eye diagram measurement at GTH2 Tx in far-end PMA loopback topology as shown in Figure 49. This test point is equivalent to TP4 according to link model in Figure 43. This is a good eye diagram with a mask hit ratio of 5.7×10^{-7}. There is big horizontal margin in the eye diagram. The GTH equalization settings should be able to improve the vertical eye opening further.



Description	Mean	Std Dev	Max	Min	p-p	Population
Mask Hits1, Math1	8.0000		2.0000	1.0000		13.929M
Hits In Segment 1	0.0000		0.0000	0.0000		13.929M
Hits In Segment 2	8.0000		2.0000	1.0000		13.929M
Hits In Segment 3	0.0000		0.0000	0.0000		13.929M
TIE1, Math1	-446.57fs	6.2044ps	22.596ps	-20.600ps	43.196ps	6.9664M
Current Acquisition	-555.67fs	6.2090ps	21.575ps	-19.481ps	41.056ps	995430
TJ@BER1, Math1	83.477ps	128.75fs	83.662ps	83.362ps	299.55fs	7
Current Acquisition	83.452ps	0.0000s	83.452ps	83.452ps	0.0000s	1
RJ1, Math1	5.7814ps	10.625fs	5.7968ps	5.7715ps	25.309fs	7
Current Acquisition	5.7750ps	0.0000s	5.7750ps	5.7750ps	0.0000s	1
DJ1, Math1	9.9898ps	382.48fs	10.768ps	9.7393ps	1.0290ps	7
Current Acquisition	10.768ps	0.0000s	10.768ps	10.768ps	0.0000s	1
PJ1, Math1	9.9537ps	374.57fs	10.709ps	9.6921ps	1.0167ps	7
Current Acquisition	10.709ps	0.0000s	10.709ps	10.709ps	0.0000s	1
DDJ1, Math1	0.0000s	0.0000s	0.0000s	0.0000s	0.0000s	7
Current Acquisition	0.0000s	0.0000s	0.0000s	0.0000s	0.0000s	1
DCD1, Math1	36.069fs	13.525fs	59.493fs	21.428fs	38.065fs	7
Current Acquisition	59.493fs	0.0000s	59.493fs	59.493fs	0.0000s	1

Figure 61. TP4 eye diagram after Far-end PMA loopback

4 Conclusions

All the challenging areas of signal integrity in multi-Gb/s high-speed design needed for the eFEX system have been explored systematically with HSD and very good results have been achieved.

Very good solutions have been found for clock jitter reduction, differential skew control, low noise power supply and high-speed data-sharing scheme.

High-speed PCB simulation has been successfully integrated into the RAL PCB design flow and played a critical role in HSD PCB design. Very good correlation has been achieved between the PCB simulation and real measurement on HSD.

Several PCB production issues, which led to out-of-spec impedance on certain layers on HSD, have been identified. Corrective actions have been agreed for future high-speed module design/production.

HSD high-speed link tests have achieved compliance to industry standard IEEE 802.3ba (40 and 100 Gigabit Ethernet Architecture). It has been agreed to use the eye masks from IEEE 802.3ba for the high-speed link interface definition between future DPS and eFEX.

The BNL/RAL joint 10Gb/s tests on Xilinx Virtex-7 together with Avago MicroPOD have shown much better performance than Xilinx Virtex-6 together with Avago PPOD. It is recommended to target the future DPS and eFEX engineering prototype at 10Gb/s using Xilinx Virtex-7 and Avago MicroPOD/MiniPOD.

5 Acknowledgement

I would like to thank my colleagues at STFC for their contributions to the HSD project over the last two years. My completion of this project could not have been accomplished with the strong support of Ian Brawn, Dan Beckett and Saeed Taghavi.

I would like to thank Hucheng Chen, Kai Chen, Joe Mead and Hao Xu at Brookhaven National Laboratory, who kindly provided the opportunity of the joint BNL/RAL 10 Gb/s link tests, which was extremely constructive and fruitful.

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