LAPP IPMC Test Board manual

Manual for LAPP Intelligent Platform Management Controller Mezzanine Test

Version V1.2

For IPMC test board V1.1

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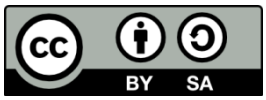


I. Overview

This document describes the LAPP_IPMC Test Board and how to use it. The LAPP IPMC Test Board has been developed to test and debug the LAPP IPMC Mezzanine. This board has also functionalities to help debugging of AMC cards.

LAPP IPMC Mezzanine

The LAPP IPMC Mezzanine has been developed at LAPP laboratory in order to provide the IPMC function for ATCA board as described in the ATCA specification. For more information, see the IPMC Mezzanine documentation.

The mezzanine has the following features:

- Redundant IPMB-0 interface with buffer for hot-swap capabilities
- Hot Swap management with ATCA blue led and front panel switch
- FRU LED management
- Payload power management (enable and monitoring through I2C bus)
- Hardware address detection
- ATCA board sensor management (through I2C bus)
- Management for up to 8 AMCs plus one Intelligent RTM through an IPMB-L bus
- FRU Information and Sensor Data Record access through I2C bus
- On board Event Log
- Compliant with PICMG 3.0 R3.0 for the AdvancedTCA base specification and IPMI v1.5 and the relevant subset of IPMI v2.0
- Configurable signals for custom payload interface. (E-Keying…)

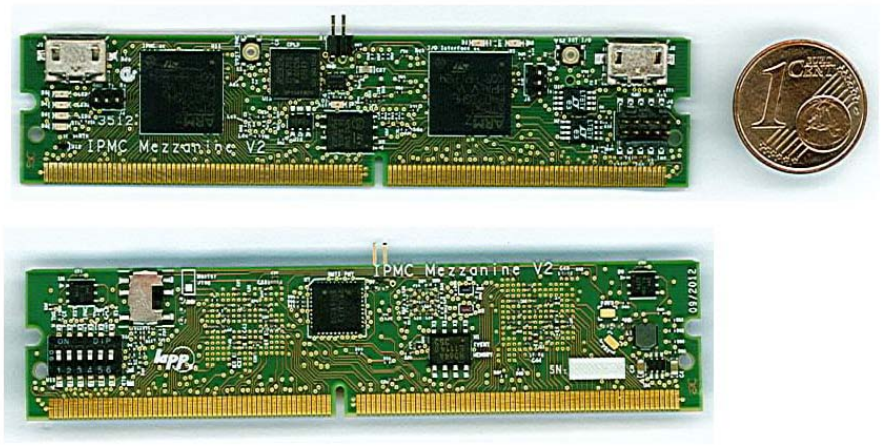


Figure 1: LAPP IPMC Mezzanine

The LAPP IPMC Test board provides a tool for debugging this mezzanine.

IPMC Test Board: General Description

The LAPP IPMC Test Board is an ATCA board and follows requirements to be inserted in an ATCA shelf. It has an IPMC slot in order to comply with the ATCA hardware platform management and IPMI specifications.

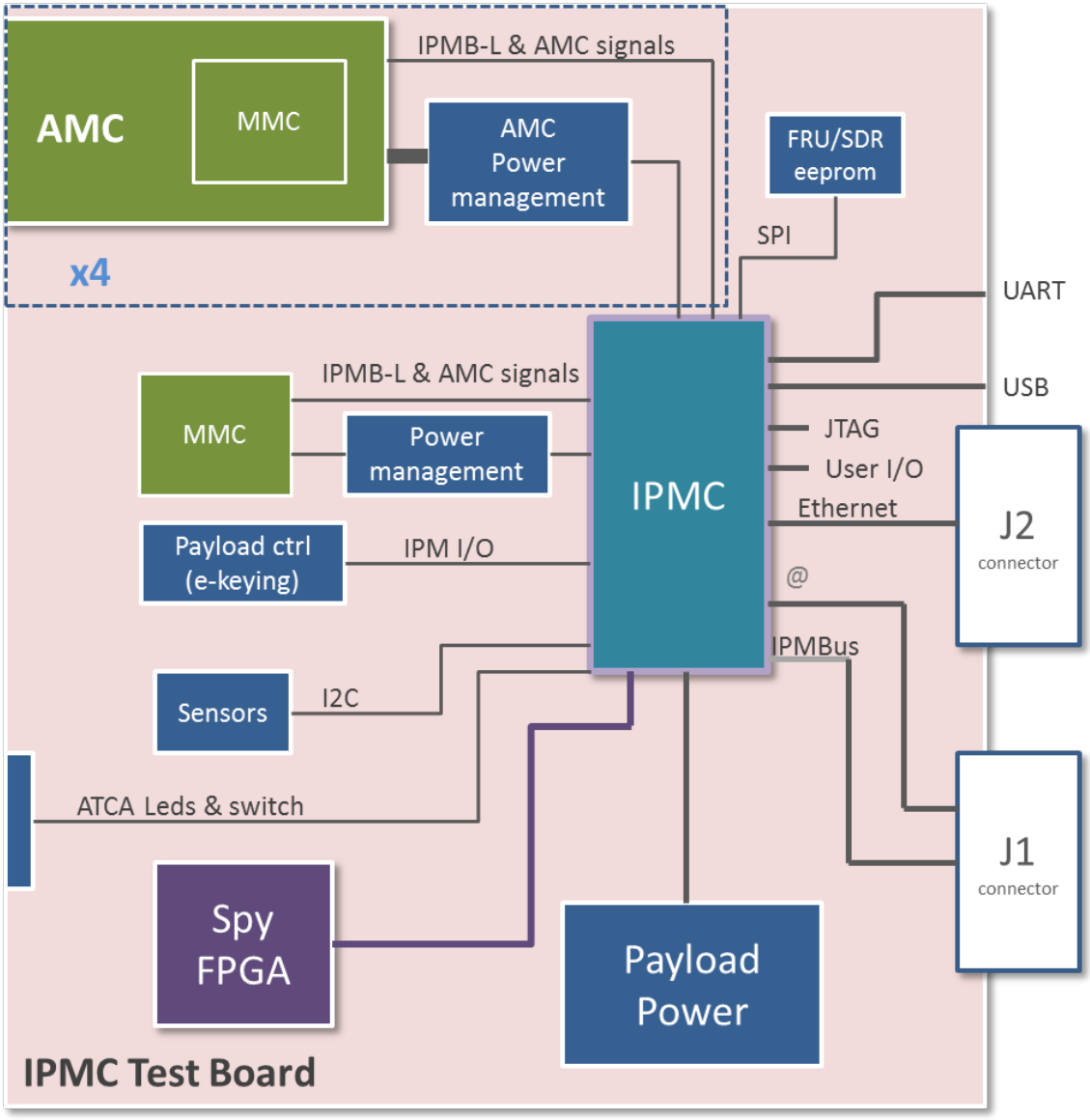


Figure 2: IPMC Test Board architecture

The board has the following features:

- One LAPP IPMC Mezzanine V2
- 4 AMC slots with AMC power supply management
- 1 MMC slot with power supply management
- An EEPROM for FRU & SDR information
- Voltage, current, temperature sensors
- An FPGA to spy IPMC signals or to implement other users functionalities
- Connectivity: Ethernet connection with IPMC Mezzanine through RTM or backplane, UART, USB, I2C
- High speed connections between two AMCs with e-keying
- High speed connection between one AMC and ATCA backplane e-keying
- ADCs to spy I2C busses
- JTAG connectivity

II. Board component description

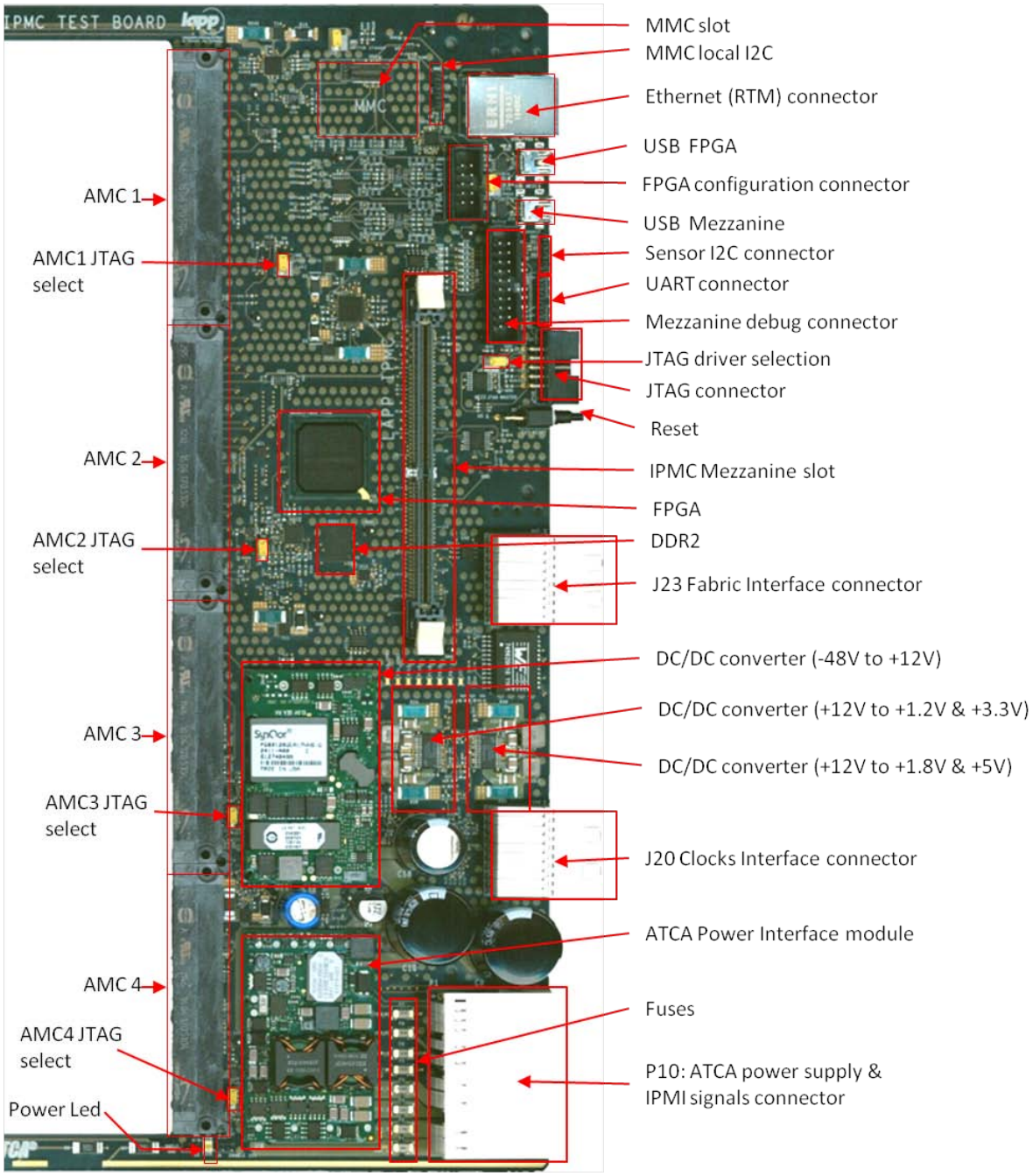


Figure 3: Overview of the LAPP IPMC Test Board

Power supplies

The following bloc diagram explains the board power supplies distribution:

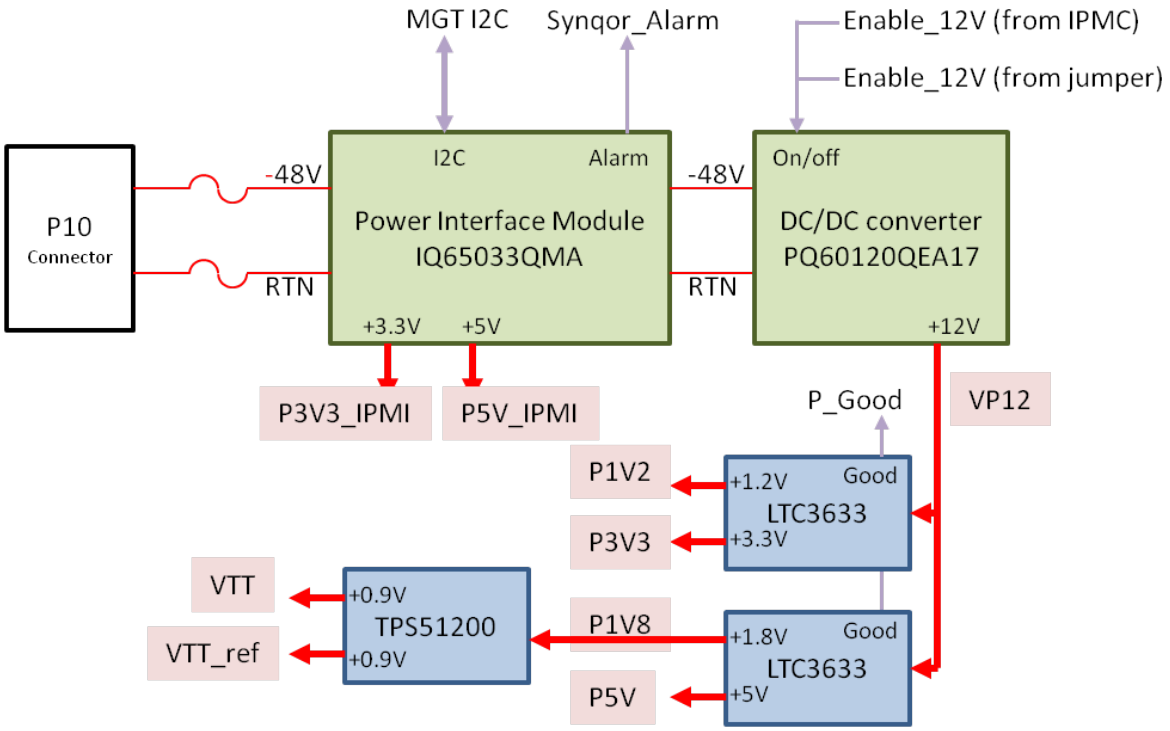


Figure 4: Architecture of the board power supplies distribution

The board power is coming from ATCA connector P10. This connector provides two -48V supplies rails (-48V_A and -48V_B) for redundancy, Enables signals and Early supplies (see ATCA specification). Only one supply rail is represented on the diagram. All these supplies are fused.

The Power Interface Module *IQ65033QMA* from *SynQor* integrates all features required by the ATCA specification:

- Management power over-voltage protection
- Management power over-current protection
- Main output over-current protection
- Thermal shutdown protects the unit from abnormal environmental conditions
- Input fuse/feed loss alarm
- Input ORing for A & B power feeds
- Hot swap control with voltage transient
- Hold-up capacitor with automatic discharge
- Isolated management power of 3.3 V at 3.6 A and 5.0 V at 150 mA

This module has also an I2C bus for monitoring (status, voltage, current, temperature…) and an alarm signal connected to the IPMC Mezzanine. The +3.3V provided by this module is used to supply the IPMC mezzanine and AMCs Management Power.

The -48V supply is converted into +12V supply by an isolated DC/DC converter *PQ60120QEA17* from *SynQor*. This converter has an *Enable* pin driven by the IPMC Mezzanine. This pin can also be driven by a jumper. **BEWARE: DO NOT LEAVE THE JUMPER CLOSED WHEN THE POWER IS SWITCHED ON**. The power must be switched on with the jumper removed, and closed one second or more after the power is applied. If the jumper is closed at power up, the inrush current is

too high and the power interface module switches off its output. The jumper is located on the bottom right part of the board. Near this jumper is located a white Led which is on when the +12V rail is on.

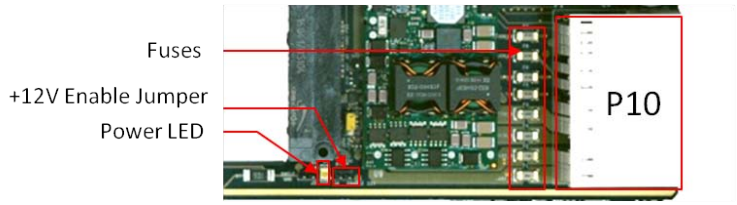


Figure 5: Details of the +12V Enable jumper and power led

Two *LTC3633* DC/DC converters from *Linear Technology* provide +3.3V, +1.2V, +1.8V and +5V from the +12V supply. Each converter has an open collector *PGOOD* pin. These four signals are connected together to the *P_GOOD* signals. *P_GOOD* must rise to +3.3V when all supplies have reached their power rails. P_GOOD can be monitored by the IPMC Mezzanine. These supplies power all the board devices (FPGA etc..)

A *TPS51200* from *Texas Instrument* provides voltage references for the DDR2 memory.

Two devices monitor these supplies:

- A *LTC4151* from *Linear Technology* for +12V current and voltage monitoring.
- A *LTC2499* from *Linear Technology* for +3.3V, +1.2V, +5V, +1.8V current and voltage monitoring.

ATCA Test Board signal	IPMC Mezzanine IO
P_GOOD	IPM_IO_2
SYNCOR_ALARM	ALARM_A

Table 1: Power supplies monitoring signals on IPMC Mezzanine

AMC and MMC supplies

Power controllers

The ATCA test board has four AMC slots. Each slot has a power controller in order to comply with the AMC specification:

- +3.3V MP (Management Power) switch and current limitation
- +12V PWR switch and current limit and fast trip
- Power good and fault indication

The IPMC mezzanine must manage AMCs power. Seven signals per AMC are connected between the Power Controller device and the IPMC:

Signal	Dir.*	Comment
AMC_EN12_n	MtoA	Enable +12V AMC power supply
AMC_EN3_n	MtoA	Enable +3.3V AMC Management Power
AMC_OREN_n	MtoA	Power Oring. Not used except for AMC4 and the LTC4222 (ON signal)
AMC_PG12_n	AtoM	+12V power good
AMC_PG3_n	AtoM	+3.3V power good
AMC_FLT12_n	AtoM	+12V Fault indicator
AMC_FLT3_n	AtoM	+3V Fault indicator

*Table 2: AMC power controller signals. - * MtoA: signal is going from Mezzanine to AMC*

Each AMC and MMC slot has a different power controller. This allows the IPMC Mezzanine to comply with all main power controllers available on the market.

Slot	Power Controller	Comment
AMC1	TPS2358A	This device deals with two slots (AMC1 and AMC2)
AMC2	TPS2358B	
AMC3	TPS2459	I2C interface for control and monitoring. The I2C interface is mandatory to power on the AMC. **BEWARE: control signals have inverted polarity.**
AMC4	LTC4222	I2C interface for control and monitoring (I2C interface not mandatory)
MMC	TPS2458	Same as TPS2358 but for one AMC.

Table 3: AMC power controller devices

LEDs

There are two leds per AMC/MMC slot to indicate the presence of AMC/MMC supplies:

- A amber led for AMC/MMC +3.3V Management Power
- A green led for AMC/MMC +12V PWR

I2C busses

Five I2C busses are connected between the IPMC mezzanine and the ATCA Test Board:

- I2C_IPMB_A
- I2C_IPMB_B
- I2C_IPMB_L
- I2C_MGT
- I2C_SENSOR

All needed pull-up resistors are located on the IPMC Mezzanine.

IPMB_A and IPMB_B I2C

These two I2C busses are connected to the ATCA shelf manager through the P10 ATCA connector. These two buses are similar and are used for bus redundancy. The ATCA specification makes it compulsory to use bus buffers to be able to disconnect the bus. These mandatory buffers are located on the IPMC Mezzanine.

IPMB_L

This I2C bus is the “Local” bus used for AMC management. This bus connects each AMC to the IPMC. To comply with the AMC specification, a *LTC4307* device is used as bus buffer for each

mezzanine. An *AMCx_IPMB_L_ENA* signal going from the mezzanine to the buffer allows the IPMC to connect or disconnect the IPMB_L bus to the AMCx. Figure 6 shows the IPMB_L architecture:

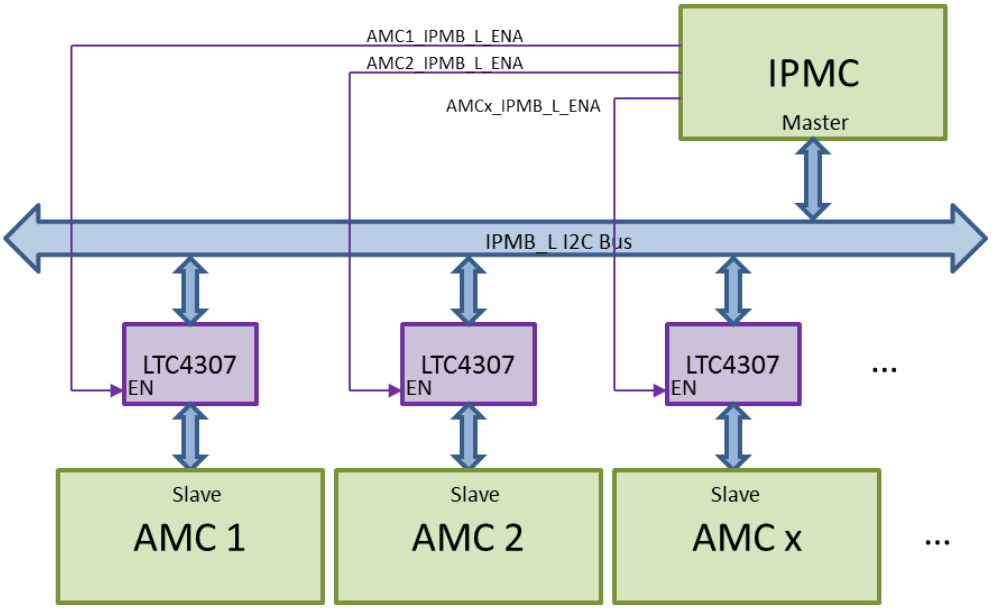


Figure 6: IPMB_L I2C bus architecture

The following table gives the I2C bus address to access AMC/MMC:

	Site number*	**Geographical Address GA[2..0]**	**IPMB_L Address**
AMC 1	GGU	1	0x72
AMC 2	GUG	2	0x74
AMC 2	GUU	3	0x76
AMC 4	UGG	4	0x78
MMC	UGU	5	0x7A

*Table 4: AMC / MMC IPMB_L address - * G=Ground, U=Unconnected*

I2C_Mgt

This bus is the "Management" bus. It is used by the IPMC mezzanine to access the FRU & SDR EEPROM and to control power supplies devices. The following figure shows the bus architecture:

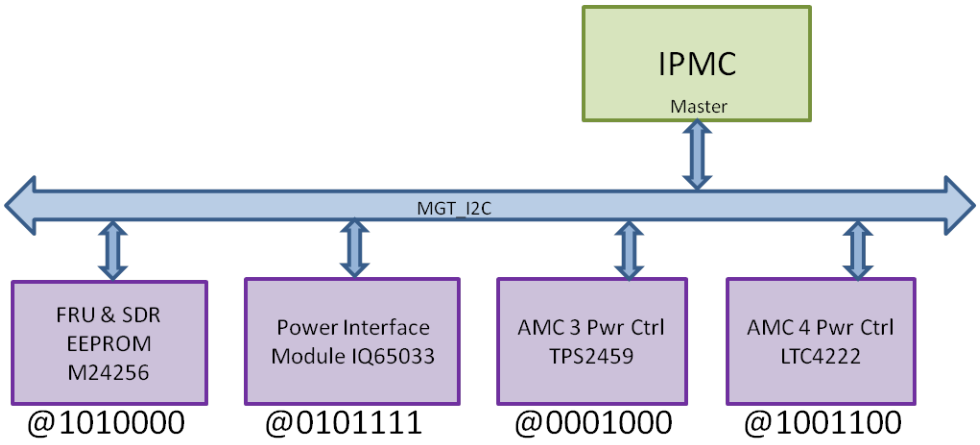


Figure 7: MGT_I2C bus architecture

Table 5 gives the I2C bus address to access I2C_MGT bus devices:

Device	Description	I2C_MGT address
M24256	EEPROM	0x50
IQ65033	Power Interface Module	0x2F
TPS2459	AMC3 Power Controller	0x08
LTC4222	AMC4 Power Controller	0x4C

Table 5: MGT_I2C bus devices

I2C_Sensor

This bus is controlled by the IMPC Mezzanine to read board sensors like temperature (mandatory), current, voltage etc… The following figure shows the bus architecture:

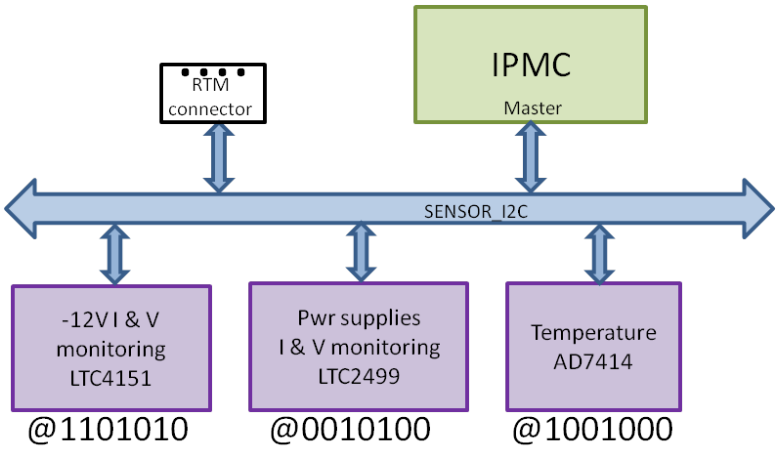


Figure 8: Sensor_I2C bus architecture

Table 6 gives the I2C bus address to access I2C_Sensor bus devices:

Device	Description	I2C_SENSOR address
LTC4151	-12V current and voltage monitoring	0x6A
LTC2499	+3.3V, +1.2V, +1.8V, +5V current and voltage monitoring	0x14
AD7414	Temperature monitoring	0x48

Table 6: Sensor_I2C bus devices

I2C busses monitoring

Four I2C busses can be monitored by sampling their lines (SDA and SCL) with an ADC running at 1MHz max. These busses are:

- IPMB_A
- IPMB_B
- IPMB_L
- I2C_MGT

Figure 9 shows the architecture of one bus line monitoring:

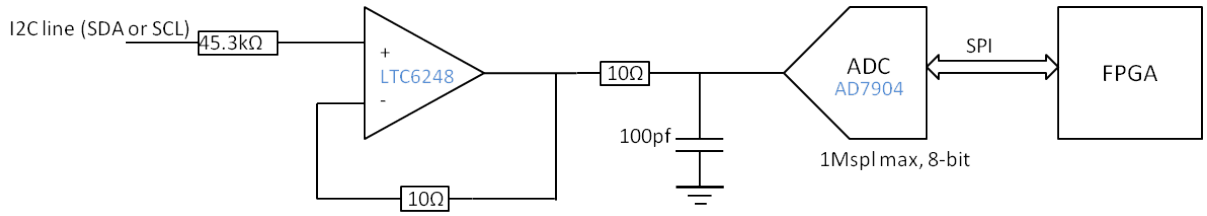


Figure 9: I2C line monitoring architecture

Each I2C line is buffered by an OPA (*LT6248* from *Linear Technology*) and sampled by an 8-bit ADC *AD7904* from *Analog Devices*. This ADC is a four channels ADC. There are two ADC on the IPMC Test Board: one for SCL lines and the other for SDA lines. ADCs are read by the FPGA through SPI busses.

Clocks architecture

The following figure shows the ATCA Test Board clock architecture:

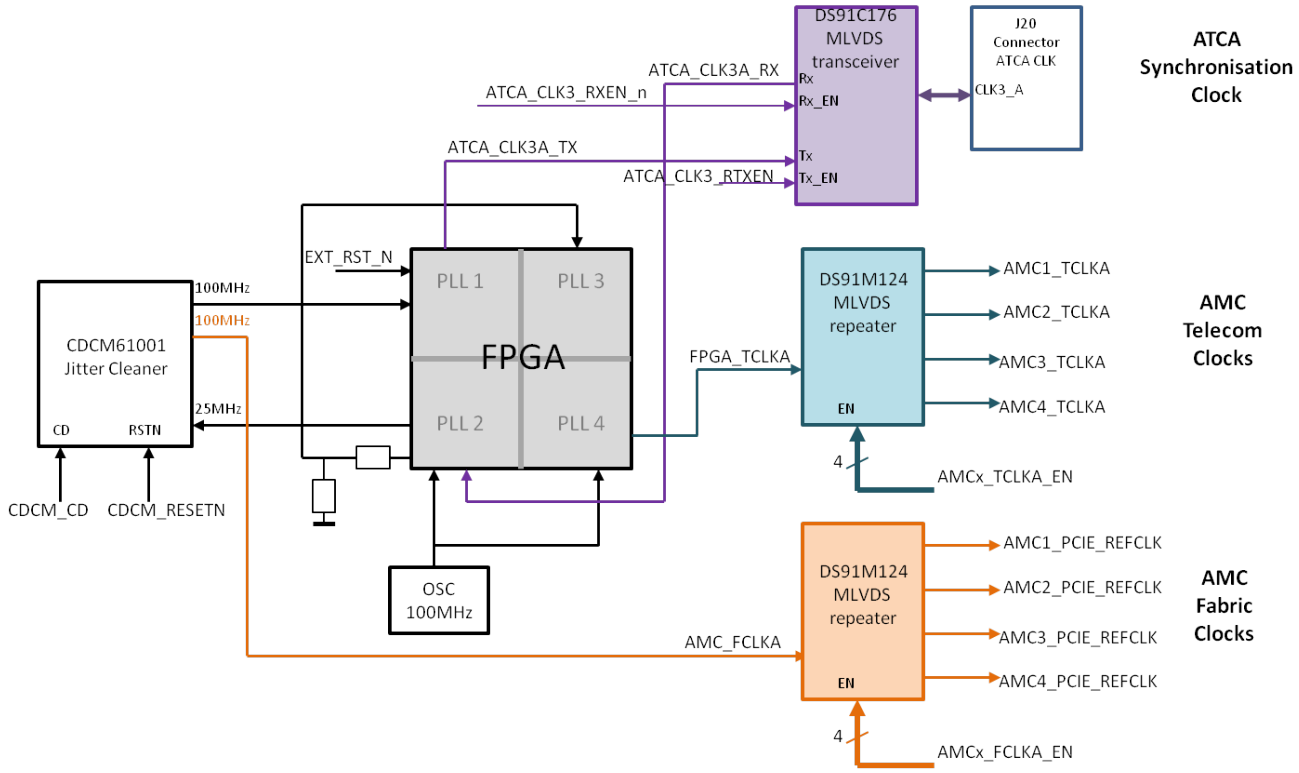


Figure 10: IPMC Test Board clocks architecture

The on-board FPGA has four PLL used to generate several clocks. One of the clock source is the 100MHz oscillator that feeds PLL2 and PLL4. PLL2 feeds a *CDCM61001* from *Texas Instrument* used to generate a “clean” clock for PCI express applications.

PLL2 also provides a clock to PLL1 through a resistor divider because PLL2 output is a +3.3V level and PLL1 input is at +1.8V. Be careful with this clock frequency because this resistor divider acts as a low pass filter with the input pin capacitor.

ATCA Synchronization Clock

ATCA synchronization clocks are used to synchronize ATCA boards inside a shelf. The ATCA Test Board can use the CLK3A clock to distribute or receive a clock from the ATCA backplane. An M-LVDS transceiver *DS91C176* from *Texas Instrument* is used to select the clock side (Rx or Tx) and enable or disable the clock with the ATCA E-keying process. The two control signals are managed by the IPMC Mezzanine on the IPM_IO.

DS91C176 control signal	IPMC Mezzanine IO
ATCA_CLK3_RXEN_N	IPM_IO_11
ATCA_CLK3A_TXEN	IPM_IO_12

Table 7: CLK3A clock control signals on IPMC Mezzanine

AMC Telecom and Fabric clocks

The AMC specification provides two types of clocks, Telecom Clocks and a Fabric Reference Clock. The ATCA Test Board provides one clock to the AMC Telecom Clock A and on clock to the Fabric clock. PLL4 provides the TCLKA to the four AMCs through a fan-out M-LVDS buffer *DS91M124*. Each AMC TCLKA clock can be enabled or disables by the IPMC Mezzanine by *AMCx_TCLKA_EN* signals.

In the same way, the board provides a fabric clock FCLK to each AMC. These clocks are also distributed through a M-LVDS buffer and can also be enabled or disables individually by the IPMC Mezzanine. The activation / deactivation of these clocks should be part of the ATCA E-keying process.

TCLKA DS91M124 control signal	IPMC Mezzanine IO
AMC1_TCLKA_EN	IPM_IO_7
AMC2_TCLKA_EN	IPM_IO_8
AMC3_TCLKA_EN	IPM_IO_9
AMC4_TCLKA_EN	IPM_IO_10

Table 8: TCLKA clock control signals on IPMC Mezzanine

FCLKA DS91M124 control signal	IPMC Mezzanine IO
AMC1_FCLKA_EN	IPM_IO_13
AMC2_FCLKA_EN	IPM_IO_14
AMC3_FCLKA_EN	IPM_IO_15
AMC4_FCLKA_EN	IPM_IO_16

Table 9: FCLKA clock control signals on IPMC Mezzanine

Reset

An active low reset coming from the RTM push button is connected to one FPGA dedicated clock input. This reset signal is also connected to the IPMC Mezzanine reset input.

AMC Fabric Interfaces

AMC1 and AMC2

Fabric interfaces of AMC1 and AMC2 are connected together for high-speed transfers between these two mezzanines. The 20 Rx and 20 Tx high speed links of these mezzanines are fully connected. **BEWARE: THESE LINKS HAVE NOT BEEN TESTED YET.**

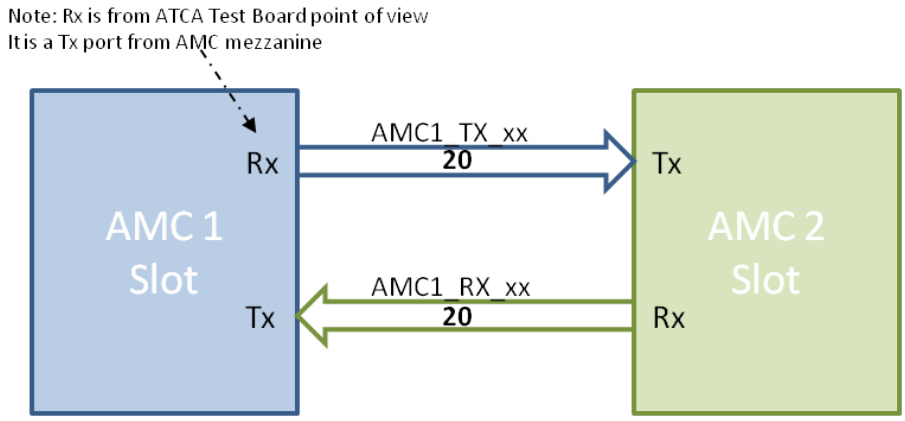


Figure 11: AMC1 and AMC2 inter-connections

AMC3

AMC3 slot Fabric interface is partially connected to the ATCA Fabric interface through J23 connector. Figure 12 shows AMC ports connected to the ATCA connector. *DS25BR440* LVDS buffers from *Texas Instrument* are used to connect or disconnect these high speed signals from or to the ATCA backplane through the ATCA E-keying process. The IPMC Mezzanine deals with this process by turning on or off these buffers. Table 10 shows signals used for this mechanism. Buffers also provide LOS indication that can be read by the IPMC Mezzanine. **BEWARE: THESE LINKS HAVE NOT BEEN TESTED YET.**

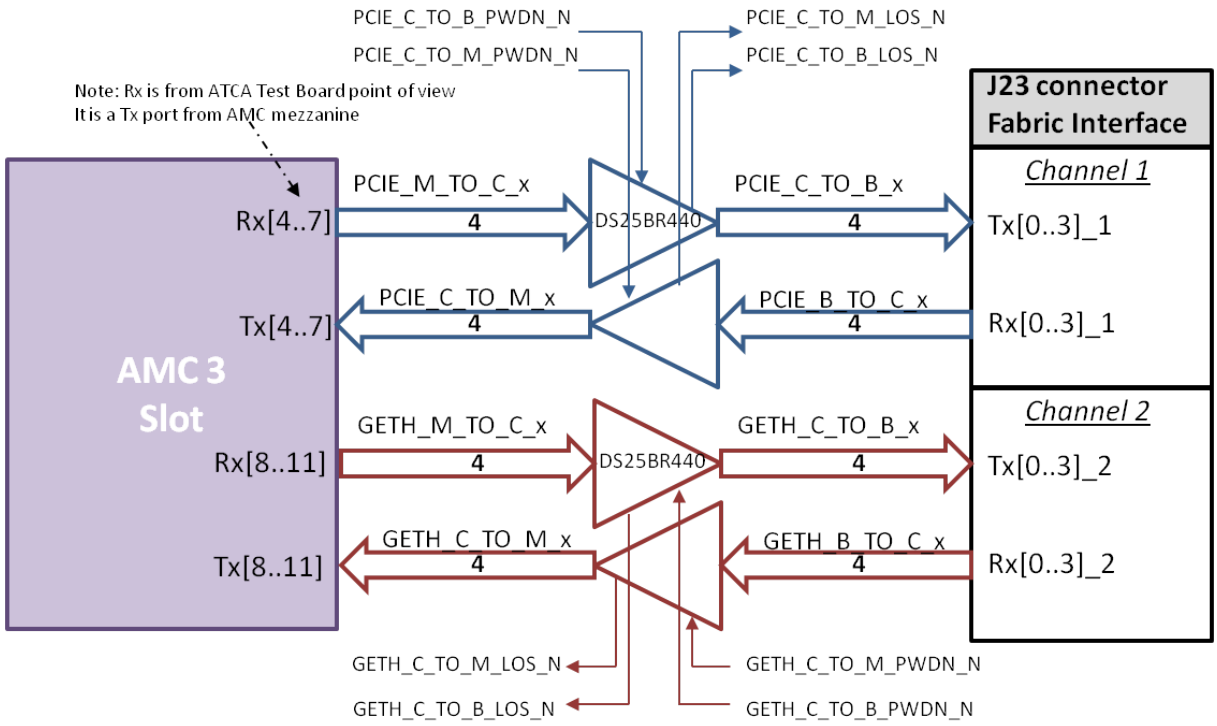


Figure 12: AMC3 and IPMC Test Board backplane inter-connections

AMC Fabric DS25BR440 control signal	IPMC Mezzanine IO
PCIE_C_TO_B_PWDN_N	IPM_IO_3
GETH_C_TO_B_PWDN_N	IPM_IO_4
PCIE_C_TO_M_PWDN_N	IPM_IO_5
GETH_C_TO_M_PWDN_N	IPM_IO_6
PCIE_C_TO_B_LOS_N	USR_4
GETH_C_TO_B_LOS_N	USR_5
PCIE_C_TO_M_LOS_N	USR_6
GETH_C_TO_M_LOS_N	USR_7

Table 10: AMC3 – backplane connections control signals on IPMC Mezzanine
C_TO_M = Carrier to Mezzanine, C_TO_B = Carrier to Backplane.

Back panel Interfaces

Ethernet

The ATCA Test Board back panel provides Ethernet connections with the IPMC Mezzanine. The Ethernet link runs at 100Mbit/s max. There are two ways to establish the Ethernet link:

- The Ethernet connector at the top rear of the board
- The ATCA backplane Base Interface through J23 connector

A switch device *TS31110* from *Texas Instrument* allows a selection between these two links. This switch is controlled by the IPMC Mezzanine with the *BASE_INTF_CH_SELECT* signal (0=base interface, 1=Eth connector) or by an on-board jumper. The Mezzanine can also control the two Ethernet connector led. The following figure explains the Ethernet architecture:

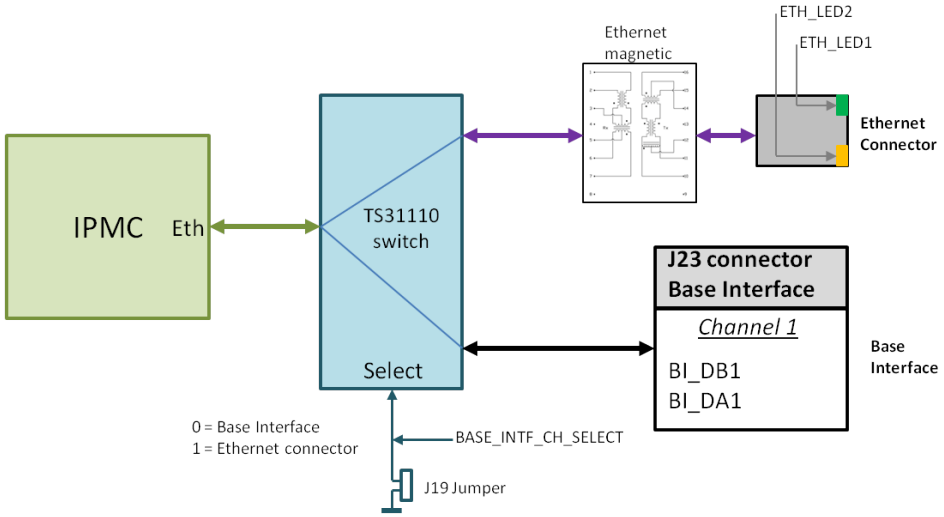


Figure 13: Ethernet link architecture

Figure 14: Details of the Ethernet selector jumper J19

ATCA Test Board signal	IPMC Mezzanine IO
BASE_INTF_CH_SELECT	USR_3
ETH_LED1	USR_1
ETH_LED2	USR_2

Table 11: Ethernet control signals on IPMC Mezzanine

USB

The IPMC Test Board has two USB port:

- One is connected to the IPMC Mezzanine
- The other is connected to the FPGA through a *FT240X* device from *FTDI*. This device is a USB to 8-bit parallel FIFO interface that makes it easy to implement USB interfaces with the FPGA. Drivers can be found on the *FTDI* web site. One driver allows using the USB link as a serial COM port.

UART

The IPMC Test Board provides one UART connector connected to the IPMC Mezzanine UART port. The following schematic shows the connector pin out. This pin out is compatible with the USB/RS232 cable ref: *TTL-232R-3V3* from *FTDI*.

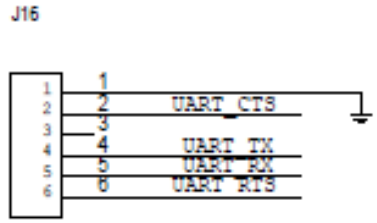


Figure 15: UART connector schematic

FPGA

Architecture

The ATCA Test Board has a FPGA connected to IPMC Mezzanine signals and other interfaces (see figure below). It can be used to probe or source signals and for many other applications.

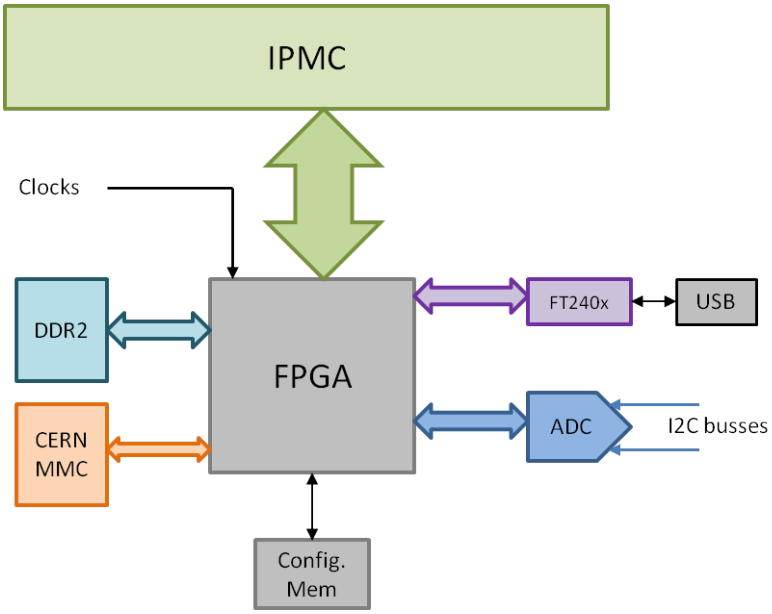


Figure 16: IPMC Test Board FPGA JTAG architecture

Configuration

The FPGA is associated with a configuration memory (*Altera EPCS16*). The *Altera CycloneII* FPGA used on the board is based on a RAM technology. At power-up the RAM is not configured and the FPGA configures its RAM from the configuration memory.

There are two ways to configure the FPGA:

- By using the JTAG bus. The JTAG bus allows programming the FPGA RAM. In this case the FPGA will lose its firmware after a power-down. Or the JTAG Indirect Configuration method with the Serial Flash Loader can be used to write the configuration memory (see Altera application notes)
- By using the FPGA configuration connector. In QuartusII software, the mode “Active Serial Configuration” must be chosen. This mode directly programs the *EPCS16* configuration memory.

The easiest way to program the FPGA or/and the configuration memory is to use a USB-Blaster cable (or a Terasic-Blaster which is cheaper) and the Altera QuartusII software in JTAG mode or Active Serial mode. Below is a view of the QuartusII programming window.

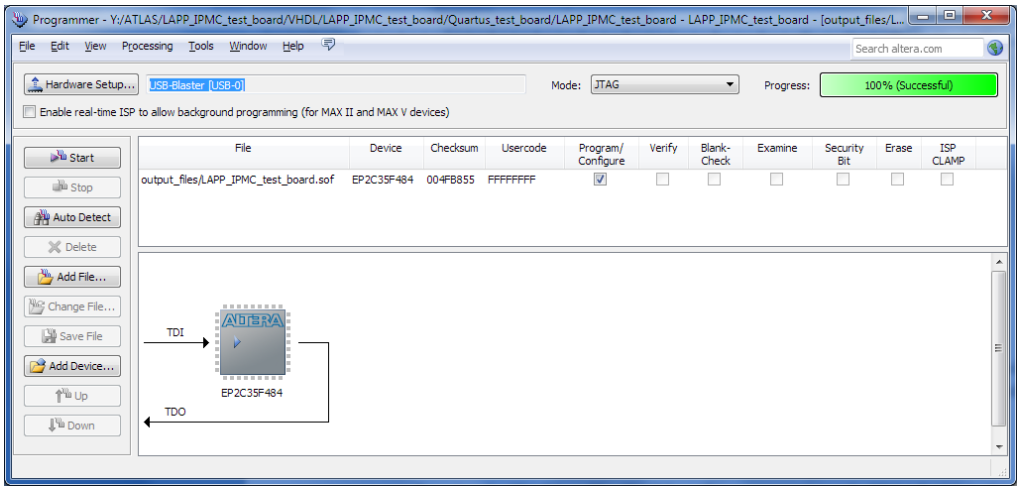


Figure 17: View of the QuartusII JTAG programmer

Another way is to use the JTAG bus driven by the IPMC Mezzanine. The board has a jumper J22 to select the JTAG master: the IPMC Mezzanine or the JTAG connector (see JTAG section). In this mode the IPMC Mezzanine firmware must have the capability to drive the JTAG bus.

DDR2

The IPMC Test Board has a 1-GBit DDR2 memory *MT47H128M8CF* from *Micron* connected to the FPGA. It can be used for any user application. **CAUTION: THIS DDR2 HAS NOT BEEN TESTED. Moreover there is a mistake in the schematic**: the DDR2_DQ(7) signal is not connected to the proper FPGA IO Bank. The FPGA cannot drive this pin when configured in DDR2 standard. One way to use the DDR2 is to use only the 4-bits DQ(0..3) and merge 4-bit data into 8-bit data in the FPGA.

MMC slot

The IPMC Test Board has a slot dedicated to the MMC mezzanine developed by the CPPM laboratory and CERN. This MMC is connected to the IPMC Mezzanine through AMC standard signals (MMC_EN3_N, MMC_EN12_N etc… see AMC section).

Moreover the MMC mezzanine has some “local” signals for AMC mezzanine local control (AMC power supplies control, FPGA firmware loading… See CPPM MMC specification for more information). These signals have been connected on the IPMC Test Board FPGA in order to emulate an AMC mezzanine.

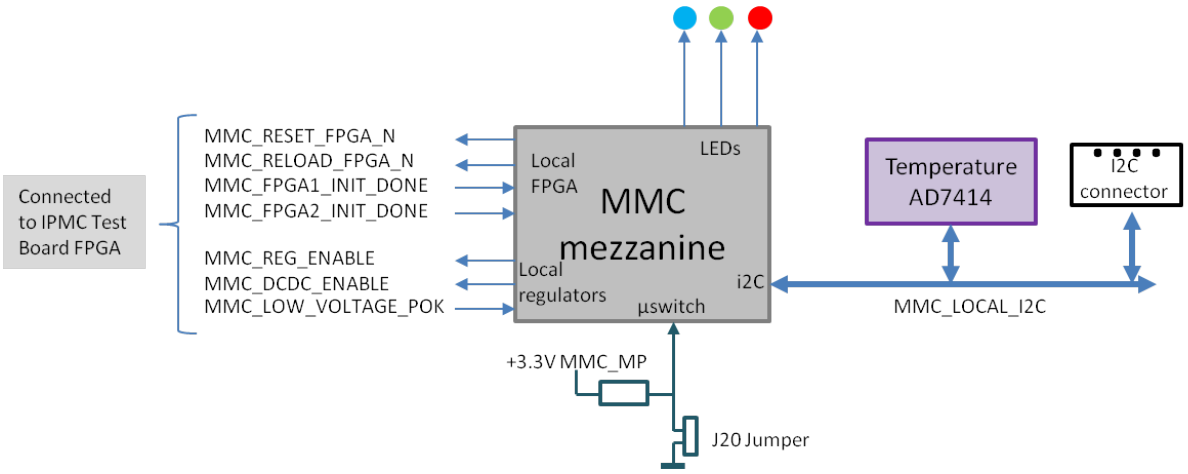


Figure 18: MMC mezzanine slot "local" signals

The J20 jumper emulates the AMC mezzanine micro switch, an *AD7414* temperature sensor is connected to the local I2C bus. Other sensors can be connected to this bus through the MMC I2C connector.

JTAG

IPMC Mezzanine Debugging

The first JTAG chain is dedicated to the IPMC Mezzanine. This chain is accessible by the "Mezzanine debug connector". This connector is a standard ARM 20-pin debug connector. Several USB to JTAG cables are available on the market.

The *NGX ARM USB JTAG* from *NGX Technologies* is well suited for the IPMC Mezzanine Debugging.

Figure 19: NGX ARM USB JTAG in-circuit debugger and programmer

FPGA and AMC JTAG

The second JTAG chain is used for the FPGA and the AMC. This JTAG chain is driven by:

- The 10-pin JTAG connector
- The IPMC Mezzanine Master JTAG port

The selection of the JTAG chain driver is made by J22 jumper located closed to the 10-pin JTAG connector.

This chain goes to the FPGA and the four AMC. For each AMC a Jumper allows to choose whether the AMC is included in the JTAG chain or not. The following figure shows the architecture of this JTAG chain:

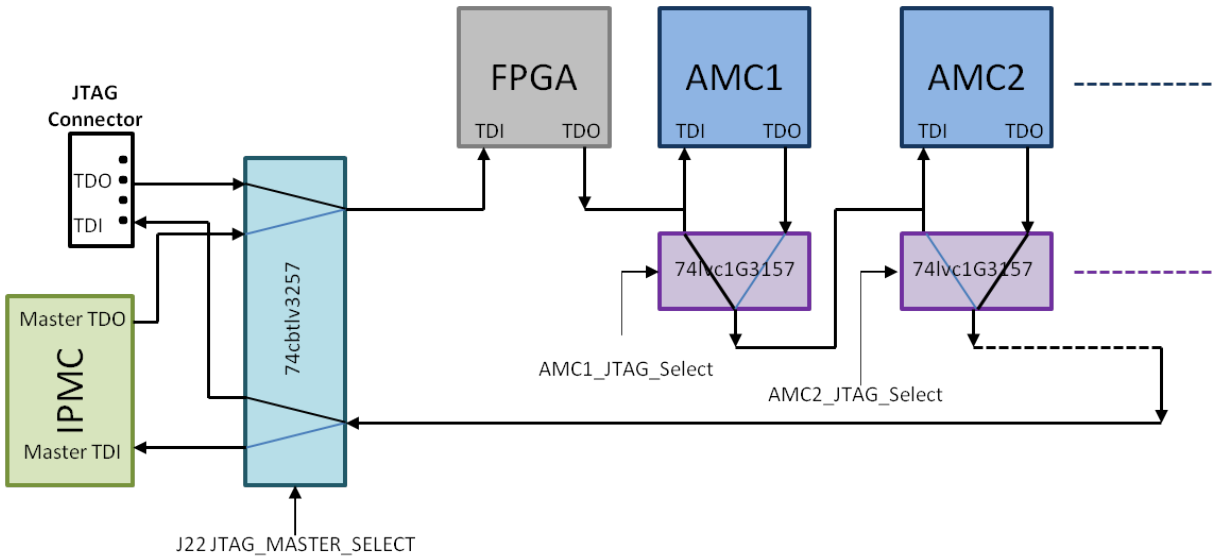


Figure 20: FPGA and AMC JTAG bus architecture

An Altera USB-Blaster or Terasic-Blaster cable can be used to drive the chain with the JTAG Connector.

III. Debugging with LAPP IPMC Test Board

The on-board FPGA is connected to most of the IPMC Mezzanine signals. Therefore the FPGA is an excellent tool to probe or drive IPMC Mezzanine signals. The user can build its own FPGA firmware according to its debugging needs or the default firmware can be used. This default firmware allows the use of the two following tools. Note that these tools works with the Altera QuartusII software with the USB-Blaster or Terasic-Blaster cable connected to the JTAG connector. **NOTE:** The FPGA must be powered on to use these tools. This means that the ENABLE_12V signal must be at a logic '1'.

Signal Tap logic analyzer

Altera QuartusII software provides a tool named "Signal Tap". This tool is a logic analyzer for signals listed in the setup tab (see Figure 21). The user can select the trigger type (rising / falling edge, low / high level) and the trigger signal. The right window of Figure 20 shows the signals analyzer after a trigger condition occurs. In the default design, signals are sampled at 10MHz and stored in a 2k depth RAM.

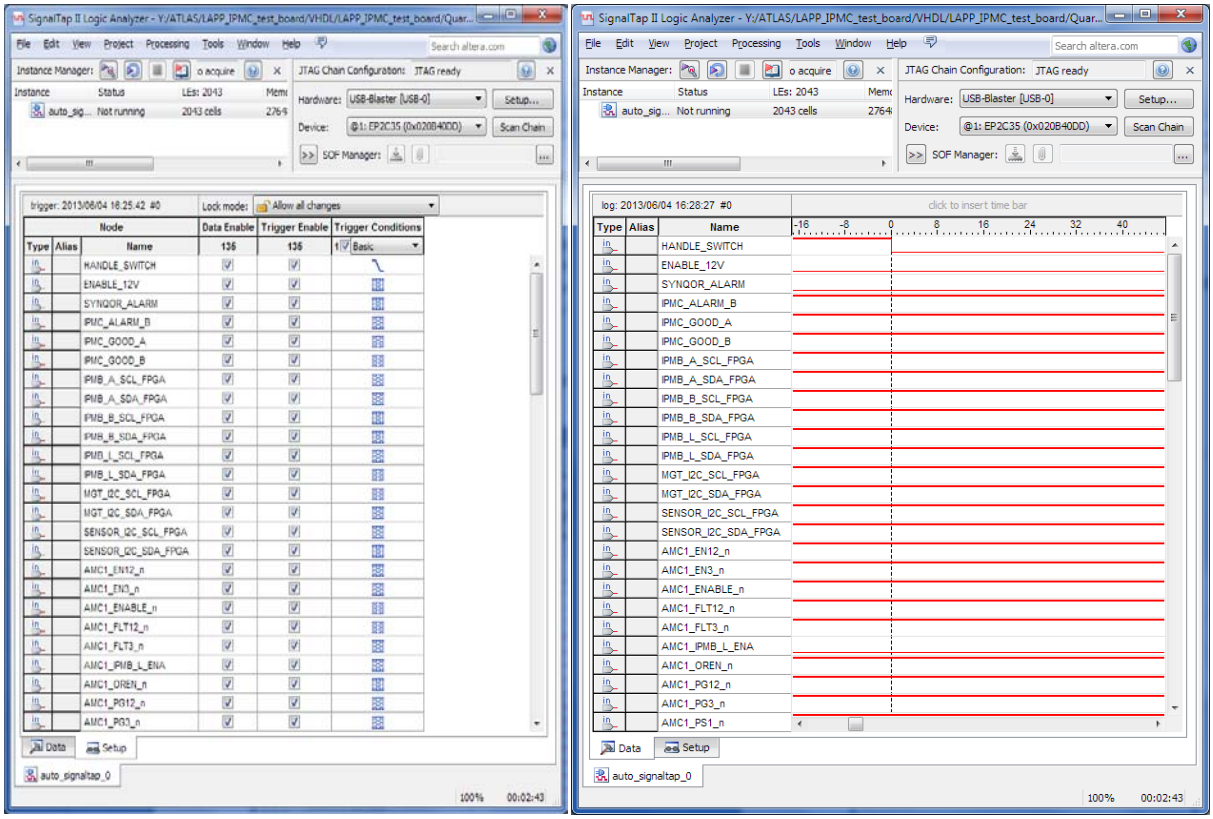


Figure 21: Left: setup view of the signal tap tool. Right: data view.

The analyzed signals, the sampling frequency and the memory depth can be easily modified to comply with user needs. In this case the design must be recompiled and the FPGA firmware reloaded.

GUI signal probe

QuartusII software also provides the "In System Sources and Probes" tool. This tool allows reading or writing signals through the JTAG interface. Moreover, Altera provides TCL functions for accessing signal with a TCL script. The *ATCA_Test_Board_probe* project provides scripts written in TCL/TK

for visualizing the state of almost all IPMC Mezzanine signals. The following figure shows this graphical interface.

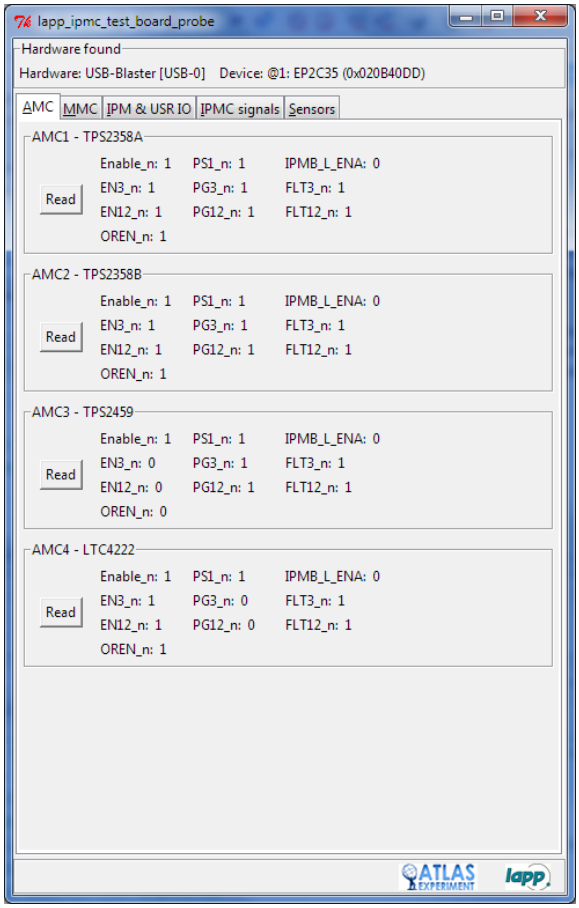


Figure 22: View of the probe tool

To use this tool:

- Connect the USB-Blaster (or Terasic-Blaster) to the JTAG connector
- Open the Tcl console in QuartusII: **View → Utility Windows → Tcl Console**
- Type the following command in the Tcl Console:
  exec quartus_stp –t *tcl_script_path*/lapp_ipmc_test_board_probe.tcl *tcl_script_path*/
  Ex: *exec quartus_stp -t C:/Tcl/lapp_ipmc_test_board_probe.tcl C:/Tcl/*

Advanced GUI debugger

This graphical interface is also build with TCL/TK scripts interfaced with the QuartusII “In System Sources and Probes” tool. This interface allows probing IPMC signals, but also driving some of these signals. **BEWARE**: The FPGA drives some IPMC signals. Then if this interface is used with the IPMC Mezzanine plugged on the ATCA Test Board, some conflicts can happened and destroy FPGA or IPMC Mezzanine IOs**. It is not recommended to use this interface with the IPMC Mezzanine plugged**. This interface has the following features:

- ATCA Test Board I2C component access (Temperature, voltage, current monitoring, AMC power controller access etc…). **In order to drive I2C busses with the FPGA, add 0Ω**

resistor for R214 to R223. Be careful: when the +12V supply is not enable the FPGA is not supplied and I2C busses are pulled low.

- FRU & SDR EEPROM access (read and write)
- AMC and MMC signals reading and writing (Enable_3.3V, Enable_12V etc..)
- IPMC IO reading and writing

This interface has been first designed for testing the LAPP_IPMC_Test_Board.

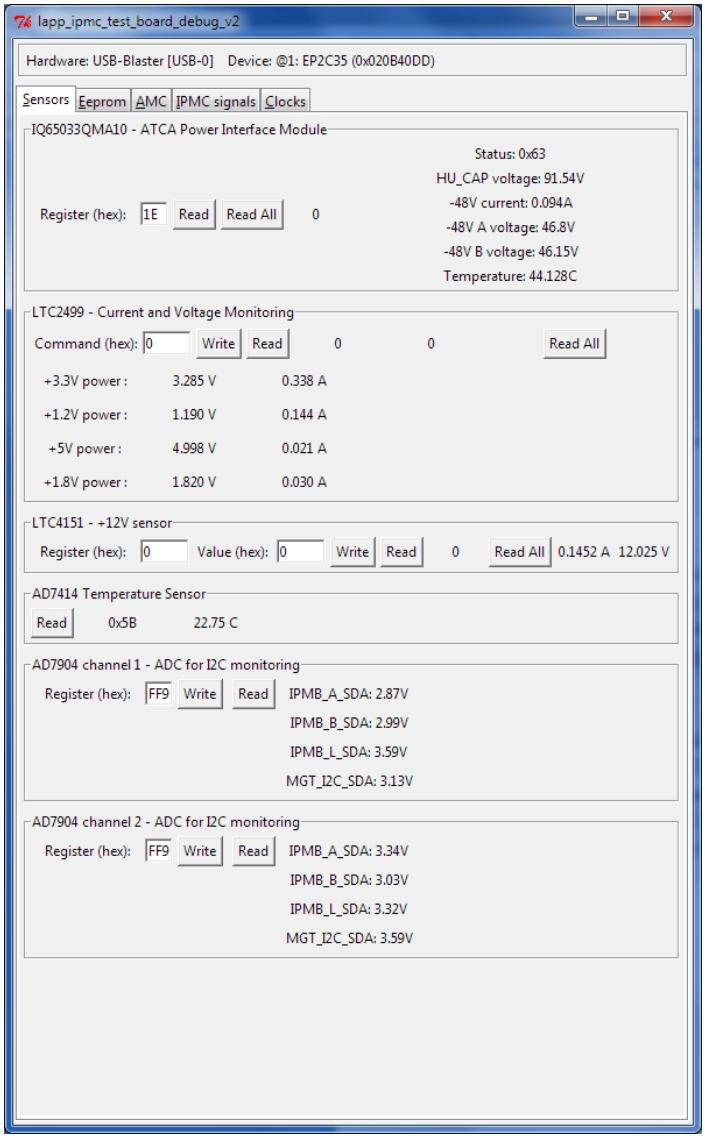


Figure 23: View of the advanced debugger tool

To use this tool:

- Connect the USB-Blaster (or Terasic-Blaster) to the JTAG connector
- Load the FPGA firmware. The firmware is located in the "*LAPP_IPMC_test_board_advanced.qar*" file.
- Launch the TCL script with the following command in the QuartusII TCL Console:
  ***exec quartus_stp -t** tcl_script_path/**LAPP_IPMC_Test_Board_advanced.tcl** tcl_script_path/*

IV. Errata

I2C busses

I2C busses are disconnected from FPGA (R214 to R223 removed). When the +12V supply is disable the FPGA is not supplied. In this condition I2C busses are pulled low by FPGA IOs and can cause troubles on these busses.

V. Annexes

A. Schematic

POWER SUPPLIES

atca_board_cutaway_carrier

U8
ESD_SEG_1
ESD_SEG_2
ESD_SEG_3
R7 10.00M
R8 10.00M
SHELF_GND

J3 CON2P
SEE ATCA REQ 4.96
SHELF_GND

OPTIONAL TO ENABLE +12V
J4 CON2P
P3V3_IPMI
R16 1K
R17 1K
ENABLE_12V
IN
R13 10.0K

HOLD-UP CAPACITOR
CHARGED AT 90V
C9 470U
C10 470U
R15 12.49K
C195 100U
C12 47N

U10 ACPL_217
C16 1N

U11 SynQor DC/DC PQ60120QEA17
VIN+ VOUT+ SENSE+ ON/OFF TRIM SENSE- VIN- VOUT-
VP12_M
R22 0.0045
VP12
+12V
17A
DNC R20
DNC R21
C17 10U
C18 3900U

D1 BLANC_PLCC_2
R23 10.0K

P3V3_IPMI
R18 10.0K

U9 SynQor IQ65033QMA10
-48V_A -48V_B VRTN_A VRTN_B ENABLE_A ENABLE_B SHELF_GND
HU_CAP HU_TRIM VRTN_OUT -48V_OUT
ALARM LOGIC_GND I2C_CLK I2C_DAT I2C_ADR 3V3 5V
OUT SYNQOR_ALARM
IN B1 MGT_I2C_SCL
B1 MGT_I2C_SDA
DNC R19

IF DNC= N.C
I2C ADDR=0101111

P1 con_atca_z1
JTAG: TCK TDO TDI TMS
Metallic Test: MT1_TIP MT2_TIP MT1_RING MT2_RING
Ringing Generator: -RING_A -RING_B RRTN_A RRTN_B
POWER SUPPLIES: -48V_A -48V_B VRTN_A VRTN_B EARLY_A EARLY_B ENABLE_A ENABLE_B
HARDWARE MANAGEMENT: Hardware @ HA0 HA1 HA2 HA3 HA4 HA5 HA6 HA7/P
IPMB_A: SCL_A SDA_A
IPMB_B: SCL_B SDA_B
SHELF_GND LOGIC_GND

F1 7A
F2 7A
F3 10A
F4 10A
F5 1A
F6 1A
F7 1A
F8 1A
R11 100.00
R12 100.00

B1 IPMB_A_SCL
B1 IPMB_B_SCL
B1 IPMB_A_SDA
B1 IPMB_B_SDA

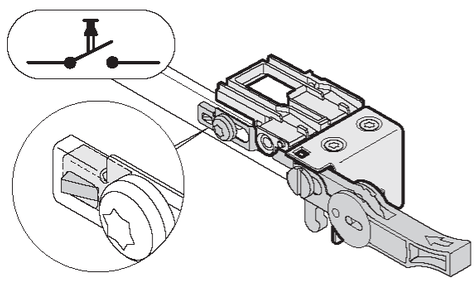
P5V_IPMI
+5V
150MA
C13 10U
C14 10U
P3V3_IPMI
+3.3V
3.6A
C15 470U

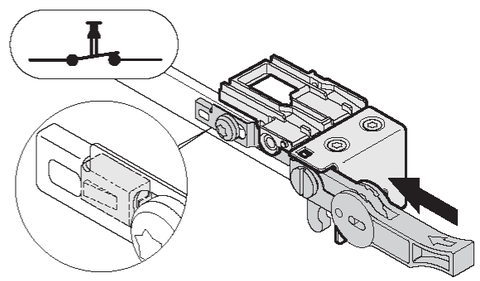
P3V3_IPMI P5V_IPMI VP12
T1 T2 T3
TEST test_pin

P3V3_IPMI
R1 R2 R3 R4 R5 R6 R9 R10 10.0K
HA<7..0>
C1 C2 C3 C4 C5 C6 C7 C8 1N
SEE PICMG 3.0 SEC 2.4.1.5

P3V3_IPMI
S1 5switch
OUT HANDLE_SWITCH_N
R177 DNC
R14 1.00K
C11 X

FACE PLATE HANDLE SWITCH (S1)
REF. SCHROFF : 20849235
NORMALLY CLOSED





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ipmc_test_board

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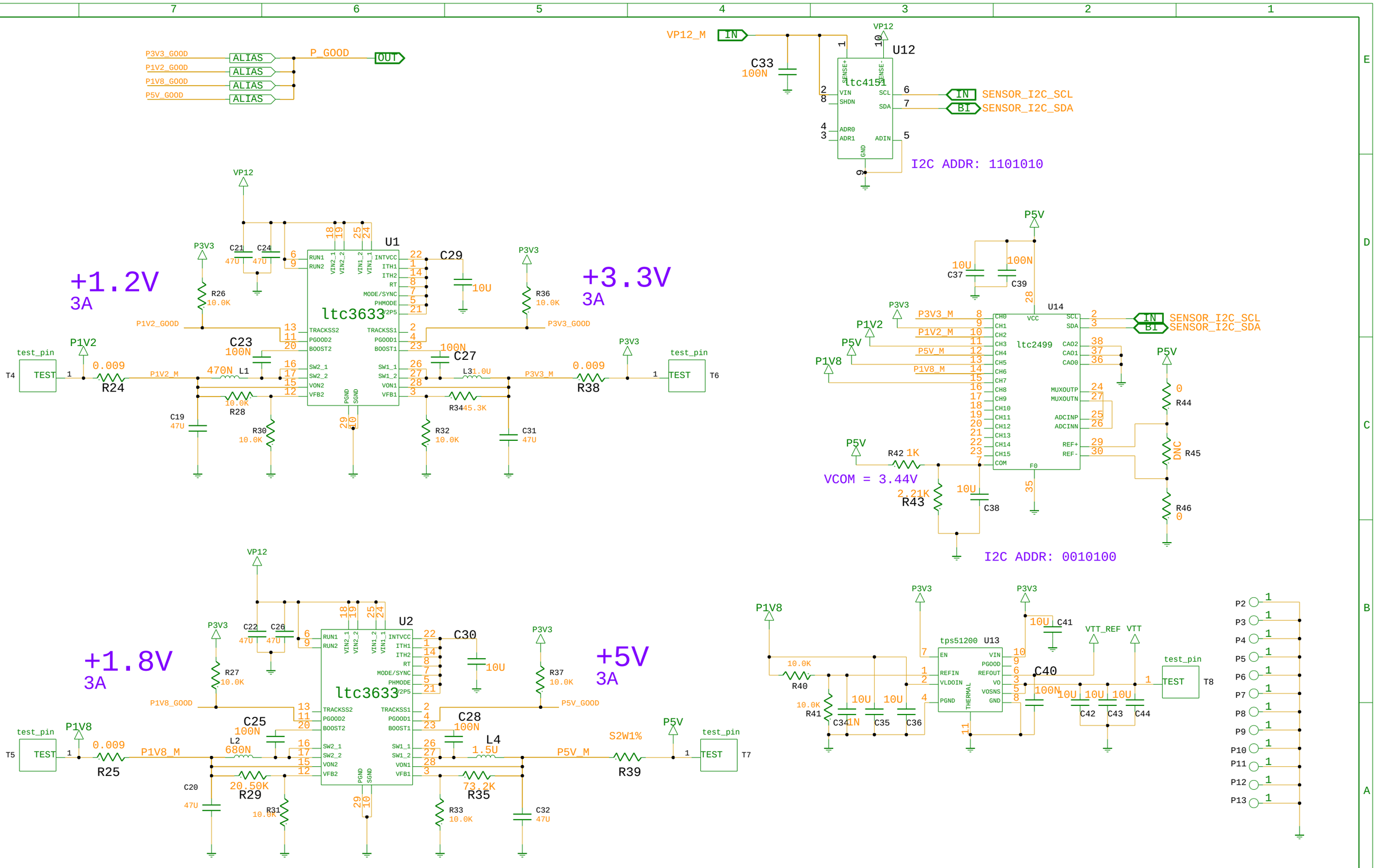

POWER SUPPLIES 2

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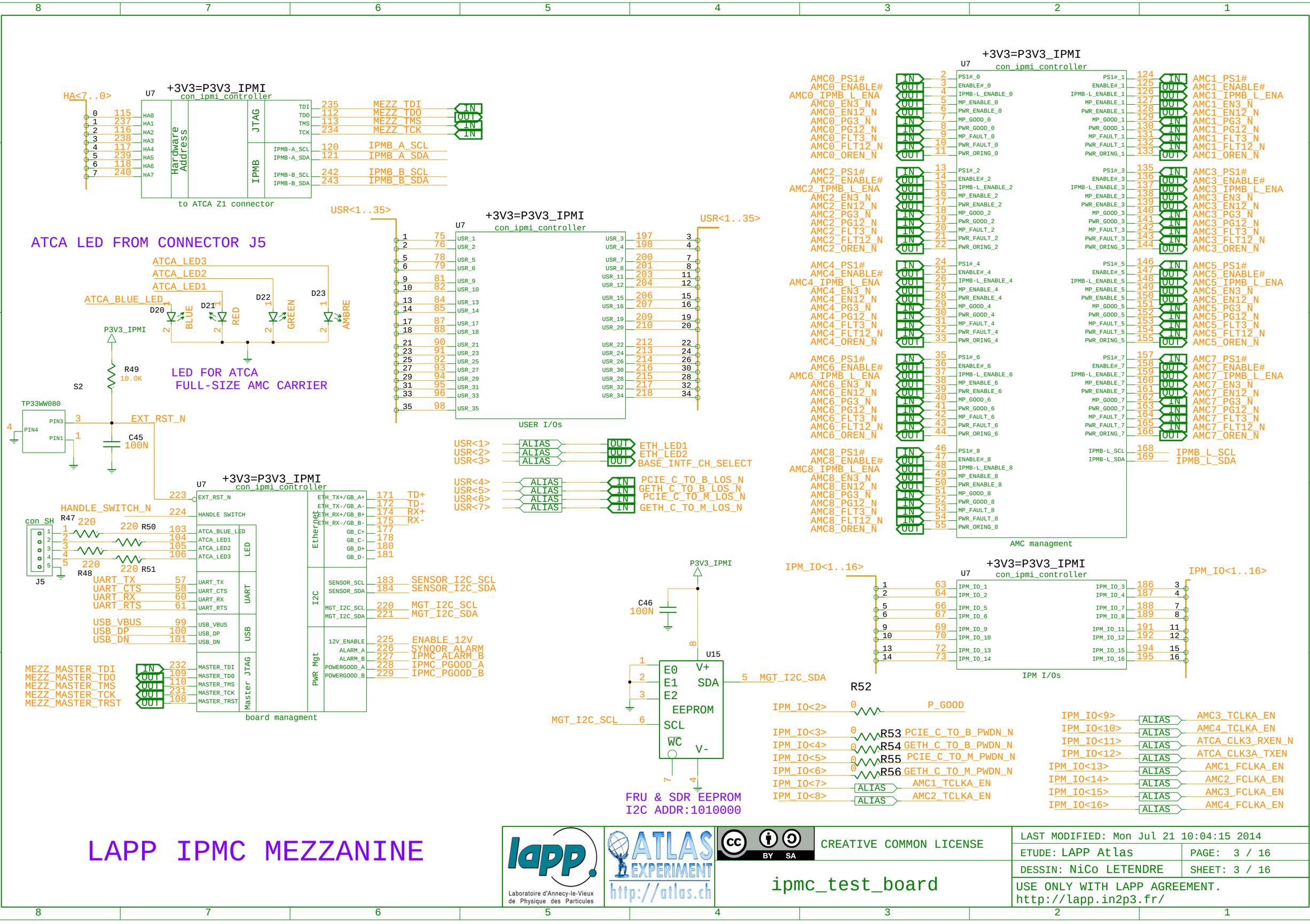
HA<7..0>
U7
+3V3=P3V3_IPMI
con_ipmi_controller
Hardware Address
JTAG
IPMB
to ATCA Z1 connector
MEZZ_TDI
MEZZ_TDO
MEZZ_TMS
MEZZ_TCK
IPMB_A_SCL
IPMB_A_SDA
IPMB_B_SCL
IPMB_B_SDA
USR<1..35>
USER I/Os
ATCA LED FROM CONNECTOR J5
ATCA_LED3
ATCA_LED2
ATCA_LED1
ATCA_BLUE_LED
D20
D21
D22
D23
BLUE
RED
GREEN
AMBRE
P3V3_IPMI
R49
10.0K
LED FOR ATCA
FULL-SIZE AMC CARRIER
S2
TP33WW080
EXT_RST_N
C45
100N
HANDLE_SWITCH_N
R47
R48
R50
R51
con SH
J5
UART_TX
UART_CTS
UART_RX
UART_RTS
USB_VBUS
USB_DP
USB_DN
MEZZ_MASTER_TDI
MEZZ_MASTER_TDO
MEZZ_MASTER_TMS
MEZZ_MASTER_TCK
MEZZ_MASTER_TRST
Ethernet
LED
UART
USB
Master JTAG
I2C
PWR Mgt
board managment
ALIAS
ETH_LED1
ETH_LED2
BASE_INTF_CH_SELECT
PCIE_C_TO_B_LOS_N
GETH_C_TO_B_LOS_N
PCIE_C_TO_M_LOS_N
GETH_C_TO_M_LOS_N
AMC0_PS1#
AMC0_ENABLE#
AMC0_IPMB_L_ENA
AMC0_EN3_N
AMC0_EN12_N
AMC0_PG3_N
AMC0_PG12_N
AMC0_FLT3_N
AMC0_FLT12_N
AMC0_OREN_N
AMC2_PS1#
AMC2_ENABLE#
AMC2_IPMB_L_ENA
AMC2_EN3_N
AMC2_EN12_N
AMC2_PG3_N
AMC2_PG12_N
AMC2_FLT3_N
AMC2_FLT12_N
AMC2_OREN_N
AMC4_PS1#
AMC4_ENABLE#
AMC4_IPMB_L_ENA
AMC4_EN3_N
AMC4_EN12_N
AMC4_PG3_N
AMC4_PG12_N
AMC4_FLT3_N
AMC4_FLT12_N
AMC4_OREN_N
AMC6_PS1#
AMC6_ENABLE#
AMC6_IPMB_L_ENA
AMC6_EN3_N
AMC6_EN12_N
AMC6_PG3_N
AMC6_PG12_N
AMC6_FLT3_N
AMC6_FLT12_N
AMC6_OREN_N
AMC8_PS1#
AMC8_ENABLE#
AMC8_IPMB_L_ENA
AMC8_EN3_N
AMC8_EN12_N
AMC8_PG3_N
AMC8_PG12_N
AMC8_FLT3_N
AMC8_FLT12_N
AMC8_OREN_N
AMC managment
AMC1_PS1#
AMC1_ENABLE#
AMC1_IPMB_L_ENA
AMC1_EN3_N
AMC1_EN12_N
AMC1_PG3_N
AMC1_PG12_N
AMC1_FLT3_N
AMC1_FLT12_N
AMC1_OREN_N
AMC3_PS1#
AMC3_ENABLE#
AMC3_IPMB_L_ENA
AMC3_EN3_N
AMC3_EN12_N
AMC3_PG3_N
AMC3_PG12_N
AMC3_FLT3_N
AMC3_FLT12_N
AMC3_OREN_N
AMC5_PS1#
AMC5_ENABLE#
AMC5_IPMB_L_ENA
AMC5_EN3_N
AMC5_EN12_N
AMC5_PG3_N
AMC5_PG12_N
AMC5_FLT3_N
AMC5_FLT12_N
AMC5_OREN_N
AMC7_PS1#
AMC7_ENABLE#
AMC7_IPMB_L_ENA
AMC7_EN3_N
AMC7_EN12_N
AMC7_PG3_N
AMC7_PG12_N
AMC7_FLT3_N
AMC7_FLT12_N
AMC7_OREN_N
IPMB_L_SCL
IPMB_L_SDA
C46
100N
U15
E0
E1
E2
EEPROM
SCL
WC
V+
SDA
V-
FRU & SDR EEPROM
I2C ADDR:1010000
IPM_IO<1..16>
IPM I/Os
R52
P_GOOD
R53 PCIE_C_TO_B_PWDN_N
R54 GETH_C_TO_B_PWDN_N
R55 PCIE_C_TO_M_PWDN_N
R56 GETH_C_TO_M_PWDN_N
AMC1_TCLKA_EN
AMC2_TCLKA_EN
AMC3_TCLKA_EN
AMC4_TCLKA_EN
ATCA_CLK3_RXEN_N
ATCA_CLK3A_TXEN
AMC1_FCLKA_EN
AMC2_FCLKA_EN
AMC3_FCLKA_EN
AMC4_FCLKA_EN
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CURRENT LIMIT = 8.25A
FAST TRIP = 11.1A

FAULT TIMER = 10MS

AMC 1

S=GND <-> A=B1
<-> AMC IN JTAG CHAIN

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CURRENT LIMIT = 8.25A
FAST TRIP = 11.1A

FAULT TIMER = 10MS

AMC 2

S=GND <-> A=B1
<-> AMC IN JTAG CHAIN

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CURRENT LIMIT = 8.25A
FAST TRIP = 11.1A

VP12
C64 100N
R98 0.009
T11
AMC3_PWR
D8 I26
R99 750
R100 100
U24
AMC3_EN12_N IN
R97 10.0K
MGT_I2C_SCL IN
MGT_I2C_SDA BI
P3V3_IPMI
AMC3_OREN_N IN
C63 100N
AMC3_EN3_N IN
R95 10.0K
R96 10.0K
C65 100N
TPS2459
+12V
+3.3V
R103 10.0K
R105 10.0K
P3V3_IPMI
6.81K R102
R104 10.0K
R106 10.0K
AMC3_MP
R101 3.32K
AMC3_PG12_N OUT
AMC3_FLT12_N OUT
AMC3_PG3_N OUT
AMC3_FLT3_N OUT

U25 sn74lvc2g125dcu
IN AMC3_TDI
AMC3_TDO_BUF
R109 33
R110 33
AMC3_TDI_BUFF
OUT AMC3_TDO

P3V3
R111 10.0K
AMC3_TDI_BUFF
CON_AMC3_TDO
AMC3_TMS IN
AMC3_TCK IN
AMC3_TRST IN
AMC_JTAG
con_amc_b_plus
AMC3_MP
C66 1U

AMC3_PWR
J10
AMC SLOT 3
AMC3_ENABLE# IN
P3V3_IPMI
R112 2.21K
AMC3_PS1# OUT

AMC3_MP
R113 3.32K
R114 3.32K
P3V3_IPMI
C67 100N
U26 ltc4307
IPMB_L_SDA BI
IPMB_L_SCL IN
AMC3_IPMB_L_ENA IN
R115 10.0K
C68 100N
C69 100N

CMS
SOT-23
sn74lvc1g3157
U27
AMC3_TDO_BUF
AMC3_TDI_BUFF
CON_AMC3_TDO
P3V3
R116 10.0K
late_spst_2054
J11
S=GND <-> A=B1
<-> AMC IN JTAG CHAIN

D9 VERT_0603_CMS
D10 AMBRE_0603_CMS
AMC3_PWR
AMC3_MP
2.21K R107
220 R108

J10
con_amc_b_plus
AMC FABRIC 1
PCIE_M_TO_C_0+ / PCIE_M_TO_C_0- 44 45
PCIE_M_TO_C_1+ / PCIE_M_TO_C_1- 50 51
PCIE_M_TO_C_2+ / PCIE_M_TO_C_2- 59 60
PCIE_M_TO_C_3+ / PCIE_M_TO_C_3- 65 66
GETH_M_TO_C_0+ / GETH_M_TO_C_0- 91 90
GETH_M_TO_C_1+ / GETH_M_TO_C_1- 97 96
PCIE_C_TO_M_0+ / PCIE_C_TO_M_0- 47 48
PCIE_C_TO_M_1+ / PCIE_C_TO_M_1- 53 54
PCIE_C_TO_M_2+ / PCIE_C_TO_M_2- 62 63
PCIE_C_TO_M_3+ / PCIE_C_TO_M_3- 68 69
GETH_C_TO_M_0+ / GETH_C_TO_M_0- 88 87
GETH_C_TO_M_1+ / GETH_C_TO_M_1- 94 93

J10
con_amc_b_plus
AMC FABRIC 2
GETH_M_TO_C_2+ / GETH_M_TO_C_2- 103 102
GETH_M_TO_C_3+ / GETH_M_TO_C_3- 109 108
GETH_C_TO_M_2+ / GETH_C_TO_M_2- 100 99
GETH_C_TO_M_3+ / GETH_C_TO_M_3- 106 105

J10
AMC3_TCLKA+ 74
AMC3_TCLKA- 75
AMC3_PCIE_REFCLK+ 80
AMC3_PCIE_REFCLK- 81
CLOCKS
TCLKB+ 77
TCLKB- 78
TCLKC+ 136
TCLKC- 135
TCLKD+ 139
TCLKD- 138
con_amc_b_plus

AMC 3

AMC.1 TYPE 4 AMC.2 TYPE 4/5
OR AMC.2 TYPE 6

I2C ADDR: 0001000

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UV=10.80V
OV=13.44V

CURRENT LIMIT = 8.25A
PG12 WHEN >10.53V
PG3 WHEN >2.94V

I2C ADDR: 1001100

AMC 4

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AMC SLOT 5

CURRENT LIMIT = 8.25A
FAST TRIP = 11.1A

FAULT TIMER = 10MS

MMC I2C SENSORS

MMC

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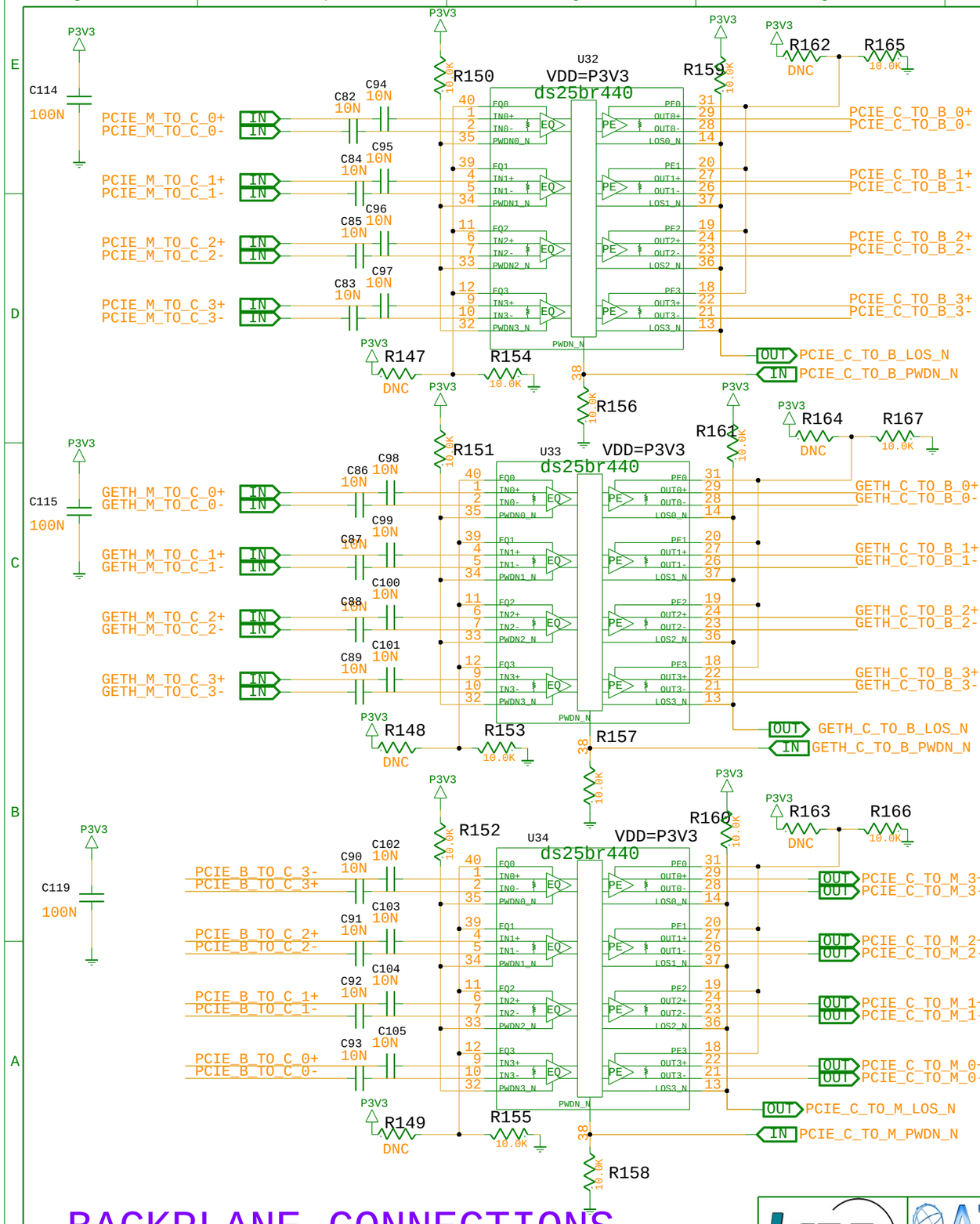
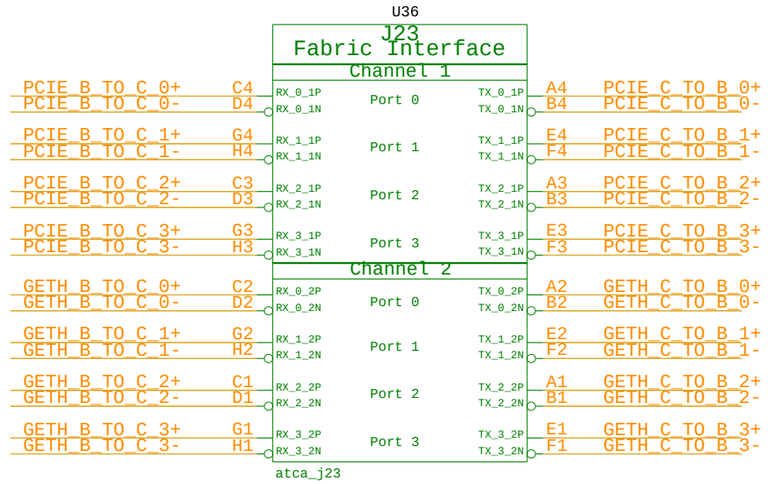
BACKPLANE CONNECTIONS





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RS-232

J16

UART_CTS
UART_TX
UART_RX
UART_RTS

FTDI TTL-232R PINOUT
COMPATIBLE

USB

J15 CON USB MINI B

USB_VBUS
C116 100N
THERMAL_PAD=GND
U39 DRSR tpd2e001
USB_DN
USB_DP
P5V
THERMAL_PAD=GND
U37 DRSR tpd2e001

J14 CON USB MINI B

C118 100N
C121 10U
C123 100N
C124 100N
C117 100N
P5V
P1V8
U3 FT240X
R179 33
R180 33
R181 1K
IN USB_RESET_N
R175 10.0K
R176 6.65K

BI USB_D<7..0>
IN USB_RD_N
IN USB_WR
OUT USB_TXE_N
OUT USB_RXF_N
IN USB_SIWU_N
BI USB_CBUS5
BI USB_CBUS6

I2C SENSORS

I2C ADDR:1001000

J17
P3V3
C265 100N
U40 AD7414
SENSOR_I2C_SDA
SENSOR_I2C_SCL

ETHERNET

P3V3_IPMI
R182 220
IN ETH_LED1
J18 conrj45_leds_10mm_erni
4x10nF
4x75 ohms
1000pF/2kV
R183 220
IN ETH_LED2

ETH_TX+
ETH_TX-
ETH_RX+
ETH_RX-

U36 J23 Base Interface
Channel 1
Channel 2
atca_j23

BASE_RX1_P
BASE_RX1_N
BASE_TX1_P
BASE_TX1_N

R186 0
R189 0
TCT2
TCT4
C126 100N
C128 100N

U41 wurth_74902001
R184 75
R185 75
1N C125
RX1+
RX1-
TD1+
TD1-

U42 ts31110
PWE4
C127 100N
BASE_INTF_CH_SELECT
R187 1K
R188 10.0K
J19 byte_spst_2054

0 = BASE INTERFACE
1 = RTM CONNECTOR

RTM

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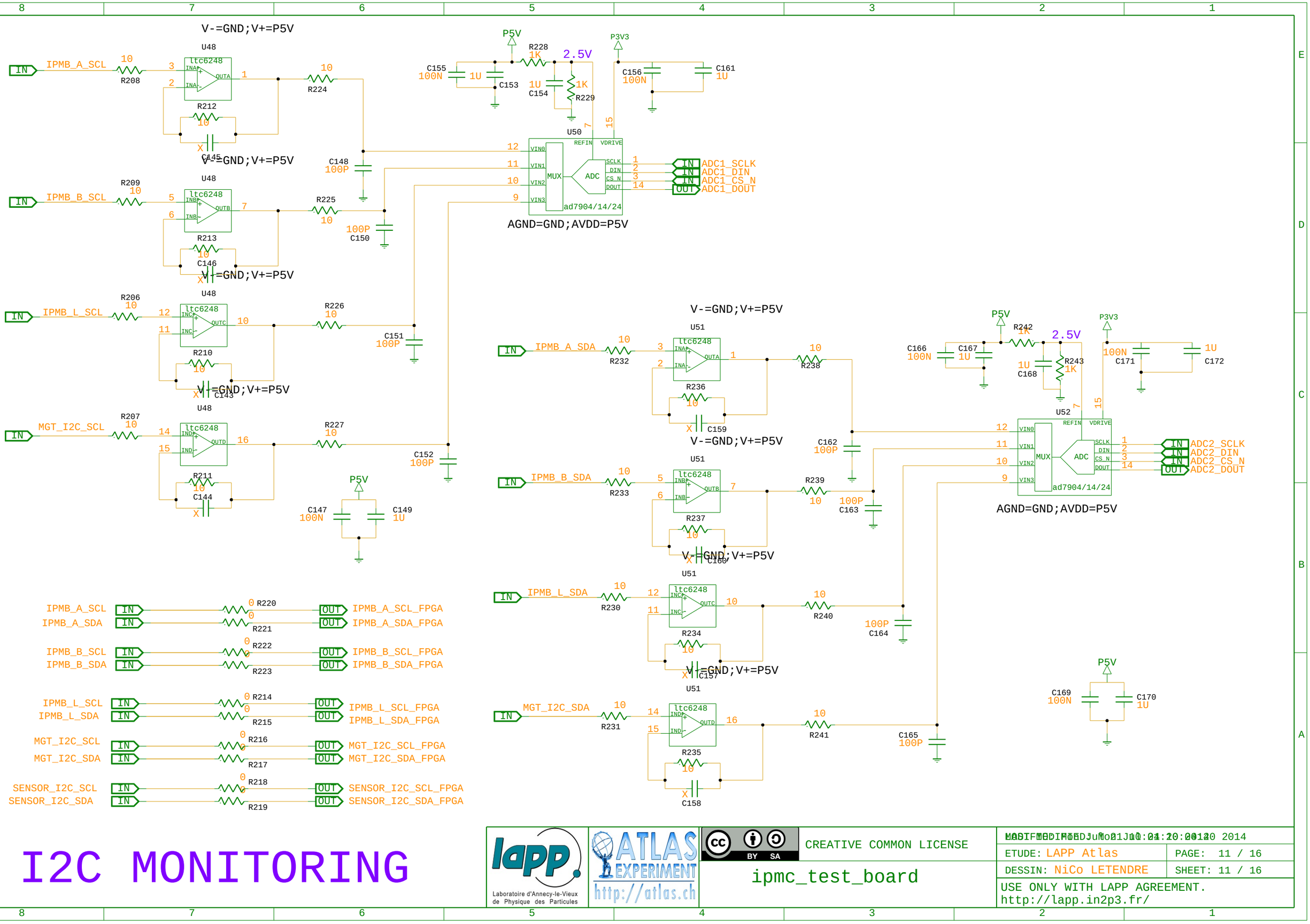
V-=GND;V+=P5V
U48
ltc6248
IPMB_A_SCL
R208
R212
C145
R224
C148
100P
V-=GND;V+=P5V
IPMB_B_SCL
R209
R213
C146
R225
100P
C150
V+=GND;V+=P5V
IPMB_L_SCL
R206
R210
C143
R226
C151
100P
V-=GND;V+=P5V
MGT_I2C_SCL
R207
R211
C144
R227
C152
100P
P5V
C147
100N
C149
1U
P5V
R228
1K
2.5V
C155
100N
1U
C153
1U
C154
1K
R229
P3V3
C156
100N
C161
1U
U50
REFIN
VDRIVE
VIN0
VIN1
VIN2
VIN3
MUX
ADC
SCLK
DIN
CS_N
DOUT
ad7904/14/24
AGND=GND;AVDD=P5V
ADC1_SCLK
ADC1_DIN
ADC1_CS_N
ADC1_DOUT
V-=GND;V+=P5V
U51
IPMB_A_SDA
R232
R236
C159
R238
V-=GND;V+=P5V
IPMB_B_SDA
R233
R237
C160
R239
C162
100P
C163
V-=GND;V+=P5V
IPMB_L_SDA
R230
R234
C157
R240
100P
C164
V+=GND;V+=P5V
MGT_I2C_SDA
R231
R235
C158
R241
C165
100P
P5V
R242
1K
2.5V
C166
100N
C167
1U
1U
C168
R243
1K
P3V3
100N
C171
1U
C172
U52
REFIN
VDRIVE
MUX
ADC
ad7904/14/24
AGND=GND;AVDD=P5V
ADC2_SCLK
ADC2_DIN
ADC2_CS_N
ADC2_DOUT
P5V
C169
100N
C170
1U
IPMB_A_SCL
IPMB_A_SDA
IPMB_B_SCL
IPMB_B_SDA
IPMB_L_SCL
IPMB_L_SDA
MGT_I2C_SCL
MGT_I2C_SDA
SENSOR_I2C_SCL
SENSOR_I2C_SDA
R220
R221
R222
R223
R214
R215
R216
R217
R218
R219
IPMB_A_SCL_FPGA
IPMB_A_SDA_FPGA
IPMB_B_SCL_FPGA
IPMB_B_SDA_FPGA
IPMB_L_SCL_FPGA
IPMB_L_SDA_FPGA
MGT_I2C_SCL_FPGA
MGT_I2C_SDA_FPGA
SENSOR_I2C_SCL_FPGA
SENSOR_I2C_SDA_FPGA
I2C MONITORING
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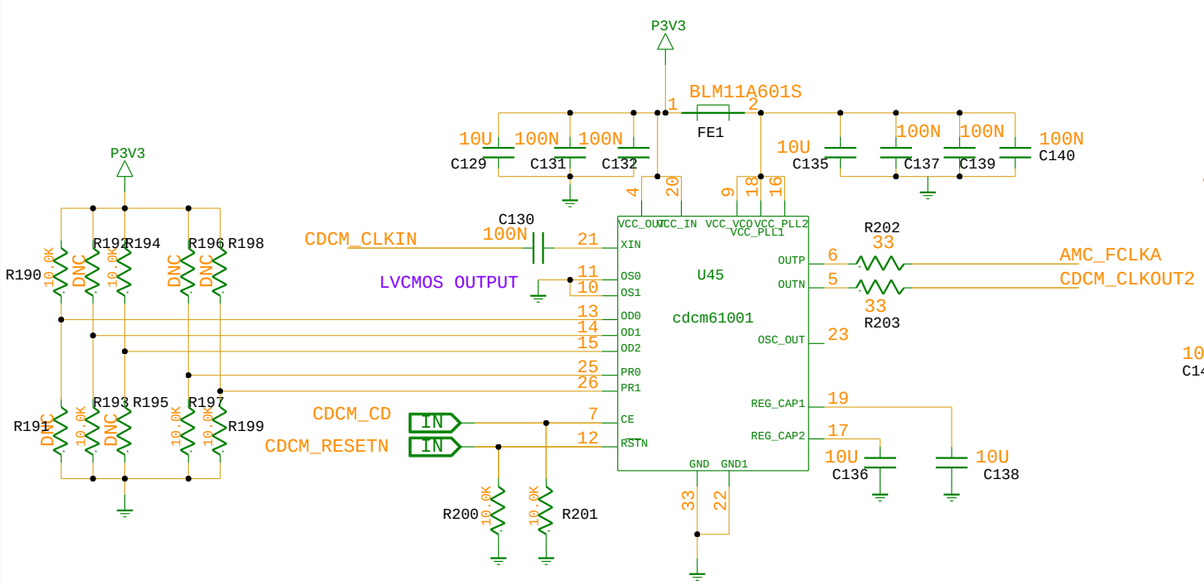
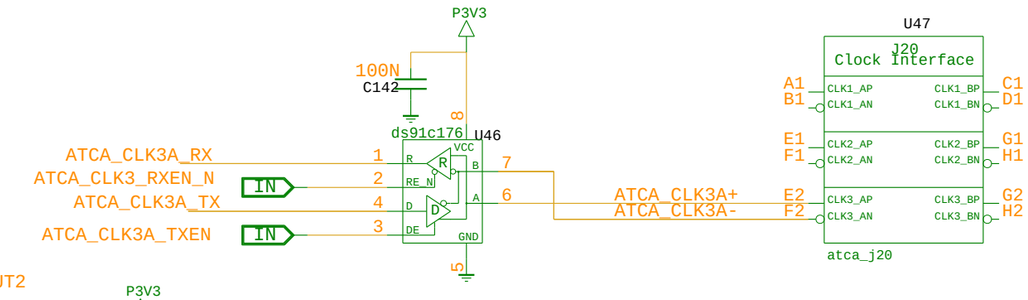
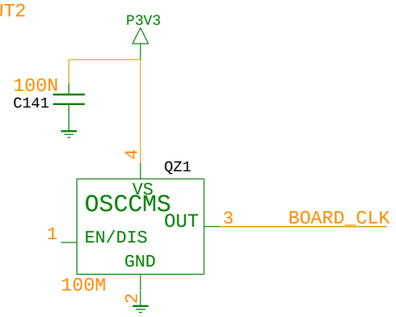
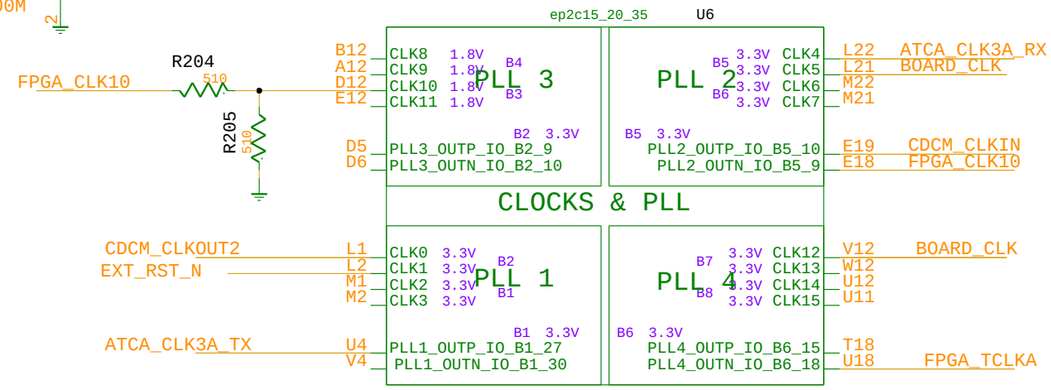
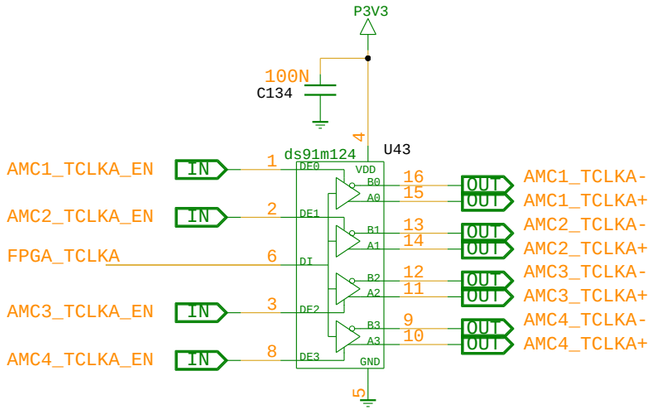
JITTER CLEANER

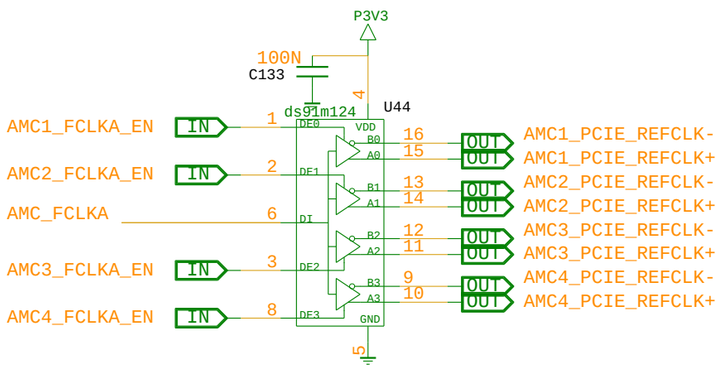












CLOCKS

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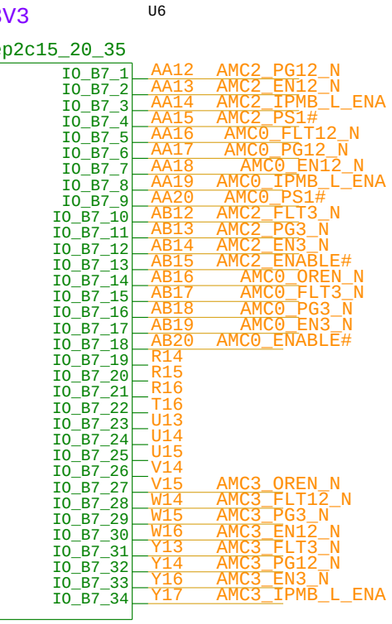

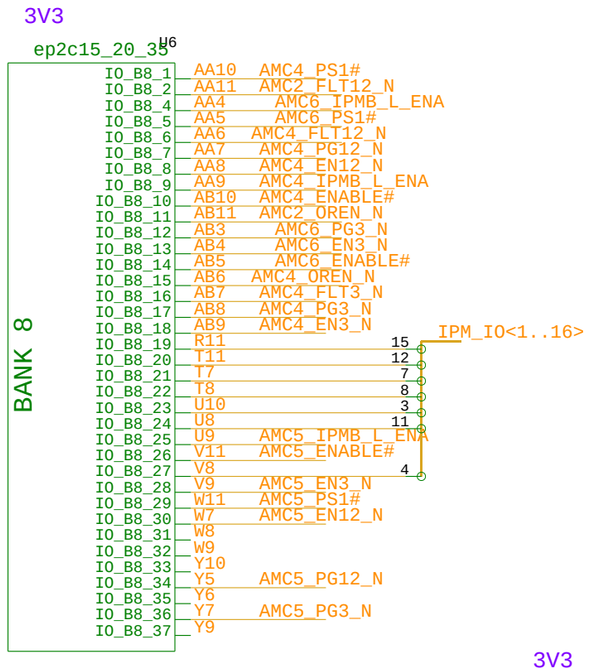

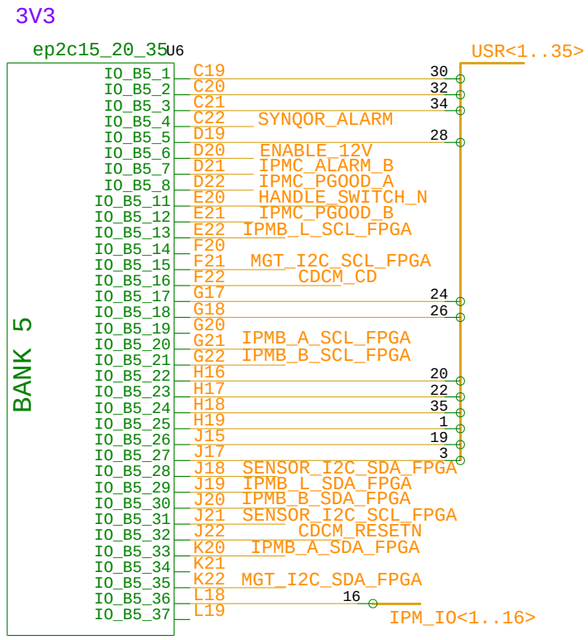

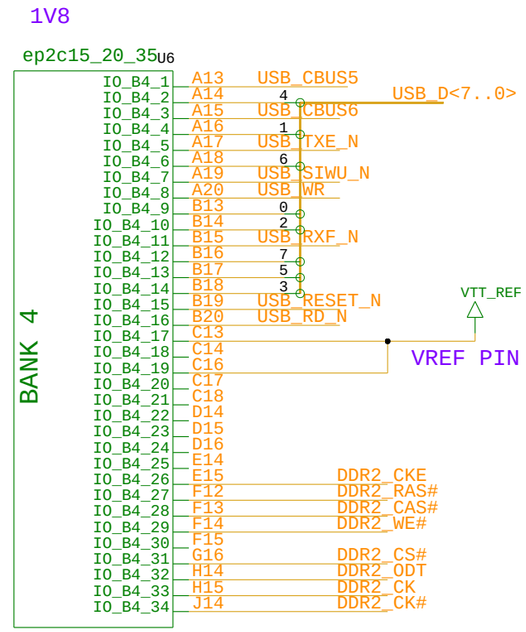

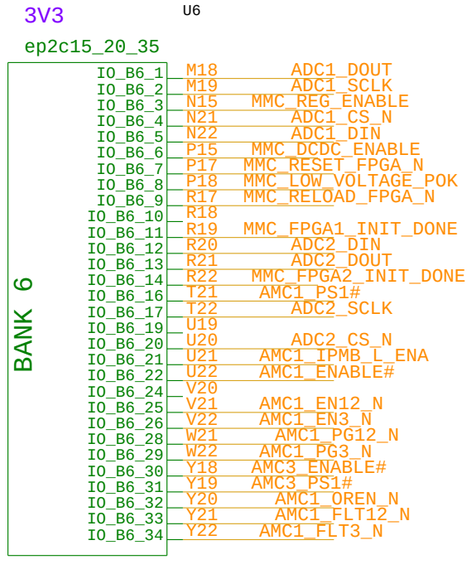

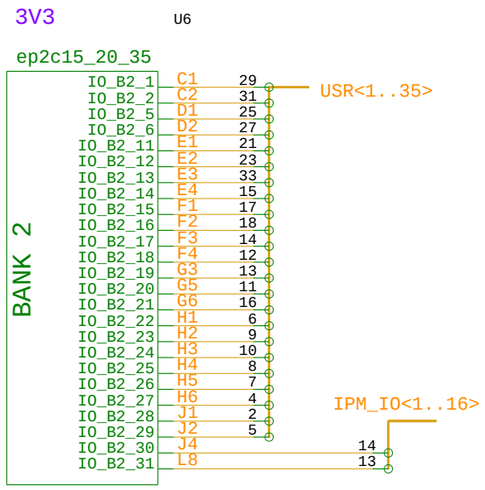

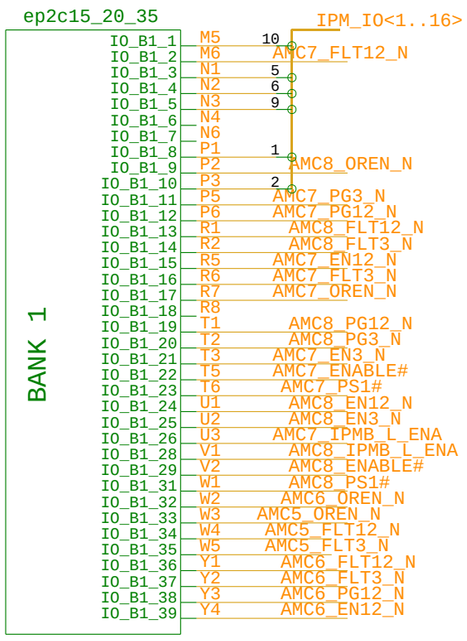

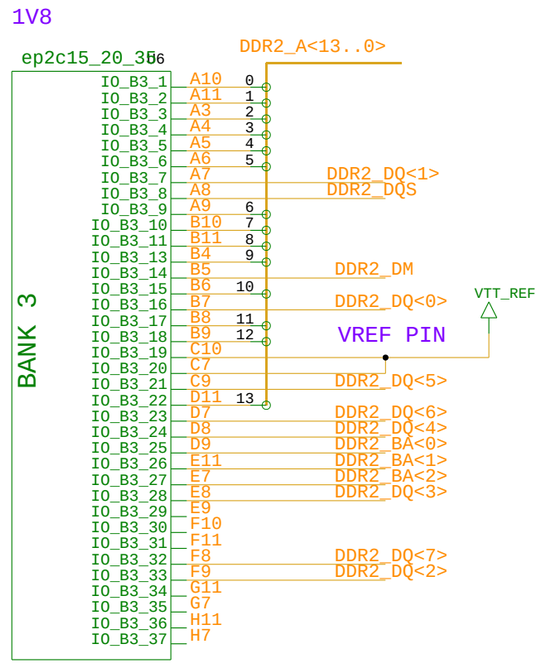

FPGA

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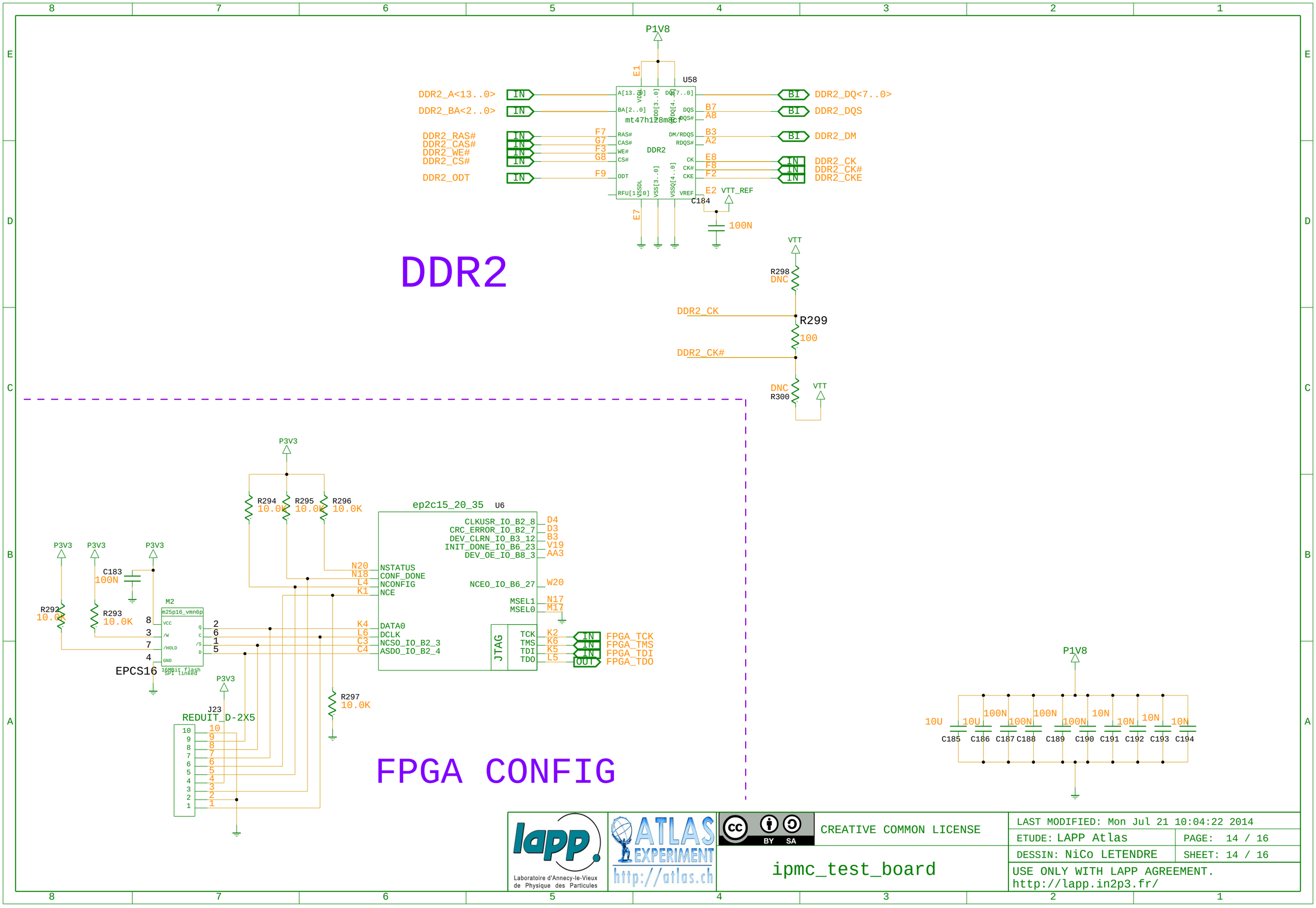

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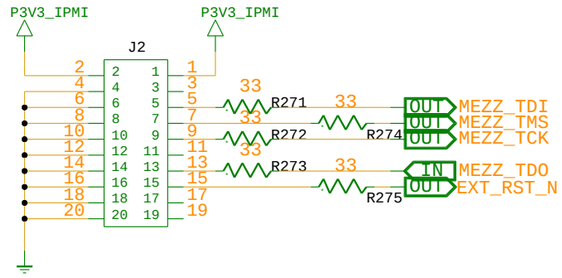
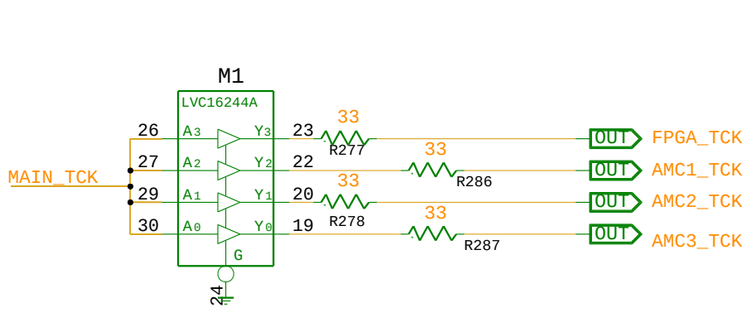
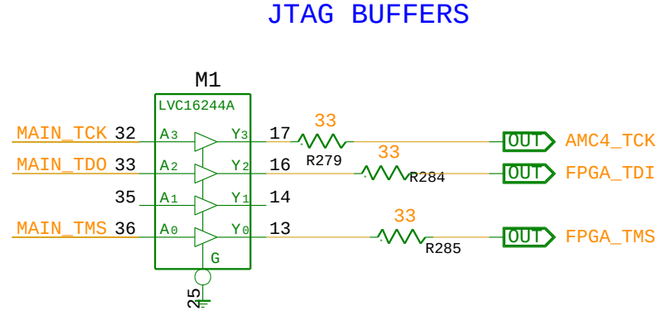
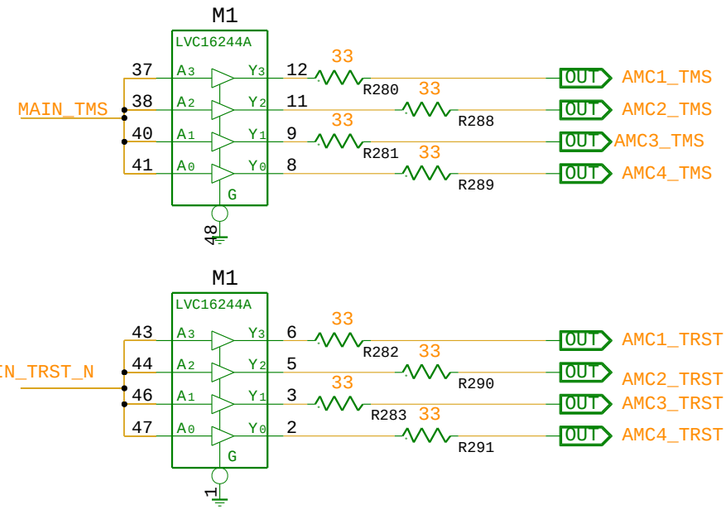


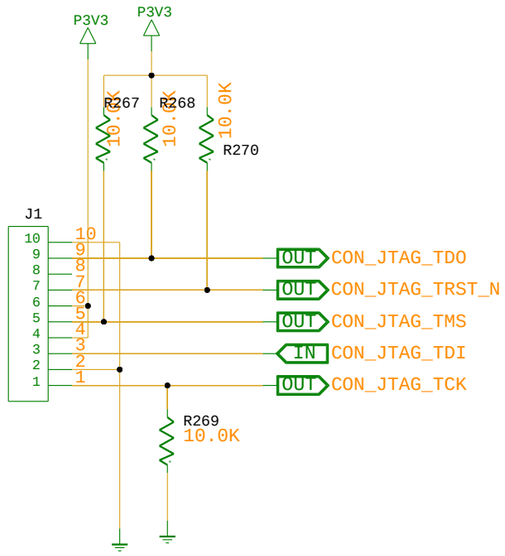
ARM STANDARD JTAG
20 PIN CONNECTOR
CONNECTED TO IPMC



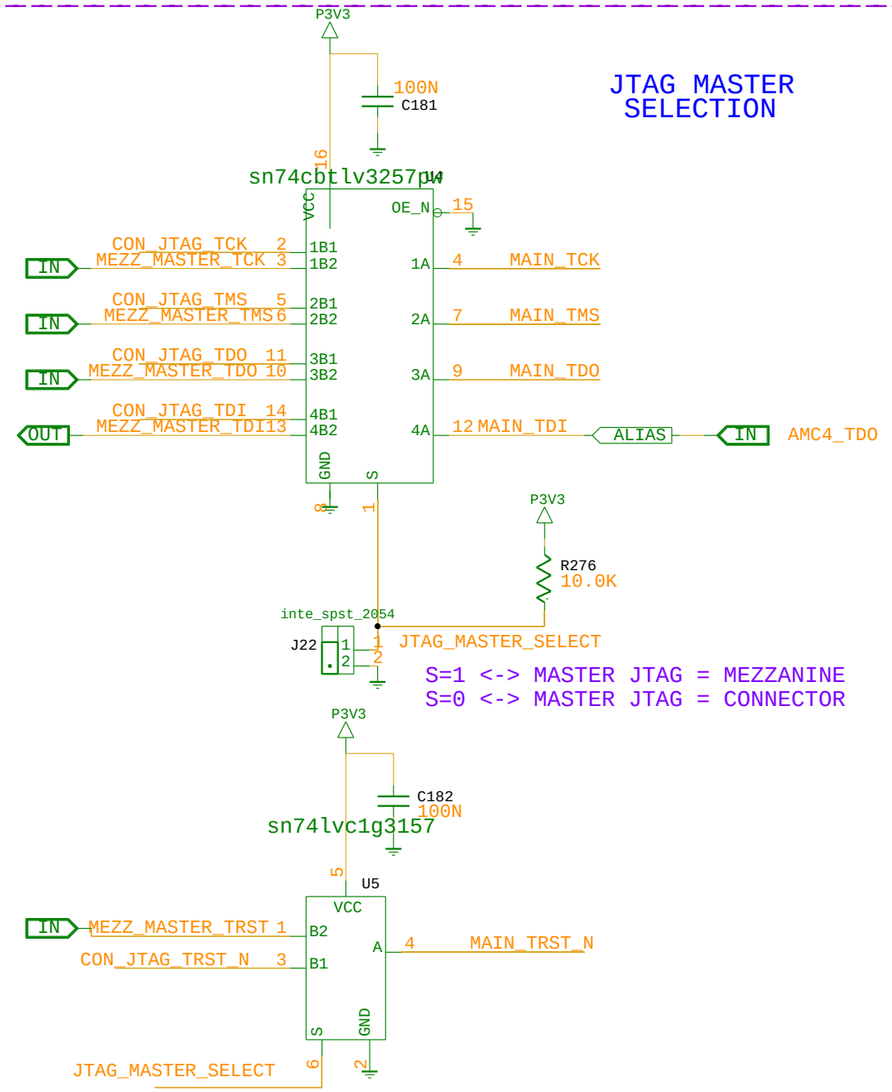
JTAG BUFFERS







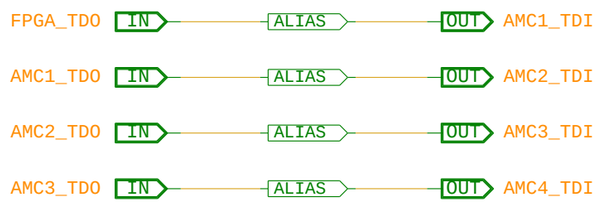
JTAG
CONNECTOR



JTAG MASTER
SELECTION

S=1 <-> MASTER JTAG = MEZZANINE
S=0 <-> MASTER JTAG = CONNECTOR

JTAG CHAIN



JTAG

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FPGA POWER-SUPPLY

FPGA SUPPLIES

P1V2

BLM11A601S

FE2

10U C196

G12 G8 H12 H13 H8 J10 J11 J12 J13 K14 K8 K9 L14 L16 L9 M14 M9 N14 N9 P10 P11 P12 P13 P14 R10 R12 T12 T15

VCCINT_1 VCCINT_2 VCCINT_3 VCCINT_4 VCCINT_5 VCCINT_6 VCCINT_7 VCCINT_8 VCCINT_9 VCCINT_10 VCCINT_11 VCCINT_12 VCCINT_13 VCCINT_14 VCCINT_15 VCCINT_16 VCCINT_17 VCCINT_18 VCCINT_19 VCCINT_20 VCCINT_21 VCCINT_22 VCCINT_23 VCCINT_24 VCCINT_25 VCCINT_26 VCCINT_27 VCCINT_28

U6 F17 E5 U17

VCCD_PLL1 VCCD_PLL2 VCCD_PLL3 VCCD_PLL4

U6

VCCA_PLL1 U7
GNDA_PLL1 V7
VCCA_PLL2 F16
GNDA_PLL2 E16
VCCA_PLL3 E6
GNDA_PLL3 F7
VCCA_PLL4 U16
GNDA_PLL4 V16

1N 100N C197 C205
1N 100N C198 C201
1N 100N C199 C202
1N 100N C200 C203

GND_PLL1_1 U5
GND_PLL1_2 V5
GND_PLL2_1 E17
GND_PLL2_2 F18
GND_PLL3_1 F5
GND_PLL3_2 F6
GND_PLL4_2 V18
GND_PLL4_1 T17

NC_23 W18
NC_22 R4
NC_21 P4
NC_20 P22
NC_19 P21
NC_18 P20
NC_17 P19
NC_16 N5
NC_15 M8
NC_14 M7
NC_13 M16
NC_12 M15
NC_11 L7
NC_10 L17
NC_9 K18
NC_8 K17
NC_7 J6
NC_6 J5
NC_5 J3
NC_4 H22
NC_3 H21
NC_2 G2
NC_1 G1

ep2c15_20_35

P3V3

P1V8

AA1 M3 P7 T4 VCCIO1_1 VCCIO1_2 VCCIO1_3 VCCIO1_4 BANK 1
B1 J7 L3 VCCIO2_1 VCCIO2_2 VCCIO2_3 BANK 2
A2 C11 C6 E10 G9 VCCIO3_1 VCCIO3_2 VCCIO3_3 VCCIO3_4 VCCIO3_5 BANK 3
A21 C12 D17 E13 G14 VCCIO4_1 VCCIO4_2 VCCIO4_3 VCCIO4_4 VCCIO4_5 BANK 4
B22 G19 J16 L20 VCCIO5_1 VCCIO5_2 VCCIO5_3 VCCIO5_4 BANK 5
AA22 M20 P16 T19 VCCIO6_1 VCCIO6_2 VCCIO6_3 VCCIO6_4 BANK 6
AB21 T14 V13 W17 Y12 VCCIO7_1 VCCIO7_2 VCCIO7_3 VCCIO7_4 VCCIO7_5 BANK 7
AB2 T9 V10 W6 Y11 VCCIO8_1 VCCIO8_2 VCCIO8_3 VCCIO8_4 VCCIO8_5 BANK 8

GND_1 GND_2 GND_3 GND_4 GND_5 GND_6 GND_7 GND_8 GND_9 GND_10 GND_11 GND_12 GND_13 GND_14 GND_15 GND_16 GND_17 GND_18 GND_19 GND_20 GND_21 GND_22 GND_23 GND_24 GND_25 GND_26 GND_27 GND_28 GND_29 GND_30 GND_31 GND_32 GND_33 GND_34 GND_35 GND_36 GND_37 GND_38 GND_39 GND_40 GND_41 GND_42 GND_43 GND_44 GND_45 GND_46 GND_47 GND_48 GND_49 GND_50 GND_51 GND_52 GND_53 GND_54 GND_55 GND_56 GND_57 GND_58 GND_59 GND_60 GND_61 GND_62 GND_63 GND_64 GND_65 GND_66 GND_67

A1 A22 AA2 AA21 AB1 AB22 B2 B21 C15 C5 C8 D10 D13 D18 F19 G10 G13 G15 G4 H10 H20 H9 J8 J9 K10 K11 K12 K13 K15 K16 K19 K3 K7 L10 L11 L12 L13 L15 M10 M11 M12 M13 M4 N10 N11 N12 N13 N16 N19 N7 N8 P8 P9 R13 R3 R9 T10 T13 T20 V17 V3 V6 W10 W13 W19 Y15 Y8

P1V2

10U C221 10U C230 10U C234 10U C239

P1V2

100N C214 100N C219 100N C225 100N C231 100N C236 100N C241 100N C244 100N C248 100N C252 100N C255

P1V2

10N C215 10N C220 10N C226 10N C232 10N C237 10N C242 10N C245 10N C249 10N C253 10N C256

P3V3

100N C206 100N C209 100N C212 100N C217 100N C223 100N C228

P3V3

100N C233 100N C238 100N C243 100N C247 100N C251 100N C254

P3V3

10N C207 10N C210 10N C213 10N C218 10N C224 10N C229

P1V8

100N C204 100N C208 100N C211 100N C216 100N C222 100N C227

P1V8

10N C235 10N C240 10N C246 10N C250

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