LAPP IPMC Mezzanine

LAPP Intelligent Platform Management Controller Mezzanine

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I. Introduction

AdvancedTCA© specification defines the hardware platform management layer which provides management capabilities to monitor, control, and assure proper operation of AdvancedTCA© boards. The hardware platform management system watches over basic health of the system, manages the power, hot swap, cooling and interconnects of ATCA board, modules or shelves. The hardware platform management is based on the Intelligent Platform Management Interface (IPMI) architecture that provides communication, management and control to the system. To comply with these specifications, ATCA boards are required to contain an Intelligent Platform Management Controller (IPMC). IPMC provides a local management for the ATCA board and communicates with the shelf manager via a dual redundant bus called IPMB (Intelligent Platform Management Bus). Fig 1 shows the management aspect of an ATCA shelf.

ATCA provides a powerful management system, but building a fully compliant ATCA board can be a lot of work for a designer. That is why this document describes a versatile custom IPM Controller. Using this IPMC allows designer to focus on their board functionalities rather than losing time developing the management system on their own. Moreover this IPMC is enhanced with added functionalities like blade JTAG manager, Ethernet configuration,(I2C bus debugger)…

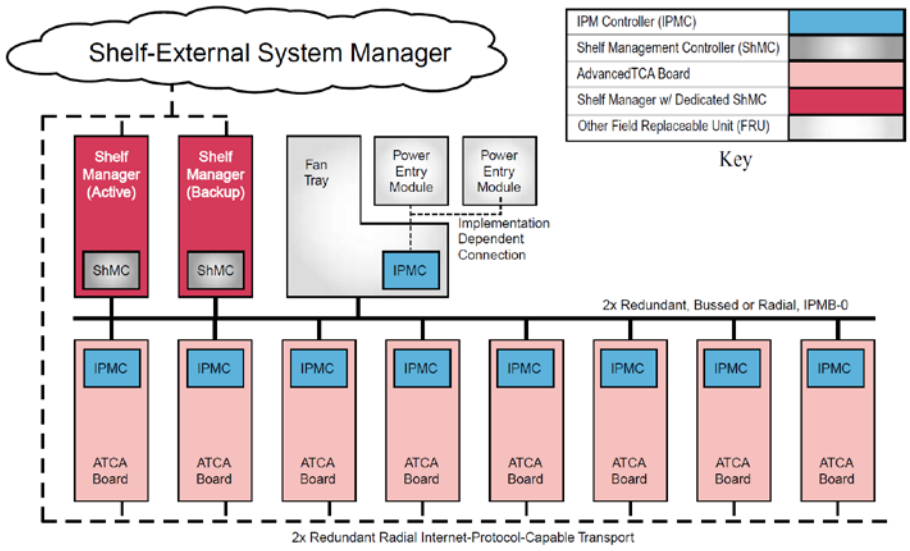

Figure 1: management aspect of an ATCA shelf

I.1. IPMC Mezzanine overview

The LAPP IPMC Mezzanine is a DDR3 VLP mini-DIMM mechanical size and therefore can be mounted vertically or horizontally on an ATCA carrier. The processing is based on two ARM microcontrollers. The IPMC microcontroller deals mainly with IPMC features and the IOIF (IO InterFace) microcontroller deals with non-IPMC features. The two µC communicates via an IMC bus (Inter Microcontrollers Communication). The Mezzanine also contains the mandatory buffers for IPMB0, a memory for event log, Ethernet PHY in order to decrease the number of peripherals needed to use the IPMC.

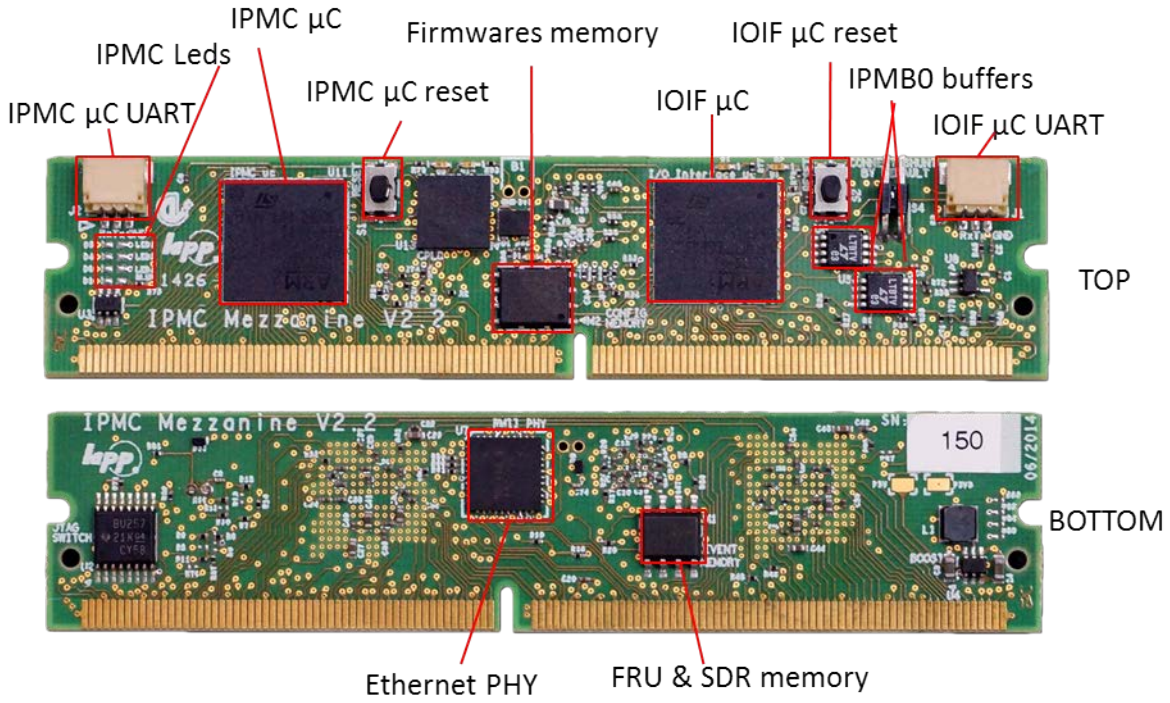

Figure 2: Overview of the LAPP IPMC Mezzanine.

II. IPMC Features

The first goal of this mezzanine is to provide the IPMC functionalities for ATCA board as described in the ATCA specification.

The mezzanine is an IPMC for ATCA board and has the following features:

- Redundant IPMB-0 interface with buffer for hot-swap capabilities
- Hot Swap management with ATCA blue led and front panel switch
- FRU LED management
- Payload power management (enable and monitoring with I2C bus)
- Hardware address detection
- ATCA board sensor management (through I2C bus)
- Management for up to 8 AMC plus one Intelligent RTM through an IPMB-L
- FRU Information and Sensor Data Record access through I2C bus
- On board Event Log
- Compliant with PICMG 3.0 R3.0 for the AdvancedTCA base specification and IPMI v1.5 and the relevant subset of IPMI v2.0
- Configurable signals for custom payload interface. (E-Keying…)

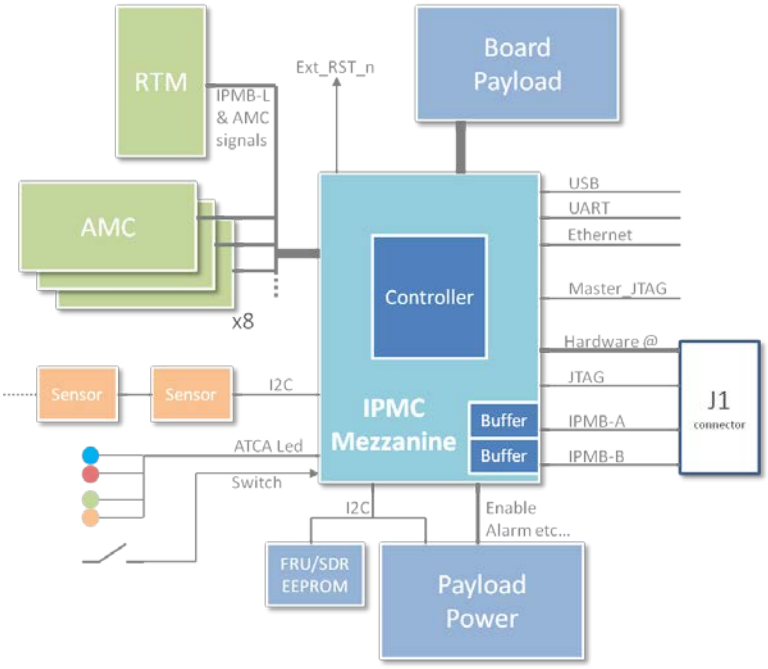

Figure 3 : IPMC architecture

II.1. Zone 1 connector

The zone 1 connector of the ATCA board provides power for the board and also the Hardware Address of the slot, the IPMB-0 bus for communication with the shelf manager and the JTAG bus.

II.1.1. IPMB-0

The IPMC mezzanine receives the IPMB-0 bus (IPMB-A and IPMB-B). The mezzanine contains two I2C buffers for buffering the IPMB-0 and to comply with the hot swap requirement. These buffers are LTC4307 from Linear Technology.

II.1.2. Hardware Address

The Hardware Address is assigned to an ATCA blade by the backplane. According to the ATCA specification the blade must de-couple each Hardware Address signal to the Logic Ground using a 1 nF capacitor and must provide a pull-up resistor of not less than 4.46 kΩ and not greater than 10.5 kΩ to VCC. See *VII.2 Hardware address* in design guidelines for more information. Below are requirements from ATCA specification:

*« REQ 2.298 The Front Board **shall** implement a 1 nF bypass capacitor to Logic Ground for each ofthe HA0, HA1, HA2, HA3, HA4, HA5, HA6, and HA7/P Backplane connections.*

*REQ 2.299 The Front Board **shall** provide a pull-up resistor of not less than 4.46 k∧ and not greater than 10.5 kΩ to an internal voltage rail appropriate for the logic circuit interfacing the HA0, HA1, HA2, HA3, HA4, HA5, HA6, and HA7/P Backplane signals. »*

II.1.3. JTAG slave

JTAG bus on the ATCA backplane is rarely used, but JTAG signals of the IPMC mezzanine can be connected to the Zone 1 connector if the shelf supports it. It is also recommended to add a JTAG connector on the blade for debugging and upgrade purposes. (See:*VIII.2 Debugging the IPMC Mezzanine Firmware, VIII.1.1 JTAG upgrade, VII.4 JTAG slave bus*)

Signal	Dir.	Pin	Description
IPMB_A_SCL	INOUT	120	IPMB-A I2C clock
IPMB_A_SDA	INOUT	121	IPMB-A I2C data
IPMB_B_SCL	INOUT	242	IPMB-B I2C clock
IPMB_B_SDA	INOUT	243	IPMB-B I2C data
HA[7..0]	IN		Hardware address (8-bits)
TCK	IN	234	JTAG TCK
TMS	IN	113	JTAG TMS
TDI	IN	235	JTAG TDI
TDO	OUT	112	JTAG TDO

Table 1: Zone 1 connector signals

II.2. Front Panel

The mezzanine receives the board insertion signal and manages the four ATCA Leds. (Mandatory Blue Led and Led1 and the optional Led2 and Led3). The blue led is driven with a +5V level to face the high voltage drop of blue leds. The mezzanine has a +5V boost regulator.

Signal	Dir.	Pin	Description
Handle_Switch	IN	224	Front panel handle switch for board insertion detection
ATCA_Blue_LED	OUT	103	Front panel blue led (mandatory). This led is driven with +5V level.
ATCA_LED1	OUT	104	Front panel LED 1 (Amber or Red, mandatory)
ATCA_LED2	OUT	105	Front panel LED 2 (Green, optional)
ATCA_LED3	OUT	106	Front panel LED 3 (Amber, optional)

Table 2: Front Panel signals

II.3. Payload Power

The IPMC mezzanine must enable the payload power only once the shelf manager has given its authorization. To fulfill ATCA standard, ATCA boards often use power management modules for power supply ORing, fuse control, inrush protection, hot swap, EMI filtering and other protections. The IPMC mezzanine receives information from the power management module, and provides an enable signal for the DC-DC payload converter. In order to support the majority of power management modules, the following signals are connected to the IPMC mezzanine:

Signal	Dir.	Pin	Description
12V_Enable	OUT	225	Enable DC-DC (-48V to 12V) payload power. This signal has a pull-down resistor on the mezzanine.
Alarm_A	IN	226	Alarm from power management module for -48V_A
Alarm_B	IN	227	Alarm from power management module for -48V_B
PowerGood_A	IN	228	Power good from power management module -48V_A
PowerGood_B	IN	229	Power good from power management module -48V_B
Mgt_I2C_SCL	OUT	220	I2C bus clock for power management module. (shared with FRU & SDR eeprom bus)
Mgt_I2C_SDA	INOUT	221	I2C bus data for power management module. (shared with FRU & SDR eeprom bus)

Table 3: Payload power signals

II.4. Reset

A reset is provided to reset the carrier. This signal can be used as the payload cold reset as defined in the ATCA base specification.

Signal	Dir.	Pin	Description
Ext_RST_n	OUT	223	IPMC Mezzanine active-low reset

Table 4: External reset signal

II.5. FRU & SDR EEPROM

This EEPROM located on the ATCA blade is connected to the mezzanine via an I2C bus and stores FRU and SDR information of the ATCA board. This I2C bus is shared with the payload and AMC management power bus.

This EEPROM must be a 256Kbit (32x8Kbit) I2C memory with a +3.3V interface at a minimum of 400 KHz clock frequency. (24xx256 from Microchip, M24256 from ST etc...) The EEPROM must be reached at address “1010000” (Pin A0 = A1 = A2 = GND).

BEWARE: The EEPROM must be powered with the ATCA 3.3V Management Power in order to be reachable even when the payload power is off.

Mgt_I2C bus pull-up resistors (4.7kΩ) are mounted on the mezzanine.

Signal	Dir.	Pin	Description
Mgt_I2C_SCL	OUT	220	I2C bus clock for FRU & SDR EEPROM (shared with management power bus)
Mgt_I2C_SDA	INOUT	221	I2C bus data for FRU & SDR EEPROM (shared with management power bus)

Table 5: FRU & SDR EEPROM signals

II.6. Board Payload

The IPMC mezzanine has signals connected to the ATCA board payload. These signals are “payload” dependent and can be used as enable / disable interface in the E-Keying process. The IPMC mezzanine has 16 signals configurable by the user (IPM_IO[0..15]). These signals are +3.3V LVTTL compatible. These IO must be used for IPMI functionalities, and mostly for e-keying.

Moreover, an UART interface allows the user to control its payload.

Signal	Dir.	Pin	Description
IPM_IO_[0..15]	INOUT		User I/O for payload interface
UART_Tx	OUT	57	UART transmit signal
UART_CTS	IN	58	UART Clear to Send signal
UART_Rx	IN	60	UART receive signal
UART_RTS	OUT	61	UART Request to Send signal

Table 6: Board Payload signals

II.7. Sensors

The IPMC mezzanine need to know the health of the ATCA board like temperature, power supply voltage etc… in order to inform the shelf manager. The interface for the sensors or Analog to Digital Converters (ADC) is an I2C bus as many sensors or ADCs are available with an I2C interface.

Sensor I2C bus pull-up resistors (4.7kΩ) are mounted on the mezzanine.

Signal	Dir.	Pin	Description
Sensor_SCL	OUT	183	I2C bus clock for sensor interface
Sensor_SDA	INOUT	184	I2C bus data for sensor interface

Table 7: I2C sensor signals

II.8. AMC and RTM

From the shelf manager point of view, AMC and RTM are viewed through the ATCA board IPMC. AMC and Intelligent RTM (IRTM) are managed by a Module Management Controller (MMC).

MMCs and IPMC are linked together with an IPMB-L (Local I2C bus). An ATCA board can support up to eight AMCs and one RTM. For that the IPMC mezzanine can support up to nine modules.

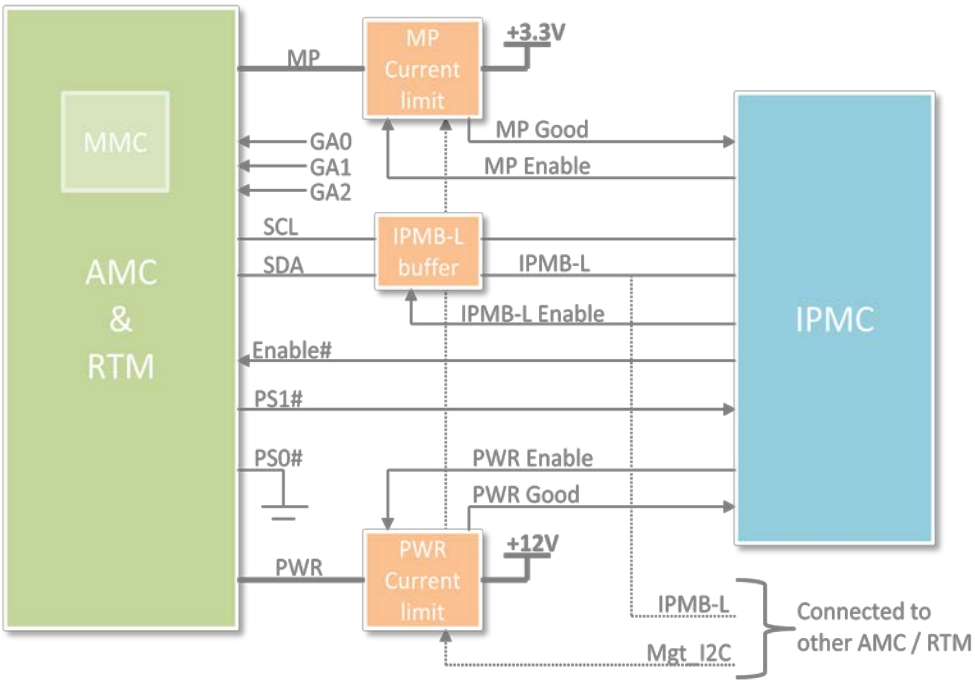

Figure 4: AMC management architecture

Figure 3 shows the AMC management architecture on an ATCA board. The management bus IPMB-L is chained to all AMCs. This bus is controlled for each AMC by a buffer that can be enables or disabled by the IPMC in order to isolate the AMC. The IPMC receives the PS1# signal indicating that an AMC is connected, and asserts the Enable# signal.

The IPMC must also control the power for AMC. It must activate or disable power supplies and check that the AMC does not draw too much current on the Management Power (MP) supply and on the Payload Power (PWR) supply. Several devices are available to deal with the power interface like TPS2358, TPS2359, TPS2458, TPS2459 from Texas Instrument or LTC4222, LTC4223, LTC4242 from Linear Technology. Some devices (TPS2359, TPS2459, TLC4222) can have an I2C bus for current limit programming and other functionalities. These components share the same I2C bus as the payload power management bus and the FRU and SDR EEPROM bus (Mgt_I2C_SCL and Mgt_I2C_SDA).

IPMB-L and Mgt_I2C bus pull-up resistors (4.7kΩ) are mounted on the mezzanine. IPMB-L is foreseen to be used in a bused architecture on the carrier.

The following table shows the IPMC mezzanine signals common to all AMC:

Signal	Dir.	Pin	Description
IPMB-L_SCL	INOUT	168	IPMB-L I2C clock
IPMB-L_SDA	INOUT	169	IPMB-L I2C data
Mgt_I2C_SCL	OUT	220	I2C bus clock for power management module (same signal as payload power and FRU eeprom)
Mgt_I2C_SDA	INOUT	221	I2C bus data for power management module (same signal as payload power and FRU eeprom)

Table 8: IPMB_L and AMC power control signals

The following table shows the IPMC mezzanine signals going to each AMC: ("x" is the AMC site number from 0 to 8)

Signal	Dir.	Description
To AMC		
PS1#_x	IN	Low level indicates that the AMC module is inserted in the carrier.
Enable#_x	OUT	When active, indicates to the AMC module that it is fully inserted in the carrier.
To IPMB-L and AMC power management		
IPMB-L_Enable_x	OUT	Connect AMC to the IPMB-L bus.
MP_Enable_x	OUT	Activate the Management Power (+3.3V to AMC)
PWR_Enable_x	OUT	Activate the module Payload Power (+12V to AMC).
MP_Good_x	IN	Asserted when the Management Power voltage are within the required levels.
PWR_Good_x	IN	Asserted when the Payload Power voltage are within the required levels.
MP_Fault_x	IN	Asserted when the Management Power current reaches the limit
PWR_Fault_x	IN	Asserted when the Payload Power current reaches the limit
PWR_ORing_x	OUT	Optional – for 12V redundancy

Table 9: IPMC to AMCs and RTM signals

Except for PS1# and Enable#, signals in the previous table do not have an active level specification. Since many devices for AMC power management exist, these signals can be active high or low. The active level is selected by "software" in the IPMC mezzanine software.

III. NON-IPMC features

The mezzanine has non-impc features that can be useful for an ATCA board designer. One must note that the following features are **not related to IPMI** functionalities.

- Ethernet link & USB link.
- JTAG Master. The mezzanine can act as a JTAG master through Ethernet for the ATCA board. This feature can be used to load firmware for digital devices located on the ATCA board or for debugging purpose.
- User IO. The user can drive some mezzanines IO. For example, the user can drive these IO through the Ethernet link.

III.1. Ethernet

The IPMC mezzanine can be connected to ATCA Base Interface. This communication allows using the mezzanine for different functions:

- JTAG master, for motherboard firmware upgrade for example
- User configuration (with USR pin) through Ethernet
- Mezzanine firmware upgrade: As there is no standard for IPMC firmware upgrade, for the moment the Ethernet connection is the only way to upgrade the mezzanine firmware.

The first version of the mezzanine has a 100Mbit/s Ethernet link. But for future version, a 1Gbit/s link is foreseen.

100Mbit/s link:

Signal	Dir.	Pin	Description
Eth_Tx+	OUT	171	Tx+ of the Ethernet PHY
Eth_Tx-	OUT	172	Tx- of the Ethernet PHY
Eth_Rx+	IN	174	Rx+ of the Ethernet PHY
Eth_Rx-	IN	175	Rx- of the Ethernet PHY

Table 10: 100Mbit/s Ethernet interface signals

1Gbit/s link:

Signal	Dir.	Pin	Description
Gb_A+	INOUT	171	A+ of the Gigabit Ethernet PHY
Gb_A-	INOUT	172	A- of the Gigabit Ethernet PHY
Gb_B+	INOUT	174	B+ of the Gigabit Ethernet PHY
Gb_B-	INOUT	175	B- of the Gigabit Ethernet PHY
Gb_C+	INOUT	177	C+ of the Gigabit Ethernet PHY
Gb_C-	INOUT	178	C- of the Gigabit Ethernet PHY
Gb_D+	INOUT	180	D+ of the Gigabit Ethernet PHY
Gb_D-	INOUT	181	D- of the Gigabit Ethernet PHY

Table 11: Gigabit Ethernet signals

III.2. JTAG Master

The IPMC mezzanine acts as a bridge between the Ethernet link and the JTAG bus. This configuration allows the user to control the ATCA board JTAG bus through Ethernet. This way, the user can use JTAG functionalities like firmware upgrade or others.

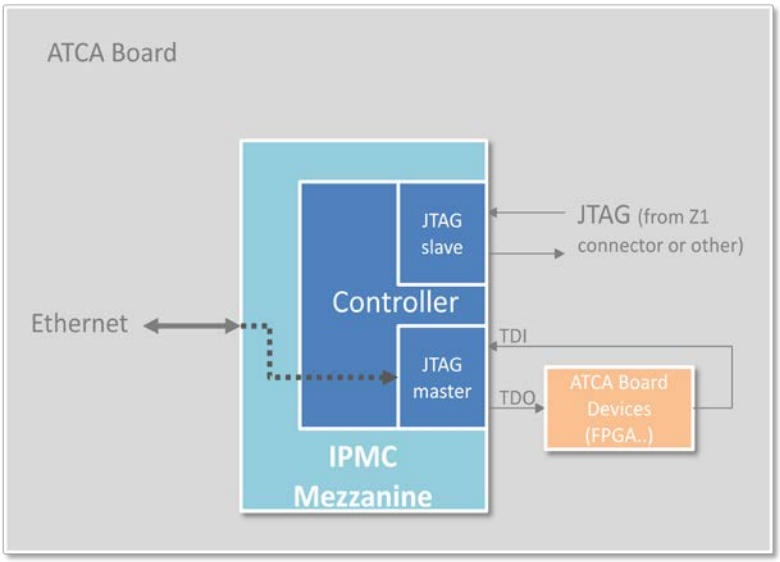

Figure 5: IPMC mezzanine JTAG functionality

Signal	Dir.	Pin	Description
Master_TCK	OUT	231	Master JTAG Test Clock signal
Master_TMS	OUT	110	Master JTAG Test Mode Select signal
Master_TDI	IN	232	Master JTAG Test Data In signal
Master_TDO	OUT	109	Master JTAG Test Data Out signal
Master_TRST	OUT	108	Master JTAG Test ReSeT signal

Table 12: JTAG Master signals

III.3. User IO

The mezzanine provides 35 IO for user purposes. These IO can be used for instance to interface some on-board functionalities with Ethernet or USB. These IO are controlled by user software implemented in the mezzanine microcontroller. This user software **MUST NOT** use IPMI information to control these IO. This means that these IO have no relationship with IPMI functionalities. (IPM_IO must be used for IPMI functionalities)

Signal	Dir.	Pin	Description
USR_[0..34]	INOUT		IO for user purposes

Table 13: User Configuration signals

III.4. Debug

In the development phase of the IPMC Mezzanine, it is important to have tools for debugging purposes. For that the UART can be routed on the ATCA board to a console and a USB bus is also provided.

III.5. USB

The IMPC Mezzanine acts as a USB Full Speed peripheral device.

Signal	Dir.	Pin	Description
USB_Vbus	IN	99	USB Vbus +5V from USB
USB_Dp	INOUT	100	USB data +
USB_Dn	INOUT	101	USB data -

Table 14: USB signals

IV. Mechanical

The IPMC mezzanine is design to minimize its area on the ATCA board. The solution is to plug the mezzanine in a vertical position on the carrier. This way the area is minimized and if the mezzanine is inserted parallel to the backplane, connectors the airflow is not obstructed.

DDRx form factor can be a good mechanical standard for the IPMC mezzanine. The maximum height for a mezzanine on a ATCA board is 21.33mm. The DDRx defines VLP (Very Low Profile) size with enough available IO for our application. This form factor is interesting for our application:

IV.1. DDR3 VLP Mini-DIMM

Width: 82mm – Height: 18.29mm – Depth: 5.6mm

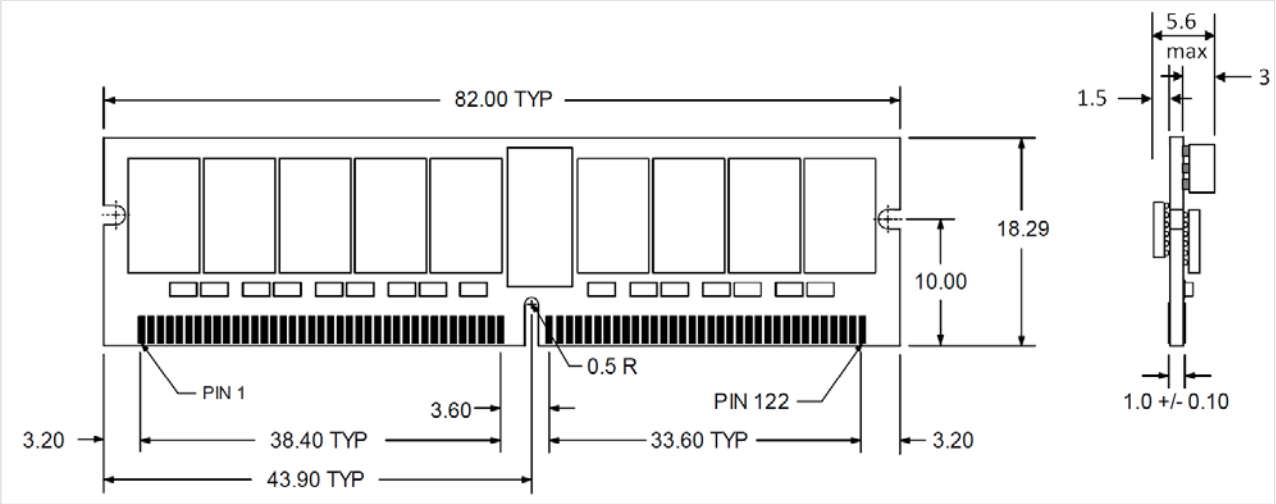

Figure 6: DDR3 VLP Mini-DIMM form facor

This form factor has 244 pins. One possible mated receptacle is ref: 877823003 from Molex.

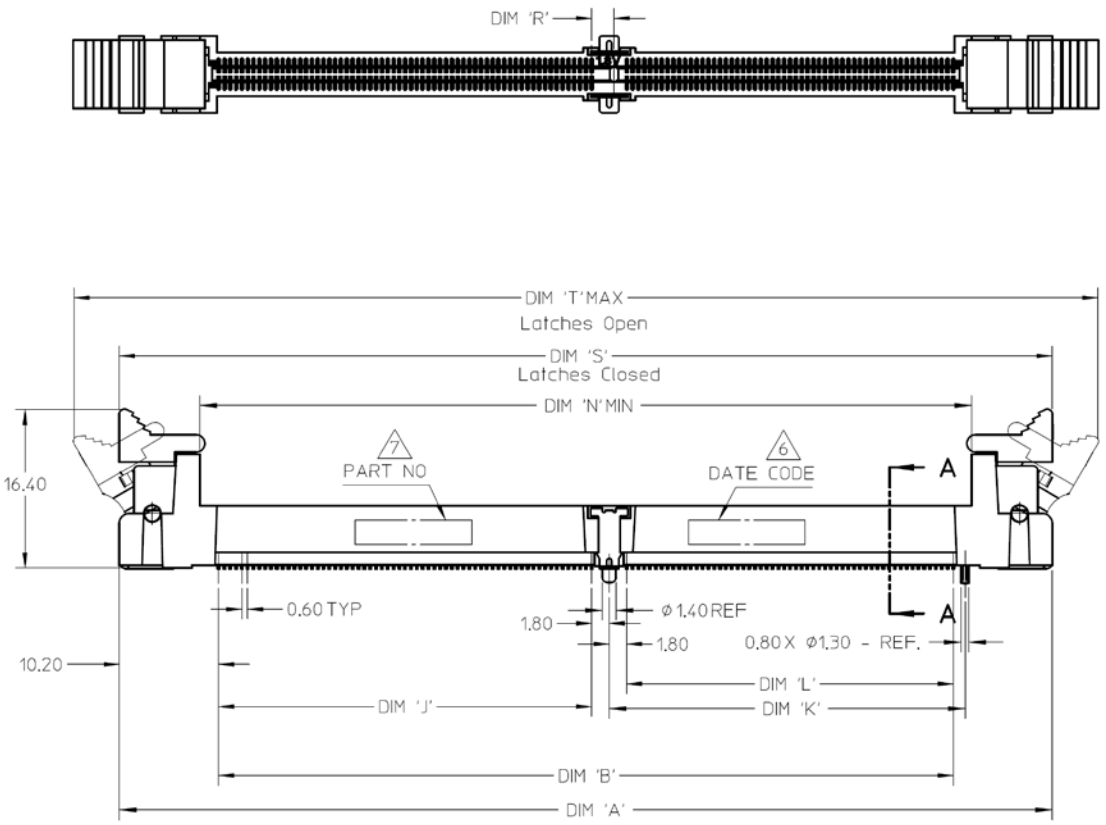

Figure 7: DDR3 VLP Mini-DIMM receptacle

V. Pin out

The IPMC mezzanine is power by a +3.3V power supply by the VCC pins. All the I/O (except the Ethernet interface and Blue Led) are +3.3V LVTTL compatible. (See Electrical specifications)

IPMC mezzanine pinout:

Pin	Frontside	Dir	Pin	Backside	Dir
1	GND	-	123	GND	-
2	PS1#_0	I	124	PS1#_1	I
3	Enable#_0	O	125	Enable#_1	O
4	IPMB-L_Enable_0	O	126	IPMB-L_Enable_1	O
5	MP_Enable_0	O	127	MP_Enable_1	O
6	PWR_Enable_0	O	128	PWR_Enable_1	O
7	MP_Good_0	I	129	MP_Good_1	I
8	PWR_Good_0	I	130	PWR_Good_1	I
9	MP_Fault_0	I	131	MP_Fault_1	I
10	PWR_Fault_0	I	132	PWR_Fault_1	I
11	PWR_ORing_0	O	133	PWR_ORing_1	O
12	GND	-	134	GND	-
13	PS1#_2	I	135	PS1#_3	I
14	Enable#_2	O	136	Enable#_3	O
15	IPMB-L_Enable_2	O	137	IPMB-L_Enable_3	O
16	MP_Enable_2	O	138	MP_Enable_3	O
17	PWR_Enable_2	O	139	PWR_Enable_3	O
18	MP_Good_2	I	140	MP_Good_3	I
19	PWR_Good_2	I	141	PWR_Good_3	I
20	MP_Fault_2	I	142	MP_Fault_3	I
21	PWR_Fault_2	I	143	PWR_Fault_3	I
22	PWR_ORing_2	O	144	PWR_ORing_3	O
23	GND	-	145	GND	-
24	PS1#_4	I	146	PS1#_5	I
25	Enable#_4	O	147	Enable#_5	O
26	IPMB-L_Enable_4	O	148	IPMB-L_Enable_5	O
27	MP_Enable_4	O	149	MP_Enable_5	O
28	PWR_Enable_4	O	150	PWR_Enable_5	O
29	MP_Good_4	I	151	MP_Good_5	I
30	PWR_Good_4	I	152	PWR_Good_5	I^{pu}
31	MP_Fault_4	I	153	MP_Fault_5	I
32	PWR_Fault_4	I	154	PWR_Fault_5	I
33	PWR_ORing_4	O	155	PWR_ORing_5	O
34	GND	-	156	GND	-
35	PS1#_6	I	157	PS1#_7	I
36	Enable#_6	O	158	Enable#_7	O
37	IPMB-L_Enable_6	O	159	IPMB-L_Enable_7	O
38	MP_Enable_6	O	160	MP_Enable_7	O
39	PWR_Enable_6	O	161	PWR_Enable_7	O
40	MP_Good_6	I	162	MP_Good_7	I
41	PWR_Good_6	I	163	PWR_Good_7	I
42	MP_Fault_6	I	164	MP_Fault_7	I
43	PWR_Fault_6	I	165	PWR_Fault_7	I
44	PWR_ORing_6	O	166	PWR_ORing_7	O
45	GND	-	167	GND	-
46	PS1#_8	I	168	IPMB-L_SCL	I/O^{pu}
47	Enable#_8	O	169	IPMB-L_SDA	I/O^{pu}
48	IPMB-L_Enable_8	O	170	GND	-
49	MP_Enable_8	O	171	Eth_Tx+/Gb_A+	I/O
50	PWR_Enable_8	O	172	Eth_Tx-/Gb_A-	I/O
51	MP_Good_8	I	173	GND	
52	PWR_Good_8	I	174	Eth_Rx+/Gb_B+	I/O
53	MP_Fault_8	I	175	Eth_Rx-/Gb_B-	I/O
54	PWR_Fault_8	I	176	GND	
55	PWR_ORing_8	O	177	Gb_C+	I/O
56	GND	-	178	Gb_C-	I/O
57	Uart_Tx	O	179	GND	
58	Uart_CTS	I	180	Gb_D+	I/O
59	GND	-	181	Gb_D-	I/O
60	Uart_Rx	I	182	GND	
61	Uart_RTS	O	183	Sensor_SCL	O^{pu}
62	GND	-	184	Sensor_SDA	I/O^{pu}

Table 15: IPMC mezzanine pinout (Front side pin 1 to 62, Back side pin 123 to 184). pu=pull up 4.7kΩ resistor on mezzanine, pd=pull down 4.7kΩ resistor on mezzanine.

Pin	Frontside	Dir	Pin	Backside	Dir
63	IPM_IO_0	I/O	185	GND	-
64	IPM_IO_1	I/O	186	IPM_IO_2	I/O
65	VCC	-	187	IPM_IO_3	I/O
KEY					
66	IPM_IO_4	I/O	188	IPM_IO_6	I/O
67	IPM_IO_5	I/O	189	IPM_IO_7	I/O
68	VCC	-	190	GND	-
69	IPM_IO_8	I/O	191	IPM_IO_10	I/O
70	IPM_IO_9	I/O	192	IPM_IO_11	I/O
71	VCC	-	193	GND	-
72	IPM_IO_12	I/O	194	IPM_IO_14	I/O
73	IPM_IO_13	I/O	195	IPM_IO_15	I/O
74	VCC	-	196	GND	-
75	USR_0	I/O	197	USR_2	I/O
76	USR_1	I/O	198	USR_3	I/O
77	VCC	-	199	GND	-
78	USR_4	I/O	200	USR_8	I/O
79	USR_5	I/O	201	USR_7	I/O
80	VCC	-	202	GND	-
81	USR_8	I/O	203	USR_10	I/O
82	USR_9	I/O	204	USR_11	I/O
83	VCC	-	205	GND	-
84	USR_12	I/O	206	USR_14	I/O
85	USR_13	I/O	207	USR_15	I/O
86	VCC	-	208	GND	-
87	USR_16	I/O	209	USR_18	I/O
88	USR_17	I/O	210	USR_19	I/O
89	GND	-	211	GND	-
90	USR_20	I/O	212	USR_21	I/O
91	USR_22	I/O	213	USR_23	I/O

Pin	Frontside	Dir	Pin	Backside	Dir
92	USR_24	I/O	214	USR_25	I/O
93	USR_26	I/O	215	USR_27	I/O
94	USR_28	I/O	216	USR_29	I/O
95	USR_30	-	217	USR_31	I/O
96	USR_32	I/O	218	USR_33	I/O
97	GND	-	219	GND	-
98	USR_34	I/O	220	Mgt_I2C_SCL	O^{pu}
99	USB_Vbus	I	221	Mgt_I2C_SDA	I/O^{pu}
100	USB_Dp	I/O^{pu}	222	GND	-
101	USB_Dn	I/O^{pu}	223	Ext_RST_n	O^{pu}
102	GND	-	224	Handle switch	I
103	ATCA_Blue_LED	O^{+5V}	225	12V_Enable	O^{pd}
104	ATCA_LED1	O	226	Alarm_A	I
105	ATCA_LED2	O	227	Alarm_B	I
106	ATCA_LED3	O	228	PowerGood_A	I
107	GND	-	229	PowerGood_B	I
108	Master_TRST	O^{pu}	230	GND	-
109	Master_TD0	O^{pu}	231	Master_TCK	O^{pd}
110	Master_TMS	O^{pu}	232	Master_TDI	I^{pu}
111	GND	-	233	GND	-
112	TDO	O^{pu}	234	TCK	I^{pd}
113	TMS	I^{pu}	235	TDI	I^{pu}
114	GND	-	236	GND	-
115	HA0	I	237	HA1	I
116	HA2	I	238	HA3	I
117	HA4	I	239	HA5	I
118	HA6	I	240	HA7	I
119	GND	-	241	GND	-
120	IPMB-A_SCL	I/O	242	IPMB-B_SCL	I/O
121	IPMB-A_SDA	I/O	243	IPMB-B_SDA	I/O
122	GND	-	244	GND	-

Table 16: IPMC mezzanine pinout (Front side pin 63 to 122, Back side pin 185 to 244). pu=pull up 4.7kΩ resistor on mezzanine, pd=pull down 4.7kΩ resistor on mezzanine.

IPMC Mezzanine pinout with pin definition.

IPMC to AMC				
Nbr	Name	Dir	µC	Description
1	GND			
2	PS1#_0	IN	IPMC	Low level indicates that the AMC module is inserted in the carrier.
3	Enable#_0	OUT	IPMC	When active, indicates to the AMC module that it is fully inserted in the carrier.
4	IPMB-L_Enable_0	OUT	IPMC	Connect AMC to the IPMB-L bus.
5	MP_Enable_0	OUT	IPMC	Activate the Management Power (+3.3V to AMC)
6	PWR_Enable_0	OUT	IPMC	Activate the module Payload Power (+12V to AMC).
7	MP_Good_0	IN	IPMC	Asserted when the Management Power voltage are within the required levels.
8	PWR_Good_0	IN	IPMC	Asserted when the Payload Power voltage are within the required levels.
9	MP_Fault_0	IN	IPMC	Asserted when the Management Power current reaches the limit
10	PWR_Fault_0	IN	IPMC	Asserted when the Payload Power current reaches the limit
11	PWR_ORing_0	OUT	IPMC	Optional – for 12V redundancy
12	GND			
13	PS1#_2	IN	IPMC	Low level indicates that the AMC module is inserted in the carrier.
14	Enable#_2	OUT	IPMC	When active, indicates to the AMC module that it is fully inserted in the carrier.
15	IPMB-L_Enable_2	OUT	IPMC	Connect AMC to the IPMB-L bus.
16	MP_Enable_2	OUT	IPMC	Activate the Management Power (+3.3V to AMC)
17	PWR_Enable_2	OUT	IPMC	Activate the module Payload Power (+12V to AMC).
18	MP_Good_2	IN	IPMC	Asserted when the Management Power voltage are within the required levels.
19	PWR_Good_2	IN	IPMC	Asserted when the Payload Power voltage are within the required levels.
20	MP_Fault_2	IN	IPMC	Asserted when the Management Power current reaches the limit
21	PWR_Fault_2	IN	IPMC	Asserted when the Payload Power current reaches the limit
22	PWR_ORing_2	OUT	IPMC	Optional – for 12V redundancy
23	GND			
24	PS1#_4	IN	IPMC	Low level indicates that the AMC module is inserted in the carrier.
25	Enable#_4	OUT	IPMC	When active, indicates to the AMC module that it is fully inserted in the carrier.
26	IPMB-L_Enable_4	OUT	IPMC	Connect AMC to the IPMB-L bus.
27	MP_Enable_4	OUT	IPMC	Activate the Management Power (+3.3V to AMC)
28	PWR_Enable_4	OUT	IPMC	Activate the module Payload Power (+12V to AMC).
29	MP_Good_4	IN	IPMC	Asserted when the Management Power voltage are within the required levels.
30	PWR_Good_4	IN	IPMC	Asserted when the Payload Power voltage are within the required levels.
31	MP_Fault_4	IN	IPMC	Asserted when the Management Power current reaches the limit
32	PWR_Fault_4	IN	IPMC	Asserted when the Payload Power current reaches the limit
33	PWR_ORing_4	OUT	IPMC	Optional – for 12V redundancy
34	GND			
35	PS1#_6	IN	IPMC	Low level indicates that the AMC module is inserted in the carrier.
36	Enable#_6	OUT	IPMC	When active, indicates to the AMC module that it is fully inserted in the carrier.
37	IPMB-L_Enable_6	OUT	IPMC	Connect AMC to the IPMB-L bus.
38	MP_Enable_6	OUT	IPMC	Activate the Management Power (+3.3V to AMC)
39	PWR_Enable_6	OUT	IPMC	Activate the module Payload Power (+12V to AMC).
40	MP_Good_6	IN	IPMC	Asserted when the Management Power voltage are within the required levels.
41	PWR_Good_6	IN	IPMC	Asserted when the Payload Power voltage are within the required levels.
42	MP_Fault_6	IN	IPMC	Asserted when the Management Power current reaches the limit
43	PWR_Fault_6	IN	IPMC	Asserted when the Payload Power current reaches the limit
44	PWR_ORing_6	OUT	IPMC	Optional – for 12V redundancy
45	GND			
46	PS1#_8	IN	IPMC	Low level indicates that the AMC module is inserted in the carrier.
47	Enable#_8	OUT	IPMC	When active, indicates to the AMC module that it is fully inserted in the carrier.
48	IPMB-L_Enable_8	OUT	IPMC	Connect AMC to the IPMB-L bus.
49	MP_Enable_8	OUT	IPMC	Activate the Management Power (+3.3V to AMC)
50	PWR_Enable_8	OUT	IPMC	Activate the module Payload Power (+12V to AMC).
51	MP_Good_8	IN	IPMC	Asserted when the Management Power voltage are within the required levels.
52	PWR_Good_8	IN	IPMC	Asserted when the Payload Power voltage are within the required levels.
53	MP_Fault_8	IN	IPMC	Asserted when the Management Power current reaches the limit
54	PWR_Fault_8	IN	IPMC	Asserted when the Payload Power current reaches the limit
55	PWR_ORing_8	OUT	IPMC	Optional – for 12V redundancy
56	GND			
57	Uart_Tx	OUT	IOIF	UART transmit signal
58	Uart_CTS	IN	IOIF	UART Clear To Send signal
59	GND			
60	Uart_Rx	IN	IOIF	UART receive signal
61	Uart_RTS	OUT	IOIF	UART Request To Send signal
62	GND			
63	IPM_IO_0	INOUT	IOIF	IPM I/O 0 for payload interface
64	IPM_IO_1	INOUT	IOIF	IPM I/O 1 for payload interface
65	VCC			
66	IPM_IO_4	INOUT	IOIF	IPM I/O 4 for payload interface
67	IPM_IO_5	INOUT	IOIF	IPM I/O 5 for payload interface

68	VCC			
69	IPM_IO_8	INOUT	IOIF	IPM I/O 8 for payload interface
70	IPM_IO_9	INOUT	IOIF	IPM I/O 9 for payload interface
71	VCC			
72	IPM_IO_12	INOUT	IOIF	IPM I/O 12 for payload interface
73	IPM_IO_13	INOUT	IOIF	IPM I/O 13 for payload interface
74	VCC			
75	USR_0	INOUT	IOIF	User IO pin 0
76	USR_1	INOUT	IOIF	User IO pin 1
77	VCC			
78	USR_4	INOUT	IOIF	User IO pin 4
79	USR_5	INOUT	IOIF	User IO pin 5
80	VCC			
81	USR_8	INOUT	IOIF	User IO pin 8
82	USR_9	INOUT	IOIF	User IO pin 9
83	VCC			
84	USR_12	INOUT	IOIF	User IO pin 12
85	USR_13	INOUT	IOIF	User IO pin 13
86	VCC			
87	USR_16	INOUT	IOIF	User IO pin 16
88	USR_17	INOUT	IOIF	User IO pin 17
89	GND			
90	USR_20	INOUT	IOIF	User IO pin 20
91	USR_22	INOUT	IOIF	User IO pin 22
92	USR_24	INOUT	IOIF	User IO pin 24
93	USR_26	INOUT	IOIF	User IO pin 26
94	USR_28	INOUT	IOIF	User IO pin 28
95	USR_30	INOUT	IOIF	User IO pin 30
96	USR_32	INOUT	IOIF	User IO pin 32
97	GND			
98	USR_34	INOUT	IOIF	User IO pin 34
99	USB_Vbus	IN	IOIF	USB Vbus +5V from USB
100	USB_Dp	INOUT^{pu}	IOIF	USB data +
101	USB_Dn	INOUT^{pu}	IOIF	USB data -
102	GND			
103	ATCA_Blue_LED	OUT^{+5V}	IPMC	Front panel blue led (mandatory). +5V level.
104	ATCA_LED1	OUT	IPMC	Front panel LED 1 (Amber or Red, mandatory)
105	ATCA_LED2	OUT	IPMC	Front panel LED 2 (Green, optional)
106	ATCA_LED3	OUT	IPMC	Front panel LED 3 (Amber, optional)
107	GND			
108	Master_TRST	OUT^{pu}	IOIF	Master JTAG Test ReSeT signal
109	Master_TDO	OUT^{pu}	IOIF	Master JTAG Test Data Out signal
110	Master_TMS	OUT^{pu}	IOIF	Master JTAG Test Mode Select signal
111	GND			
112	TDO	OUT^{pu}		JTAG TDO
113	TMS	IN^{pu}		JTAG TMS
114	GND			
115	HA0	IN	IPMC	Hardware address 0
116	HA2	IN	IPMC	Hardware address 2
117	HA4	IN	IPMC	Hardware address 4
118	HA6	IN	IPMC	Hardware address 6
119	GND			
120	IPMB-A_SCL	INOUT	IPMC	IPMB-A I2C clock
121	IPMB-A_SDA	INOUT	IPMC	IPMB-A I2C data
122	GND			
123	GND			
124	PS1#_1	IN	IPMC	Low level indicates that the AMC module is inserted in the carrier.
125	Enable#_1	OUT	IPMC	When active, indicates to the AMC module that it is fully inserted in the carrier.
126	IPMB-L_Enable_1	OUT	IPMC	Connect AMC to the IPMB-L bus.
127	MP_Enable_1	OUT	IPMC	Activate the Management Power (+3.3V to AMC)
128	PWR_Enable_1	OUT	IPMC	Activate the module Payload Power (+12V to AMC).
129	MP_Good_1	IN	IPMC	Asserted when the Management Power voltage are within the required levels.
130	PWR_Good_1	IN	IPMC	Asserted when the Payload Power voltage are within the required levels.
131	MP_Fault_1	IN	IPMC	Asserted when the Management Power current reaches the limit
132	PWR_Fault_1	IN	IPMC	Asserted when the Payload Power current reaches the limit
133	PWR_ORing_1	OUT	IPMC	Optional – for 12V redundancy
134	GND			
135	PS1#_3	IN	IPMC	Low level indicates that the AMC module is inserted in the carrier.
136	Enable#_3	OUT	IPMC	When active, indicates to the AMC module that it is fully inserted in the carrier.
137	IPMB-L_Enable_3	OUT	IPMC	Connect AMC to the IPMB-L bus.
138	MP_Enable_3	OUT	IPMC	Activate the Management Power (+3.3V to AMC)

139	PWR_Enable_3	OUT	IPMC	Activate the module Payload Power (+12V to AMC).
140	MP_Good_3	IN	IPMC	Asserted when the Management Power voltage are within the required levels.
141	PWR_Good_3	IN	IPMC	Asserted when the Payload Power voltage are within the required levels.
142	MP_Fault_3	IN	IPMC	Asserted when the Management Power current reaches the limit
143	PWR_Fault_3	IN	IPMC	Asserted when the Payload Power current reaches the limit
144	PWR_ORing_3	OUT	IPMC	Optional – for 12V redundancy
145	GND			
146	PS1#_5	IN	IPMC	Low level indicates that the AMC module is inserted in the carrier.
147	Enable#_5	OUT	IPMC	When active, indicates to the AMC module that it is fully inserted in the carrier.
148	IPMB-L_Enable_5	OUT	IPMC	Connect AMC to the IPMB-L bus.
149	MP_Enable_5	OUT	IPMC	Activate the Management Power (+3.3V to AMC)
150	PWR_Enable_5	OUT	IPMC	Activate the module Payload Power (+12V to AMC).
151	MP_Good_5	IN	IPMC	Asserted when the Management Power voltage are within the required levels.
152	PWR_Good_5	IN^{pu}	IPMC	Asserted when the Payload Power voltage are within the required levels.
153	MP_Fault_5	IN	IPMC	Asserted when the Management Power current reaches the limit
154	PWR_Fault_5	IN	IPMC	Asserted when the Payload Power current reaches the limit
155	PWR_ORing_5	OUT	IPMC	Optional – for 12V redundancy
156	GND			
157	PS1#_7	IN	IPMC	Low level indicates that the AMC module is inserted in the carrier.
158	Enable#_7	OUT	IPMC	When active, indicates to the AMC module that it is fully inserted in the carrier.
159	IPMB-L_Enable_7	OUT	IPMC	Connect AMC to the IPMB-L bus.
160	MP_Enable_7	OUT	IPMC	Activate the Management Power (+3.3V to AMC)
161	PWR_Enable_7	OUT	IPMC	Activate the module Payload Power (+12V to AMC).
162	MP_Good_7	IN	IPMC	Asserted when the Management Power voltage are within the required levels.
163	PWR_Good_7	IN	IPMC	Asserted when the Payload Power voltage are within the required levels.
164	MP_Fault_7	IN	IPMC	Asserted when the Management Power current reaches the limit
165	PWR_Fault_7	IN	IPMC	Asserted when the Payload Power current reaches the limit
166	PWR_ORing_7	OUT	IPMC	Optional – for 12V redundancy
167	GND			
168	IPMB-L_SCL	INOUT^{pu}	IPMC	IPMB-L I2C clock
169	IPMB-L_SDA	INOUT^{pu}	IPMC	IPMB-L I2C data
170	GND			
171	Eth_Tx+/Gb_A+	INOUT		Tx+ of the Ethernet PHY (OUT) - A+ of the Gigabit Ethernet PHY (INOUT)
172	Eth_Tx-/Gb_A-	INOUT		Tx- of the Ethernet PHY(OUT) – A- of the Gigabit Ethernet PHY (INOUT)
173	GND			
174	Eth_Rx+/Gb_B+	INOUT		Rx+ of the Ethernet PHY(IN) - B+ of the Gigabit Ethernet PHY (INOUT)
175	Eth_Rx-/Gb_B-	INOUT		Rx- of the Ethernet PHY(IN) – B- of the Gigabit Ethernet PHY (INOUT)
176	GND			
177	Gb_C+	INOUT		C+ of the Gigabit Ethernet PHY
178	Gb_C-	INOUT		C- of the Gigabit Ethernet PHY
179	GND			
180	Gb_D+	INOUT		D+ of the Gigabit Ethernet PHY
181	Gb_D-	INOUT		D- of the Gigabit Ethernet PHY
182	GND			
183	Sensor_SCL	OUT^{pu}	IOIF	I2C bus clock for sensor interface
184	Sensor_SDA	INOUT^{pu}	IOIF	I2C bus data for sensor interface
185	GND			
186	IPM_IO_2	INOUT	IOIF	IPM I/O 2 for payload interface
187	IPM_IO_3	INOUT	IOIF	IPM I/O 3 for payload interface
188	IPM_IO_6	INOUT	IOIF	IPM I/O 6 for payload interface
189	IPM_IO_7	INOUT	IOIF	IPM I/O 7 for payload interface
190	GND			
191	IPM_IO_10	INOUT	IOIF	IPM I/O 10 for payload interface
192	IPM_IO_11	INOUT	IOIF	IPM I/O 11 for payload interface
193	GND			
194	IPM_IO_14	INOUT	IOIF	IPM I/O 14 for payload interface
195	IPM_IO_15	INOUT	IOIF	IPM I/O 15 for payload interface
196	GND			
197	USR_2	INOUT	IOIF	User IO pin 2
198	USR_3	INOUT	IOIF	User IO pin 3
199	GND			
200	USR_6	INOUT	IOIF	User IO pin 6
201	USR_7	INOUT	IOIF	User IO pin 7
202	GND			
203	USR_10	INOUT	IOIF	User IO pin 10
204	USR_11	INOUT	IOIF	User IO pin 11
205	GND			
206	USR_14	INOUT	IOIF	User IO pin 14
207	USR_15	INOUT	IOIF	User IO pin 15
208	GND			
209	USR_18	INOUT	IOIF	User IO pin 18

210	USR_19	INOUT	IOIF	User IO pin 19
211	GND			
212	USR_21	INOUT	IOIF	User IO pin 21
213	USR_23	INOUT	IOIF	User IO pin 23
214	USR_25	INOUT	IOIF	User IO pin 25
215	USR_27	INOUT	IOIF	User IO pin 27
216	USR_29	INOUT	IOIF	User IO pin 29
217	USR_31	INOUT	IOIF	User IO pin 31
218	USR_33	INOUT	IOIF	User IO pin 33
219	GND			
220	Mgt_I2C_SCL	OUT^{pu}	IOIF	I2C bus clock for power management module
221	Mgt_I2C_SDA	INOUT^{pu}	IOIF	I2C bus data for power management module
222	GND			
223	Ext_RST_n	OUT^{pu}	IPMC	External Reset signal for payload cold reset
224	Handle_Switch	IN	IPMC	Front panel handle switch for board insertion detection
225	12V_Enable	OUT^{pd}	IOIF	Enable DC-DC (-48V to 12V) payload power
226	Alarm_A	IN	IOIF	Alarm from power management module for -48V_A
227	Alarm_B	IN	IOIF	Alarm from power management module for -48V_B
228	PowerGood_A	IN	IOIF	Power good from power management module -48V_A
229	PowerGood_B	IN	IOIF	Power good from power management module -48V_B
230	GND			
231	Master_TCK	OUT^{pd}	IOIF	Master JTAG Test Clock signal
232	Master_TDI	IN^{pu}	IOIF	Master JTAG Test Data In signal
233	GND			
234	TCK	IN^{pd}		JTAG TCK
235	TDI	IN^{pu}		JTAG TDI
236	GND			
237	HA1	IN	IPMC	Hardware address 1
238	HA3	IN	IPMC	Hardware address 3
239	HA5	IN	IPMC	Hardware address 5
240	HA7	IN	IPMC	Hardware address 7
241	GND			
242	IPMB-B_SCL	INOUT	IPMC	IPMB-B I2C clock
243	IPMB-B_SDA	INOUT	IPMC	IPMB-B I2C data
244	GND			

Table 17: IPMC mezzanine pinout.). pu=pull up 4.7kΩ resistor on mezzanine, pd=pull down 4.7kΩ resistor onr mezzanine.

VI. Electrical specifications

VI.1. Power supply

The IPMC Mezzanine is powered by signal VCC.

Pin	Description	Absolute (V)		Recommended (V)		
		Min	Max	Min	typ	max
VCC	Mezzanine power supply (with respect to GND)	-0.3	+4.2	+3.0	+3.3	+3.6

Table 18: IPMC power supply characteristics.

VI.2. I/Os

Only few IPMC Mezzanine I/Os are not connected to the controllers (STM32F407 from ST). These are the following signals:

- ATCA_Blue_LED
- IPMB_A and IPMB_B signals connected to a LTC4307.
- Ethernet signal connected to a DP83848 PHY.

The following characteristics are valid for all I/Os connected to the controllers.

Symbol	Description	Min	Max	Unit
V_{IL}	Input low level voltage	-0.3	0.8	V
V_{IH}	Input high level voltage	2.0	5.5	V
V_{OL}	Output low level voltage	-	0.4	V
V_{OH}	Output high level voltage	2.4	VCC	V
I_O(1)	Output driving current	-	±8	mA
$C_{I/O}$(2)	I/O pin capacitance	5 Typ		pF

(1) The sum of the currents sourced or sunk by all the I/Os, plus the maximum Run consumption of the Microcontroller sourced or sunk, cannot exceed the absolute maximum rating IVDD (150 mA)

(2) This is the capacitance of the Microcontroller I/Os and does not include added capacitors due to the I/Os routing on the mezzanine and due to the mezzanine connector.

Table 19: I/Os electrical specifications.

VI.3. ATCA Blue LED output

The mezzanine provide a +5V output in order to drive blue leds that can have a forward voltage greater than +3.3V.

Symbol	Description	Min	Max	Unit
V_{OL}	Output low level voltage	-	0.55	V
V_{OH}	Output high level voltage	4.2	5.2	V
I_O(1)	Output driving current	-	±32	mA

Table 20: ATCA blue led electrical characteristics.

VI.4. Ethernet I/Os

Ethernet differential input pair Eth_Rx± and differential output pair Eth_Tx± are connected to a DP83848 PHY Ethernet transceiver. These I/Os are compatible with the ANSI X3.263 TP-PMD physical sublayer standard. The following specifications are extracted from the DP83848 datasheet.

Symbol	Parameter	Min	Typ	Max	Unit
V_{TPTD_100}	100M Transmit Voltage	0.95	1	1.05	V
V_{TPTD_sym}	100M Transmit Voltage Symmetry	-	-	±2	%
V_{TPTD_10}	10M Transmit Voltage	2.2	2.5	2.8	V
SD_{THon}	100BASE-TX Signal detect turn on threshold	-	-	1000	mv_{pk-pk}
SD_{THoff}	100BASE-TX Signal detect turn off threshold	200	-	-	mv_{pk-pk}
V_{TH1}	10BASE-T Receive Threshold	-	-	585	mV

Table 21: Ethernet I/Os electrical specifications.

VI.5. IPMB-A and IPMB-B I/Os

IPM Bus signals (IPMB-A_SCL, IPMB-A_SDA, IPMB-B_SCL, IPMB-B_SDA) are buffered by a LTC4307 Low Offset Hot Swappable 2-Wire Bus Buffer. The following IPMB-A/B IOs specifications are extracted from the LTC4307 datasheet.

Absolute Maximum Ratings

Symbol	Parameter	Value
IPMB-A_SCL, IPMB-A_SDA, IPMB-B_SCL, IPMB-B_SDA	DC Input voltage	-0.3V to 6V
	Maximum sink current	50mA

Table 22: IPMBus I/Os absolute maximum ratings

Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OS}	Input-Output Offset Voltage	2.7k to VCC on SDA, SCL, VCC = 3.3V, Driven SDA/SCL = 0.2V	20	60	100	mV
V_{THR}	Logic Input Threshold Voltage	Rising Edge	0.45Vcc	0.55Vcc	0.65Vcc	V
V_{HYS}	Logic Input Threshold Voltage Hysteresis		-	50	-	mV
C_{IN}	Digital Input Capacitance		-	-	10	pF
I_{LEAK}	Input Leakage Current		-	-	±5	µA
V_{OL}	Output Low Voltage	SDA, SCL Pins, ISINK = 4mA, Driven SDA/SCL = 0.2V, VCC = 2.7V	0	-	0.4	V
		2.7k to VCC on SDA, SCL, VCC = 3.3V, Driven SDA/SCL = 0.1V	120	160	205	mV
V_{ILmax}	Input Logic Low Voltage	VCC = 3.3V	-	-	1.2	V

Table 23: IPMBus I/Os electrical specifications.

VI.6. Unused I/Os

Unused I/Os can be left unconnected.

VII. Design Guidelines

VII.1. Handle switch

Although the active level of the Handle_Switch signal is not well defined and can be changed in the IPMC firmware, we recommend that this signal has a logic level '0' when the board is in working condition. The Handle_Switch signal has a low pass filter (R=4.7kΩ, C=100nF) located on the IPMC mezzanine for de-bouncing purpose. The following schematic gives an idea of what can be done on a blade.

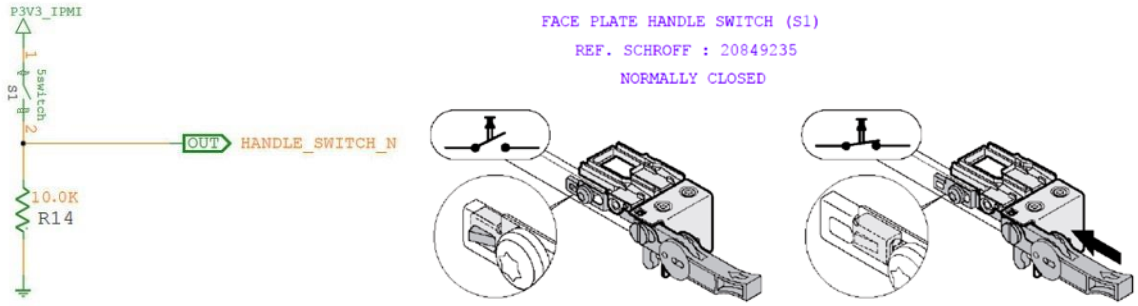

Figure 8: Handle Switch schematic example.

VII.2. Hardware address

The ATCA blade zone 1 connector has eight Hardware Address pins (HA[7..0]). The blade must de-couple each Hardware Address signal to the Logic Ground using a 1 nF capacitor and must provide a pull-up resistor of not less than 4.46 kΩ and not greater than 10.5 kΩ to VCC.

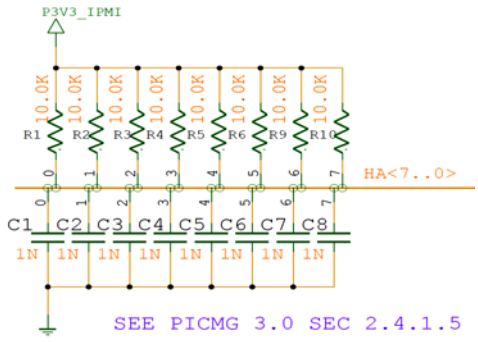

Figure 9: Hardware Address schematic example.

VII.3. IPMBus

IPMBus signals (IPMB_A_SCL, IPMB_A_SDA, IPMB_B_SCL, IPMB_B_SDA) can be directly connected to pin of Zone 1 connector of the blade (pin SCL_A, SDA_A, SCL_B, SDA_B). Buffers are not needed on the blade because the IPMC Mezzanine already has these buffers. Pull-up resistors are located on the shelf.

VII.4. JTAG slave bus

It is recommended to add a JTAG connector on the carrier for debugging and to upgrade the IPMC Mezzanine. The ARM 20-pin connector is a quite standard connector. An example of schematic is provided on the following figure.

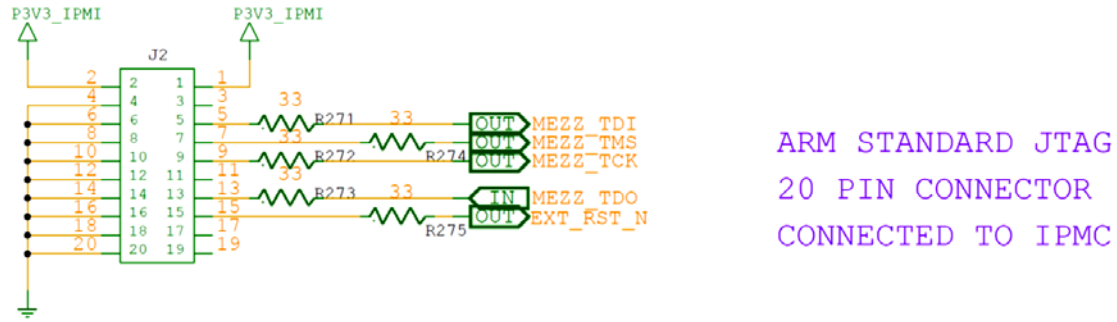

Figure 10: ARM 20-pin JTAG connector schematic.

VIII. Software

VIII.1. IPMC Firmware Upgrade

There are two ways to upgrade the IPMC Firmware. The first one uses the **Ethernet link**, and the second one uses the **JTAG bus** (IPMC Mezzanine TDI, TDO, TMS, TCK signals). The Ethernet link or the JTAG bus must be cabled to ensure the IPMC Mezzanine firmware upgrade.

At power-up each µC boots from its internal Flash memory.

VIII.1.1. JTAG upgrade

For a firmware upgrade through the JTAG bus, the new firmware is written directly into the µC Flash memory.

VIII.1.2. Ethernet upgrade

For a firmware upgrade through Ethernet the new firmware is written in an EEPROM located on the IPMC Mezzanine. Once this new firmware is written an upgrade firmware command is sent to the IPMC Mezzanine via Ethernet. The new firmware is then written from the EEPROM to the µC internal Flash memory.

The EEPROM stores two firmwares per µC: a “Factory Firmware” and a “User Firmware”. When a µC upgrades from the EEPROM it tries to load the User Firmware. If the µC does not start with this new firmware the factory firmware is automatically loaded. This mechanism prevents from stuck situations in case of bad firmware or problems during firmware upgrade.

VIII.2. Debugging the IPMC Mezzanine Firmware

VIII.2.1. JTAG

The JTAG chain is the best way to debug the IPMC Mezzanine. The access to the JTAG chain must be done through the IPMC Mezzanine carrier.

A possible solution is to add a JTAG connector on the carrier. This connector can be a standard ARM 20-pin debug connector. Several USB to JTAG cables are available on the market and can be easily used to debug the IPMC. (see: JTAG slave bus for an example of schematic)

The NGX ARM USB JTAG from NGX Technologies is well suited for the IPMC Mezzanine Debugging.

Figure 11: NGX ARM USB JTAG in-circuit debugger and programmer

VIII.2.2. UART

Two UART connectors are provided for debugging purposes. There is one UART connector per microcontroller. UART signals must respect the electrical specifications defined in table 19.

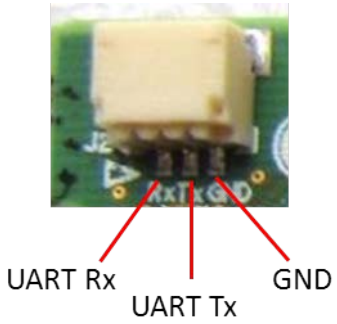

Figure 12: Signals description of UART connectors.

Pin number	Signal
1	UART_Rx
2	UART_Tx
3	GND

Table 24: UART connector signals.

IPMC UART connectors have the following reference from JST: SM03B-SRSS-TB

Mated parts can be found with these references: JST SHR-03V-S-B and SH3-SS5-28150.

In order to communicate with microcontrollers through UART, a USB ↔ RS232 converter can be used.

IX. Document Revision History

Date	Version	Changes
January 2016	1.7	• Added IPMB-L is bused on the carrier • Description of UART connectors • Update overview picture with V2.2
June 2014	1.6	• Date in US format • Added: Electrical specifications • Rename +3.3Vpin to VCC • Added: hardware address, handle switch, IPMBus in design guidelines • Removed pull-up on IPMB_A and IPMB_B • Added Software part • Added IO to µC connection on IPMC Mezzanine pin definition • Added pull-up info on Hardware Address • Added Mezzanine depth on mechanical size
November 2013	1.5	Added this “document revision history”
October 2013	1.4	• Rename USR_[1..35] to USR[0..34] • Rename IPM_IO_[1..16] to IPM_IO[0..15] • Signal **Ext_RST_n** is an output for IPMC V2.1. It was an input for IPMC V2.0