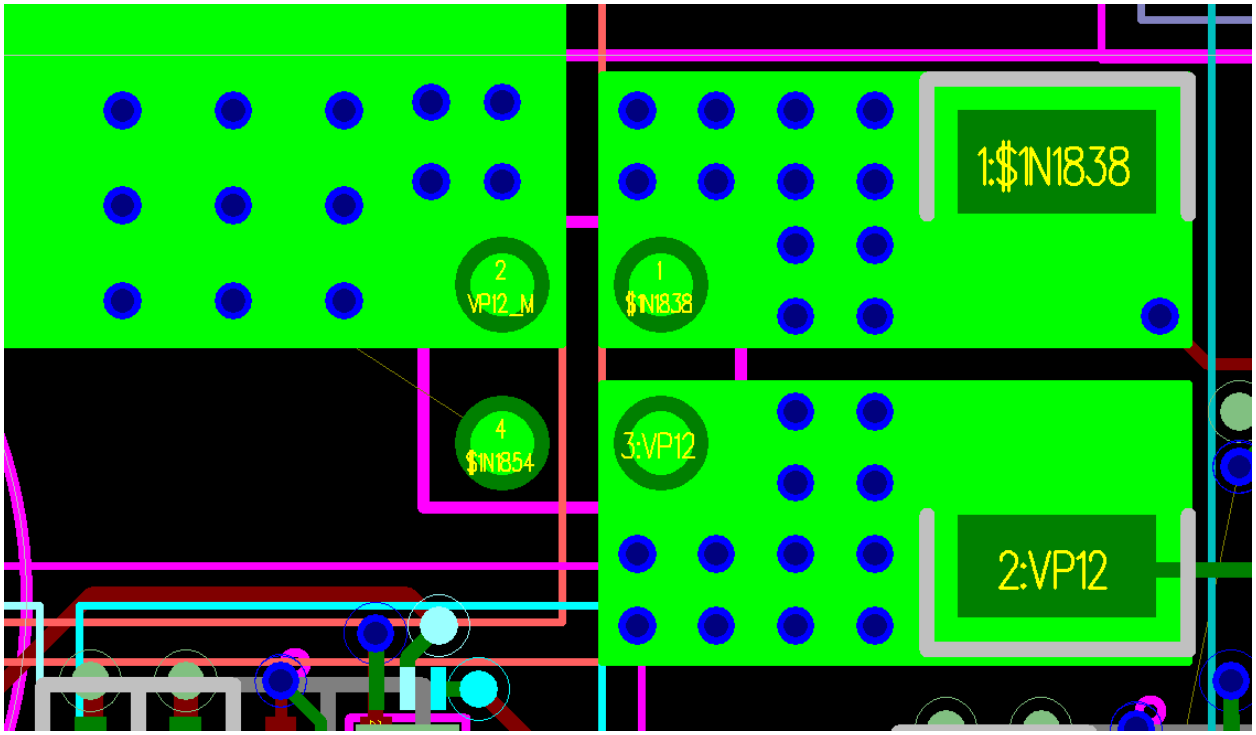
from Hucheng Chen:

1. There are 10uF capacitors, symbol is CC0402, should double check if it is available in 0402 package.

   The part number in the latest BOM is digi-key #1276-1405-1-ND, which is a 10V, 10uF 0402 cap, which does exist. The link in Column K is the (old) 16V cap which was an 0603. Since these caps are only used on voltage below 5V, a 10V cap should be fine. So a 10V rated cap does exist, and is still in stock (as of now).

2. Connector J5 is in the current path, please make sure the pins of J5 can support up to 33A.

   The jumper is certainly not rated at 33 A. We have a solution which uses multiple jumpers to get the necessary current rating. The layout has the solution we will use on the boards, as soon as we know that the 12Volt is correct when isolated from the rest of the board. A .gif blowup of the layout is below.



3. LTM4628 has different connection between 5V and 1.0V, what is the consideration?

   The follow the manufacturer data sheets, and we have tested this on a power test board. The detailed issue is that the internal differential op amp output is limited to 0.6V to 3.3V (as we found out the hard way on the initial power test board). The 5V supply therefore is wired differently, as suggested by the manufacturer, to allow 5V operation.

4. IPMC GbE, in the design one pair of serdes is connected to FPGA MGT, it seems that the SGMII is used. However, it is not clear whether the SGMII interface is supported by the next version of IPMC.

   We asked our Annecy colleagues about potential 1 GbE to/from the IPMC. We were told it will not be implemented even though the connections are there. The IPMC CPU provides only 10/100 Mbps interfaces, not gigabit.

   However, we agree it isn't obvious this will work. We imagine that we may have to force 100 Mbps through the MGT (with or without auto-negotiation). The Xilinx PCS/PMA core says it can support this mode, and Xilinx also provides a dedicated 100 Mbps MAC IP core (which is free). We are in the process of checking this part of the design both via VC707 connection to a 100 Mbps switch (already done through the PHY+RJ45 and pending through SFP+sgmii). The ultimate test will use a small board which was designed to test this. The board will fit in an SFP cage and have an RJ45 (with magnetics) and a level shifter. This simulates the circuit we currently have for the IPMC<->FPGA 100 Mbps connection. (Thanks, Chen for producing the PCB for us.)

5. The one pair of serdes are driven by an SN74AVC4T245, the maximum data rate of this chip is about 380Mbps, not sure it is suitable for MGT link.

   The link speed is fixed at 100 Mbps. This is part of the testing mentioned in the answer to part 4, and we are planning a test of this in the next couple of weeks, prior to sending the carrier for PCB manufacturing.

6. Two LVDS repeaters are used to fan out the clocks, a dedicated clock buffer might be more suitable for clock fan out, which has good jitter performance and low skew.

   Although we use these only for GbE and XAUI connection, we will look into a low jitter fanout. On our AMC card and our Ethernet test board, we used an LVDS fanout (CDCLVD2102) with <300 fs jitter so we know this is available.

7. From the power design, the VCC1V8 is generated from 2V5 and 3P3V. It violates the power sequence of Xilinx. And there is no power sequence control of 1P8V, so the time gap between the 3P3V and 1P8V is uncontrollable and uncertain. However, the SPI flash has critical power sequence between the core voltage and VIO. So the 3.3V and 1.8V power up sequence should be examined.

   Neither the 2.5V nor the 3.3V supplies are used directly by the FPGA. We checked the timing for the flash and VIO and it we think it's OK because the 2.5V and 3.3V come up together, and the 3.3V provides power to the 1.8V which according to the spec must track each other. We will power the linear regulator from the 3.3V with the enable always tied high, but we'll look into it further as well. We will also change C172, C173 and C176 from 0.1uF to 0.01uF. These are the "soft start" capacitors for the LTM4628 DCDC converters.

8. DDR3 Banks VREF resistors value should be 80.6, not 100.

We agree.

From Dan Edmunds:

1. 10**9 High speed signals:

Your ATCA Carrier card is complicated because of all the high speed differential signals but I know that you will be careful and can take care of all of that.

We are trying to be careful…

2. 400 Watts:

What perhaps looks more risky for the over all system reliability is the power level of the card. It looks like you will need to run things right up near their maximum current levels. I know that there is nothing that you can do about this, i.e. the current draws are what they are and the available ATCA power modules are what they are.

- Are all of the slots in a crate (I know "shelf") going to operate that the 400 Watt level ?

Yes, except for the hub modules.

- Have you gotten all of the test crates and tools and such that you need so that you can make tests and be comfortable running things this close to their max ?

We have a crate with 400 W capability in many slots at 40 C, but not all. At a reasonable temperature 23C, all slots are 400 W capable. We plan to fully load a crate as a test.

- Do you need a recommendation from this review that Stony Brook should be given more funds to purchase high power level test setups or instruments or whatever to make a detailed study at this power density ?

- Heat sink layout and air flow must be complicated.

Yes. We are nervous about this and eager to get a fully loaded carrier for testing. There are thermal simulations of a single AMC card which differ from measurements by 50%.

- I assume that your Carrier cards are "behind the wall" so that reliability is quite important. Is that right? If a Carrier goes down a lot of the detector goes down.

3. Use of the IPMC:

We are finally getting started on an ATCA card for L1Calo that will also use the IPMC card from Annecy/LAPP. Like you I wanted to use some of its nice features, e.g. the User I/O Lines and mastering the JTAG by the IPMC as controlled by the Ethernet link to it.

I *think* that I remember being told that no software actually exists to do any of this nice reasonable stuff and that none was likely to exist soon or perhaps ever exist. I *think* I was told that people were

even considering going to some commercial software or commercial IPMC or something like that. What do you know?

We talked with the Annecy folks in early Nov. The shelf management parts are already available. The AMC enabling we need will not be available, hence the jumpers on our board to bypass IPMC control of the AMC power. The Ethernet isn't ready yet, but is a high priority, except that the JTAG portion is the lowest priority. We decided that prudence dictated a JTAG jumper on the carrier to allow selection of the JTAG source, either IPMC or connector.

4. I2C Monitoring: This looks complicated on your Carrier card (as it needs to be on a card were you need to monitor a lot of stuff). In the fullness of time you might like a line drawing that shows how all of this is laid out, i.e. the table on page 6 but in a graphic form.

Will do.

5. Possible Typos:

I think that I saw a few typos or mismatches between the written document and the schematics, e.g. the table on page 4 shows Bank 14 being an LVDS connections to AMC-2 but I don't think that I see that in the schematics.

We'll check this and fix the documentation.

6. The PCB on page 14:

I've used the FR408HR laminate on a recent card with 6.4 Gb/sec traces and it worked well. It's a nice solid material to work with. We've changed some SMD resistors on this PCB (to adjust the full scale range of some current monitoring) and there is no problem with the card falling apart during rework - this was with hot lead free solder.

Good news!

The bare board house and the assembly house had no trouble with FR408HR. I've used fancy halogen free high frequency laminate for a LAr TPC card, "Taconic" laminate, and that stuff was very annoying.

Page 14 says, "maximum finished holes size is ...".

Did you mean minimum hole size is ... ? I do not know what, "18 mil page" means.

These are indeed typos. It should be "minimum" as you suggest and "page" should be "pad"

7. Base Interface 1 GbE Ethernet and Switch:

I know that you are still working on this. I'm only just now starting to work on it for the "Hub" card that we need to make for L1Calo - so there is a whole lot that I do not yet understand about Base Interface and Switches.

- Your schematic shows the GbE going directly to Xilinx MGT Transceivers including the GbE for the Zone 2 Base Interface. I know that a Xilinx MGT Transceiver can handle the 1 GbE data rate but I did not know that it could work directly with the signal levels that exist in the normal 4 pair RJ45 type of 1 GbE Ethernet setup aka 1000BASE-T.

> See the answer to Chen's questions 4 and 5. In short, yes, we are also worried and plan an independent test.

- I thought that the ATCA Base Interface was just the normal 1000BASE-T signal levels. I must just be missing something here. Maybe you are running something different on your backplane Base Interface or I'm missing a "Phy" interface chip or I need to read a Xilinx book.

> We think we are doing it correctly. We've tested this in our microTCA crate with our AMC card, but the design on the carrier is identical. The Dresden group has done some testing in ATCA, and we understand the direct FPGA connection worked for them. We will double check this though. It would be a nasty surprise.