LTP INTERFACE

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Rev 4.3 17 August 2005

History

Version 1	15 June 2005	Ph. Farthouat	First draft
Version 2	30 June 2005	Ph. Farthouat	Interface connected on the CTP-LINK to allow full functionality
Version 2.01	5 July 2005	Ph. Farthouat	Modification Fig.1 and 5 according to Th. Pauly comments.
Version 3.0	7 July 2005	Ph. Farthouat	Including the generation of Trigger-Type in the Interface module.
Version 4.0	8 July 2005	Ph. Farthouat	Connection of all the interfaces on a ring.
Version 4.1	8 Aug. 2005	Ph. Farthouat	Add a complete block diagram. Define the VME interface.
Version 4.2	10 Aug. 2005	Ph. Farthouat	Including remarks from Th. Pauly.
Version 4.3	17 Aug. 2005	Ph. Farthouat	Including remarks from D. Nunes

1. Introduction

The Local Trigger Processor (LTP) [1] [2] [3] connects the sub-detector partitions to the Central Trigger Processor and allows sub-systems to work either in global mode (under control of the CTP) or in local (or stand-alone) mode for test, commissioning or calibration purposes.
Several LTPs from the same sub-detector are connected together with the CTP-LINK and it is possible to define a partition gathering several or all these LTPs and to run this partition in stand-alone mode. One of the LTP is configured as being the master of the partition (it is playing the role of the CTP in that case) and all the others are slaves.
It is also requested to be able to run several sub-detectors in stand-alone mode, mainly for commissioning purposes although this functionality may still be used in the future. Such functionality must not require any cabling operation and must be fully controlled by software. In order to be able to do so, a special interface module must be fabricated. This note defines its specification.

2. Overview of the interface module

Fig. 1 shows three sets of LTPs connected to three different CTP-LINKs and the position of the interface module that is used to run these three sets in one stand-alone run. The extra link, organised as a ring, between the interface modules can be seen as an extension of the CTP-LINKs.
One of the LTP is acting as the master of the newly formed partition (the top left one in Fig. 1, but it could be any other) while all the others are slaves.
Each left side LTP of each sub-system is controlling its CTP-LINK output and is interacting with the Interface module through its input CTP-LINK when in local mode.
Three sets of signals must be distributed:

- The timing, trigger and control signals
- The Trigger-Type word
- The BUSY signals

The Timing and control signals are:

- BC
- Orbit
- Test-Trigger<3..0>
- B-Go<3..0>

The Trigger-Type word is an 8-bit word issued by the Interface module connected to the master LTP .

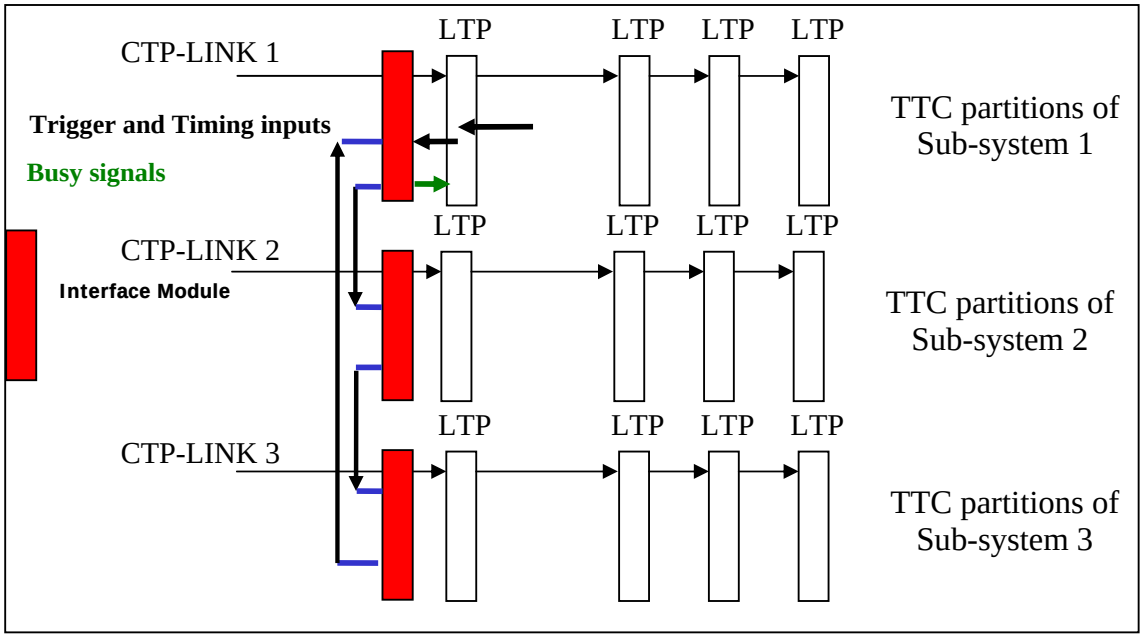

Figure 1. Regrouping several sub-detector partitions

The BUSY signals are the ROD-BUSY signals used for throttling the L1A signals in case some dead-time must be introduced. They have to be sent to the master LTP.
The Interface module connected to the master LTP gets the timing, trigger and control signals from the master LTP and sends them to its differential Output Port B link. The Trigger-Type is issued by the Interface module connected to the master LTP and is sent to its CTP-LINK output and to its differential Output Port B link. It takes the BUSY signals from its differential Input Port A link and feeds it to the master LTP.
The Interface module connected to a slave LTP gets the timing, trigger and control signals and the Trigger-Type word from the differential Input Port A link. It takes the BUSY signals from the CTP-LINK to which it is connected and from the differential Input Port A and feeds the logical OR of them to the master LTP through the differential Output Port B.

3. Interface module connected to the master LTP

A simplified block diagram of the Interface module when connected to the master LTP is shown in Fig. 2.

It has to be noted that every individual signal has a programmable output control. This allows for instance to still have the slave LTPs using the BC and Orbit signals coming from their CTP-LINKs (BC and Orbit should always be available on the CTP-LINKs).

The timing and trigger signals, as well as the Trigger-Type word are sent to the differential Output Port B link. The BUSY signal is taken from the differential Input Port A link and sent to the LTP.

The Trigger-Type is issued by the Interface module on the basis of the Test-Trigger used. Seven VME accessible registers are used for this purpose, one for each combination of the three Test-Trigger signals (the combination "000" being unused). This allows to have different Trigger-Type for different trigger. The Trigger-Type is sent to the master LTP through the CTP-Link output.

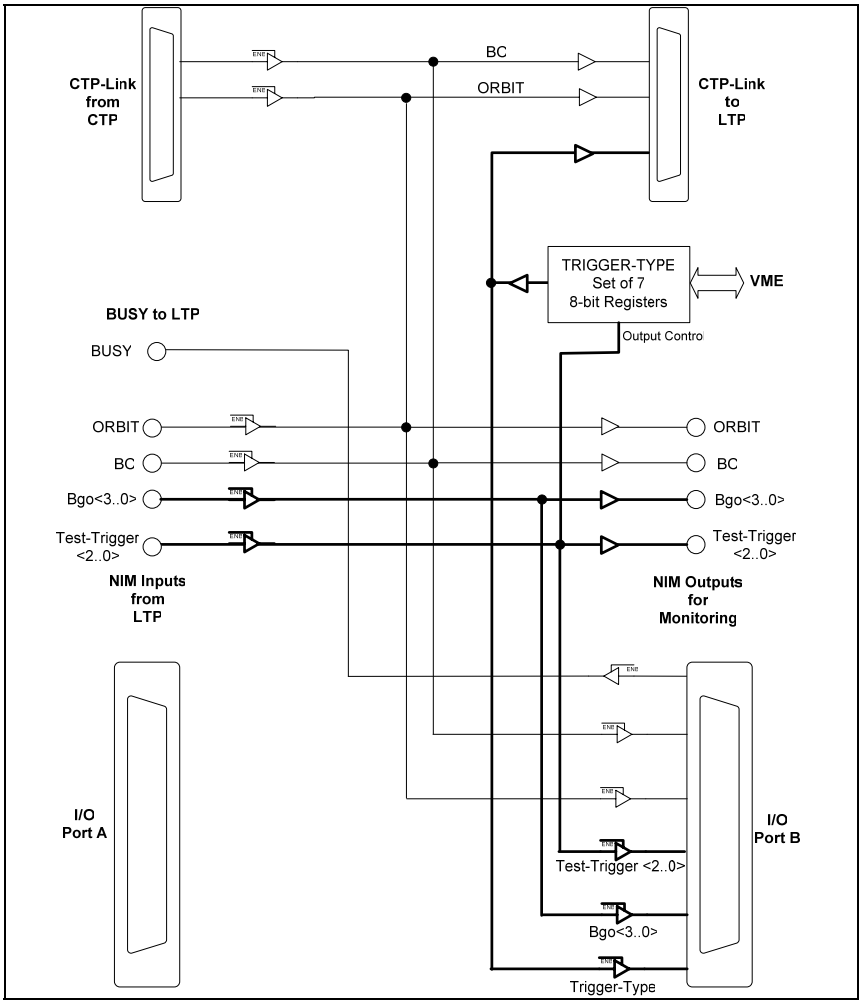

Figure 2. Simplified block diagram of the Interface module connected to the master LTP

4. Interface module connected to a slave LTP

In that case the interface receives the timing and trigger signals as well as the Trigger-Type word from the differential Input Port A link. These signals are then made available on the CTP-LINK output to be used by the LTPs connected to it. These signals be transmitted on the differential Output Port B link.

The BUSY signal from the slave LTPs is received on the CTP-LINK. It is ORed with the BUSY signal coming from the differential Input Port A link. The result of this OR has to be sent on the differential Output Port B link.

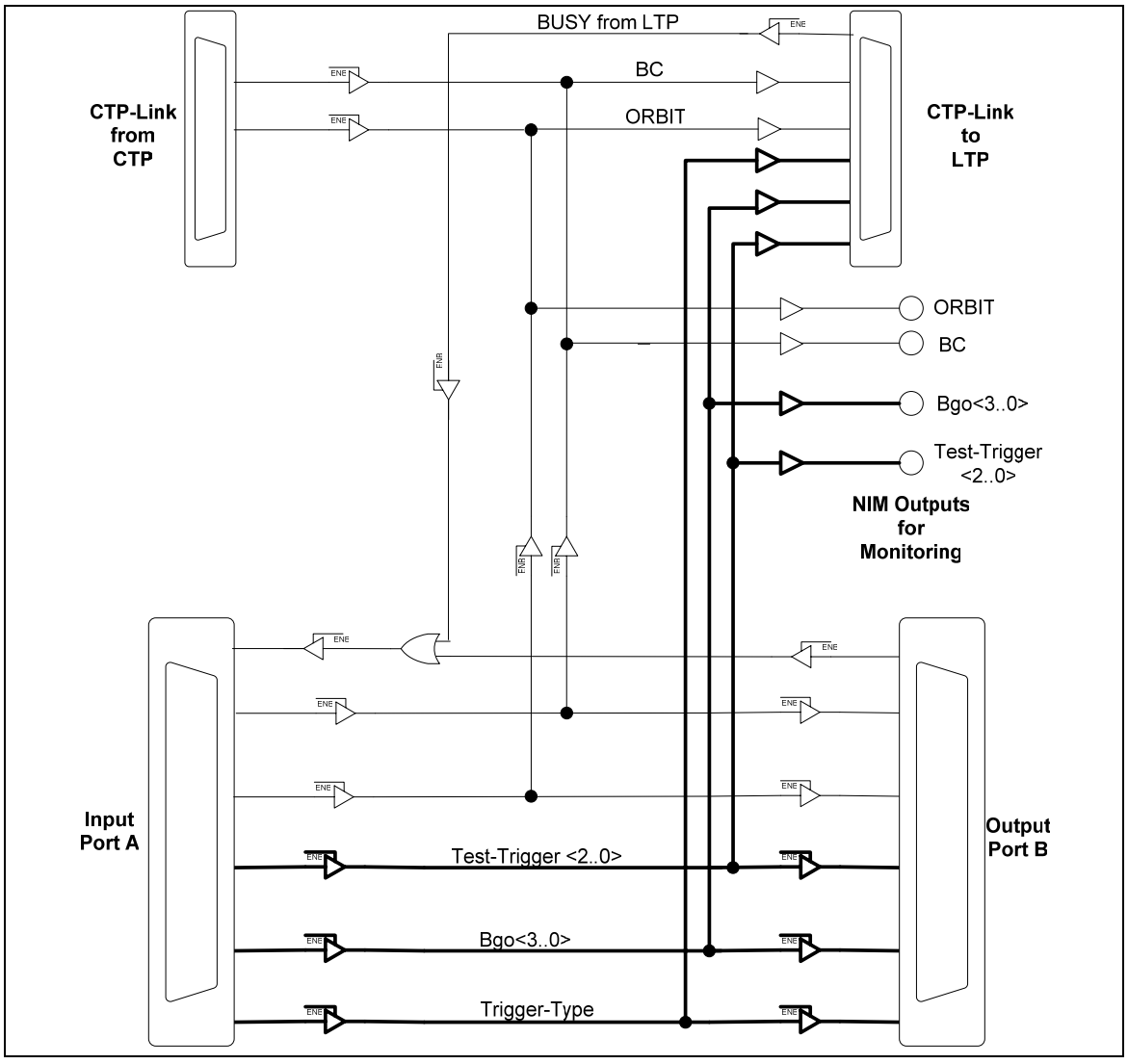

Figure 3. Simplified block diagram of the Interface module connected to a slave LTP

It has to be noted that it is also possible to have the Interface module in a mode where Input Port A and Output Port B are connected together without any interaction with the local LTPs. This mode is to be used if for example

in a configuration similar to Fig. 1, it is needed to have a combined run between the LTPs connected to the CTP-LINKs 1 and 3, while the LTPs connected to the CTP-LINK 2 are running in a different partition.

5. Interface module in transparent mode

When in global mode, i.e. running with the CTP, the Interface in transparent mode. The CTP-LINK input is connected to the CTP-LINK output as shown in Fig. 4.

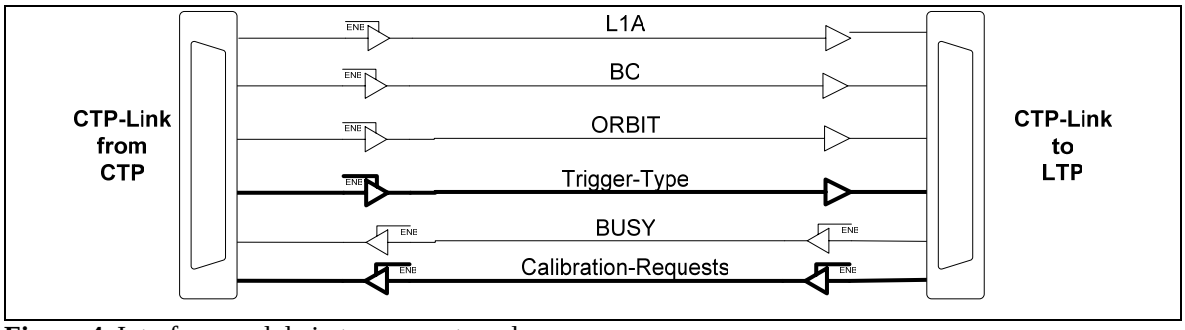

Figure 4. Interface module in transparent mode

The L1A transmitted from the CTP on the CTP-LINK is of course subject to an additional delay (receiver and driver chips, traces on the PCB, de facto increased length of the CTP-LINK). This delay will be maintained as small as possible and should not exceed 10 – 15 ns.

6. Overall block diagram

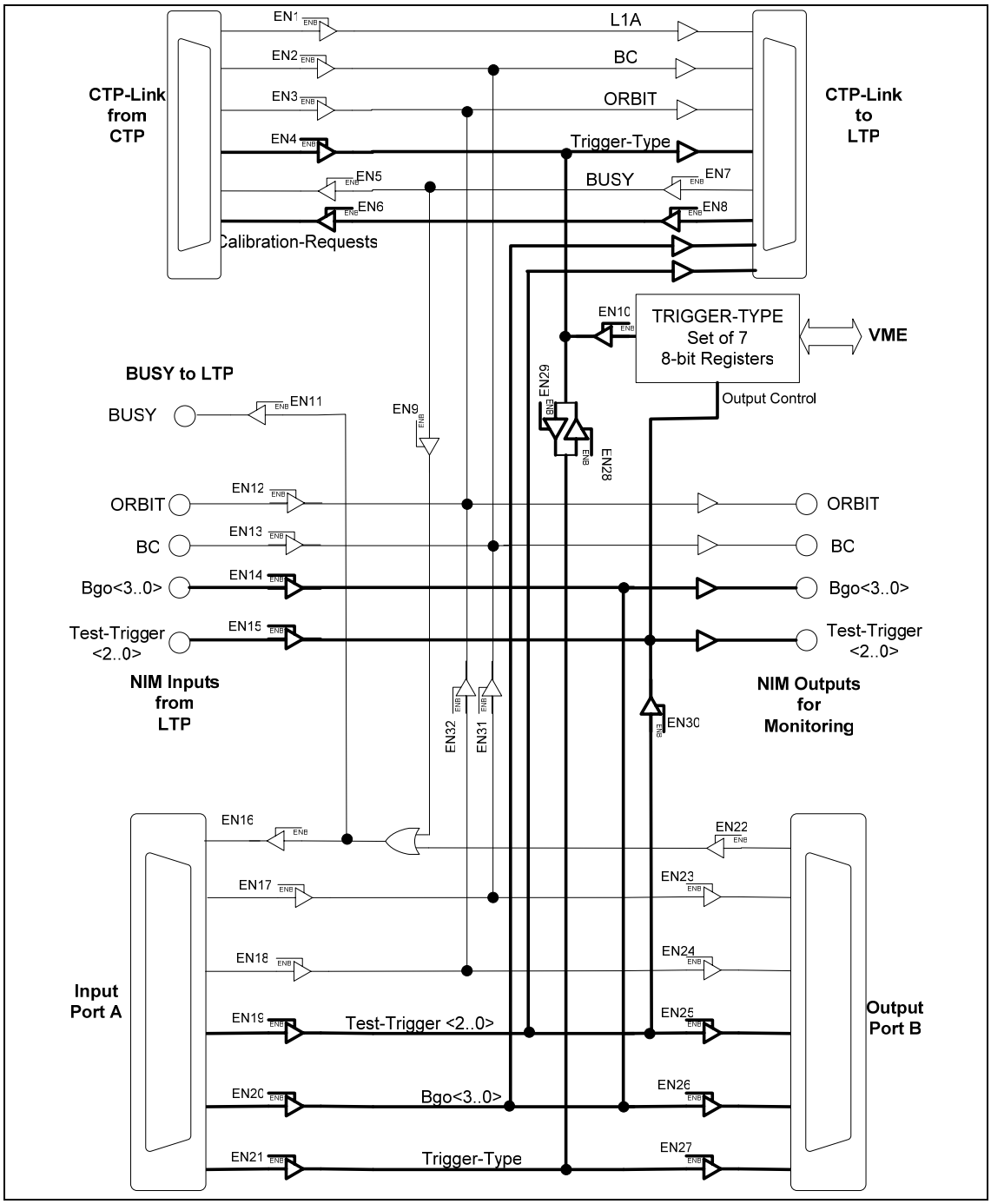

Figure 5. LTP Interface Block Diagram

7. Electrical characteristics

The electrical characteristics of the different signals are given in Table 1.

Signal	Type	Connector
I/O Links Port A and B	LVDS	Tbd
CTP-LINK input and output	LVDS	
BC from LTP	NIM	Lemo 00
Orbit from LTP	NIM	Lemo 00
Test-Trigger<2..0> from LTP	NIM	Lemo 00
B-Go<3..0> from LTP	NIM	Lemo 00
BUSY to LTP	NIM	Lemo 00
BC Monitoring	NIM	Lemo 00
Orbit Monitoring	NIM	Lemo 00
Test-Trigger<2..0> Monitoring	NIM	Lemo 00
B-Go<3..0> Monitoring	NIM	Lemo 00

Table 1. Characteristics of the signals

8. VME interface

This module is a 6U VME64x module supporting the A24/D16 cycles.
Five registers (read and write access) will be used to program the module.

CSR1 Control of the CTP-LINK from/to the CTP and from/to the LTP

Base Address + $0

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	EN6	EN5	EN4	EN3	EN2	EN1	EN32	EN31	EN30	EN29	EN28	EN7	EN8	EN9	EN10

CSR2 Control of the signals to/from the LTP

Base Address + $2

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	EN15	EN14	EN13	EN12	EN11

CSR3 Control of the I/O ports A and B

Base Address + $4

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	EN27	EN26	EN25	EN24	EN23	EN22	X	X	EN21	EN20	EN19	EN18	EN17	EN16

Trigger-Type Registers

Base Address + $6 to $C
Set of 7 8-bit registers (concatenated in 16-bit words) associated to the Test-Trigger<2..0> combination from $1 to $7.

Base Address + $6

D15-D8	D7-D0
Trigger Type associated to Test-Trigger<2..0>=”010”	Trigger Type associated to Test-Trigger<2..0>=”001”

Base Address + $8

D15-D8	D7-D0
Trigger Type associated to Test-Trigger<2..0>=”100”	Trigger Type associated to Test-Trigger<2..0>=”011”

Base Address + $A

D15-D8	D7-D0
Trigger Type associated to Test-Trigger<2..0>=”110”	Trigger Type associated to Test-Trigger<2..0>=”101”

Base Address + $C

D15-D8	D7-D0
X	Trigger Type associated to Test-Trigger<2..0>=”111”

9. Connections

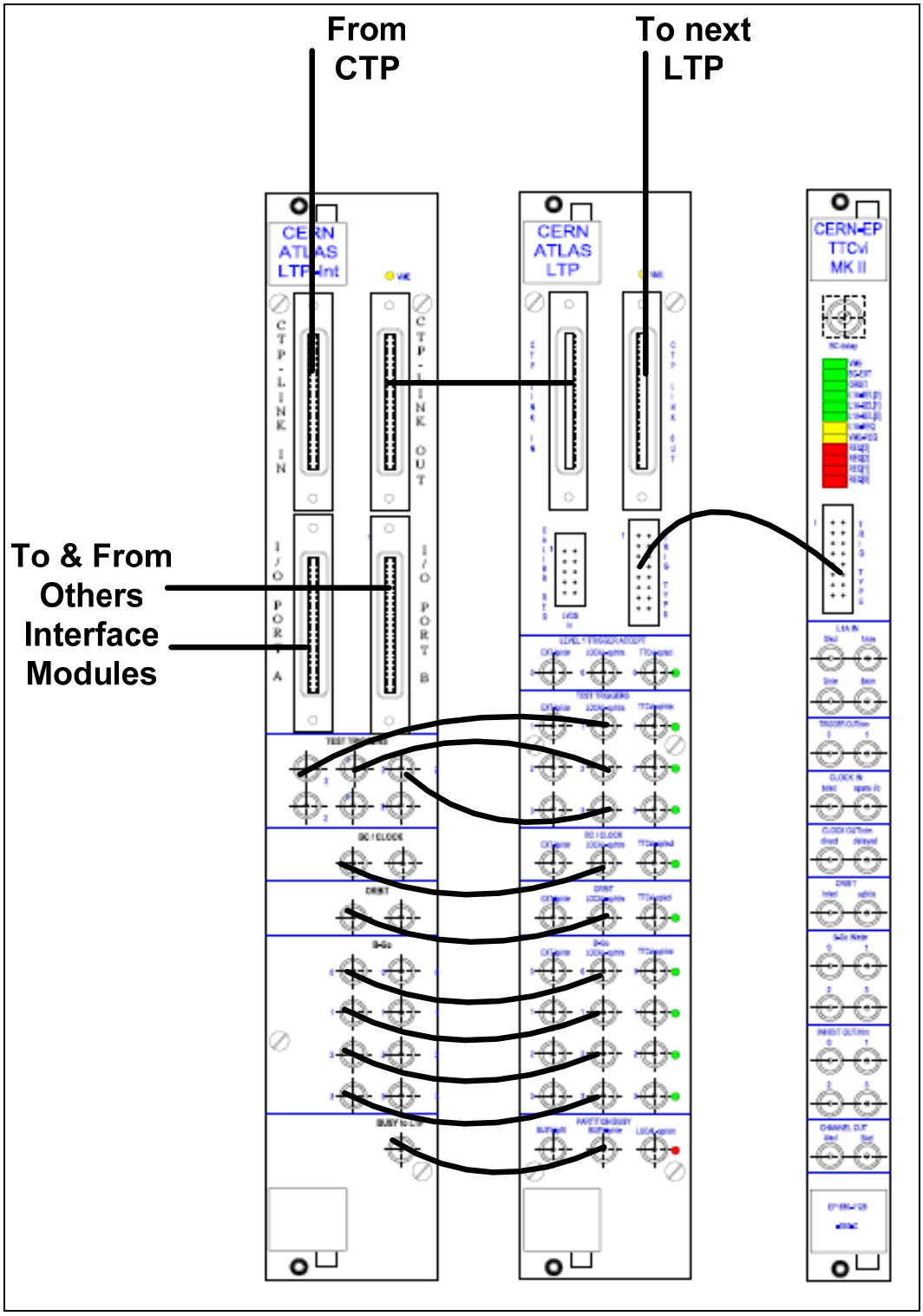

Figure 6. Interconnections Interface – LTP. The standard connections LTP – TTCvi are not affected and not shown on this figure (at the exception of the Trigger-Type).

10. References

[1] The ATLAS LTP in Proceedings of the 10th Workshop on Electronics for LHC Experiments and Future Experiments. Available at http://lhc-workshop-2004.web.cern.ch/lhc%2Dworkshop%2D2004/5-Posters/65-farthouat_proceedings.pdf

[2] ATLAS LTP Hardware Manual. https://edms.cern.ch/cedar/plsql/doc.info?cookie=3684697&document_id=551992&version=2

[3] ATLAS LTP EDMS site https://edms.cern.ch/cedar/plsql/navigation.tree?cookie=3684697&top=1630162406&open=1630162406