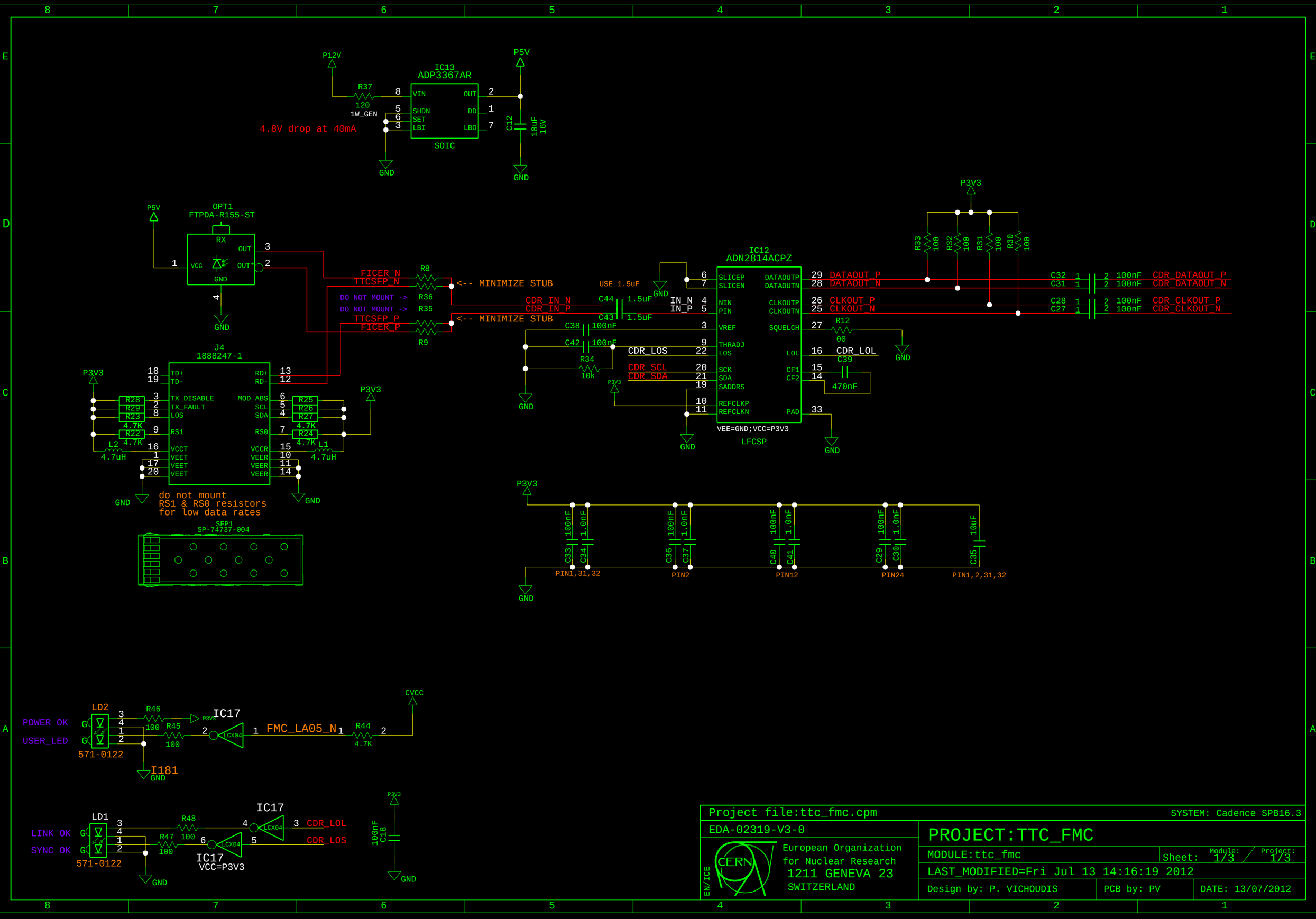
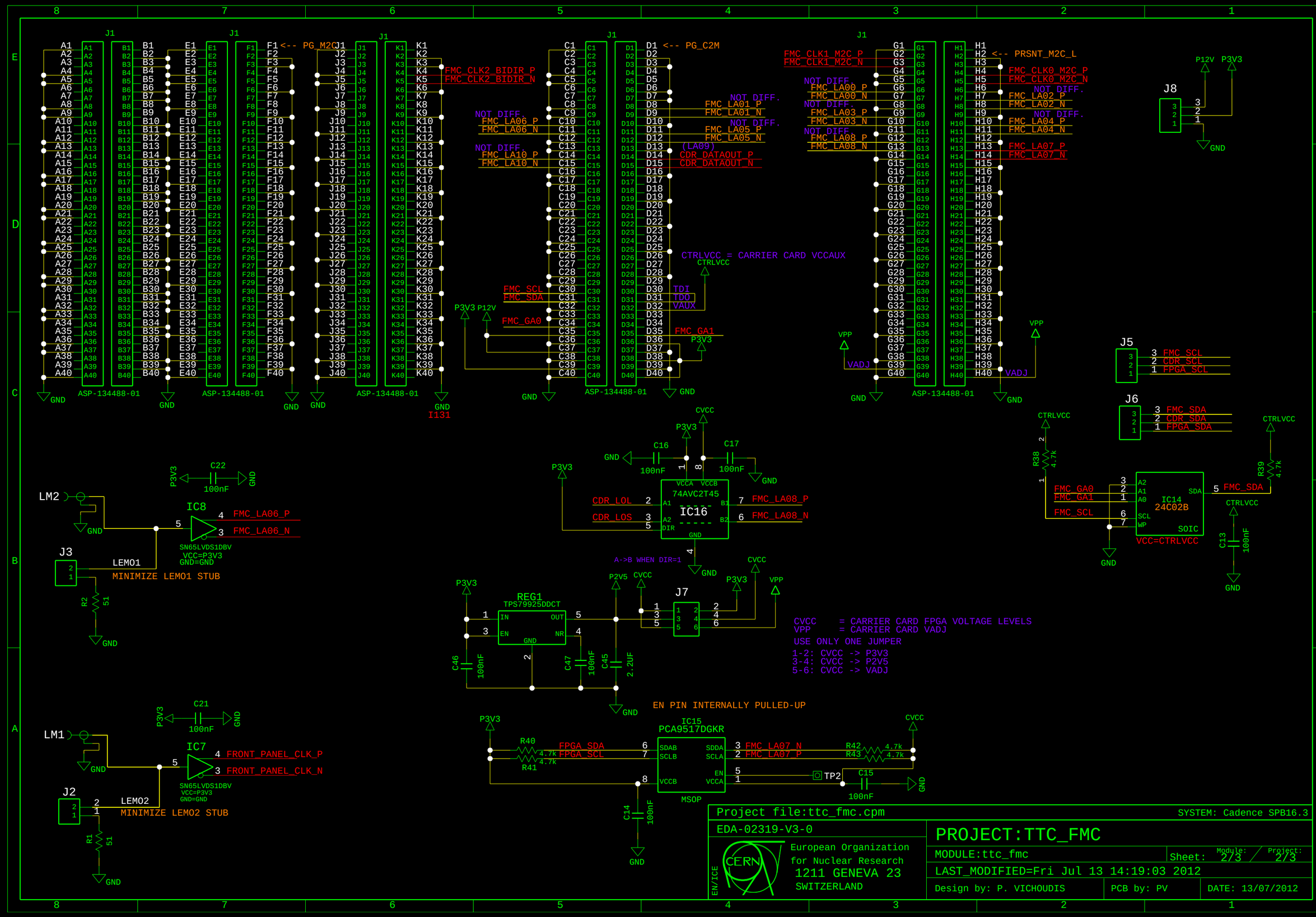


Project file:ttc_fmc.cpm		SYSTEM: Cadence SPB16.3
EDA-02319-V3-0		PROJECT:TTC_FMC
European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND		MODULE:ttc_fmc
		Sheet: Module: 1/3 Project: 1/3
		LAST_MODIFIED=Fri Jul 13 14:16:19 2012
	Design by: P. VICHOUDIS	PCB by: PV DATE: 13/07/2012


J1
ASP-134488-01
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 A21 A22 A23 A24 A25 A26 A27 A28 A29 A30 A31 A32 A33 A34 A35 A36 A37 A38 A39 A40
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20 B21 B22 B23 B24 B25 B26 B27 B28 B29 B30 B31 B32 B33 B34 B35 B36 B37 B38 B39 B40
E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17 E18 E19 E20 E21 E22 E23 E24 E25 E26 E27 E28 E29 E30 E31 E32 E33 E34 E35 E36 E37 E38 E39 E40
F1 F2 F3 F4 F5 F6 F7 F8 F9 F10 F11 F12 F13 F14 F15 F16 F17 F18 F19 F20 F21 F22 F23 F24 F25 F26 F27 F28 F29 F30 F31 F32 F33 F34 F35 F36 F37 F38 F39 F40
J1 J2 J3 J4 J5 J6 J7 J8 J9 J10 J11 J12 J13 J14 J15 J16 J17 J18 J19 J20 J21 J22 J23 J24 J25 J26 J27 J28 J29 J30 J31 J32 J33 J34 J35 J36 J37 J38 J39 J40
K1 K2 K3 K4 K5 K6 K7 K8 K9 K10 K11 K12 K13 K14 K15 K16 K17 K18 K19 K20 K21 K22 K23 K24 K25 K26 K27 K28 K29 K30 K31 K32 K33 K34 K35 K36 K37 K38 K39 K40
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40
D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23 D24 D25 D26 D27 D28 D29 D30 D31 D32 D33 D34 D35 D36 D37 D38 D39 D40
G1 G2 G3 G4 G5 G6 G7 G8 G9 G10 G11 G12 G13 G14 G15 G16 G17 G18 G19 G20 G21 G22 G23 G24 G25 G26 G27 G28 G29 G30 G31 G32 G33 G34 G35 G36 G37 G38 G39 G40
H1 H2 H3 H4 H5 H6 H7 H8 H9 H10 H11 H12 H13 H14 H15 H16 H17 H18 H19 H20 H21 H22 H23 H24 H25 H26 H27 H28 H29 H30 H31 H32 H33 H34 H35 H36 H37 H38 H39 H40
GND
F1 <-- PG_M2C
FMC_CLK2_BIDIR_P
FMC_CLK2_BIDIR_N
NOT DIFF.
FMC_LA06_P
FMC_LA06_N
NOT DIFF.
FMC_LA10_P
FMC_LA10_N
FMC_SCL
FMC_SDA
FMC_GA0
D1 <-- PG_C2M
NOT DIFF.
FMC_LA01_P
FMC_LA01_N
NOT DIFF.
FMC_LA05_P
FMC_LA05_N
(LA09)
CDR_DATAOUT_P
CDR_DATAOUT_N
TDI
TDO
VAUX
CTRLVCC
CTRLVCC = CARRIER CARD VCCAUX
FMC_GA1
P3V3
P12V
FMC_CLK1_M2C_P
FMC_CLK1_M2C_N
NOT DIFF.
FMC_LA00_P
FMC_LA00_N
NOT DIFF.
FMC_LA03_P
FMC_LA03_N
NOT DIFF.
FMC_LA08_P
FMC_LA08_N
VPP
VADJ
H1
H2 <-- PRSNT_M2C_L
FMC_CLK0_M2C_P
FMC_CLK0_M2C_N
NOT DIFF.
FMC_LA02_P
FMC_LA02_N
NOT DIFF.
FMC_LA04_P
FMC_LA04_N
FMC_LA07_P
FMC_LA07_N
J8
P12V P3V3
GND
J5
3 FMC_SCL
2 CDR_SCL
1 FPGA_SCL
J6
3 FMC_SDA
2 CDR_SDA
1 FPGA_SDA
CVCC
P3V3
C16 100nF
C17 100nF
GND
CDR_LOL
CDR_LOS
74AVC2T45
IC16
VCCA VCCB
A1 A2 DIR
B1 B2
FMC_LA08_P
FMC_LA08_N
A->B WHEN DIR=1
R38 4.7k
R39 4.7k
FMC_GA0
FMC_GA1
FMC_SCL
IC14
24C02B
SOIC
A2 A1 A0 SCL WP SDA
FMC_SDA
VCC=CTRLVCC
C13 100nF
LM2
IC8
FMC_LA06_P
FMC_LA06_N
SN65LVDS1DBV
VCC=P3V3
GND=GND
J3
LEMO1
MINIMIZE LEMO1 STUB
R2 51
C22 100nF
REG1
TPS79925DDCT
IN OUT EN NR GND
P2V5
J7
C46 100nF
C47 100nF
C45 2.2UF
CVCC = CARRIER CARD FPGA VOLTAGE LEVELS
VPP = CARRIER CARD VADJ
USE ONLY ONE JUMPER
1-2: CVCC -> P3V3
3-4: CVCC -> P2V5
5-6: CVCC -> VADJ
EN PIN INTERNALLY PULLED-UP
LM1
IC7
FRONT_PANEL_CLK_P
FRONT_PANEL_CLK_N
SN65LVDS1DBV
VCC=P3V3
GND=GND
J2
LEMO2
MINIMIZE LEMO2 STUB
R1 51
C21 100nF
IC15
PCA9517DGKR
MSOP
SDAB SCLB VCCB
SDDA SCLA EN VCCA
FPGA_SDA
FPGA_SCL
FMC_LA07_N
FMC_LA07_P
R40 4.7k
R41 4.7k
R42 4.7k
R43 4.7k
TP2
C15 100nF
C14 100nF
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1211 GENEVA 23
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Design by: P. VICHOUDIS
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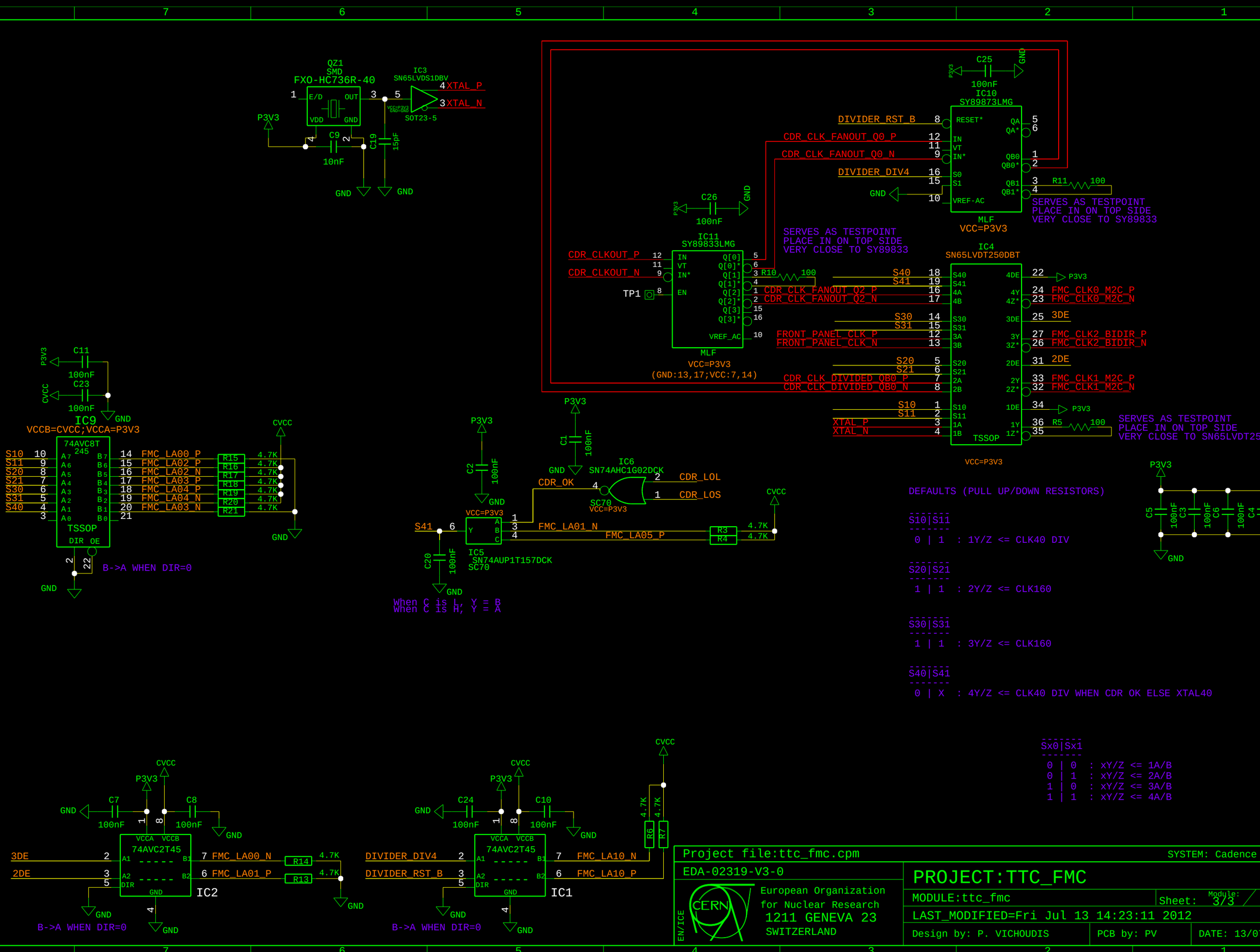

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SWITZERLAND
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PROJECT:TTC_FMC

MODULE:ttc_fmc — Sheet: Module: 3/3 Project: 3/3

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Design by: P. VICHOUDIS | PCB by: PV | DATE: 13/07/2012