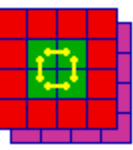# Preliminary Design Review:
Hub Implementation

Dan Edmunds, Wade Fisher,

Yuri Ermoline, Philippe Laurens

Michigan State University
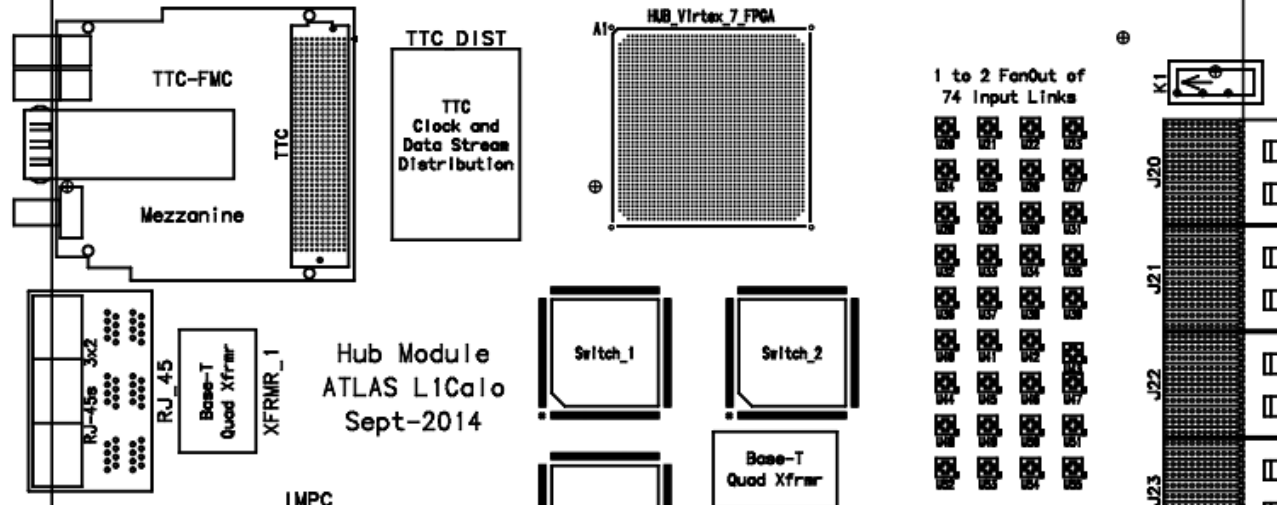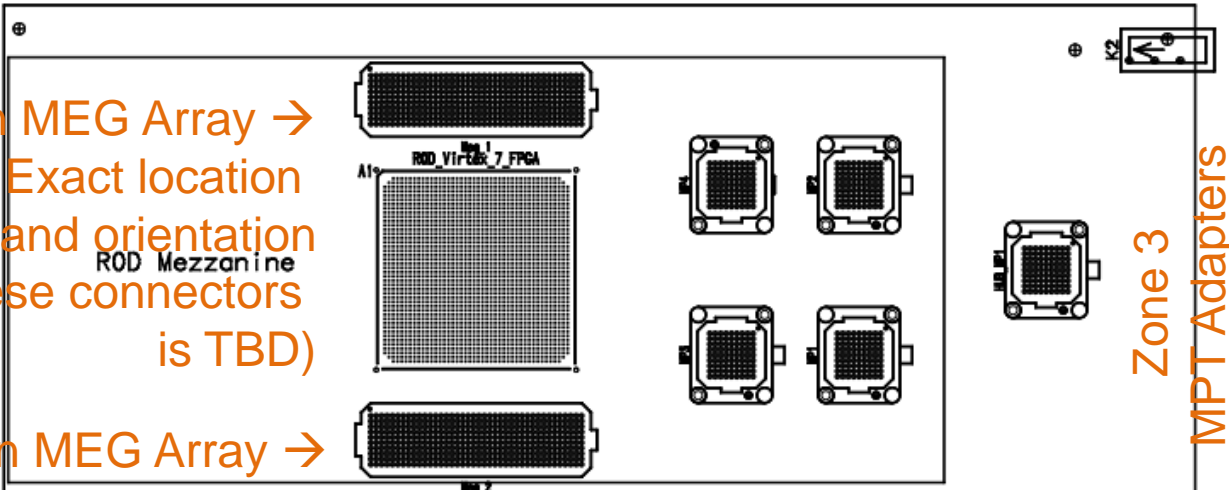
01-Oct-2014

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Outline: follow Hub Main functions

❑ Support for Daughter Cards
- ROD (& IPMC)

❑ High-Speed Readout Data Streams
- Hub's main function: data path from FEXs to ROD

❑ Un-managed Ethernet Switch
- Gigabit Ethernet to Node Slots (et al) via Basic Interface

❑ LHC Clock and TTC Data Stream distribution

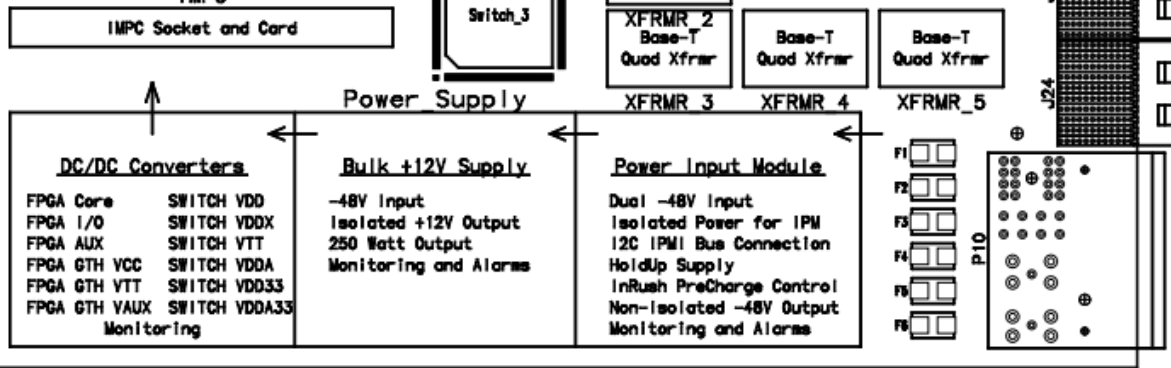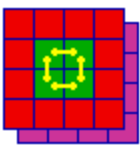**MICHIGAN STATE**
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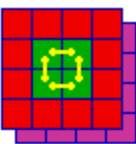
400 pin MEG Array → (Exact location and orientation of these connectors is TBD)

400 pin MEG Array →

IPMC → (needs to be rotated 90 degree for proper airflow)

Zone 3

MPT Adapters

ROD_Virtex_7_FPGA

ROD Mezzanine

HUB_Virtex_7_FPGA

TTC-FMC

TTC

Mezzanine

TTC DIST

TTC Clock and Data Stream Distribution

1 to 2 FanOut of 74 Input Links

RJ-45s 3x2

RJ 45

Base-T Quad Xfrmr

XFRMR_1

Hub Module ATLAS L1Calo Sept-2014

Switch_1

Switch_2

Switch_3

Base-T Quad Xfrmr

XFRMR_2 Base-T Quad Xfrmr

Base-T Quad Xfrmr

Base-T Quad Xfrmr

IMPC

IMPC Socket and Card

Power_Supply

XFRMR 3   XFRMR 4   XFRMR 5

DC/DC Converters		Bulk +12V Supply	Power Input Module
FPGA Core	SWITCH VDD	-48V Input	Dual -48V Input
FPGA I/O	SWITCH VDDX	Isolated +12V Output	Isolated Power for IPM
FPGA AUX	SWITCH VTT	250 Watt Output	I2C IPMI Bus Connection
FPGA GTH VCC	SWITCH VDDA	Monitoring and Alarms	HoldUp Supply
FPGA GTH VTT	SWITCH VDD33		InRush PreCharge Control
FPGA GTH VAUX	SWITCH VDDA33		Non-Isolated -48V Output
Monitoring			Monitoring and Alarms

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3

Hub Daughter Cards

❑ **Motherboard for ROD mezzanine**

- Two 400-pin MEG Array connectors (low profile)
  - All Readout Data Streams (72 from FEXs, 76 total, more details later)
  - LHC Clock and TTC data stream to ROD
  - Optional readout control data from ROD
  - 8-bit Geographical Address to ROD specifying the Slot and Shelf ID
  - 1000Base-T connection to IPBus Ethernet switch
  - I2C bus and JTAG connections
  - 12V bulk power and power control/status signals
- Pin allocation on MEG array under way
  - Will let the relative position and polarity of all MGT signals "float" and be determined by the cleanest routing of these traces on ROD & Hub
- Hub's front panel has a cutout for ROD's own front panel
- MPT adapters on Hub in Zone 3 (or protruding) to mate with an RTM

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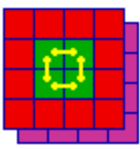
# Hub Daughter Cards (2)

❑ TTC-FMC

- **Temporary** until TTC information available over GBT (more details later)
  - Hub provides power
  - Hub receives a **40.08 MHz LHC Clock** , cleaned on Hub before fan out
  - Hub receives a **TTC control data stream**, further processed on Hub FPGA

❑ IPMC "mezzanine" (DIMM-style)

- ATCA slot power management
- I2C bus for environment monitoring (voltages, currents, temperatures)
- **We are counting on the IPMC to retrieve the Shelf ID from the Shelf Manager and make it available on user pins**
- its Ethernet port is connected on Hub, but likely not supported by LAPP

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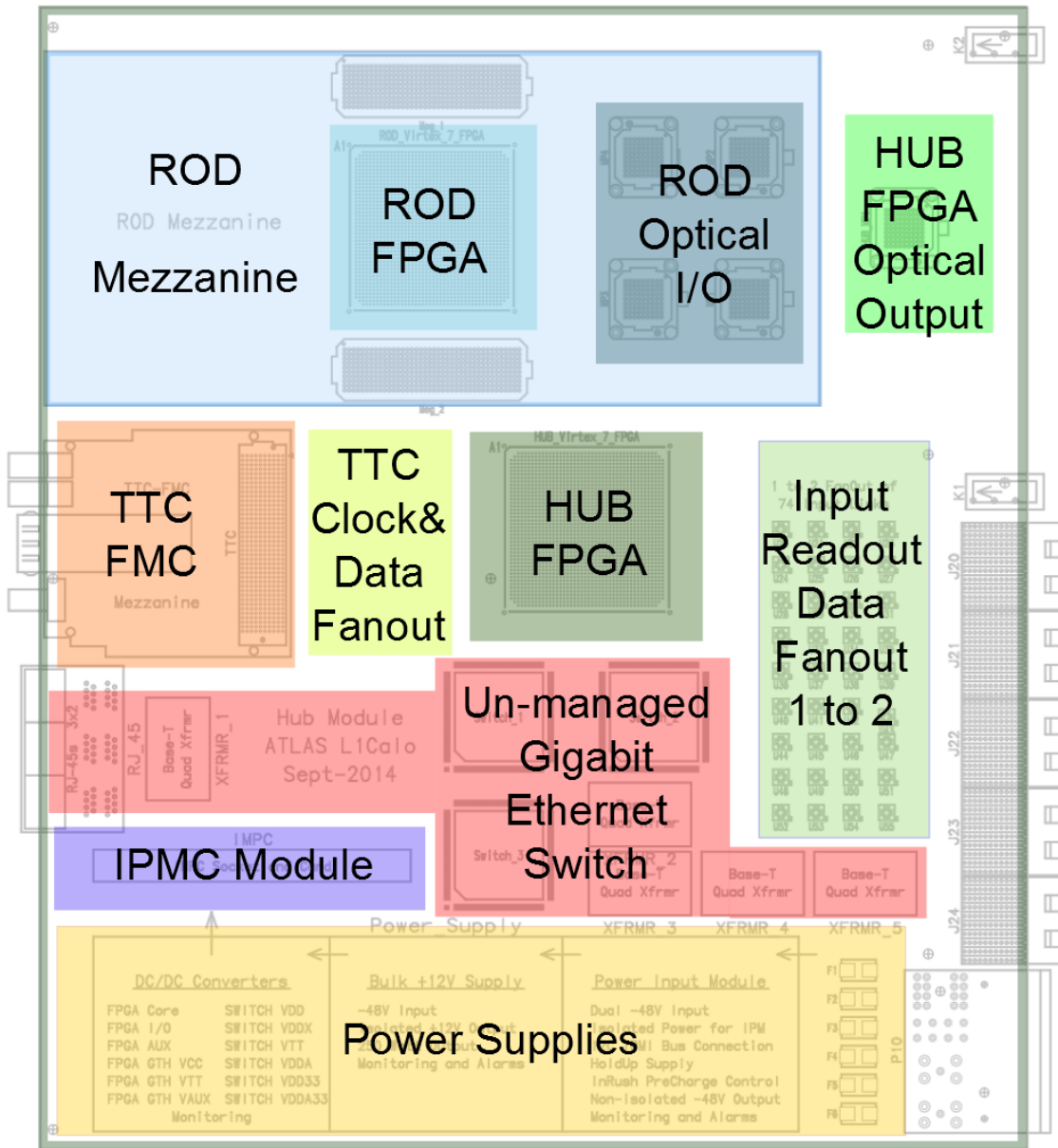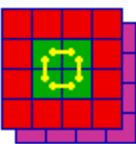
L1Calo HUB Module
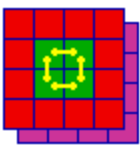
High-Speed Readout Data Streams

❑ 6x readout data streams from each FEX (6x12=72)

    – High speed differential lines via Fabric Interface

    – Speed TBD: likely 6.4 or 9.6 Gbps

❑ Hub fans out all readout streams from backplane

    – One copy sent to ROD, One copy to Hub FPGA

❑ Optional readout data streams from Hub FPGAs

    – 2x data streams from local Hub FPGA

    – 2x data streams from other Hub FPGA (over Fabric Interf.)

    – Routed to ROD connector while ROD resources TBD

→ Both ROD & Hub FPGAs see all readout data
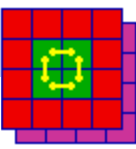
Hub-Module Readout Data Distribution
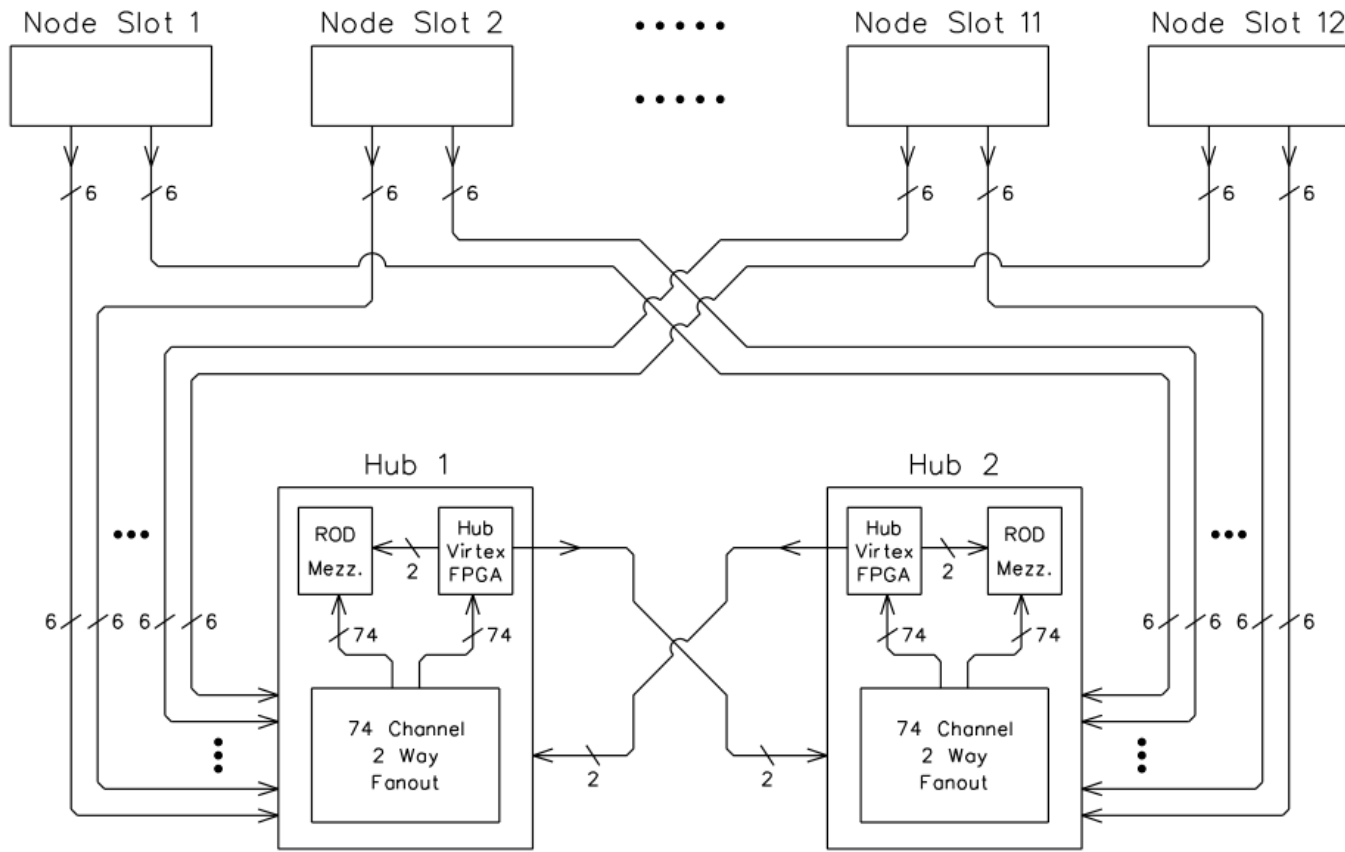
Each line indicates six Fabric Interface Channels carrying Node Slot Readout Data to the ROD's and to the Hub-Module's Virtex FPGAs
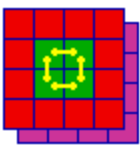
Hub to Hub Links use the Fabric Interface.

The Node Slot Readout Data on each Fabric Interface Channel is received by a GTH Transceiver on both the ROD's and the Hub-Module's Virtex FPGAs

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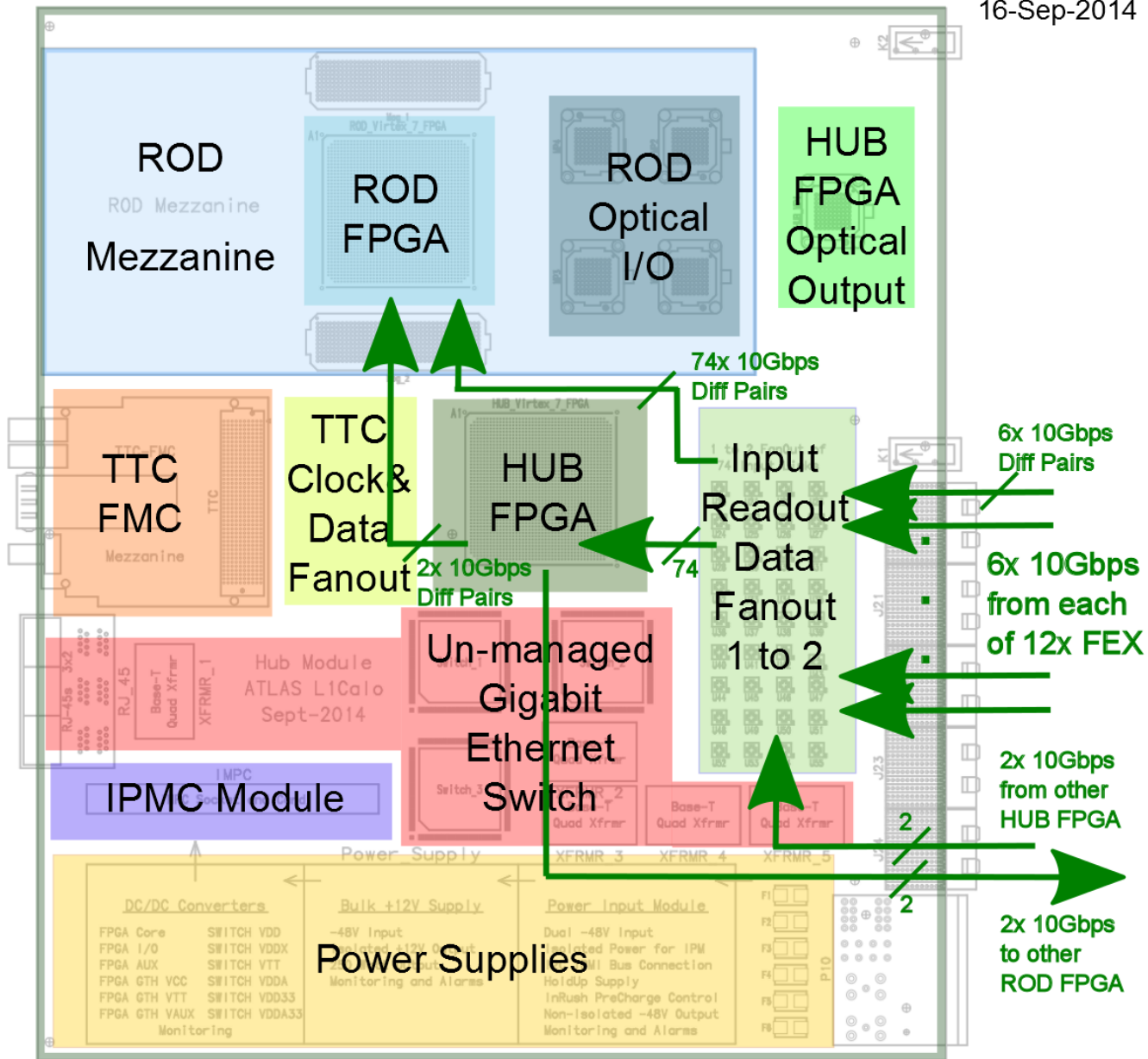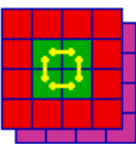
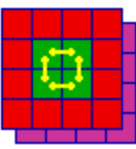L1Calo HUB Module **ROD Readout path including HUB Data**

Ethernet Switch

☐ Un-managed 1Gb Ethernet switch on each Hub

– Up-link via front panel RJ45 (or multiple up-links)

– Connection to each FEX via Basic Interface

– Connection to other Hub FPGA via Service Interface

– Connection to Hub ROD and Hub IPMC via front panel

– **New: No connection from Hub switch to ATCA Shelf Manager**

– Use 3 or 4 Broadcom or Marvel 6-8 port GE switch chips

☐ Hub-1's switch for Control subnet via IPbus

☐ Hub-2's switch for IPMC subnet

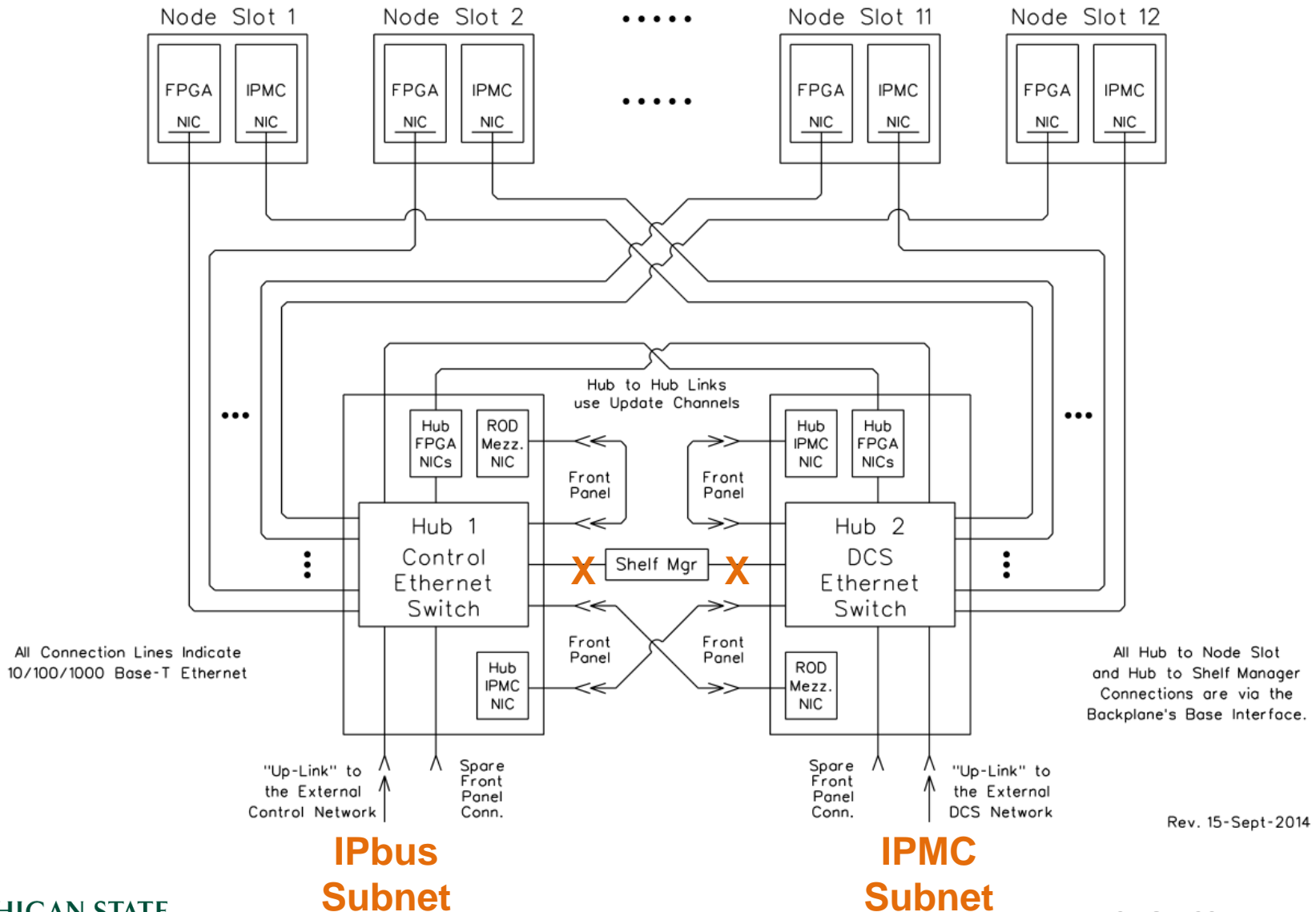– Subject to IPMC capabilities; **New understanding: may remain unused**

New understanding :

DCS has independent direct Ethernet connection to Shelf Manager
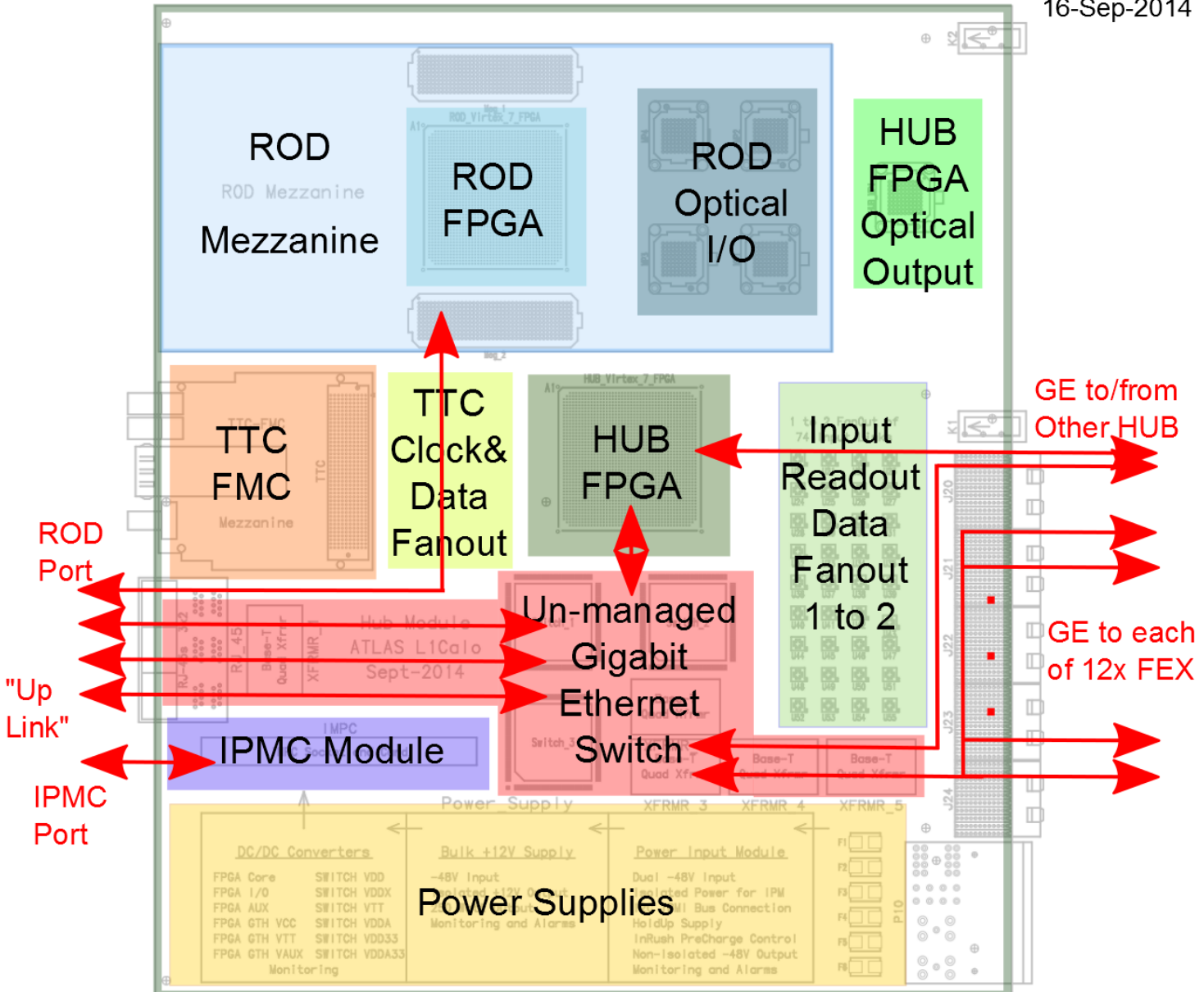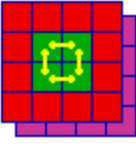
• For basic environment measurements (I, V, temp); I2C via IPMC and Zone 1 IPMB

• Higher level measurements also available to DCS via IPbus

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Hub-Module Ethernet Switch Connections

ROD Mezzanine

ROD FPGA

ROD Optical I/O

HUB FPGA Optical Output

TTC FMC

TTC Clock& Data Fanout

HUB FPGA

Input Readout Data Fanout 1 to 2

GE to/from Other HUB

ROD Port

"Up Link"

Un-managed Gigabit Ethernet Switch

IPMC Module

IPMC Port

GE to each of 12x FEX

Power Supplies

L1Calo HUB Module   Gigabit Ethernet (GE) Connections

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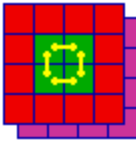
LHC Clock and TTC Data Stream

❑ Receives and distributes the 40.08 MHz LHC Clock & TTC control data stream

– All 12x node slot FEXs

– ROD & Hub FPGA on Hub-1

– ROD & Hub FPGA on Hub-2

– via Fabric Interface

– TTC data stream format defined elsewhere

❑ Only Hub-1 distributes LHC Clock & TTC Data Stream

– Hub-2 circuitry is just as capable; but not used in base plan

❑ Optional merging of readout flow control information from RODs of both Hub-1 &Hub-2
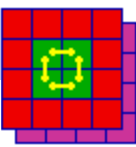
– Optional feature, may not be needed

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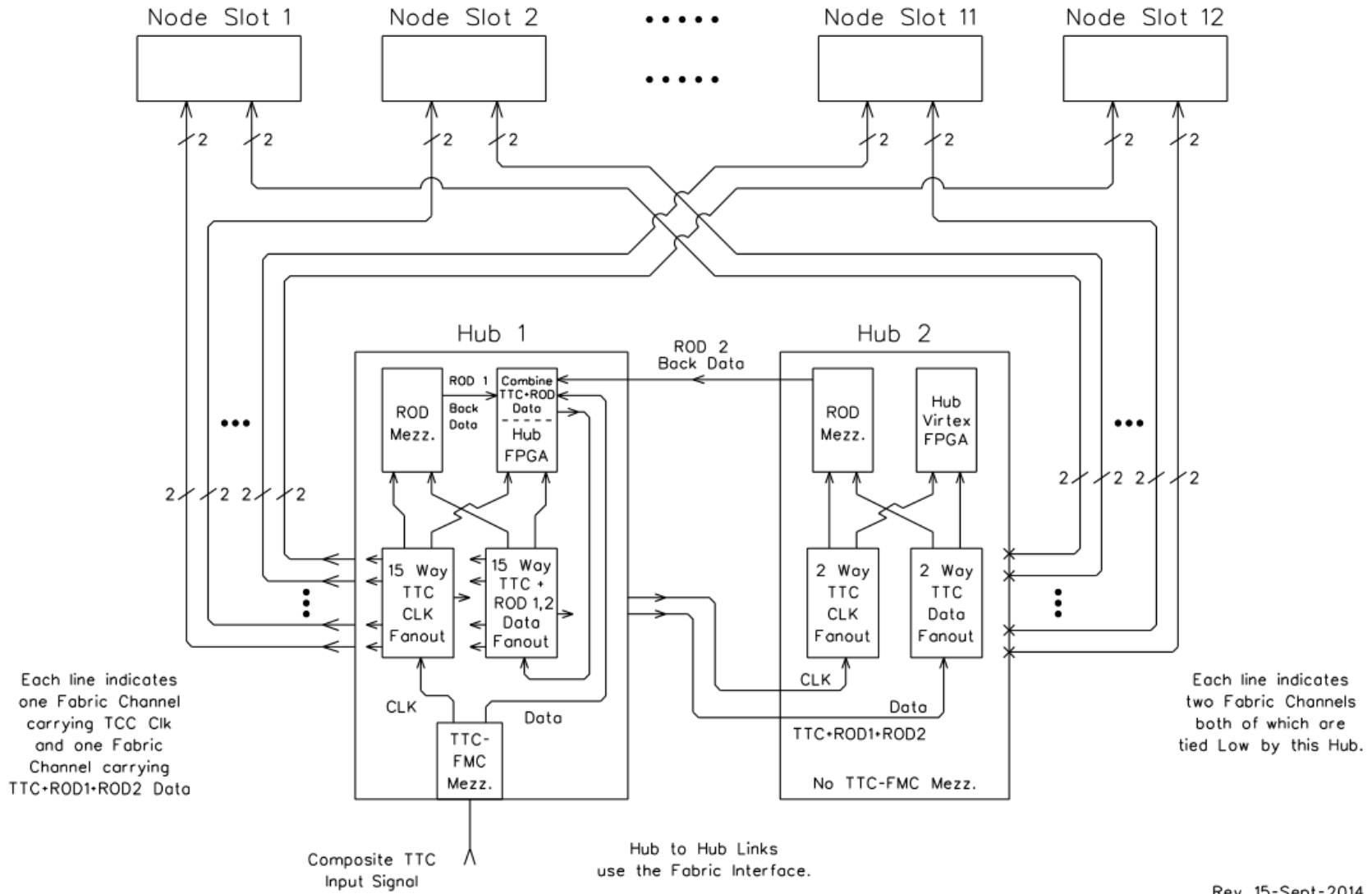**U N I V E R S I T Y**
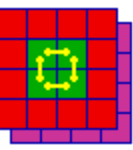
LHC Clock and TTC Data Stream (2)

❑ Prototype stage (2015): use TTC-FMC

- We now understand: no benefit by waiting for FELIX FMC
- **But** need to secure enough TTC-FMCs for prototype stage
  - More details later on

New since PDR document:

❑ Ready for future TTC input media (201?): GBT fiber

- Add **one SFP transceiver** on Hub with (at least) its receiver section connected to a GTH input on the Hub FPGA.
- Firmware provided to recover LHC clock and TTC data stream
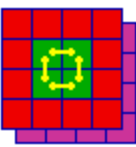
Hub-Module TTC Distribution

Node Slot 1 Node Slot 2 • • • • • Node Slot 11 Node Slot 12

Hub 1

ROD Mezz.

ROD 1 Back Data

Combine TTC+ROD Data

Hub FPGA

ROD 2 Back Data

Hub 2

ROD Mezz.

Hub Virtex FPGA

15 Way TTC CLK Fanout

15 Way TTC + ROD 1,2 Data Fanout

2 Way TTC CLK Fanout

2 Way TTC Data Fanout

CLK

Data

CLK

Data

TTC-FMC Mezz.

TTC+ROD1+ROD2

No TTC-FMC Mezz.

Composite TTC Input Signal

Hub to Hub Links use the Fabric Interface.

Each line indicates one Fabric Channel carrying TCC Clk and one Fabric Channel carrying TTC+ROD1+ROD2 Data

Each line indicates two Fabric Channels both of which are tied Low by this Hub.

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# LHC Clock and TTC Data Stream (3)

New: Alternate Proposal

- TTC-FMC is a **temporary** and **"bulky"** solution
  - Only used during early tests
  - FMC footprint is and will remain unusable for anything else
- Board space for Hub's own functionality is scarce resource

→ Proposal: **No TTC-FMC on Hub** (i.e. only SFP for GBT)

- Still always provide a clean 40.08 MHz clock to whole crate
- Hub FPGA Firmware would **emulate TTC data stream**
  - Minimum: L1Accept and Beam Crossing Reset (what else?)
  - Controlled via IPbus, e.g. L1A "on demand" or "prescaled"

Is this sufficient for all tests of FEXs & ROD at prototype stage?

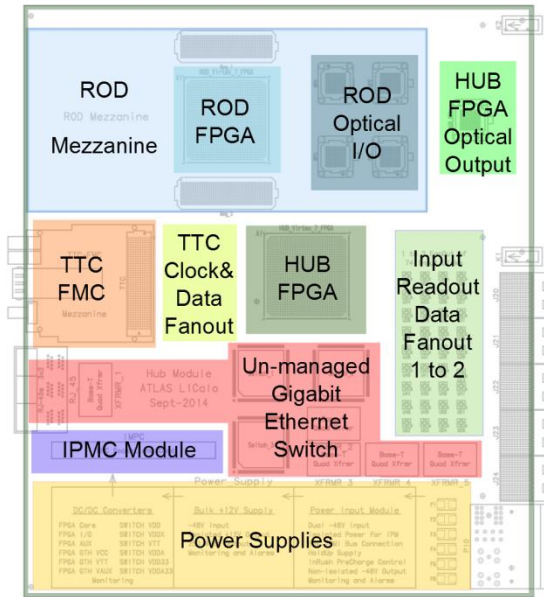- Is such emulation **sufficient until GBT input available?**

HUB website

Hub-Module TTC Distribution
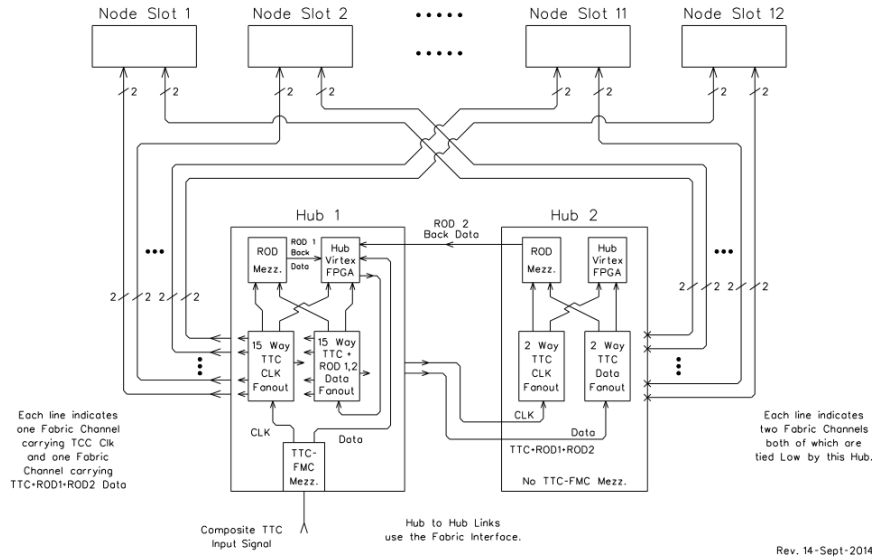
L1Calo HUB Module

http://www.pa.msu.edu/hep/atlas/l1calo/
http://www.pa.msu.edu/hep/atlas/l1calo/hub/
http://www.pa.msu.edu/hep/atlas/l1calo/hub/hardware/drawings/
http://www.pa.msu.edu/hep/atlas/l1calo/hub/specification**1_preliminary_design_review/**

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