Technical Specification

ATLAS Level-1 Calorimeter Trigger Upgrade

FEX System Switch Module (FEX Hub) Prototype

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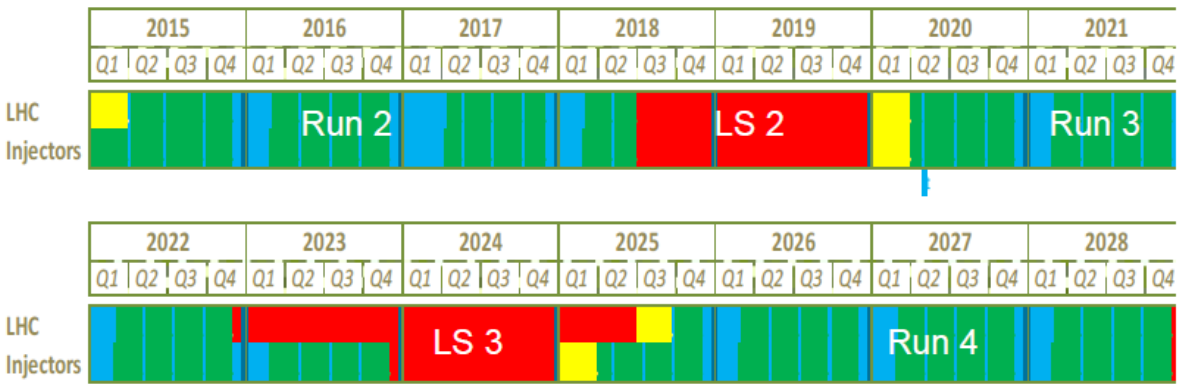
Contents

1 Conventions

The following conventions are used in this document:

- The term “Hub” or “FEX-Hub” is used to refer to the Phase-I L1Calo FEX system ATCA switch (hub) module in the rest of this document.
- The L1Calo FEX system Readout Driver (ROD) mezzanine is referred to as the “Hub-ROD” or just “ROD” in this document.
- FEX-Hub modules can be physically located in logical slots 1 or 2. The convention for the remainder of this document is to refer to these different modules as Hub-1 and Hub-2, respectively.
- The convention in this document will be that Hub-1 is the host of the TTC-FMC mezzanine card.
- A programmable parameter is defined as one that can be altered under computer control, for example between runs, not on an event-by-event basis. Changing such a parameter does not require a re-configuration of any firmware.
- Where multiple options are given for a link speed, for example, the readout links of the FEX modules are specified as running ≤6.4 Gb/s, this indicates that the link speed has not yet been fully defined. Once it is defined, that link will run at a single speed.
- In accordance with the ATCA convention, a crate of electronics is here referred to as a shelf.
- Figure 1 explains the timeline for ATLAS running and shutdowns: Phase-I upgrades will be installed before the end of long shutdown LS 2; Phase-II upgrades will be installed before the end of LS 3.



- **Figure 1**: LHC Shutdown and Run Schedule

- The term "*buffer"* is used to mean electrical reception and re-transmission of signals (possibly with fan-out), but without any storage or memory function. The terms "*storage buffer*", "*FIFO*", "*Dual Port RAM*" et al. are used where storage is involved.

2 Related Documents

[1.1] ATLAS TDAQ System Phase-I Upgrade Technical Design Report, CERN-LHCC-2013-018, http://cds.cern.ch/record/1602235/files/ATLAS-TDR-023.pdf

[1.2] L1Calo Phase-I eFEX Specification *(v0.1)*, twiki.cern.ch/twiki/pub/Atlas/LevelOneCaloUpgradeModules/eFEX_spec_v0.2.pdf

[1.3] L1Calo Phase-I jFEX Specification *(v0.2)*, *http://www.staff.uni-mainz.de/rave/jFEX_PDR/jFEX_spec_v0.2.pdf*

[1.4] L1Calo gFEX Specification *(not yet available)*

[1.5] L1Calo Hub-ROD Specification (*v0_9_5*), https://edms.cern.ch/file/1404559/2/Hub-ROD_spec_v0_9_5.docx

[1.6] L1Calo Phase-I Optical plant Specification *(not yet available)*

[1.7] ATCA Short Form Specification, http://www.picmg.org/pdf/picmg_3_0_shortform.pdf

[1.8] PICMG 3.0 Revision 3.0 AdvancedTCA Base Specification, *access controlled*, http://www.picmg.com/

[1.9] TTC-FMC Specification (*not yet available*) https://edms.cern.ch/nav/EDA-02319-V3-0

[1.10] GBT Specification (*not yet available*) http://indico.cern.ch/event/170595/session/53/material/slides/0?contribId=104

[1.11] Development of an ATCA IPMI controller mezzanine board to be used in the ATCA developments for the ATLAS Liquid Argon upgrade, http://cds.cern.ch/record/1395495/files/ATL-LARG-PROC-2011-008.pdf

[1.12] IPbus Protocol, https://svnweb.cern.ch/trac/cactus/export/trunk/doc/ipbus_protocol_v2_0.pdf

[1.13] Front-End Link Exchange (Felix), https://edms.cern.ch/document/13111772/1

3 Introduction

This document describes the ATCA switch module (FEX-Hub) of the ATLAS Level-1 Calorimeter Trigger Processor (L1Calo) system [1.1] . The FEX-Hub is one of several modules being designed to upgrade L1Calo, providing the increased discriminatory power

necessary to maintain trigger efficiency as the LHC luminosity is increased beyond that for which ATLAS was originally designed.

The function of the FEX-Hub module is to provide common communications functions for the FEX ATCA shelves including the routing of FEX readout data, network communications to and from FEX modules and distribution of clock and control signals.

The FEX-Hub modules will be installed in L1Calo during the long shutdown LS2, as part of the Phase-1 upgrade, and will operate during Run 3. They will remain in the system after the Phase-2 upgrade in LS3, and will operate during Run 4, at which time they will form part of L0Calo. The following sections provide overviews of L1Calo in Run 3 and L0Calo in Run 4.

This is a specification for a prototype FEX-Hub module. This prototype is intended to exhibit the full functionality of the final module, but with minor differences in external interfaces (*eg, TTC and ROD interfaces may change*). The prototype specification further describes anticipated use cases not critical to the core Hub functionality that represent fall-back options for the L1Calo (L0Calo) readout system if needed. Aside from these differences, the functionality described here can be regarded as that of the final FEX-Hub.

3.1 L1Calo Overview

3.1.1 Overview of the L1Calo System in Phase I (Run 3)

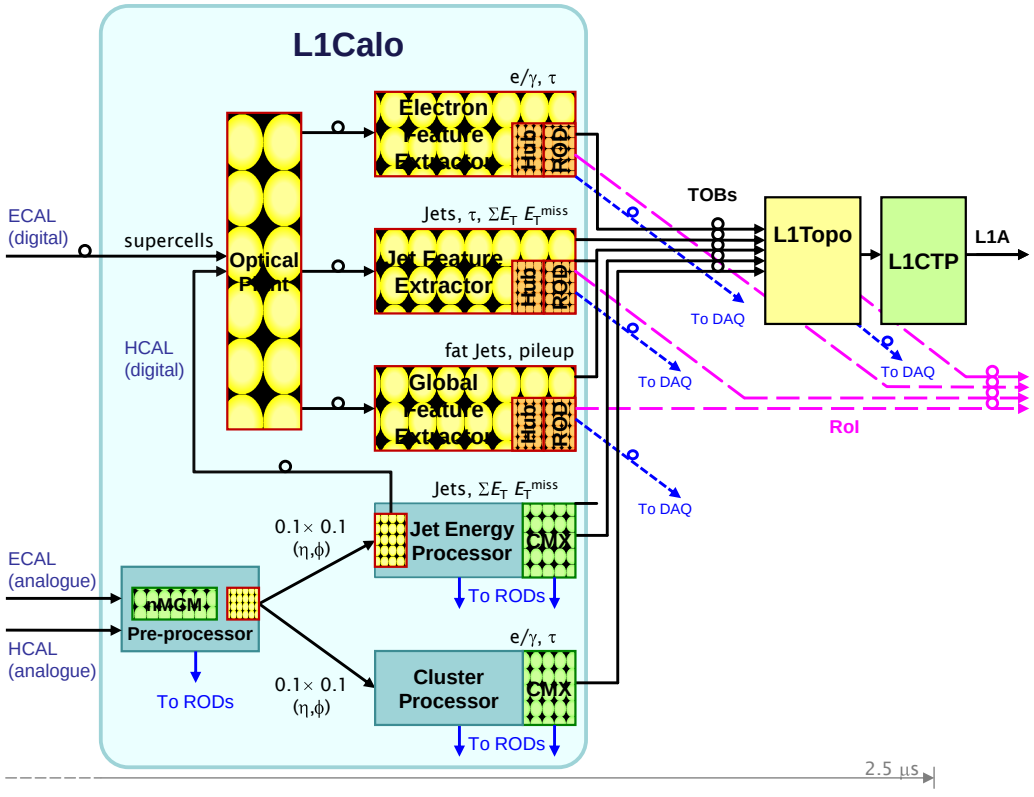


Figure 2: The L1Calo system in Run 3. *Components installed during LS2 are shown in yellow/orange*

In Run 3, L1Calo contains three subsystems installed prior to LS2, as shown in Figure 2 (see document [1.1]):

- the Pre-processor, which receives shaped analogue pulses from the ATLAS calorimeters, digitises and synchronises them, identifies the bunch-crossing from which each pulse originated, scales the digital values to yield transverse energy (E_T), and prepares and transmits the data to the following processor stages;
- the Cluster Processor (CP) subsystem (comprising Cluster Processing Modules (CPMs) and Common Merger Extended Modules (CMXs)) which identifies isolated e/γ and τ candidates;
- the Jet/Energy Processor (JEP) subsystem (comprising Jet-Energy Modules (JEMs) and Common Merger Extended Modules (CMXs)) which identifies energetic jets and computes various local energy sums.

Additionally, L1Calo contains the following three subsystems installed as part of the Phase-I upgrade in LS2:

- The electromagnetic Feature Extractor eFEX subsystem, comprising eFEX modules and FEX-Hub modules, the latter carrying Readout Driver (ROD) daughter cards. The eFEX subsystem identifies isolated e/γ and τ candidates, using data of finer granularity than is available to the CP subsystem.;
- The jet Feature Extractor (jFEX) subsystem, comprising jFEX modules, and Hub modules with ROD daughter cards. The jFEX subsystem identifies energetic jets and computes various local energy sums, using data of finer granularity than that available to the JEP subsystem.
- The global Feature Extractor (gFEX) subsystem, comprising jFEX modules, and Hub modules with ROD daughter cards. The gFEX subsystem identifies calorimeter trigger features requiring the complete calorimeter data.

In Run 3, the Liquid Argon Calorimeter provides L1Calo both with analogue signals (for the CP and JEP subsystems) and with digitised data (for the FEX subsystems). From the hadronic calorimeters, only analogue signals are received. These are digitised on the Pre-processor, transmitted electrically to the JEP, and then transmitted optically to the FEX subsystems. Initially at least, the eFEX and jFEX subsystems will operate in parallel with the CP and JEP subsystems. Once the performance of the FEX subsystems has been validated, the CP sub system will be removed, and the JEP used only to provide hadronic data to the FEX subsystems.

The optical signals from the JEP and LDPS electronics are sent to the FEX subsystems via an optical plant. This performs two functions. First, it separates and reforms the fibre bundles, changing the mapping from that employed by the LDPS and JEP electronics to that required by the FEX subsystems. Second, it provides any additional fan-out of the signals necessary to map them into the FEX modules where this cannot be provided by the calorimeter electronics.

The outputs of the FEX subsystems (plus CP and JEP) comprise Trigger Objects (TOBs): data structures which describe the location and characteristics of candidate trigger objects. The TOBs are transmitted optically to the Level-1 Topological Processor (L1Topo), which

merges them over the system and executes topological algorithms, the results of which are transmitted to the Level-1 Central Trigger Processor (CTP).

The eFEX, jFEX, gFEX and L1Topo subsystems comply with the ATCA standard. The eFEX subsystem comprises two shelves each of 12 eFEX modules. The jFEX subsystem comprises a single ATCA shelf holding 7 jFEX modules. The gFEX subsystem comprises a single ATCA shelf holding a single gFEX module. The L1Topo subsystem comprises a single ATCA shelf housing up to four L1Topo modules, each of which receives a copy of all data from all FEX modules. All L1Calo processing modules produce Region of Interest (RoI) and DAQ readout on receipt of a Level-1 Accept signal from the CTP. RoI information is sent both to the High-Level Trigger (HLT) and the DAQ system, while the DAQ data goes only to the DAQ system. In the FEX and L1Topo subsystems, these data are transmitted by each FEX or L1Topo module via the shelf backplane to two Hub modules. Each of these buffers the data and passes a copy to their ROD daughter board. The RODs perform the processing needed to select and transmit the RoI and DAQ data in the appropriate formats; it is likely that the required tasks will be partitioned between the two RODs. Additionally, the Hub modules provide distribution and switching of the TTC signals and control and monitoring networks.

3.1.2 Overview of the L1Calo System in Phase-II (Run 4)

The Phase-II upgrade will be installed in ATLAS during LS3. At this point, substantial changes will be made to the trigger electronics. All calorimeter input to L1Calo from the electromagnetic and hadronic calorimeters will migrate to digital format, the structure of the hardware trigger will change to consist of two levels, and a Level-1 Track Trigger (L1Track) will be introduced and will require TOB seeding. The Pre-processor, CP and JEP subsystems will be removed, and the FEX subsystems, with modified firmware, will be relabelled to form the L0Calo system in a two stage (Level-0/Level-1) real-time trigger, as shown in Figure 3. Hence, the FEX subsystems must be designed to meet both the Phase-I and Phase-II upgrade requirements. The main additional requirements are to provide real-time TOB data to L1Track, and to accept Phase-II timing and control signals including Level-0 Accept (L0A) and Level-1 Accept. Additional calorimeter trigger processing will be provided by a new L1Calo trigger stage.

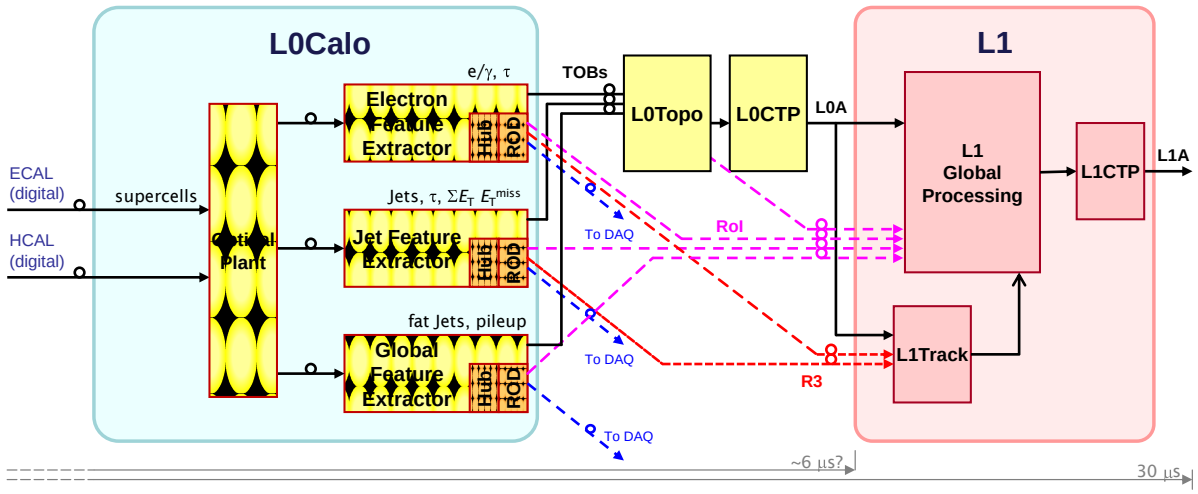


Figure 3: The L0/L1Calo system in Run 4. *The new Level-1 system is shown in red and pink. Other modules (yellow /orange) are adapted from the previous system to form the new L0Calo.*

3.2 FEX-Hub Overview

The FEX-Hub module is an integral part of the L1Calo system. Its primary functions are to support FEX system readout, provide switching functionality for module control and DCS IPbus networks and to distribute timing and control signals to the FEX modules. **Figure 4** shows a sketch of the Hub modules within the FEX ATCA shelves. There are to be two Hub modules per shelf. Both Hub modules will receive high-speed FEX data over the ATCA Fabric Interface, which will be fanned out to a ROD mezzanine on the Hub and to the Hub's own FPGA. This high-speed data path will include two data channels from the other Hub module. The Hub module in logical slot 1 will provide switching capability for a network that routes module control signals on the base interface, while the Hub in logical slot 2 will provide switching for a network that routes DCS information. The Hub module in slot 1 will further host a TTC or GBT mezzanine card, whose signals will be decoded and fanned out to the FEX modules and also the Hub in slot 2. The fanned-out TTC control data stream will be interleaved with ROD-to-FEX communications including, for example, back-pressure signals.

The Hub module has connections to the other slots in the ATCA shelf over three distinct electrical interfaces, as illustrated in **Figure 4**. ATCA backplane Zone-2 consists of the Fabric Interface and the Base Interface. The Fabric Interface provides 8 differential pairs (channels) from each node slot to each Hub slot (8 to Hub-1 and 8 to Hub-2). There are a total of 8 Fabric Interface channels between Hub-1 and Hub-2 (not 16 total). The Fabric Interface pairs have a nominal bandwidth specification of 10 Gbps / channel. The Base Interface provides 4 differential pairs between each node slot and each Hub slot. There are a total of 4 Base Interface channels between Hub-1 and Hub-2. The Base Interface lines have a nominal bandwidth specification of 500 Mbps / channel, suitable for Gbps Ethernet protocol. Finally, ATCA backplane Zone-1 provides each node and Hub slot with a connection to the Intelligent Platform Management Bus (IPMB) with a total bandwidth of 100 kbps.

The L1Calo FEX-Hub system will consist of eight modules. There will be two eFEX shelves, one jFEX shelf and one gFEX shelf.

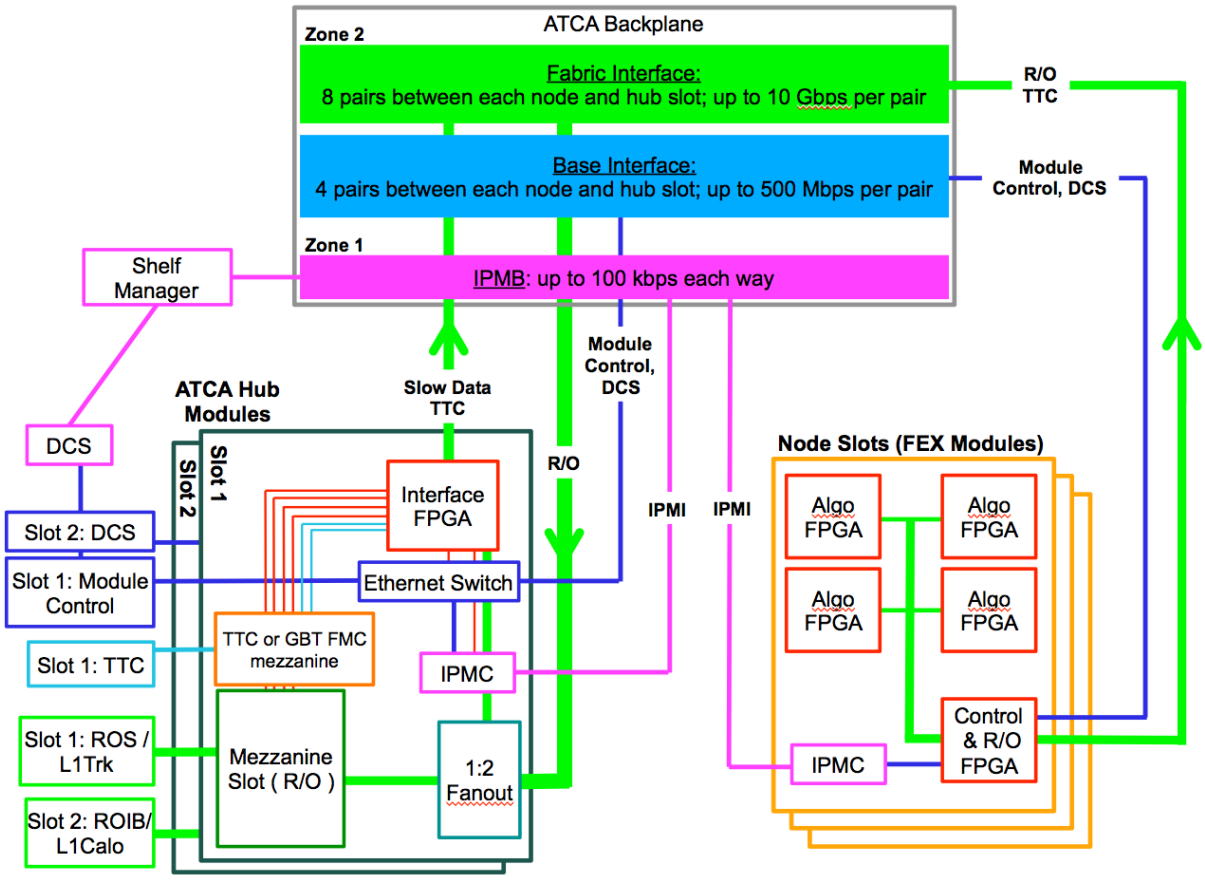


Figure 4: Illustration of the functions of FEX-Hub modules within the FEX readout system.

4 Hub Functionality

This section describes the functionality required for the FEX-Hub module within the L1Calo FEX trigger system. Details of the implementation of these functions will be described in Section 6 of this document.

4.1 Support of the ROD Mezzanine Card

The FEX-Hub physically holds the ROD Mezzanine Card and provides electrical connections to it through two 400 pin Meg-Array connectors.

4.2 FEX and FEX-Hub Readout Data Distribution

The FEX-Hub receives over the Fabric Interface 6 serial streams of Readout Data from each FEX Module. Each FEX-Hub also receives over the Fabric Interface 2 serial streams of Readout Data from the other FEX-Hub in the crate. These 74 high speed serial streams are fanned out on the FEX-Hub. One copy of each stream is sent to the ROD and one copy is sent to the Hub's own Virtex-7 FPGA. The Hub FPGA also sends 2 serial streams with its own Readout Data to its own ROD. Each ROD thus receives a total of 76 high speed

Readout Data streams: 6 streams from each FEX, 2 streams from the local Hub FPGA and 2 streams from the other Hub's Hub FPGA. The data rate per readout stream will be 10 Gbps or less.

4.3 TTC Clock and Data Stream Distribution

The FEX-Hub in Slot 1 uses a TTC-FMC mezzanine card to receive the TTC signals. The FEX-Hub receives two types of signals from the TTC-FMC: a copy of the LHC clock and TTC control data. These signals need to be fanned out to each FEX module, to the local ROD, to the local Hub FPGA and to the FEX-Hub in Slot 2. The LHC clock is directly forwarded without any processing on the FEX-Hub. The TTC control data may need to be merged with additional control information coming from the ROD module from each FEX-Hub before being fanned out. The FEX-Hub uses two ports from the Fabric Interface Channel to each Node Slot to fanout these two signals to each FEX. These two TTC and control signals sent to the FEX plus the 6 Readout Data streams received from each FEX use all 8 signals pairs of each Fabric Channel connecting one FEX to the FEX-Hub, albeit with an unconventional port direction usage.

The FEX-Hub in Slot 2 does not have a TTC-FMC mezzanine card but receives the TTC Clock and the TTC and ROD readout control stream from the FEX-Hub in Slot 1. The FEX-Hub in Slot 2 sends any required ROD readout control data generated by its own ROD to the FEX-Hub in Slot 1 for inclusion in the combined TCC and ROD readout control data stream.

4.4 Ethernet Network Switch

The FEX-Hub hosts an un-managed 10/100/1000 Base-T switch to provide the following 19 Gigabit Ethernet connections:

- 1 connection on the front panel for the "up-link";
- 12 connections to the "FEX Node" modules in this crate via the Base Channel Fabric.
- 1 connection to the ROD on this Hub (or IPMC on the other Hub) via the front panel;
- 1 connection to the ROD on the other Hub (or IPMC on this Hub) via the front panel;
- 1 direct connection to the Hub's Virtex-7 FPGA on this Hub;
- 1 connection to the other Hub's Virtex-7 FPGA via the Update Channel Interface;
- 1 spare front panel connection;

4.5 Slow Control

An IPBus interface is provided for high-level, functional control of the FEX-Hub module. This allows, for example, any firmware parameters to be set, modes of operation to be controlled and monitoring data to be read.

4.6 Connections to the IPMB

The FEX-Hub maintains a connection to the Intelligent Platform Management Bus (IPMB) via an IPM Controller (IPMC) located on the Hub module. Communications between monitorable targets on the Hub, including the ROD mezzanine, are managed via an I2C Bus on the Hub module.

4.7 Power Supplies

The FEX-Hub provides all of the normal ATCA redundant power input, power isolation, and power control from the Shelf Manager via an IPMC card. Bulk +12 Volt power is provided to the ROD Mezzanine Card. Control signals are sent from the Hub to the ROD and Status signals are returned from the ROD to manage the ROD's own power up sequence. DC/DC converters are used to provide the power rails for the Hub itself. The required voltages are supplied to the TTC-FMC card.

4.8 Future Use Cases

The FEX-Hub module is intended to be used in the L1Calo and L0Calo trigger systems through Run 4. As such, future use cases in which the Hub may need to augment the capacity of the FEX-Hub-ROD readout path have been identified. This extra functionality is being implemented on the FEX-Hub so long as it does not complicate the core Hub functions and design. These extra Hub functions are as follows:

- The Hub main FPGA receives a fanned-out copy of all high-speed FEX data being sent to the ROD mezzanine card, allowing at a minimum the monitoring of FEX data. This feature can also support Hub commissioning and diagnostics, as it further provides a Fabric Interface connection to the other Hub module.

- The Hub main FPGA provides additional MGT links to the ROD mezzanine, which will be instrumented on the ROD if sufficient input MGT links are available. Similarly, MGT links from the ROD to the Hub main FPGA are defined on the HUB-ROD interface.

- External data output paths from the Hub main FPGA are provided electrically via Ethernet and optically via one Minipod transmitter. The Minipod socket and routings are implemented by default, but the Minipod transmitter is only installed if required.

Together, this Hub functionality can provide supplemental trigger processing if required. However, all of this functionality could instead be ignored or disabled with no negative impact on the Hub core functions.

4.9 Commissioning and Diagnostic Facilities

The FEX-Hub module provides sufficient Hub-to-Hub electrical connections over the Fabric Interface, Base Interface and front-panel connections to commission and perform standalone diagnostic tests of the Ethernet switching functions, Fabric Interface high-speed data paths and TTC clock/data distribution using either one or two FEX-Hub modules.

4.10 Environment Monitoring

The Hub monitors the voltage and current of every power rail on the board. It also monitors the temperatures of FPGAs, of the Minipod transmitter (if installed), and of other areas of dense logic. Where possible, this is done using sensors embedded in the relevant devices

themselves. Where this is not possible, discrete sensors are used. The voltage and temperature data are collected by the IPMC, via an I2C bus. From there, they are transmitted via ethernet to the ATLAS DCS system. The Hub hardware also allows these data to be transmitted to the DCS via IPMB and the ATCA Shelf Controller, but it is not foreseen that ATLAS will support this route.

4.11 ATCA Form Factor

The FEX-Hub module is an ATCA module, conforming to the PICMG® 3.0 Revision 3.0 specification. The FEX-Hub is only capable of supporting a Dual-Star 14-slot (not 16) ATCA crate. Within the L1calo system some of the Fabric Interface and Update Interface Channel ports are not used according to their conventional ATCA manner.

5 Interfaces to Other L1Calo Modules

The FEX-Hub module has mechanical and electrical connections to three other module types within the L1Calo trigger system: the Hub-ROD Mezzanine card, the e/j/gFEX modules and the other Hub module when used in a shelf with two Hubs. This section describes and illustrates the electrical connections between these modules.

5.1 TTC Clock and Data Stream Interfaces

Figure 5 shows the Hub's distribution of the TTC Clock and Data signals in the context of the other cards in the ATCA shelf. The composite TTC signal is received by a TTC-FMC mezzanine on the Hub-1 card. The TTC Clock is fanned out from the Hub-1 card to all other modules in the shelf (including Hub-2) over the Fabric Interface. The TTC Data is combined with the back data from both ROD-1 and ROD-2 on Hub-1 and this combined data stream is also fanned out from the Hub-1 module over the Fabric Interface. When a second Hub is used as shown in **Figure 5**, no TTC information is sent from Hub-2 to any of the Node slots, as the corresponding Fabric Interface ports are not driven on Hub-2. The Hub-1 and Hub-2 cards are identical printed circuit boards and could support independent fan out of clock and data streams from both Hubs if that were desired in the future. Each Node slot has access to both the Hub-1 and the Hub-2 TTC clock and data streams. L1calo shelves are however currently explicitly defined to provide and use the TTC clock and data information fanned out from Hub-1 only.

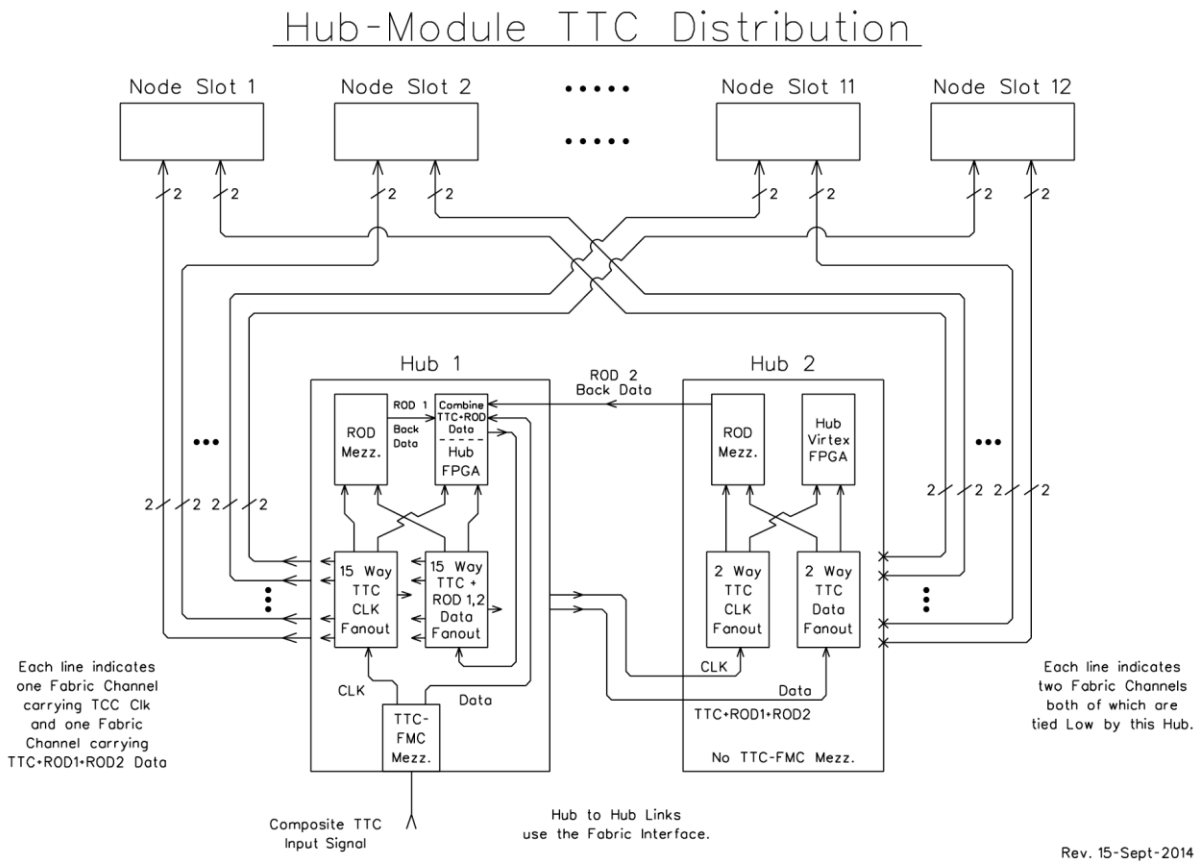


Figure 5: Illustration of FEX-Hub distribution of TTC clock and control data stream signals.

5.2 High-Speed Readout Data Interfaces

Figure 6 shows the Hub's distribution of readout data in the context of the cards in the ATCA shelf. The readout data comes from the Node slots and from the Virtex-7 FPGA on each Hub module. All of this data flows to both the ROD and to the Virtex-7 FPGA on each Hub. The arrangement shown in **Figure 6** supports 2 independent streams of readout data. That is, the readout stream processed by the ROD and Hub FPGA on Hub-1 can be independent of the readout stream flowing into Hub-2.

The Hub's high-speed readout data path as described at the level of the Hub board is illustrated in **Figure 11**, which can be found in the section describing the Hub PCB layout (**Section 7**).

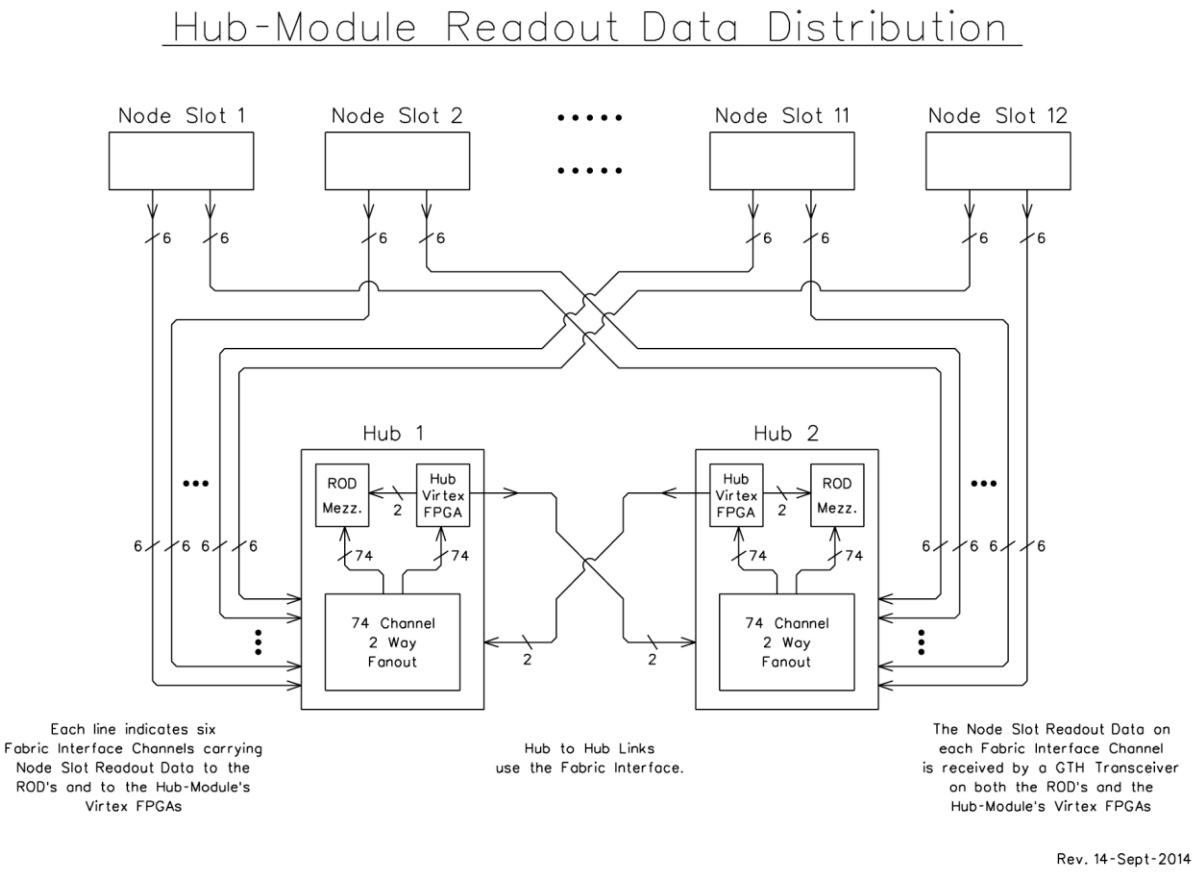


Figure 6: Illustration of FEX-Hub distribution of high-speed data signals.

5.3 Ethernet Network Interfaces

Figure 7 shows the Hub's Base Interface Ethernet Switch in the context of the other cards in the ATCA shelf. As shown in **Figure 7** the switch on Hub-1 is used to handle all connections to the IPbus Control network and the switch on Hub-2 is used to handle all connections to the IPMC/DCS network. Operation with only a Hub-1 in the shelf is possible but does not provide a Base Interface Ethernet connection to the IPMCs in the Node slots. In this situation the Node slot IPMCs can use their IPMB connection to the Shelf Manager and pass monitoring data to the DCS network.

The Ethernet interfaces are described at the level of the Hub board is illustrated in **Figure 10**, which can be found in the section describing the Hub PCB layout (**Section 7**).

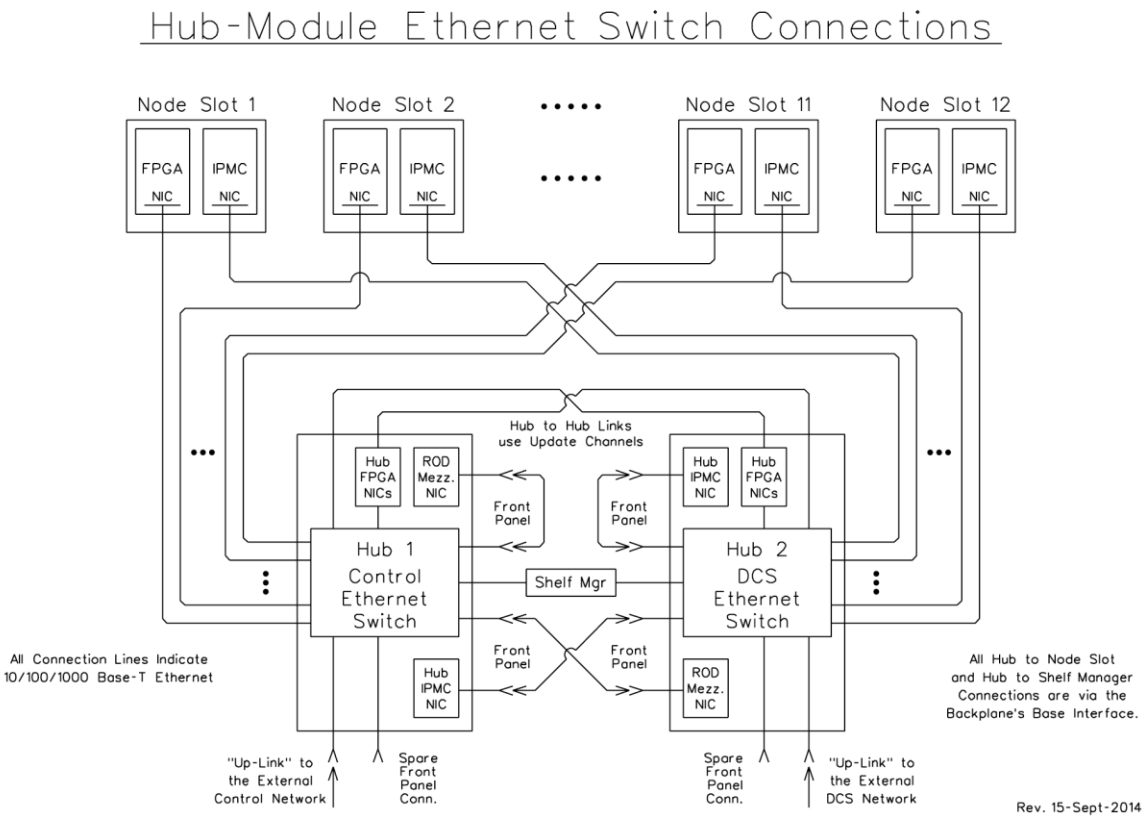


Figure 7: Illustration of FEX-Hub Ethernet network connections.

5.4 Hub Interfaces to FEX Modules

This subsection summarizes the Hub electrical interfaces to the FEX modules. A more complete specification of the connector/pin assignments is illustrated in **Section 0**. Please refer to that section for more details.

5.4.1 Interface with Hub-1

Hub-1 resides in logical slot 1 and hosts the TTC-FMC mezzanine. It thus distributes the TTC clock and control data signals. Hub-1 also hosts the slow control IPbus network.

5.4.1.1 Base Interface

The 2 ports of Base Channel 1 (4 pairs of differential signals) of the base interface are used to provide a Gigabit Ethernet connection to be used by the FEX module for its IPbus port.

The usage of the ports on this channel follows the ATCA PICMG 3.0 specification for 1000BASE-T Ethernet.

5.4.1.2 Fabric Interface

The ports of the Fabric Interface Channel 1 are not used according to the ATCA convention and notation.

The 4 ports of Fabric Channel 1 (8 pairs of differential signals) are defined by ATCA as 4 transmitting and 4 receiving pairs.

Hub-1 is instead transmitting on only 2 of these pairs and receiving readout data from the FEX on the other 6 pairs

5.4.1.3 Hub-1 Module signals as Seen from a FEX Module

The FEX modules receive the LHC clock on the receive signal pair of Fabric Interface Channel 1 port 0. (Note: this clock is provided by the TTC FMC mezzanine on Hub-1). This signal is meant to be received as a logic clock and not as data stream. It is not driven by an FPGA MGT Transceiver on the HUB and is not meant to be received by an MGT on a FEX.

The FEX modules receive the combined TTC and ROD control data stream on the receive signal pair of Fabric Interface Channel 1 port 1. Note: the TTC control information is provided by the TTC FMC mezzanine on Hub-1. The two RODs on Hub-1 and Hub-2 may need to also send control information to the FEXs. This optional ROD control is merged with the TTC control data stream according to a format to be determined.

The FEX modules send their primary readout data streams 0-3 destined to the ROD on Hub-1 on the transmit signal pair of Fabric Interface Channel 1 port 0-3. The FEX module is SENDING its secondary readout data streams 4-5 destined to the ROD on Hub-1 on the RECEIVE signal pair of Fabric Interface Channel 1 port 2-3 which means it is using these two ports in the opposite direction from their conventional usage and ATCA naming.

5.4.2 Interface with Hub-2

Hub-2 resides in logical slot 2 and hosts the IPMC network. It does not host a TTC-FMC mezzanine.

5.4.2.1 Base Interface

The 2 ports of Base Channel 2 (4 pairs of differential signals) of the base interface are used to provide a Gigabit Ethernet connection to be used by the FEX module for its IPMC.

The usage of the ports on this channel follows the ATCA PICMG 3.0 specification for 1000BASE-T Ethernet.

5.4.2.2 Fabric Interface

The ports of Fabric Interface channel 2 are not used according to the ATCA convention and notation.

The 4 ports of Fabric Channel 2 (8 pairs of differential signal) are defined by ATCA as 4 transmitting and 4 receiving pairs.

Hub-2 is instead transmitting nothing on 2 of these pairs and receiving readout data from the FEX on the other 6 pairs.

5.4.2.3 Hub-2 Module Signals as Seen from a FEX Module

The receive signal pair of Fabric Interface Channel 2 port 0 is unused on FEX modules. The receive signal pair of Fabric Interface Channel 2 port 1 is also unused on FEX modules.

The FEX modules send their primary readout data streams 0-3 destined to the ROD on Hub-2 on the transmit signal pair of Fabric Interface Channel 2 port 0-3.

The FEX module is SENDING its secondary readout data streams 4-5 destined to the ROD on Hub-2 on the RECEIVE signal pair of Fabric Interface Channel 2 port 2-33 which means it is using these two ports in the opposite direction from their conventional usage and ATCA naming.

5.5 Hub Interface to its ROD Mezzanine

Two 400 pin MEG Array connectors interface the ROD Mezzanine to the FEX-Hub. This section identifies the signals carried through these connectors. The pin allocation on these two connectors is still a work in progress.

Note: there are a maximum of 80 MultiGigabitTransceiver (MGT) Transmitter ports and 80 MGT Receiver ports available on the Virtex-7 devices being used on the ROD and on the Hub itself.

5.5.1 MGT Differential Inputs to ROD from Hub

These differential signals are connected to MGT Receiver on the ROD FPGA.

- 12x6 = 72 serial streams of Readout Data from the FEX modules
- 2x serial streams of Readout Data from the local HUB FPGA
- 2x serial streams of Readout Data from the other HUB FPGA
- 1x serial stream of combined TTC and ROD control data stream

5.5.2 MGT Differential Outputs from ROD to Hub

- 1x serial stream of ROD Readout Control information

This signal needs to be merged with the TTC control data stream by the HUB FPGA. A copy of *this* combined TTC and ROD control data stream is sent to the ROD, cf. Previous section.

5.5.3 Other signals between ROD and Hub

- LHC Clock
    - 1x Differential signal pair
- Geographic Address
    - 8x signals coming from the HUB FPGA

- The HUB FPGA determines this System Geographic Address by combining the J10 Hardware Address pins with the Shelf Address retrieved from the Shelf Manager by the IPMC.
- The crate and slot addressing scheme for this 8-bit address needs to be defined.

- IPbus port
  - 4x Bi-directional Signal Pairs forming a 1000BASE-T Gigabit Ethernet connection.
- Sensor I2C Bi-directional Bus
  - 2x I2C Signals (Clock and Data) connected to the IPMC
- JTAG access
  - 4x JTAG Signals
- Power Supply Connections
  - +12V bulk power is made available to the ROD
  - The number of power and ground pins required is still being studied.
- Power Control signals
  - 2x Power Control Signals to the ROD
  - 2x Power Status Signals from the ROD

Hub->ROD: Dual MEG Array 400: Proposed pin usage

Last Updated: 16-Sep-2014 **SUBJECT TO CHANGE**

Row	A	B	C	D	E	F	G	H	I	J
1	T	G	T	V	V	V	V	V	S	S
2	G	+	G	V	V	V	V	V	S	S
3	G	-	G	T	G	T	S	S	S	S
4	T	G	+	G	+	G	S	S	S	S
5	T	G	-	G	-	G	S	S	S	S
6	G	+	G	+	G	T	S	S	S	S
7	G	-	G	-	G	T	S	S	S	S
8	T	G	+	G	+	G	S	S	S	S
9	T	G	-	G	-	G	S	S	S	S
10	G	+	G	+	G	T	S	S	S	S
11	G	-	G	-	G	T	S	S	S	S
12	T	G	+	G	+	G	S	S	S	S
13	T	G	-	G	-	G	S	S	S	S
14	G	+	G	+	G	T	S	S	S	S
15	G	-	G	-	G	T	S	S	S	S
16	T	G	+	G	+	G	S	S	S	S
17	T	G	-	G	-	G	S	S	S	S
18	G	+	G	+	G	T	S	S	S	S
19	G	-	G	-	G	T	S	S	S	S
20	T	G	+	G	+	G	S	S	S	S
21	T	G	-	G	-	G	S	S	S	S
22	G	+	G	+	G	T	S	S	S	S
23	G	-	G	-	G	T	S	S	S	S
24	T	G	+	G	+	G	S	S	S	S
25	T	G	-	G	-	G	S	S	S	S
26	G	+	G	+	G	T	S	S	S	S
27	G	-	G	-	G	T	S	S	S	S
28	T	G	+	G	+	G	S	S	S	S
29	T	G	-	G	-	G	S	S	S	S
30	G	+	G	+	G	T	S	S	S	S
31	G	-	G	-	G	T	S	S	S	S
32	T	G	+	G	+	G	S	S	S	S
33	T	G	-	G	-	G	S	S	S	S
34	G	+	G	+	G	T	S	S	S	S
35	G	-	G	-	G	T	S	S	S	S
36	T	G	+	G	+	G	S	S	S	S
37	T	G	-	G	-	G	S	S	S	S
38	G	+	G	T	G	T	S	S	S	S
39	G	-	G	V	V	V	V	V	S	S
40	T	G	T	V	V	V	V	V	S	S

Notes
(1)Differential Signal polarities are arbitrary: there may be a case for re-arranging them.
(2) Terminator pins have 50Ω to Ground: not fully established if better than Grounds
(3) The Signal pins are available for the other ROD-Hub signals
[4] Pins rated at 0.45 A/pin, so 20 OK for 9A: i.e. 108 W at 12V. All 12V on one connector?
[5] Mate/Un-Mate forces for 400 pins are 140/80N
[6] Only have to route Differential Pairs 4 columns back: simpler, less layers?

	A	B	C	D	E	F	G	H	I	J
Signal Pairs	0	10	9	8	9	0	0	0	0	0
Grounds	20	20	20	18	18	18	0	0	0	0
Terminators	20	0	2	2	0	18	0	0	0	0
12V Power	0	0	0	4	4	4	4	4	0	0
Other Signals	0	0	0	0	0	0	36	36	40	40

Total Pins	
for Signal Pairs	72
Grounds	114
Terminators	42
12V Power	20
Other Signals	152
Total Totals	400

Figure 8: Preliminary pin assignments for the Dual MEG Array connector used for the Hub-to-ROD interface.

5.6 Hub Interfaces to Second Hub Modules

5.6.1 Base Interface

The Base Channel 1 is reserved for the Shelf Manager Controller and is unused.

The Base Channel 2 port (4 pairs of differential signals) is not currently allocated.

5.6.2 Fabric Interface

The Fabric Interface channel 1 is used according to the ATCA convention and notation with one caveat for Hub-2: Hub-2 is transmitting nothing on 2 of its transmitter pairs.

5.6.3 Hub-2 usage of the Fabric Interface connection to Hub-1

Hub-2 is receiving the LHC clock on the receiving signal pair of Fabric Interface Channel 1 port 0.

Hub-2 is receiving the combined TTC and ROD control data stream on the receiving signal pair of Fabric Interface Channel 1 port 1.

Hub-2 is sending on the transmitting signal pair of Fabric Interface Channel 1 port 0-1 its readout data streams 1-2 destined to the ROD on Hub-1.

5.6.3.1 Hub-1 usage of the Fabric Interface connection to Hub-2

The receiving signal pair of Fabric Interface Channel 1 port 0 is unused on Hub-1.

Hub-1 is receiving on the receive signal pair of Fabric Interface Channel 1 port 1 the ROD Readout control information from the ROD on Hub-2.

Hub-1 is sending on the transmit signal pair of Fabric Interface Channel 1 port 0-1 its readout data streams 1-2 destined to the ROD on Hub-2.

5.6.4 Update Channel Interface

The 5 ports of the Update Channel (10 pairs of differential signal) are defined by ATCA as 5 transmitting and 5 receiving pairs. The first 4 ports of the Update Channel Interface are not used according to this ATCA convention and notation. The 5th port of the Update Channel Interface is not currently allocated.

The 4 Transmit pairs of Update Channel port 0-4 form one Gigabit Ethernet link and are connected to a Switch port of the local Hub. The 4 Receive pairs of Update Channel port 0-4 form another Gigabit Ethernet link and are connected to the Hub FPGA on the local Hub.

Note: the exact pin assignment of each port to the four 1000BASE-T signal pairs will be specified later while this assignment is internal to Hub operation only (no other L1Calo modules are affected).

This Hub-to-Hub connection allows the Hub FPGA on Hub-2 to connect to the IPbus Network serviced by the Ethernet switch on Hub-1.

The Hub FPGA on Hub-1 is directly connected to the IPbus Network switch on Hub-1 and can simply ignore this additional Ethernet port that would connect it to the IPMC Network serviced by the Ethernet switch on Hub-2.

6 Hub Implementation Details

This section describes the details of how the FEX-Hub functionality is planned to be implemented for the prototype Hub module.

6.1 Physical Layout

The FEX-Hub module is implemented as a standard size 6 HP ATCA card.

The Hub holds the ROD mezzanine card. The ROD is located near the top edge of the Hub and is expected to run from the Hub's front panel edge for 220 mm towards the Hub's backplane edge. In the direction along the front panel the ROD is expected to run for 100 mm.

The Hub and ROD are electrically connected by two 400 pin Meg-Array connectors. A short 4mm stack height is used so that the Hub and ROD PCBs are quite close to each other. The component sides of the Hub and ROD both face in the same direction. The intent is to keep the path of the high speed differential signals from the Hub to the ROD as short as possible and to give the maximum available height for the MiniPODs and other components on the ROD.

The Hub and ROD are mechanically connected to each other using standoffs. The Hub holds the fiber-optic pig-tail cables and connectors that run from Zone 3 on the Hub to the MiniPOD devices on the ROD.

In its middle near the front edge the Hub module holds a TTC-FMC card. As its name suggests the TTC-FMC is electrically connected to the Hub via a 400 pin FMC connector. Four standoffs are used to mechanically mount the TTC-FMC onto the Hub. The TTC-FMC has a high standoff and most of its components are between the Hub and TTC-FMC PCBs. The FEX-Hub has penetrations through its front panel for the TTC-FMC's LEMO, optical, and LED devices.

Other Hub front panel penetrations include those for the ATCA required LEDs, for the four front panel Ethernet connections, and any that are required for the ROD Mezzanine Card.

The Hub includes heat sinks for its Virtex-7 FPGA, for its Ethernet switch components, and for it MiniPOD. Along its backplane edge the FEX-Hub uses a full complement of connectors J20 through J24 and P10.

6.2 Readout Signal Distribution

The FEX-Hub receives readout data on 6 channels of the Fabric Interface from each of the 12 node slots in the shelf. This is 72 channels of high-speed readout data from the FEX node slots. In addition the Virtex-7 FPGA on the other FEX-Hub provides 2 Fabric Interface channels of readout data. This makes a total of 74 channels of readout data from other slots in the shelf. The FPGA on the FEX-Hub holding the ROD also provides 2 GTH channels of readout data. Thus a total of 76 GTH receivers on the ROD are required to field the readout data from all sources in the shelf.

The readout data from other slots in the shelf is received by the Hub with On-Semi 2-way fan-out chips that have built-in termination. The exact chip used will depend on the final decision about the data rate of these readout signals.

One output from these fan-out chips runs to 74 GTH transceivers inputs on the FEX-Hub's Virtex-7 FPGA. The other output from these fan-out chips is routed through the 2 Meg-Array connectors to the ROD mezzanine card.

The pinout of the Meg-Array connectors to the ROD has been designed to provide optimum signal fidelity for these high-speed differential signals. The intent is to provide a clean, uniform, and short route for the traces on the ROD that connect the Meg-Array pins to its GTH transceiver inputs. On the ROD the Meg-Array connectors are located adjacent to the edges of its Virtex-7 FPGA that hold the GTH transceivers.

In the FEX-Hub module design we are not providing a predetermined mapping of backplane Fabric interface channels to Meg-Array differential pin pairs going to the ROD. Rather this mapping will be determined during Hub PCB layout. Whatever mapping provides the cleanest layout of these high speed differential traces on the FEX-Hub will be used. The only (and presumably weak) constraint that this mapping will follow is that all 6 Fabric Interface channels from a given node slot will be routed to only 2 GTH Quads on the ROD's Virtex-7 device and to only 2 GTH Quads on the Hub's Virtex-7 device. The intent of this constraint is to allow an effective power down of unused GTH Quads. Note that for this layout technique to work the Hub PCB design must be aware of the Meg-Array to GTH connections on the ROD.

In addition the direct and complement sides of these high speed differential signals will not be conserved during the Hub PCB trace layout. Whatever arrangement of the direct and complement sides of a given differential signal provides the cleanest layout will be used. Differential traces from the backplane connectors to the fan-out chips, and from the fan-out chips to the Meg-Array connectors, and from the fan-out chips to the Hub's GTH transceiver inputs will all be length matched. After PCB routing a final overall document will be prepared that lists which Virtex-7 GTH Quad and transceiver a given backplane Fabric Interface channel is actually connected to and whether or not the overall routing on the Hub and on the ROD has resulted in an inversion of the signal.

6.3 TTC Clock and TTC Data Stream Distribution

The FEX-Hub uses a TTC-FMC mezzanine card to receive the composite TTC signal. The TTC-FMC card extracts the LHC locked clock and the TTC "Data Stream" and passes them to the FEX-Hub.

The FEX-Hub distributes the TTC Clock and the TCC Data Stream to 15 different objects that use these signals. The objects that use these TTC signals are: 12 ATCA Node Slots, the ROD mezzanine card on this Hub, this Hub's own Virtex FPGA, and finally distribution of these TTC signals to the other Hub module.

Distribution of the TTC Clock by the Hub is purely by fan-out. Note that the TTC-FMC can provide a clock signal even when it is not receiving a composite TTC input signal.

Distribution of the TTC Data Stream by the Hub is more complicated. As shown in the TTC Distribution drawing the TTC Data Stream is mixed with the "back data" coming from both the ROD on Hub-1 and the ROD on Hub-2. A small part of the logic available in the Hub-1 Virtex FPGA is used to combine these 3 data streams.

Fabric Interface Channels are used to carry the TTC Clock and the combined Data Stream from Hub-1 to the Node Slots and from Hub-1 to Hub-2. When the Hubs are used this way all Node slots receive both their TTC Clock and the combined Data Stream from the Fabric Interface channels to Hub-1. Note that the PCB traces on both Hubs are the same so that distribution of TTC Data combined with back data from the ROD on Hub-1 on one set of Fabric channels while separately distributing TTC Data combined with back data from the ROD on Hub-2 on another set of Fabric channels is possible.

We assume that extraction of the information that a given object requires from the combined TTC plus ROD Data Stream will be performed by FPGA firmware in that object. Further we assume that all objects will receive the combined Data Stream using a Virtex-7 GTH Transceiver.

As noted the Hub module that holds the TTC-FMC will distribute the TTC Clock and combined Data Stream signals to the other Hub. This connection is necessary to supply these signals to the ROD and Virtex-7 FPGA on the other Hub. The physical path to carry these signals from the Hub with the TTC-FMC to the Hub without this mezzanine is a pair of Fabric Interface channels that run between the Hubs.

Note that only the Fabric Interface channels from the Hub that carries the TTC-FMC mezzanine card are actually active. The TTC Fabric Interface channels from the Hub module without the TTC-FMC (Hub-2) are tied Low by that Hub.

6.4 Base Interface Switch

Each FEX-Hub provides a 10/100/1000 Base-T Ethernet switch with 19 ports that are connected to the following:

1 connection to the front panel i.e. the "up-link";

1 connection to the ROD (or IPMC) on this Hub;

1 connection to the ROD (or IPMC) on the other Hub;

1 connection to this Hub's Virtex FPGA;

1 connection to the other Hub's Virtex FPGA;

1 connection to the Shelf Manager;

1 spare front panel connection;

12 connections to the "Node" boards in this crate.

This Hub switch is implemented using 3 Broadcom BCM53118 devices. These 8 port switches include the PHY interface to the BASE-T network connections. Besides providing the advantage of build in PHY interface the BCM53118 can be operated as either a simple unmanaged switch or if managed it can provide advanced switch features. The intent is to provide a prototype Hub switch that is easy for everyone to use but that has advanced features available via remote management if needed.

The prototype Hub module has 6 RJ45 Ethernet connectors on its front panel: 4 connectors to its switch, one to the Hub ROD and one to the Hub IPMC. The 4 switch connections are normally used for: the up-link to the external network, two ports for connections to either both Hub RODs or both Hub IPMCs (depending on whether this is Hub-1 or Hub-2), and a spare front panel Ethernet connection.

The point of having these connections accessible via front panel RJ45 connectors is to make the prototype Hub easy to uses in various test setups where either one or two Hubs may be used. The RJ45 connections to the Hub also allow the switch to be tested without any other ATCA cards in the system.

6.5 Power Supplies

The FEX-Hub module's power supply system is rather complicated because of the large number of different voltage loads on the card. The power supply system on the FEX-Hub is divided into a number of logical and physical blocks.

The features in the power entry block on the Hub are defined by the requirements of the ATCA specification. These features include the dual -48V input buses, filtering, holdup, and pre-charge. The power entry block provides isolated power to the Hub's IPMC module and it sends monitoring information to the IPMC. The IPMC provides control signals to the power entry block to tell it when it is OK to power up the FEX-Hub loads.

The bulk isolated power source on the FEX-Hub is an isolated +12 Volt supply. This block provides the bulk +12 Volts to all of the DC/DC converters that that supply the Hub's loads and it provides bulk +12 Volt to the ROD which has its own DC/DC converters. Both the power entry block and the isolated +12 Volt block are stock commercial modules. We have investigated modules up to the 350 Watt power level.

Power for the loads on the Hub are provided by a number of commercial non-isolated DC/DC bulk converters. These DC/DC converters include those for the Hub's Virtex-7 FPGA loads: core, aux, vco, gthavcc, gthavtt, gthaux and those for other bulk supply loads on the FEX-Hub including the TTC-FMC loads.

Monitoring of the Hub power supplies for both voltage and current is provided over the Sensor I2C bus to the IPMC and thus to the DCS system. In addition to this all supplies are monitored by a Hi/Low power supply supervisor to provide a 1 bit overall status of the Hub's power system.

6.6 Hub FPGA

The main Hub FPGA will be a large Xilinx Virtex-7 device, such as an XC7VX550T. This offers large logic resources and Block RAM, and adequate fast Multi Gigabit transceivers. In fact it is the number of receivers that is critical: input data from the FEXs and the second Hub module requires 74 inputs. A few more inputs are needed for Ethernet and TTC signals. The XC7VX550T is the smallest device with sufficient transceivers (80 GTH's). The XC7VX690T is pin compatible, and offers a modest increase in Logic and Block RAM, as shown in Table 1.

Device	Package	GTH RX/TX	GPIO	Logic Cells	Block RAM (Kb)
XC7VX550T	FFG1927	80	600	554,240	42,480
XC7VX690T	FFG1927	80	600	693,120	52,920

Table 1: Candidate Virtex-7 Devices

6.7 The IPM Controller

For the purposes of monitoring and controlling the power, cooling and interconnections of a module, the ATCA specification defines a low-level hardware management service based on the Intelligent Platform Management Interface standard (IPMI). The Intelligent Platform Management (IPM) Controller is that portion of a module (in this case, the FEX-Hub) that provides the local interface to the shelf manager via the IPMI bus. It is responsible for thefollowing functions:

- interfacing to the shelf manager via dual, redundant Intelligent Platform Management Buses (IPMBs); it receives messages on all enabled IPMBs and alternates transmissions on all enabled IPMBs;
- negotiating the Hub power budget with the shelf manager and powering the Payload hardware only once this is completed;

- managing the operational state of the Hub, handling activations and deactivations, hot-swap events and failure modes;
- implementing electronic keying, enabling only those backplane interconnects that are compatible with other modules in shelf, as directed by shelf manager;
- providing to the Shelf Manager hardware information, such as the module serial number and the capabilities of each port on backplane;
- collecting, via an I2C bus, data on voltages and temperatures from sensors on the Hub, and sending these data, via IPBus, to the main Hub FPGA;
- driving the BLUE LED, LED1, LED2 and LED3.

The Hub uses the IPMC mezzanine produced by LAPP as the IPM Controller [1.11] . The form factor of this mezzanine is DDR3 VLP Mini-DIMM.

7 Hub PCB Layout

Figure 9 illustrates a hypothetical layout of the main components on the FEX-Hub. **Figure 10** and **Figure 11** illustrate the core Ethernet and high-speed data distribution on the Hub module, respectively. The remainder of this section describes the PCB layout of the Hub module.

The location of the major components was selected to make the PCB trace layout as clean as possible, e.g. the power entry module is located next to the P10 connector. Special attention is needed for the many high-speed differential readout signals that flow onto the Hub from the Fabric Interface. These are the highest speed long trace length signals in the system.

These readout signals arrive on the Hub via the J20 through J23 backplane connectors. Short differential traces carry these signals to the 2-way fan-out chips that are located next to these connectors. To help maintain signal fidelity, these fan-out chips include internal terminators.

From these 2-way fan-out chips the readout data flows through relatively short traces to the Hub FPGA's GTH receivers. The Hub's FPGA is located and oriented to allow best access to its GTH inputs.

From the fan-out the readout data also flows through longer traces to the Meg-Array connectors that lead to the ROD mezzanine card. Much of this trace run is in the section of the Hub PCB that is covered by the close fitting ROD mezzanine. No other substantial components can be located in this section of the Hub PCB but this space can be used to provide clean routes for these high-speed signals.

Once on the ROD these signals have short clean routes to the ROD's GTH receivers. As described in **Section 6.2** the routes for the high speed readout signals will not implement a predetermined channel mapping or preserve signal polarity but rather will be designed for optimum signal fidelity.

The Hub includes a significant number of other high and moderate speed differential signals. These include the 1000 Base-T Ethernet, the local GTH signals between this Hub's FPGA and ROD, and the TTC clock and data stream distribution. The components involved with these signals have been located to provide a clean layout of the PCB traces that carry them.

Additional concerns in the Hub PCB layout include the distribution of the many power supply rails and dissipation of the heat generated by the Hub and its associated ROD mezzanine. The power distribution is made slightly easier because most of the loads are on the bottom half of the card where the DC/DC converters are also located. Where it is useful remote feedback to these converters is used.

Custom heat sinks are required for the Hub's Virtex-7 FPGA, MiniPOD, and the Ethernet Switch chips. The highest heat load will potentially come from the FPGA and will depend on how this FPGA is used. The MiniPOD dissipates a modest 2 Watts and the Ethernet Switch 12 Watts. The Hub heat sinks need to be designed in consultation with the ROD engineers and avoid air-flow shadowing of the ROD.

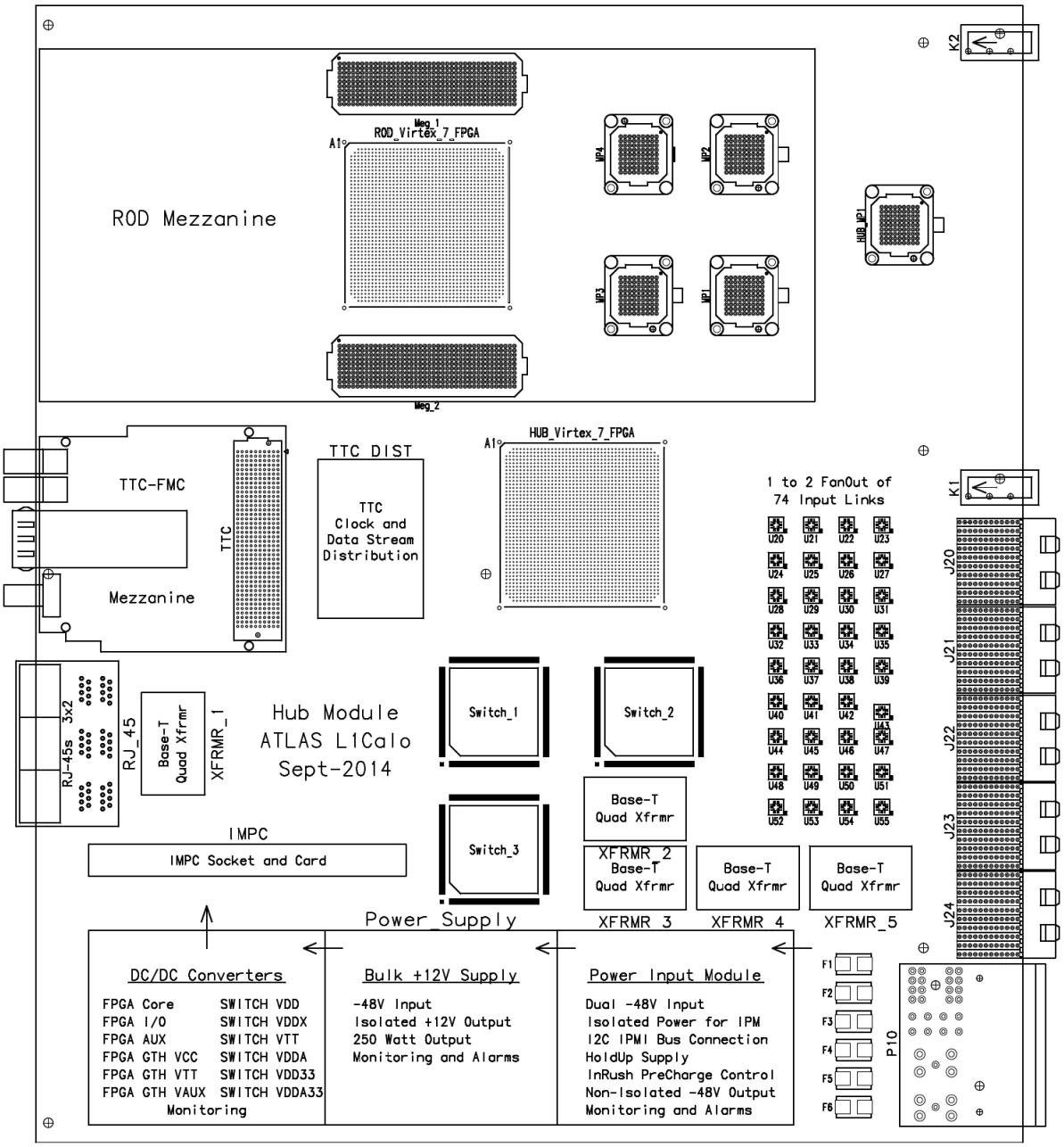


Figure 9: Illustration of the preliminary Hub PCB layout of major components.

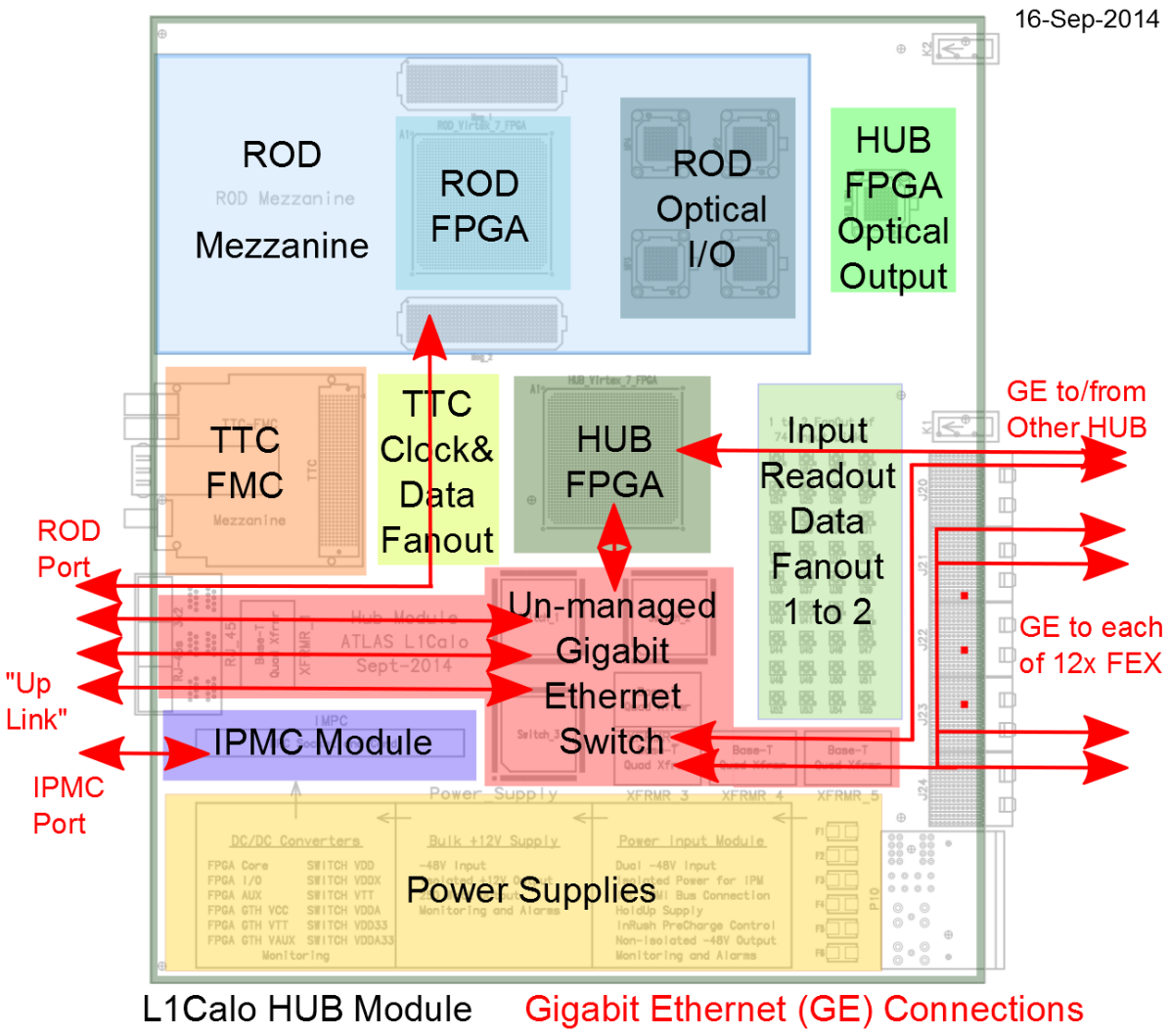


Figure 10: Board-level illustration of the Hub's Gigabit Ethernet connections.

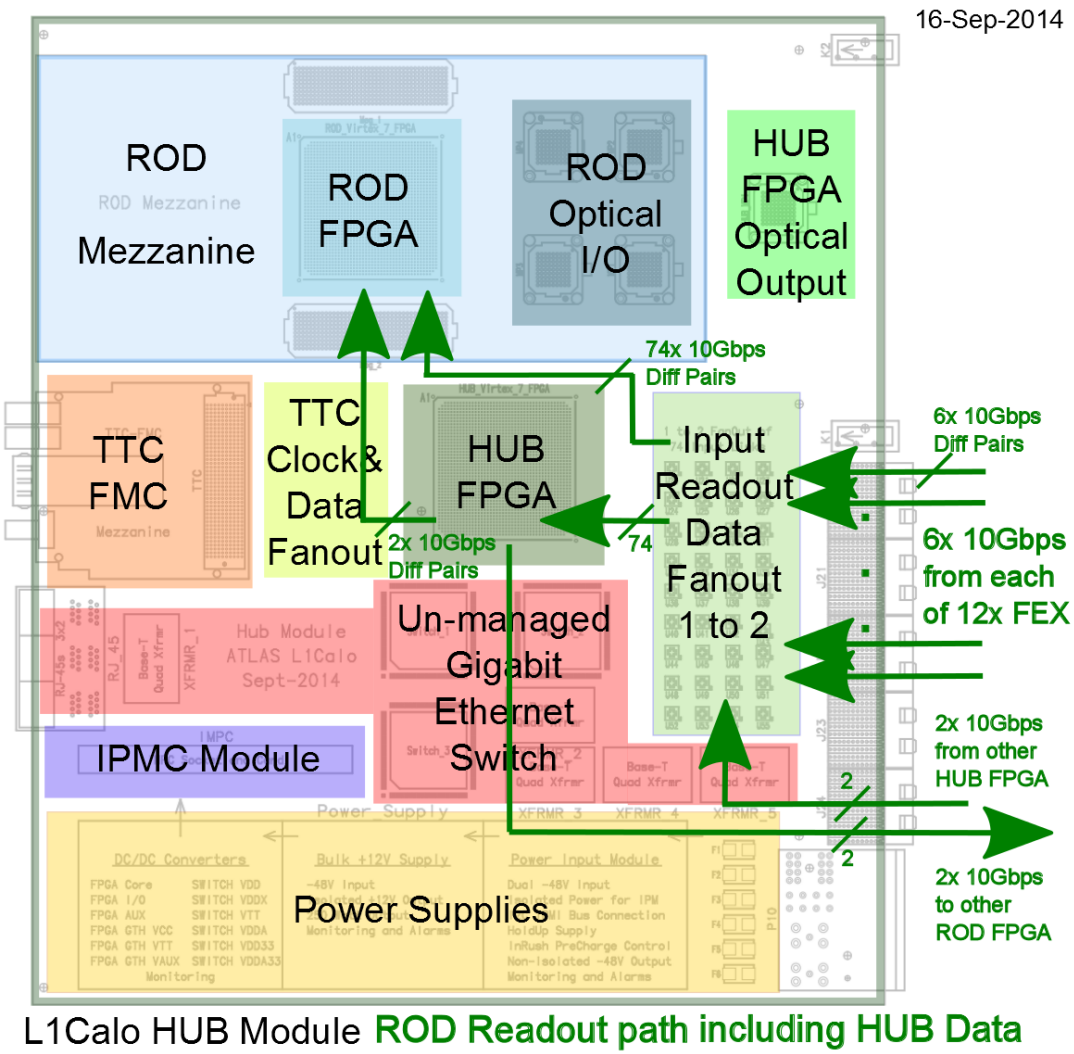


Figure 11: Board-level illustration of the high-speed data interfaces for the Hub.

8 Front-Panel Layout

The FEX-Hub includes an extruded aluminum ATCA front panel with an EMC gasket. The front panel insertion extraction handles actuate a PCB mounted micro-switch for the hot-swap function.

Penetrations through the front panel include those for the standard ATCA LEDs, those for the RJ45 Ethernet connections, those for the TTC-FMC's optical and electrical connections, and any that are required for the ROD mezzanine card.

9 Testing and Commissioning

The testing and commissioning of the FEX-Hub module will be performed in two modes: (1) together with a second Hub module to test core Hub functionality, (2) together with FEX and ROD modules to test integrated FEX system functionality.

To facilitate the requirement of Hub-to-Hub testing, the Hub module should:

- allow testing and validation of the DCS and control networks via direct connections to a second Hub module;
- allow testing and validation of the DCS and control networks via front-panel connections to external computers, allowing thorough scanning of all IPbus targets;
- allow the sending and receiving of high-speed signals from one Hub to another, providing a path to study Fabric Interface bandwidth limitations;
- allow testing and validation of the fanout of clock and TTC control data information over the Fabric Interface.

To facilitate the requirement of FEX-Hub-ROD testing, the Hub module should:

- provide Fabric Interface connections to the ROD with no Hub configuration required;
- provide network switching functions with no Hub configuration required;
- function as a single module without a second Hub module in the ATCA shelf.

10 Planned Hub Module Production Yields

The construction of FEX-Hub modules will occur in two phases, prototype and production. The prototype Hub modules should be fabricated and commissioned to coincide with L1Calo integration tests held in Aug-Sept 2015. A total of ten prototype modules will be produced, with delivery anticipated as:

- Two prototype modules for function testing at MSU;
- Two prototype modules for an integration test rig at CERN;
- One prototype module each for Rutherford, Brookhaven and Birmingham, for e/gFEX and ROD testing;
- Three spare prototype Hub modules.

The testing and commissioning aspects of the jFEX modules that require a Hub module are anticipated to be performed at CERN. A total of twenty-one production Hub modules will be produced by January 2018, with delivery anticipated as:

- Eight production modules to support the L1Calo system eFEX, jFEX and gFEX shelves at CERN (note, there are two eFEX shelves);
- Four spare production modules at CERN, dedicated for the L1Calo FEX system;
- Two production modules for function testing at MSU;
- Two production modules the CERN test rig;

- One production module each for Rutherford, Brookhaven and Birmingham, for e/gFEX and ROD testing;
- Two spare production modules to be used as needed.

11 Programming Model

The Programming model is preliminary, and is expected to change significantly during detailed design.

11.1 Guidelines

The slow-control interface of the FEX-Hub obeys the following rules.

- The system controller can read all registers; there are no ‘write only’ registers.
- Three types of register are defined: Status Registers, Control Registers and Pulse Registers.
- All Status Registers are read-only registers. Their contents can be modified only by the Hub hardware.
- All Control Registers are read/write registers. Their contents can be modified only by system controller. Reading a Control Register returns the last value written to that register.
- All Pulse Registers are read/write registers. Writing to them generates a pulse for those bits asserted. Reading them returns all bits as zero.
- Attempts to write to read-only registers, or undefined portions of registers, result in the non-modifiable fields being left unchanged.
- If the computer reads a register (e.g. a counter) which the Hub is modifying, a well-defined value is returned.
- The power-up condition of all registers bits is zero, unless otherwise stated.

11.2 Register Map & Descriptions

This section is a placeholder, to be completed during the design process.

12 Special Notes

- The FEX-Hub module is not providing Fabric or Base Interface connections to the 2 slots that do not exist in 14-slot shelves, i.e. shelves with 2 Hub slots and only 12 Node slots.
- As shown the FEX-Hub's Base Interface switch provides a connection to only one Shelf Manager.

13 Glossary

ATCA	Advanced Telecommunications Computing Architecture (industry standard).
BC	Bunch Crossing: the period of bunch crossings in the LHC and of the clock provided to ATLAS by the TTC, 24.95 ns.
BCMUX	Bunch-crossing multiplexing: used at the input to the CPM, JEM (from Phase I) and eFEX, this is a method of time-multiplexing calorimeter data, doubling the number of trigger towers per serial link.
CMX	Common Merger Extended Module.
CP	Cluster Processor: the L1Calo subsystem comprising the CPMs.
CPM	Cluster Processor Module.
CTP	Central Trigger Processor
DAQ	Data Acquisition
DCS	Detector Control System: the ATLAS system that monitors and controls physical parameters of the sub-systems of the experiment, such as gas pressure, flow-rate, high voltage settings, low-voltage power supplies, temperatures, leakage currents, etc.
ECAL	The electromagnetic calorimeters of ATLAS, considered as a single system.
ECR	Event Counter Reset signal from the TTC, used to initiate clearing of ROD memories
eFEX	Electron Feature Extractor.
FEX	Feature Extractor, referring to either an eFEX or jFEX module or subsystem.
FIFO	A first-in, first-out memory buffer.
FPGA	Field-Programmable Gate Array.
HCAL	The hadronic calorimeters of ATLAS, considered as a single system.
IPbus	An IP-based protocol implementing register-level access over Ethernet for module control and monitoring.
IPMB	Intelligent Platform Management Bus: a standard protocol used in ATCA shelves to implement the lowest-level hardware management bus.
IPM Controller	Intelligent Platform Management Controller: in ATCA systems, that portion of a module (or other intelligent component of the system) that interfaces to the IPMB.
IPMI	Intelligent Platform Management Interface: a specification and mechanism for providing inventory management, monitoring, logging, and control for elements of a computer system. A component of, but not exclusive to, the ATCA standard.
JEM	Jet-Energy Module.
JEP	Jet-Energy Processor: the L1Calo subsystem comprising the JEMs.
jFEX	Jet Feature Extractor.
JTAG	A technique, defined by IEEE 1149.1, for transferring data to/from a device

	using a serial line that connects all relevant registers sequentially. JTAG stands for Joint Technology Assessment Group.
L0A	In Run 4, the Level-0 trigger accept signal.
L0Calo	In Run 4, the ATLAS Level-0 Calorimeter Trigger.
L1A	The Level-1 trigger accept signal.
L1Calo	The ATLAS Level-1 Calorimeter Trigger.
LHC	Large Hadron Collider.
MGT	As defined by Xilinx, this acronym stands for Multi-Gigabit Transceiver. However, it should be noted that it denotes a multi-gigabit transmitter–receiver pair.
Minipod	An embedded, 12-channel optical transmitter or receiver.
MPO	Multi-fibre Push-On/Pull-Off: a connector for mating two optical fibres.
PMA	Physical Media Attachment: a sub-layer of the physical layer of a network protocol.
ROD	Readout Driver.
RoI	Region of Interest: a geographical region of the experiment, limited in η and ϕ, identified by the Level-1 trigger (during Run 3) as containing candidates for Level-2 trigger objects requiring further information. In Run 4, RoIs are used in the same between the Level-0 and Level-1 triggers.
Shelf	A crate of ATCA modules.
SMA	Sub-Miniature version A: a small, coaxial RF connector.
Supercell	LAr calorimeter region formed by combining E_T from a number of cells adjacent in η and ϕ.
TOB	Trigger Object. A Compact data structure describing a trigger feature detected by a FEX module.
TTC	The LHC Timing, Trigger and Control system.
XTOB	Extended Trigger Object. A data packet passed to the readout path, contained more information about a TOB than can be accommodated on the real-time path.

14 Document Revision History

Version	Date	Comments
0.01	16-09-14	Preliminary Draft
0.02	19-09-14	Language & grammar edits.

15 Appendix 1: Backplane Connector/Pin Tables

This Appendix enumerates the connector and pin connections intended for the Hub-FEX and Hub-Hub backplane links in the Fabric Interface, Base Interface and Update Interface.

In the convention presented here, the FEX numbering below presumes that the module called "FEX 01" is located in Logical Slot 3, FEX 02 in Slot 4,... and FEX 12 in Slot 14.

15.1 Connector and Signal Usage for a HUB Slot

Connect Number	Row Num	Channel	Connector Pin Pairs a b	c d	e f	g h
J20/P20	01	Clocks	CLK1A+ CLK1A- Unused signal pair	CLK1B+ CLK1B- Unused signal pair	CLK2A+ CLK2A- Unused signal pair	CLK2B+ CLK2B- Unused signal pair
J20/P20	02	Upd Chan & Clocks	Tx4(UP)+ Tx4(UP)- Unused signal pair	Rx4(UP)+ Rx4(UP)- Unused signal pair	CLK3A+ CLK3A- Unused signal pair	CLK3B+ CLK3B- Unused signal pair
J20/P20	03	Update Chan	Tx2(UP)+ Tx2(UP)- GE Pair C HUB FPGA	Rx2(UP)+ Rx2(UP)- GE Pair C HUB Switch	Tx3(UP)+ Tx3(UP)- GE Pair D HUB FPGA	Rx3(UP)+ Rx3(UP)- GE Pair D HUB Switch
J20/P20	04	Update Chan	Tx0(UP)+ Tx0(UP)- GE Pair A HUB FPGA	Rx0(UP)+ Rx0(UP)- GE Pair A HUB Switch	Tx1(UP)+ Tx1(UP)- GE Pair B HUB FPGA	Rx1(UP)+ Rx1(UP)- GE Pair B HUB Switch
J20/P20	05	Fabric Channel 15	Tx2[15]+ Tx2[15]- Unused signal pair	Rx2[15]+ Rx2[15]- Unused signal pair	Tx3[15]+ Tx3[15]- Unused signal pair	Rx3[15]+ Rx3[15]- Unused signal pair
	06		Tx0[15]+ Tx0[15]- Unused signal pair	Rx0[15]+ Rx0[15]- Unused signal pair	Tx1[15]+ Tx1[15]- Unused signal pair	Rx1[15]+ Rx1[15]- Unused signal pair
J20/P20	07	Fabric Channel 14	Tx2[14]+ Tx2[14]- Unused signal pair	Rx2[14]+ Rx2[14]- Unused signal pair	Tx3[14]+ Tx3[14]- Unused signal pair	Rx3[14]+ Rx3[14]- Unused signal pair
	08		Tx0[14]+ Tx0[14]- Unused signal pair	Rx0[14]+ Rx0[14]- Unused signal pair	Tx1[14]+ Tx1[14]- Unused signal pair	Rx1[14]+ Rx1[14]- Unused signal pair
J20/P20	09	Fabric Channel 13	Tx2[13]+ Tx2[13]- RO Str 5 from FEX 12	Rx2[13]+ Rx2[13]- RO Str 3 from FEX 12	Tx3[13]+ Tx3[13]- RO Str 6 from FEX 12	Rx3[13]+ Rx3[13]- RO Str 4 from FEX 12
	10		Tx0[13]+ Tx0[13]- LHC Clk to FEX 12	Rx0[13]+ Rx0[13]- RO Str 1 from FEX 12	Tx1[13]+ Tx1[13]- TTC&ROD Ctl to FEX 12	Rx1[13]+ Rx1[13]- RO Str 2 from FEX 12
J21/P21	01	Fabric Channel 12	Tx2[12]+ Tx2[12]- RO Str 5 from FEX 11	Rx2[12]+ Rx2[12]- RO Str 3 from FEX 11	Tx3[12]+ Tx3[12]- RO Str 6 from FEX 11	Rx3[12]+ Rx3[12]- RO Str 4 from FEX 11
	02		Tx0[12]+ Tx0[12]- LHC Clk to FEX 11	Rx0[12]+ Rx0[12]- RO Str 1 from FEX 11	Tx1[12]+ Tx1[12]- TTC&ROD Ctl to FEX 11	Rx1[12]+ Rx1[12]- RO Str 2 from FEX 11
J21/P21	03	Fabric Channel 11	Tx2[11]+ Tx2[11]- RO Str 5 from FEX 10	Rx2[11]+ Rx2[11]- RO Str 3 from FEX 10	Tx3[11]+ Tx3[11]- RO Str 6 from FEX 10	Rx3[11]+ Rx3[11]- RO Str 4 from FEX 10
	04		Tx0[11]+ Tx0[11]- LHC Clk to FEX 10	Rx0[11]+ Rx0[11]- RO Str 1 from FEX 10	Tx1[11]+ Tx1[11]- TTC&ROD Ctl to FEX 10	Rx1[11]+ Rx1[11]- RO Str 2 from FEX 10
J21/P21	05	Fabric Channel 10	Tx2[10]+ Tx2[10]- RO Str 5 from FEX 09	Rx2[10]+ Rx2[10]- RO Str 3 from FEX 09	Tx3[10]+ Tx3[10]- RO Str 6 from FEX 09	Rx3[10]+ Rx3[10]- RO Str 4 from FEX 09
	06		Tx0[10]+ Tx0[10]- LHC Clk to FEX 09	Rx0[10]+ Rx0[10]- RO Str 1 from FEX 09	Tx1[10]+ Tx1[10]- TTC&ROD Ctl to FEX 09	Rx1[10]+ Rx1[10]- RO Str 2 from FEX 09
J21/P21	07	Fabric Channel 09	Tx2[09]+ Tx2[09]- RO Str 5 from FEX 08	Rx2[09]+ Rx2[09]- RO Str 3 from FEX 08	Tx3[09]+ Tx3[09]- RO Str 6 from FEX 08	Rx3[09]+ Rx3[09]- RO Str 4 from FEX 08
	08		Tx0[09]+ Tx0[09]- LHC Clk to FEX 08	Rx0[09]+ Rx0[09]- RO Str 1 from FEX 08	Tx1[09]+ Tx1[09]- TTC&ROD Ctl to FEX 08	Rx1[09]+ Rx1[09]- RO Str 2 from FEX 08
J21/P21	09	Fabric Channel 08	Tx2[08]+ Tx2[08]- RO Str 5 from FEX 07	Rx2[08]+ Rx2[08]- RO Str 3 from FEX 07	Tx3[08]+ Tx3[08]- RO Str 6 from FEX 07	Rx3[08]+ Rx3[08]- RO Str 4 from FEX 07
	10		Tx0[08]+ Tx0[08]- LHC Clk to FEX 07	Rx0[08]+ Rx0[08]- RO Str 1 from FEX 07	Tx1[08]+ Tx1[08]- TTC&ROD Ctl to FEX 07	Rx1[08]+ Rx1[08]- RO Str 2 from FEX 07
P22/J22	01	Fabric Channel 07	Tx2[07]+ Tx2[07]- RO Str 5 from FEX 06	Rx2[07]+ Rx2[07]- RO Str 3 from FEX 06	Tx3[07]+ Tx3[07]- RO Str 6 from FEX 06	Rx3[07]+ Rx3[07]- RO Str 4 from FEX 06
	02		Tx0[07]+ Tx0[07]- LHC Clk to FEX 06	Rx0[07]+ Rx0[07]- RO Str 1 from FEX 06	Tx1[07]+ Tx1[07]- TTC&ROD Ctl to FEX 06	Rx1[07]+ Rx1[07]- RO Str 2 from FEX 06
P22/J22	03	Fabric Channel 06	Tx2[06]+ Tx2[06]- RO Str 5 from FEX 05	Rx2[06]+ Rx2[06]- RO Str 3 from FEX 05	Tx3[06]+ Tx3[06]- RO Str 6 from FEX 05	Rx3[06]+ Rx3[06]- RO Str 4 from FEX 05
	04		Tx0[06]+ Tx0[06]- LHC Clk to FEX 05	Rx0[06]+ Rx0[06]- RO Str 1 from FEX 05	Tx1[06]+ Tx1[06]- TTC&ROD Ctl to FEX 05	Rx1[06]+ Rx1[06]- RO Str 2 from FEX 05

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Connect Number	Row Num	Channel	Connector Pin Pairs a b	c d	e f	g h
P22/J22	05	Fabric Channel 05	Tx2[05]+ Tx2[05]- RO Str 5 from FEX 04	Rx2[05]+ Rx2[05]- RO Str 3 from FEX 04	Tx3[05]+ Tx3[05]- RO Str 6 from FEX 04	Rx3[05]+ Rx3[05]- RO Str 4 from FEX 04
	06		Tx0[05]+ Tx0[05]- LHC Clk to FEX 04	Rx0[05]+ Rx0[05]- RO Str 1 from FEX 04	Tx1[05]+ Tx1[05]- TTC&ROD Ctl to FEX 04	Rx1[05]+ Rx1[05]- RO Str 2 from FEX 04
P22/J22	07	Fabric Channel 04	Tx2[04]+ Tx2[04]- RO Str 5 from FEX 03	Rx2[04]+ Rx2[04]- RO Str 3 from FEX 03	Tx3[04]+ Tx3[04]- RO Str 6 from FEX 03	Rx3[04]+ Rx3[04]- RO Str 4 from FEX 03
	08		Tx0[04]+ Tx0[04]- LHC Clk to FEX 03	Rx0[04]+ Rx0[04]- RO Str 1 from FEX 03	Tx1[04]+ Tx1[04]- TTC&ROD Ctl to FEX 03	Rx1[04]+ Rx1[04]- RO Str 2 from FEX 03
P22/J22	09	Fabric Channel 03	Tx2[03]+ Tx2[03]- RO Str 5 from FEX 02	Rx2[03]+ Rx2[03]- RO Str 3 from FEX 02	Tx3[03]+ Tx3[03]- RO Str 6 from FEX 02	Rx3[03]+ Rx3[03]- RO Str 4 from FEX 02
	10		Tx0[03]+ Tx0[03]- LHC Clk to FEX 02	Rx0[03]+ Rx0[03]- RO Str 1 from FEX 02	Tx1[03]+ Tx1[03]- TTC&ROD Ctl to FEX 02	Rx1[03]+ Rx1[03]- RO Str 2 from FEX 02
P23/J23	01	Fabric Channel 02	Tx2[02]+ Tx2[02]- RO Str 5 from FEX 01	Rx2[02]+ Rx2[02]- RO Str 3 from FEX 01	Tx3[02]+ Tx3[02]- RO Str 6 from FEX 01	Rx3[02]+ Rx3[02]- RO Str 4 from FEX 01
	02		Tx0[02]+ Tx0[02]- LHC Clk to FEX 01	Rx0[02]+ Rx0[02]- RO Str 1 from FEX 01	Tx1[02]+ Tx1[02]- TTC&ROD Ctl to FEX 01	Rx1[02]+ Rx1[02]- RO Str 2 from FEX 01
P23/J23	03	Fabric Channel 01	Tx2[01]+ Tx2[01]- RO Str 1 to othHUB	Rx2[01]+ Rx2[01]- RO Str 1 from othHUB	Tx3[01]+ Tx3[01]- RO Str 2 to othHUB	Rx3[01]+ Rx3[01]- RO Str2 from othHUB
	04		Tx0[01]+ Tx0[01]- LHC Clk to othHUB	Rx0[01]+ Rx0[01]- LHC Clk from othHUB	Tx1[01]+ Tx1[01]- TTC/ROD Ctl to othHUB	Rx1[01]+ Rx1[01]- TTC/ROD Ctl from othHUB
P23/J23	05	ShMC	BI_ShMCA+ BI_ShMCA- Unused signal pair	BI_ShMCB+ BI_ShMCB- Unused signal pair	BI_ShMCC+ BI_ShMCC- Unused signal pair	BI_ShMCD+ BI_ShMCD- Unused signal pair
P23/J23	06	Base Chan 02	BI_DA2+ BI_DA2- Unused signal pair	BI_DB2+ BI_DB2- Unused signal pair	BI_DC2+ BI_DC2- Unused signal pair	BI_DD2+ BI_DD2- Unused signal pair
P23/J23	07	Base Chan 03	BI_DA3+ BI_DA3- GE Pair A to FEX 01	BI_DB3+ BI_DB3- GE Pair B to FEX 01	BI_DC3+ BI_DC3- GE Pair C to FEX 01	BI_DD3+ BI_DD3- GE Pair D to FEX 01
P23/J23	08	Base Chan 04	BI_DA4+ BI_DA4- GE Pair A to FEX 02	BI_DB4+ BI_DB4- GE Pair B to FEX 02	BI_DC4+ BI_DC4- GE Pair C to FEX 02	BI_DD4+ BI_DD4- GE Pair D to FEX 02
P23/J23	09	Base Chan 05	BI_DA5+ BI_DA5- GE Pair A to FEX 03	BI_DB5+ BI_DB5- GE Pair B to FEX 03	BI_DC5+ BI_DC5- GE Pair C to FEX 03	BI_DD5+ BI_DD5- GE Pair D to FEX 03
P23/J23	10	Base Chan 06	BI_DA6+ BI_DA6- GE Pair A to FEX 04	BI_DB6+ BI_DB6- GE Pair B to FEX 04	BI_DC6+ BI_DC6- GE Pair C to FEX 04	BI_DD6+ BI_DD6 GE Pair D to FEX 04
J24/P24	01	Base Chan 07	BI_DA7+ BI_DA7- GE Pair A to FEX 05	BI_DB7+ BI_DB7- GE Pair B to FEX 05	BI_DC7+ BI_DC7- GE Pair C to FEX 05	BI_DD7+ BI_DD7- GE Pair D to FEX 05
J24/P24	02	Base Chan 08	BI_DA8+ BI_DA8- GE Pair A to FEX 06	BI_DB8+ BI_DB8- GE Pair B to FEX 06	BI_DC8+ BI_DC8- GE Pair C to FEX 06	BI_DD8+ BI_DD8- GE Pair D to FEX 06
J24/P24	03	Base Chan 09	BI_DA9+ BI_DA9- GE Pair A to FEX 07	BI_DB9+ BI_DB9- GE Pair B to FEX 07	BI_DC9+ BI_DC9- GE Pair C to FEX 07	BI_DD9+ BI_DD9- GE Pair D to FEX 07
J24/P24	04	Base Chan 10	BI_DA10+ BI_DA10- GE Pair A to FEX 08	BI_DB10+ BI_DB10- GE Pair B to FEX 08	BI_DC10+ BI_DC10- GE Pair C to FEX 08	BI_DD10+ BI_DD10- GE Pair D to FEX 08
J24/P24	05	Base Chan 11	BI_DA11+ BI_DA11- GE Pair A to FEX 09	BI_DB11+ BI_DB11- GE Pair B to FEX 09	BI_DC11+ BI_DC11- GE Pair C to FEX 09	BI_DD11+ BI_DD11- GE Pair D to FEX 09
J24/P24	06	Base Chan 12	BI_DA12+ BI_DA12- GE Pair A to FEX 10	BI_DB12+ BI_DB12- GE Pair B to FEX 10	BI_DC12+ BI_DC12- GE Pair C to FEX 10	BI_DD12+ BI_DD12- GE Pair D to FEX 10
J24/P24	07	Base Chan 13	BI_DA13+ BI_DA13- GE Pair A to FEX 11	BI_DB13+ BI_DB13- GE Pair B to FEX 11	BI_DC13+ BI_DC13- GE Pair C to FEX 11	BI_DD13+ BI_DD13- GE Pair D to FEX 11
J24/P24	08	Base Chan 14	BI_DA14+ BI_DA14- GE Pair A to FEX 12	BI_DB14+ BI_DB14- GE Pair B to FEX 12	BI_DC14+ BI_DC14- GE Pair C to FEX 12	BI_DD14+ BI_DD14- GE Pair D to FEX 12
J24/P24	09	Base Chan 15	BI_DA15+ BI_DA15- Unused signal pair	BI_DB15+ BI_DB15- Unused signal pair	BI_DC15+ BI_DC15- Unused signal pair	BI_DD15+ BI_DD15- Unused signal pair
J24/P24	10	Base Chan 16	BI_DA16+ BI_DA16- Unused signal pair	BI_DB16+ BI_DB16- Unused signal pair	BI_DC16+ BI_DC16- Unused signal pair	BI_DD16+ BI_DD16- Unused signal pair

15.2 Connector and Signal Usage for a FEX Slot

Connect Number	Row Num	Name	Connector Pin Pairs a b	c d	e f	g h
J20/P20	01	Clocks	CLK1A+ CLK1A- Unused signal pair	CLK1B+ CLK1B- Unused signal pair	CLK2A+ CLK2A- Unused signal pair	CLK2B+ CLK2B- Unused signal pair
J20/P20	02	Upd Chan & Clocks	Tx4(UP)+ Tx4(UP)- Unused signal pair	Rx4(UP)+ Rx4(UP)- Unused signal pair	CLK3A+ CLK3A- Unused signal pair	CLK3B+ CLK3B- Unused signal pair

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Connect Number	Row Num	Name	Connector Pin Pairs a b	c d	e f	g h
J20/P20	03	Update Chan	Tx2(UP)+ Tx2(UP)- Unused signal pair	Rx2(UP)+ Rx2(UP)- Unused signal pair	Tx3(UP)+ Tx3(UP)- Unused signal pair	Rx3(UP)+ Rx3(UP)- Unused signal pair
J20/P20	04	Update Chan	Tx0(UP)+ Tx0(UP)- Unused signal pair	Rx0(UP)+ Rx0(UP)- Unused signal pair	Tx1(UP)+ Tx1(UP)- Unused signal pair	Rx1(UP)+ Rx1(UP)- Unused signal pair
J20/P20	05	Fabric Channel 15	Tx2[15]+ Tx2[15]- Unused signal pair	Rx2[15]+ Rx2[15]- Unused signal pair	Tx3[15]+ Tx3[15]- Unused signal pair	Rx3[15]+ Rx3[15]- Unused signal pair
	06		Tx0[15]+ Tx0[15]- Unused signal pair	Rx0[15]+ Rx0[15]- Unused signal pair	Tx1[15]+ Tx1[15]- Unused signal pair	Rx1[15]+ Rx1[15]- Unused signal pair
J20/P20	07	Fabric Channel 14	Tx2[14]+ Tx2[14]- Unused signal pair	Rx2[14]+ Rx2[14]- Unused signal pair	Tx3[14]+ Tx3[14]- Unused signal pair	Rx3[14]+ Rx3[14]- Unused signal pair
	08		Tx0[14]+ Tx0[14]- Unused signal pair	Rx0[14]+ Rx0[14]- Unused signal pair	Tx1[14]+ Tx1[14]- Unused signal pair	Rx1[14]+ Rx1[14]- Unused signal pair
J20/P20	09	Fabric Channel 13	Tx2[13]+ Tx2[13]- Unused signal pair	Rx2[13]+ Rx2[13]- Unused signal pair	Tx3[13]+ Tx3[13]- Unused signal pair	Rx3[13]+ Rx3[13]- Unused signal pair
	10		Tx0[13]+ Tx0[13]- Unused signal pair	Rx0[13]+ Rx0[13]- Unused signal pair	Tx1[13]+ Tx1[13]- Unused signal pair	Rx1[13]+ Rx1[13]- Unused signal pair
J21/P21	01	Fabric Channel 12	Tx2[12]+ Tx2[12]- Unused signal pair	Rx2[12]+ Rx2[12]- Unused signal pair	Tx3[12]+ Tx3[12]- Unused signal pair	Rx3[12]+ Rx3[12]- Unused signal pair
	02		Tx0[12]+ Tx0[12]- Unused signal pair	Rx0[12]+ Rx0[12]- Unused signal pair	Tx1[12]+ Tx1[12]- Unused signal pair	Rx1[12]+ Rx1[12]- Unused signal pair
J21/P21	03	Fabric Channel 11	Tx2[11]+ Tx2[11]- Unused signal pair	Rx2[11]+ Rx2[11]- Unused signal pair	Tx3[11]+ Tx3[11]- Unused signal pair	Rx3[11]+ Rx3[11]- Unused signal pair
	04		Tx0[11]+ Tx0[11]- Unused signal pair	Rx0[11]+ Rx0[11]- Unused signal pair	Tx1[11]+ Tx1[11]- Unused signal pair	Rx1[11]+ Rx1[11]- Unused signal pair
J21/P21	05	Fabric Channel 10	Tx2[10]+ Tx2[10]- Unused signal pair	Rx2[10]+ Rx2[10]- Unused signal pair	Tx3[10]+ Tx3[10]- Unused signal pair	Rx3[10]+ Rx3[10]- Unused signal pair
	06		Tx0[10]+ Tx0[10]- Unused signal pair	Rx0[10]+ Rx0[10]- Unused signal pair	Tx1[10]+ Tx1[10]- Unused signal pair	Rx1[10]+ Rx1[10]- Unused signal pair
J21/P21	07	Fabric Channel 09	Tx2[09]+ Tx2[09]- Unused signal pair	Rx2[09]+ Rx2[09]- Unused signal pair	Tx3[09]+ Tx3[09]- Unused signal pair	Rx3[09]+ Rx3[09]- Unused signal pair
	08		Tx0[09]+ Tx0[09]- Unused signal pair	Rx0[09]+ Rx0[09]- Unused signal pair	Tx1[09]+ Tx1[09]- Unused signal pair	Rx1[09]+ Rx1[09]- Unused signal pair
J21/P21	09	Fabric Channel 08	Tx2[08]+ Tx2[08]- Unused signal pair	Rx2[08]+ Rx2[08]- Unused signal pair	Tx3[08]+ Tx3[08]- Unused signal pair	Rx3[08]+ Rx3[08]- Unused signal pair
	10		Tx0[08]+ Tx0[08]- Unused signal pair	Rx0[08]+ Rx0[08]- Unused signal pair	Tx1[08]+ Tx1[08]- Unused signal pair	Rx1[08]+ Rx1[08]- Unused signal pair
P22/J22	01	Fabric Channel 07	Tx2[07]+ Tx2[07]- Unused signal pair	Rx2[07]+ Rx2[07]- Unused signal pair	Tx3[07]+ Tx3[07]- Unused signal pair	Rx3[07]+ Rx3[07]- Unused signal pair
	02		Tx0[07]+ Tx0[07]- Unused signal pair	Rx0[07]+ Rx0[07]- Unused signal pair	Tx1[07]+ Tx1[07]- Unused signal pair	Rx1[07]+ Rx1[07]- Unused signal pair
P22/J22	03	Fabric Channel 06	Tx2[06]+ Tx2[06]- Unused signal pair	Rx2[06]+ Rx2[06]- Unused signal pair	Tx3[06]+ Tx3[06]- Unused signal pair	Rx3[06]+ Rx3[06]- Unused signal pair
	04		Tx0[06]+ Tx0[06]- Unused signal pair	Rx0[06]+ Rx0[06]- Unused signal pair	Tx1[06]+ Tx1[06]- Unused signal pair	Rx1[06]+ Rx1[06]- Unused signal pair
P22/J22	05	Fabric Channel 05	Tx2[05]+ Tx2[05]- Unused signal pair	Rx2[05]+ Rx2[05]- Unused signal pair	Tx3[05]+ Tx3[05]- Unused signal pair	Rx3[05]+ Rx3[05]- Unused signal pair
	06		Tx0[05]+ Tx0[05]- Unused signal pair	Rx0[05]+ Rx0[05]- Unused signal pair	Tx1[05]+ Tx1[05]- Unused signal pair	Rx1[05]+ Rx1[05]- Unused signal pair
P22/J22	07	Fabric Channel 04	Tx2[04]+ Tx2[04]- Unused signal pair	Rx2[04]+ Rx2[04]- Unused signal pair	Tx3[04]+ Tx3[04]- Unused signal pair	Rx3[04]+ Rx3[04]- Unused signal pair
	08		Tx0[04]+ Tx0[04]- Unused signal pair	Rx0[04]+ Rx0[04]- Unused signal pair	Tx1[04]+ Tx1[04]- Unused signal pair	Rx1[04]+ Rx1[04]- Unused signal pair
P22/J22	09	Fabric Channel 03	Tx2[03]+ Tx2[03]- Unused signal pair	Rx2[03]+ Rx2[03]- Unused signal pair	Tx3[03]+ Tx3[03]- Unused signal pair	Rx3[03]+ Rx3[03]- Unused signal pair
	10		Tx0[03]+ Tx0[03]- Unused signal pair	Rx0[03]+ Rx0[03]- Unused signal pair	Tx1[03]+ Tx1[03]- Unused signal pair	Rx1[03]+ Rx1[03]- Unused signal pair
P23/J23	01	Fabric Channel 02	Tx2[02]+ Tx2[02]- RO Stream 3 to HUB 2	Rx2[02]+ Rx2[02]- RO Stream 5 to HUB 2	Tx3[02]+ Tx3[02]- RO Stream 4 to HUB 2	Rx3[02]+ Rx3[02]- RO Stream 6 to HUB 2
	02		Tx0[02]+ Tx0[02]- RO Stream 1 to HUB 2	Rx0[02]+ Rx0[02]- Unused signal pair	Tx1[02]+ Tx1[02]- RO Stream 2 to HUB 2	Rx1[02]+ Rx1[02]- Unused signal pair
P23/J23	03	Fabric Channel 01	Tx2[01]+ Tx2[01]- RO Stream 3 to HUB 1	Rx2[01]+ Rx2[01]- RO Stream 5 to HUB 1	Tx3[01]+ Tx3[01]- RO Stream 4 to HUB 1	Rx3[01]+ Rx3[01]- RO Stream 6 to HUB 1
	04		Tx0[01]+ Tx0[01]- RO Stream 1 to HUB 1	Rx0[01]+ Rx0[01]- LHC Clock	Tx1[01]+ Tx1[01]- RO Stream 2 to HUB 1	Rx1[01]+ Rx1[01]- TTC&ROD Ctrl stream

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Connect Number	Row Num	Name	Connector Pin Pairs a	b	c	d	e	f	g	h
P23/J23	05	Base Chan 01	BI_DA1+ GE Pair A	BI_DA1- IPbus Net	BI_DB1+ GE Pair B	BI_DB1- IPbus Net	BI_DC1+ GE Pair C	BI_DC1- IPbus Net	BI_DD1+ GE Pair D	BI_DD1- IPbus Net
P23/J23	06	Base Chan 02	BI_DA2+ GE Pair A	BI_DA2- IPMC Net	BI_DB2+ GE Pair B	BI_DB2- IPMC Net	BI_DC2+ GE Pair C	BI_DC2- IPMC Net	BI_DD2+ GE Pair D	BI_DD2- IPMC Net
P23/J23	07	Base Chan 03	BI_DA3+ Unused signal pair	BI_DA3-	BI_DB3+ Unused signal pair	BI_DB3-	BI_DC3+ Unused signal pair	BI_DC3-	BI_DD3+ Unused signal pair	BI_DD3-
P23/J23	08	Base Chan 04	BI_DA4+ Unused signal pair	BI_DA4-	BI_DB4+ Unused signal pair	BI_DB4-	BI_DC4+ Unused signal pair	BI_DC4-	BI_DD4+ Unused signal pair	BI_DD4-
P23/J23	09	Base Chan 05	BI_DA5+ Unused signal pair	BI_DA5-	BI_DB5+ Unused signal pair	BI_DB5-	BI_DC5+ Unused signal pair	BI_DC5-	BI_DD5+ Unused signal pair	BI_DD5-
P23/J23	10	Base Chan 06	BI_DA6+ Unused signal pair	BI_DA6-	BI_DB6+ Unused signal pair	BI_DB6-	BI_DC6+ Unused signal pair	BI_DC6-	BI_DD6+ Unused signal pair	BI_DD6
J24/P24	01	Base Chan 07	BI_DA7+ Unused signal pair	BI_DA7-	BI_DB7+ Unused signal pair	BI_DB7-	BI_DC7+ Unused signal pair	BI_DC7-	BI_DD7+ Unused signal pair	BI_DD7-
J24/P24	02	Base Chan 08	BI_DA8+ Unused signal pair	BI_DA8-	BI_DB8+ Unused signal pair	BI_DB8-	BI_DC8+ Unused signal pair	BI_DC8-	BI_DD8+ Unused signal pair	BI_DD8-
J24/P24	03	Base Chan 09	BI_DA9+ Unused signal pair	BI_DA9-	BI_DB9+ Unused signal pair	BI_DB9-	BI_DC9+ Unused signal pair	BI_DC9-	BI_DD9+ Unused signal pair	BI_DD9-
J24/P24	04	Base Chan 10	BI_DA10+ Unused signal pair	BI_DA10-	BI_DB10+ Unused signal pair	BI_DB10-	BI_DC10+ Unused signal pair	BI_DC10-	BI_DD10+ Unused signal pair	BI_DD10-
J24/P24	05	Base Chan 11	BI_DA11+ Unused signal pair	BI_DA11-	BI_DB11+ Unused signal pair	BI_DB11-	BI_DC11+ Unused signal pair	BI_DC11-	BI_DD11+ Unused signal pair	BI_DD11-
J24/P24	06	Base Chan 12	BI_DA12+ Unused signal pair	BI_DA12-	BI_DB12+ Unused signal pair	BI_DB12-	BI_DC12+ Unused signal pair	BI_DC12-	BI_DD12+ Unused signal pair	BI_DD12-
J24/P24	07	Base Chan 13	BI_DA13+ Unused signal pair	BI_DA13-	BI_DB13+ Unused signal pair	BI_DB13-	BI_DC13+ Unused signal pair	BI_DC13-	BI_DD13+ Unused signal pair	BI_DD13-
J24/P24	08	Base Chan 14	BI_DA14+ Unused signal pair	BI_DA14-	BI_DB14+ Unused signal pair	BI_DB14-	BI_DC14+ Unused signal pair	BI_DC14-	BI_DD14+ Unused signal pair	BI_DD14-
J24/P24	09	Base Chan 15	BI_DA15+ Unused signal pair	BI_DA15-	BI_DB15+ Unused signal pair	BI_DB15-	BI_DC15+ Unused signal pair	BI_DC15-	BI_DD15+ Unused signal pair	BI_DD15-
J24/P24	10	Base Chan 16	BI_DA16+ Unused signal pair	BI_DA16-	BI_DB16+ Unused signal pair	BI_DB16-	BI_DC16+ Unused signal pair	BI_DC16-	BI_DD16+ Unused signal pair	BI_DD16-