ATLAS Level-1 Calorimeter Trigger Update

HUB Firmware Specification

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1. FEX HUB overview

The FEX-Hub module is an integral part of the L1Calo system. Its primary functions are to support FEX system readout, provide switching functionality for module control and DCS IPbus networks and to distribute timing and control signals to the FEX modules. There are to be two Hub modules per shelf. Both Hub modules will receive multi-gigabit FEX data over the ATCA Fabric Interface, which will be fanned out to a ROD mezzanine on the Hub and to the Hub's own FPGA. This high-speed data path will include two data channels from the other Hub module. The Hub module in logical slot 1 will provide switching capability for a network that routes module control signals on the base interface, while the Hub in logical slot 2 will provide switching for a network that routes DCS information. The Hub module in slot 1 will further receive TTC information from the FELIX system, and these signals will be decoded and fanned out to the FEX modules, ROD modules and also to the Hub in slot 2. The fanned-out TTC control data stream will be interleaved with ROD-to-FEX communications including. for example, back-pressure signals. The Hub module has connections to the other slots in the ATCA shelf over three distinct electrical interfaces. ATCA backplane Zone-2 consists of the Fabric Interface and the Base Interface. The Fabric Interface provides 8 differential pairs (channels) from each node slot to each Hub slot (8 to Hub-1 and 8 to Hub-2). There are a total of 8 Fabric Interface channels between Hub-1 and Hub-2 (not 16 total). The Fabric Interface pairs have a nominal bandwidth specification of 10 Gbps / channel. The Base Interface provides 4 differential pairs between each node slot and each Hub slot. There are a total of 4 Base Interface channels between Hub-1 and Hub-2. The Base Interface lines have a nominal bandwidth specification of 500 Mbps / channel, suitable for Gbps Ethernet protocol. Finally, ATCA backplane Zone-1 provides each node and Hub slot with a connection to the Intelligent Platform Management Bus (IPMB) with a total bandwidth of 100 kbps. The Hub module will provide MPO connectors in the ATCA Zone-3 region, which will allow for the routing of fiberoptic cables to/from the MiniPODs on the Hub and ROD modules. The L1Calo FEX-Hub system will consist of eight modules. There will be two eFEX shelves, one iFEX shelf and one L1Topo shelf, each hosting two Hub modules.

1.1 HUB Functionality

1.1.1 Support of the ROD Mezzanine Card

The FEX Hub physically holds the ROD Mezzanine Card and provides electrical connections to it through two 400 pin Meg-Array connectors.

1.1.2 FEX and FEX-Hub Readout Data Distribution

The FEX-Hub receives over the Fabric Interface 6 serial streams of Readout Data from each FEX Module. Each FEX-Hub also receives over the Fabric Interface 2 serial streams of Readout Data from the other FEX-Hub in the crate. These 74 high speed serial streams are fanned out on the FEX-Hub. One copy of each stream is sent to the ROD and one copy is sent to the Hub's own UltraScale FPGA. The Hub FPGA also sends 2 serial streams with its own Readout Data to its own ROD. Each ROD thus receives a total of 76 high speed Readout Data streams: 6 streams from each FEX, 2 streams from the local Hub FPGA and 2 streams from the other Hub's Hub FPGA. The data rate per readout stream will be 10 Gbps or less.

1.1.3 TTC Clock and Data Stream Distribution

The FEX-Hub in Slot 1 uses a 12-channel MiniPOD optical receiver to receive TTC signals from the upstream FELIX system. The FEX-Hub receives two types of TTC signals: a copy of the LHC clock and TTC control data. These signals need to be fanned out to each FEX module, to the local ROD, to the local Hub FPGA and to the FEX-Hub in Slot 2 (including its ROD). The LHC clock is directly forwarded without any processing on the FEX-Hub. The TTC control data will be merged with additional control information coming from the ROD module from each FEX-Hub before being fanned out. The FEX-Hub uses two ports from the Fabric Interface Channel to each Node Slot to fanout these two signals to each FEX. These two TTC and control signals sent to the FEX plus the 6 Readout Data streams received from each FEX use all 8 signals pairs of each Fabric Channel connecting one FEX to the FEX-Hub, albeit with an unconventional port direction usage. The FEX-Hub in Slot 2 does receive the TTC information from FELIX directly, but receives the TTC Clock and the TTC/ROD readout control stream from the FEX-Hub in Slot 1. The FEX-Hub in Slot 2 sends any required ROD readout control data generated by its own ROD to the FEX-Hub in Slot 1 for inclusion in the combined TCC/ROD readout control data stream.

1.1.4 Ethernet Network Switch

The FEX-Hub hosts an un-managed 10/100/1000 Base-T switch to provide the following 19 Gigabit Ethernet connections [see Figure 1]:

- 1 connection on the front panel for the "up-link"
- 12 connections to the "FEX Node" modules in this crate via the Base Channel Fabric
- 1 connection to the ROD on this Hub (or IPMC on the other Hub) via the front panel
- 1 connection to the ROD on the other Hub (or IPMC on this Hub) via the front panel
- 1 connection to the other Hub's UltraScale FPGA via the Update Channel Interface
- 1 spare front panel connection

1.1.5 Slow Control (IPbus to HUB and ROD)

HUB: An IPbus interface provides high-level, functional control of the FEX-Hub module. This allows, for example, setting any firmware parameters, controlling modes of operation and reading monitoring data. Figure below shows the Hub's Base Interface Ethernet Switch in the context of the other cards in the ATCA shelf. ROD: An Ethernet link is provided from the main ROD FPGA to the Ethernet switch on the Hub. This will allow a computer using IPbus to:

- Access registers within the ROD FPGA, setting parameters and controlling modes of operation.
- Store FPGA configurations into the SPI-Flash Configuration Memory.
- Initiate the loading of configurations from the SPI-Flash.

This can be used to load a configuration from one of a number of other SPI-Flash sectors. These sectors can be written via IPbus.



Figure 1: Illustration of FEX-Hub Ethernet network connections.

The Hub Module requires two physical chips for the Ethernet Base Interface connections to its FPGA (Micrel KSZ9031RNX <u>http://ww1.microchip.com/downloads/en/DeviceDoc/00002117B.pdf</u> – it can operate with a 1.8V RGMII port and thus directly connect to the Virtex7 HP I/O pins). Two FPGA MACs are connected to the physical chips via RGMII ports. This chip has both the RGMII signal connection to the FPGA that is used to move the actual Ethernet data and provides access to internal registers and also has a 2 wire serial "Management Data" port.



Figure 2: Illustration of Xilinx ETHERNET MAC IP and PHYS chip (KSZ9031RNX).

Phys Chip - Power, Clock, Reset, and LED Circuits



Figure 3: Schematic view of U21 Phys chip: Power, Clock, Reset.

Phys Chip - RGMII, MDC/DMIO, and Base-T Circuits



Figure 4: Scheme of Phys Chip: RGMII, MDC/DMIO, and Base-T Circuits.

Board Reset Distribution - ROD Power Control



Figure 5: Board Reset Distribution, ROD Power Control.

For each of its two Ethernet Phys Chips (PHY) the Hub's FPGA will need to instance a MAC that supports an RGMII connection (along with MDIO/MDC lines) to the PHY. All of these signals to/from the PHY are currently routed through the 1V8 HP Select I/O Bank 68.

After power-up the KSZ9031RNX is configured to RGMII mode if the MODE [3:0] strap-in pins are set to one of the RGMII mode capability options.

There is no reset signal to the KSZ9031RNX from FPGA. An ad hoc manual push button was attached to the PHY chip on the HUB for debugging purposes.

The KSZ9031RNX RGMII port connects to HP I/O pins on the FPGA. The RGMII port consists of 12 signals:

- Transmit Clock to the KSZ9031RNX
- Transmit Control (enable) to the KSZ9031RNX
- Transmit Data 0:3 to the KSZ9031RNX
- Receive Clock from the KSZ9031RNX
- Receive Control (enable) from the KSZ9031RNX
- Receive Data 0:3 from the KSZ9031RNX

The KSZ9031RNX includes a MII Management port. This type of port is also called MDIO Management Data Input/Output. This port allows higher-level devices to monitor and control the KSZ9031RNX. This port allows direct access to the IEEE defined MIIM registers, and the vendor specific registers. This port also allows indirect access to the MMD address space and registers. This port consists of signals: MDC - the clock and MDIO - the data line.

The Hub Module has two KSZ9031RNX PHY chips. There are 14 jumpers associated with each of these PHY chips. These jumpers are resistors that bias a pin in one direction or the other and this value is read when the PHY chip first powers up or is reset.

The KSZ9031RNX has 9 pins (called "Strapping Options") that are read in this way at power up. Because of space limitations and because there is an obvious why that the Hub Module wants some of these Strapping Options set, 4 of them have only one jumper to pull that pin in the direction that is obviously needed for rational operation of the Hub Module.

The PHYADx jumpers set the address of the Management Interface Port on the KSZ9031RNX. The Management Port PHYAD bits 3 and 4 are internally always set to 0,0. Bits 2, 1 and 0 set to Low. Therefore, the PHYADx set to 0.

The Hub Module provides easy control of only the Mode_0 and Mode_1 lines. This provides the following 4 options for the Phys chip (Mode bits listed Mode_3, ..., Mode_0).

- 1100 RGMII 1000 Base-T full duplex only
- 1101 RGMII 1000 Base-T full or half duplex
- 1110 RGMII 10/100/100 all but 1000 half duplex
- 1111 RGMII 10/100/1000 full or half duplex

Mode: SET MODE {3..0} = 1100 - RGMII 1000 Base-T full duplex only

The Xilinx Tri-Mode Ethernet MAC core is a parameterizable core, in 1000 Mbps mode, the TEMAC core can also connect with industry standard PHY devices. Optional MDIO interface to managed objects in PHY layers (MII Management).



Figure 6: Scheme of Xilinx MAC Example HDL Design (UltraScale).

The following design approach is based on the suggestion by Ed Flaherty (University of Cambridge):

- Step 1: Generate Xilinx MAC Example Design (UltraScale RGMII).
- Step 2: Modify the Example Design to HUB board hardware.
- Step 3: Generate Tx packets with built-in Simple Frame Generator and capture them in Wireshark.
- Step 4: Packet generation logic replaced with simple read fifo (Rx looped back to Tx).
- Step 5: Packets sent from server (Ostinato) returned via the loopback proving Rx and Tx paths.
- Step 6: Use Wireshark to check returned packets

IPBus porting: 3 Steps Step 2: Stripped down RGMII Example Design



Stripped-down example design

- Packet generation logic replaced with simple read fifo (looped back)
- All of the example design MAC+Support logic and constraints retained
- Verification: Packets sent from server were returned via the loopback proving Rx and Tx paths

Ed Flaherty 7-June-2016	Fig
	ure
7: IPBus porting.	

As soon as the MAC part works, the IPbus control part and the IPbus slaves can be added to the design, as described in the note: Notes on Firmware Implementation of an IPbus SoC Bus, V1.0 23/5/2012, DMN".



Figure 8: IPBus topology.

The SoC bus is fully synchronous, and operates from a single system clock. There is no constraint on the relationship of the bus clock to the 125MHz GbE clock, as the firmware contains handshaking logic. For slaves, which do not require wait states, the 32b data path on the SoC bus allows full utilization of the Ethernet interface as long as it runs at >32MHz; this allows straightforward timing closure for complex multi-slave designs. Designs therefore typically drive the Ipbus clock at ¹/₄ of the GbE clock (i.e. 31.25MHz).

Hub FPGA Registers

Initial	Rev.	02-Eev-2017
THILLAI	Nev.	02-FEV-201/

Addr	туре	Name	Content	Bit	Comment
00000000	RO	hub_module	module_type hw_revision fw_type fw_version	8 8 8 8	Set in FPGA FW idem idem idem
00000001	RO	hub_address	shelf_adrs slot_adrs adrs_to_rod spare	8 8 8 8	Shelf Address from the IPMC Backplane Hardware Slot Address Overall Hardware Address to the ROD (generated) -
00000002	RO	hub_alerts	no_pll_lock phy_int mpod_int hub_smb_alert hub_pwr_not_ok no_rod rod_smb_alert rod_status no_sw_loop_det spare	2 2 1 1 1 3 3 16	From PLL lock circuits From Eth Phy chips From the MiniPODs From 7 DCDC Converters From the Power Control circuits ROD is NOT present Power supply problem on the ROD no ROD power, ROD not config, spare From the Broadcom Switch chips - * at normal operation all bits = '0'
00000003	RW	hub_control	other_hub_Clk fex_Clk_dis mgt_equ i2c_buf_dis led_drv rod_pwr_en sw_loop_det mpod_rst spare	1 13 3 1 3 2 4	FPGA internal, selects clock from other Hub Disable clock to FEXs Disable equalization in MGT Fanout chips Disable Sensor I2C Bus translator/buffer chips Front palnel LEDs control ROD may turn ON its power supplies To the Broadcom Switch chips TX and RX MiniPODs resets * after power ON all bits set to '0'

RO hub_module: general HUB information (Module ID, HW/FW versions)
 RO hub_address: external FPGA input pins for shelf and slot addresses, read internally generated address to ROD.
 RO hub_alerts: all bits ='0' in normal operation, set to '1' by external signals
 RW hub_control: on power ON all bits ='0'; set and cleared via IPbus.

Table 1: The initial HUB FPGA register map.

2. Combined_TTC/DATA

The HUB FW is obliged to distribute TTC information throughout the shelf [2]. There are several Combined_TTC links within the shelf, one between each Fex slot (slots 3-14) and each Hub, also one between each Hub and ROD and 2 links between two HUBs.

The additional feature allow to transmit the Reset signal (Aurora Initialization, Figure 9) from the Readout_Ctrl link and distribute it to the appropriate shelf slot. In total, we have the following number of links:

- 12 links between each FEX slot and each HUB
- 1 link between the ROD and each HUB
- 2 links between two HUBs



Figure 9. Example of link Reset Routing.

2.1 Combined_TTC/DATA - Physical Implementation

The Combined_TTC/Data link on the HUB FPGA is implemented with the use of several components, including the MGT transceivers (GTH and GTY), control and the diagnostic logic. The Combined_TTC/DATA link is designed to operate at 6.4 Gbps. The physical implementation of the Combined_TTC/DATA links assumes that there are 4 Control Registers on the Hub TX side, and Shadow Registers on the Rx side (Receiver: FEX, ROD and other HUB). The transmitter side generates the 128 bit message from 4 Control registers: Word_0, Word_1, Word_2, and Word_3. The transmitter side logic is in charge to write control information into these Control Registers. The contents of these registers are continuously transmitted to the modules (within the shelf) which receives the data into a duplicate set of 4 registers referred to as shadow registers. Anything written into a Control Register at the transmitter side will appear in the corresponding Shadow register at the shelf) which receives for the Sb10b Comma character K28.5.

2.2 Combined_TTC/DATA - Control Bit Definition

The bits within the Combined_TTC/DATA control words are primarily defined to provide TTC information as well as initialization functions for all of the Fex data links (Aurora in the case of eFex). The TTC information is sourced from a dedicated TTC interface on the Hub. The Reset information is received from the ROD via the Readout_Ctrl link.

Comma Character

Bits 7 to 0 of Word_0 contain the Comma character that maintains alignment of the 4 shadow registers with their corresponding Control registers. The chosen character is K28.5 = 0xBC.

Version

The 4-bit value contains the version number of this overall bit assignment. It will be held at "0000" through the initial debug phases, where many changes may occur.

Reset 3:0

These bits provide a system level reset/enable function. There are four per slot, and the functionality of these bits will be specified by the targets (eFex, jFex, etc)

Level-1 Accept (L1A)

L1 Accept is used to indicate when an event has been accepted by the Central Trigger Processor.

Bunch Counter Reset (BCR)

Entities within the shelf may keep local bunch counters. These are kept in sync using the BCR. The Bunch Counter is a local 12-bit counter that increments each LHC clock. It counts to a value of 3563 and then rolls over to 0. It is reset to a value of '0' when on BCR (Bunch Counter Reset)

Event Counter Reset (ECR)

Entities within the shelf may keep local event counters. These are kept in sync using the ECR. The Event counter is a local 24-bit counter that increments each L1A. It is reset to '-1' on ECR.

Privileged Readout

This bit indicates that a full data readout has been requested. On each 40 MHz cycle, the delayed L1A, ECR, and BCR are read from the pipeline. If the L1A bit is set, the PRO FIFO is inspected. If the FIFO is not empty (this is the expected condition), the PRO 0 or 1 value is read and asserted on the backplane at the same time as the L1A, ECR, and BCR.

TTC Reserved

These bits are reserved for possible expansion of TTC information in Phase-II.

Combined Data to FEX 08 Combined Data to FEX 07 N.C. N.C. MGT_FO_37 PF ---MGT_FO_38 ST ---MGT_FO_39 ST ---MGT_FO_40 ST ---Other_Hub_RO Other_Hub_RO FEX_9 Rx 3 Rx 2 Rx 1 → ST → ST → ST → ST Tx 3 Tx 2 Tx 1 AL_0 1 $\sqrt{\sqrt{2}}$ AL_1 AL_0 133 FEX_9 0 MGT_F0_25 MGT_F0_26 MGT_F0_27 MGT_F0_28 $\sqrt{\sqrt{\sqrt{2}}}$ Tx 3 Tx 2 Tx 1 Tx 0 → ST → ST → ST → ST FEX_7 FEX_7 FEX_7 AL_0 AL_1 AL_2 AL_3 PF PF PF PF Rx 3 Rx 2 Rx 1 Combined Data to FEX 06 ж 1 N.C. N.C. N.C. 132 0 Rx MGT_FO_35 MGT_FO_36 MGT_FO_29 MGT_FO_30 FEX_8 FEX_8 FEX_7 FEX_7 PF PF PF → ST → ST → ST → ST AL_4 AL_5 AL_4 AL_5 Rx 3 Rx 2 Rx 1 Tx 3 Tx 2 Tx 1 N.C. N.C. N.C. N.C. $\sqrt{\sqrt{\sqrt{2}}}$ 1 131 Ó Тx MGT_FO_31 MGT_FO_32 MGT_FO_17 MGT_FO_18 Rx 3 Rx 2 Rx 1 Tx 3 Tx 2 Tx 1 N.C. Combined Data to FEX 05 $\sqrt{\sqrt{\sqrt{2}}}$ ^^^ ST ST ST FEX_8 .0 PF AI ж 1 FEX_8 FEX_5 PF AL_1 AL_4 130 _ N.C. Combined Data to FEX 04 Rx 0 0 Тx MGT_FO_19 MGT_FO_20 MGT_FO_21 MGT_FO_22 Rx 3 Rx 2 Rx 1 Rx 0 PF PF PF Tx 3 Tx 2 Tx 1 $\sqrt{\sqrt{\sqrt{2}}}$ N.C. FEX_6 AL_0 1 FEX_6 FEX_6 AL_1 AL_2 AL_3 Combined Data to FEX 03 129 _ N.C. Combined Data to Other Hub PF Ťx Ó MGT_FO_23 MGT_FO_24 MGT_FO_09 MGT_FO_10 PF PF PF Rx 3 Rx 2 Rx 1 Rx 0 Tx 3 Tx 2 Tx 1 Tx 0 N.C. N.C. N.C. N.C. ST ST ST FEX_6 $\sqrt{\sqrt{\sqrt{2}}}$ 0 ₹ FEX_6 FEX_4 AL_2 <u>128</u> MGT_FO_11 MGT_FO_12 MGT_FO_13 MGT_FO_14 Rx 3 Rx 2 Rx 1 Tx 3 Tx 2 Tx 1 Hub Readout AL_0 to Other Hub N.C. AL_4 AL_5 AL_0 PF $\sqrt{\sqrt{\sqrt{2}}}$ 0 ж PF PF FEX_4 FEX_5 127 PF Rx Ò Tx 0 PP Hub Readout AL_1 to Other Hub AL_1 — C.L. C.L. -> < Rx 3 Rx 2 Rx 1 Rx 0 MGT_FO_15 MGT_FO_16 MGT_FO_01 MGT_FO_02 Tx 3 Tx 2 Tx 1 Tx 0 AL_2 AL_3 AL_0 $\sqrt{\sqrt{\sqrt{2}}}$ ST ST ST ST N.C. N.C. N.C. N.C. PF FEX_5 ≻ 0 FEX_5 FEX_3 PF PF PF Ş 126 AL_1 MGT_FO_03 MGT_FO_04 MGT_FO_05 MGT_FO_06 AL_2 AL_3 AL_4 AL_5 Rx 3 Rx 2 Rx 1 > ST >> ST >> ST >> ST >> ST FEX_3 FEX_3 FEX_3 $\sqrt{\sqrt{\sqrt{2}}}$ Tx 3 Tx 2 Tx 1 N.C. N.C. N.C. N.C. PF 0 ж PF PF PF 125 ò Ó Тx FEX_4 AL_0 MGT_FO_07 PF FEX_4 AL_1 MGT_FO_08 PF Combined Data from Other Hub PF Receiver MiniPOD Fiber 8 ST Rx 3 Rx 2 Rx 1 Tx 3 Tx 2 Tx 1 ST ST ST N.C. N.C. N.C. 0 ⇒ ÷ 124 ÷ Tx Ö Rx 0 ★ → These Quads receive ST -> Straight Through the LHC locked PF -> Polarity Flip 320.6296 MHz AL -> Aurora Lane Number reference clock. 0,1 -- UltraScale FPGA MGT_FO_ -> MGT Data Fanout Super Logic Region Channel Number N.C. - No Connection Drw: 22

Figure 10. HUB MGT assignments (GTY Transceivers – QUADs 124:133)

FEX_10 FEX_10 FEX_10 AL_3 AL_2 AL_1 Rx 3 Rx 2 Rx 1 Rx 0 Tx 3 Tx 2 Tx 1 Tx 0 → PF → PF → ST MGT_F0_48 MGT_F0_47 MGT_F0_46 ST PF PF Combined Data to FEX 09 1 2<u>33</u> 1 Combined Data to FEX 10 N.C. N.C. MGT_FO_45 FEX_9 FEX_9 FEX_9 FEX_9 MGT_F0_44 MGT_F0_43 MGT_F0_42 MGT_F0_41 Tx 3 Tx 2 Tx 1 Tx 0 AL_5 AL_4 AL_3 AL_2 PF PF PF Rx Rx Rx Rx PF ST ST ST Combined Data to FEX 11 3 2 1 0 ж 1 _ Ş N.C. N.C. N.C. <u>232</u> Rx 3 Rx 2 Rx 1 Rx 0 MGT_F0_34 MGT_F0_33 MGT_F0_56 MGT_F0_55 ST ST PF PF Tx 3 Tx 2 Tx 1 Tx 0 ST ST ST FEX_8 AL_3 AL_2 AL_5 N.C. 1 FEX_8 FEX_11 ş N.C. N.C. 231 ST PF ST MGT_F0_54 MGT_F0_53 MGT_F0_52 Rx 3 Rx 2 Rx 1 FEX_11 AL_3 AL_2 AL_1 Tx 3 Tx 2 Tx 1 Combined Data to FEX 12 N.C. N.C. ж 1 PF ₹ FEX_11 FEX_11 230 Rx Combined Data to FEX 13 FO 51 0 0 FEX_11 Rx 3 Rx 2 Rx 1 Rx 0 FEX_10 FEX_10 FEX_13 FEX_13 MGT_F0_50 MGT_F0_49 MGT_F0_64 MGT_F0_63 Tx 3 Tx 2 Tx 1 Tx 0 PF PF PF ST PF ST ST N.C. 1 Combined Data to FEX 14 N.C. AL_4 AL_1 $\wedge \wedge \wedge$ <u>229</u> Hub Readout AL_0 to This ROD AL_5 AL_4 AL_3 Tx 3 Tx 2 Tx 1 Tx 0 Hub Readout AL_1 to This ROD N.C. MGT_F0_62 MGT_F0_61 MGT_F0_60 PF PF PF Rx 3 Rx 2 Rx 1 Rx 0 ST ST ST FEX_12 FEX_12 FEX_12 0 \rightarrow ž ₹ 228 Combined Data to This ROD Rx 3 Rx 2 Rx 1 Rx 0 Tx 3 Tx 2 Tx 1 → PF → → PF PF PF PF FEX_12 N.C. $\sqrt{\sqrt{2}}$ ж 0 MGT_F0_57 MGT_F0_74 MGT_F0_73 FEX_12 FEX_14 FEX_14 AL_0 AL_5 AL_4 Transmitter MiniPOD Fiber 0 227 N.C. Transmitter MiniPOD Fiber 1 ò C.L. < - C.L. > Rx 3 Rx 2 Rx 1 Rx 0 Tx 3 Tx 2 Tx 1 Tx 0 ST PF ST PF FEX_14 FEX_14 FEX_14 FEX_14 AL_3 AL_2 AL_1 AL_0 MGT_F0_72 MGT_F0_71 MGT_F0_70 MGT_F0_69 ST PF PF N.C. 0 Ş ş Transmitter MiniPOD Fiber 2 226 N.C. Transmitter MiniPOD Fiber 4 MGT_F0_68 MGT_F0_67 MGT_F0_66 MGT_F0_65 Rx 3 Rx 2 Rx 1 Rx 0 Tx 3 Tx 2 Tx 1 Tx 0 FEX_13 FEX_13 AL_5 AL_4 AL_3 AL_2 PF $\sqrt{\sqrt{\sqrt{2}}}$ ^^^ ST PF ST PF N.C. 0 ж PF PF PF Transmitter MiniPOD Fiber 6 225 FEX_13 N.C. Transmitter MiniPOD Fiber 8 Readout Control Data from This ROD Receiver MiniPOD Fiber 2 Receiver MiniPOD Fiber 4 Rx 3 Rx 2 Rx 1 Rx 0 Tx 3 Tx 2 Tx 1 ST PF ST PF N.C. PF 0 \rightarrow ST ST ST Ź Transmitter MiniPOD Fiber 10 224 N.C. Receiver MiniPOD Fiber 6 Ó Transmitter MiniPOD Fiber 11 ★ → These Quads receive ST -> Straight Through the LHC locked PF -> Polarity Flip 320.6296 MHz AL -> Aurora Lane Number reference clock. 0,1 -> UltraScale FPGA MGT_FO_ -> MGT Data Fanout Super Logic Region Channel Number N.C. -> No Connection Drw: 23 C.L. -> Center Line of BGA Rev. 31-Jan-2018

Figure 11. HUB MGT assignments (GTH Transceivers – QUADs 224:233)

L1ID

The L1ID should match the value in a local Event Counter. However, it is broadcast explicitly over this link to enhance channel reliability. If a CRC error is detected in a message, then all four words must be discarded. In this case, the L1A may be completely missed, thus putting the local entity out of sync with the rest of the system. The L1ID however, may be correctly read in the next message that doesn't contain a crc error.

ECRID

These bits are an extension of the L1ID. In the past, this has been generated on each board independently. Now the L1ID and ECRID bits are combined into a single 32-bit counter and broadcast from the Hub to all other boards.

Control Channel

These bits are reserved for a possible future implementation of a message channel

Link Reset

As the Receiver, the ROD must control all of the Data Link (Aurora) initialisation. The Link Reset signal is therefore derived from the Readout_Ctrl link. The Hub should connect to the appropriate Readout_Ctrl Link Reset for the slot to which the Combined_TTC is connected. Each endpoint also has a local reset timer to control Aurora link establishment. Below is an example of routing from Hub to a Slot-3 Fex

ROD_BUSY

When active, this signal indicates that the ROD cannot currently accept further data from Fex sources. This signal is taken from the Readout_Ctrl and is fanned-out to the shelf FEX's over each slot's Combined TTC link.

ROD 0 Channel Up, ROD 1 Channel UP

These signals indicate to each FEX whether or not the corresponding ROD Rx Aurora channel is "Up".

ROD Reserved

These bits are reserved for future ROD functionality to be defined

Shelf Number

The Hub provides the shelf number to all Combined_TTC targets via these bits.

CRC (9-bit)

CRC is included to provide additional robustness on this link. Erroneous resets could cause loss of data. Choice of polynomial is from https://users.ece.cmu.edu/~koopman/crc/index.html

The chosen polynomial is 0x17d in Koopman format of 0x2fb in explicit+1 format.

2.2 Combined_TTC/DATA - FW development strategy

The Combined_TTC/DATA FW development comprises several stages. In terms of Combined_TTC/DATA link, the first stage assumes to provide the Combined_TTC/Data to the ROD module, also to the FEX slot 3. In order to debug the design, the standard Xilinx diagnostic components are being used to monitor the data flow (as for example like the ILA and VIO). The physical layer is configured with the use of GT wizard.

For the purpose of the current test, the HUB transmitter side generates the 128 bits from 4 Control registers but only some static patterns are written into these registers. Once the communication between the HUB and other modules within shelf is established, a test pattern generator will be replaced by real TTC component. Next development steps assumes to add (gradually) the remaining receivers within the shelf.



Figure 12. The HUB and ROD setup to test the Readout_Ctrl and Combined_TTC/Data link.

word 0		word 1		word 2		word 3	
bit	0XBC = K28.5	bit_		bit		bit	
0	0	0	L1ID(0)	0	control channel	0	Link_reset 0
1	0	1	L1ID	1	control channel	1	Link_reset 1
2	1	2	L1ID	2	control channel	2	Link_reset 2
3	1	3	L1ID	3	control channel	3	Link_reset 3
4	1	4	L1ID	4	control channel	4	ROD Busy
5	1	5	L1ID	5	control channel	5	Link Enable
6	0	6	L1ID	6	control channel	6	rod 0 channel up
7	1	7	L1ID	7	control channel	7	rod 1 channel up
8	version(0)	8	L1ID	8	control channel	8	0 (ROD reserved)
9	version(1)	9	L1ID	9	control channel	9	0 (ROD reserved)
10	version(2)	10	L1ID	10	control channel	10	0 (ROD reserved)
11	version(3)	11	L1ID	11	control channel	11	0 (ROD reserved)
12	reset	12	L1ID	12	control channel	12	0 (ROD reserved)
13	reset	13	L1ID	13	control channel	13	0 (ROD reserved)
14	reset	14	L1ID	14	control channel	14	0 (ROD reserved)
15	reset	15	L1ID	15	control channel	15	0 (ROD reserved)
16	L1A	16	L1ID	16	control channel	16	0 (ROD reserved)
17	BCR	17	L1ID	17	control channel	17	0 (ROD reserved)
18	ECR	18	L1ID	18	control channel	18	0 (ROD reserved)
19	Privileged Readout	19	L1ID	19	control channel	19	0 (ROD reserved)
20	0 (TTC reserved)	20	L1ID	20	control channel	20	shelf#
21	0 (TTC reserved)	21	L1ID	21	control channel	21	shelf#
22	0 (TTC reserved)	22	L1ID	22	control channel	22	shelf#
23	0 (TTC reserved)	23	L1ID(23)	23	control channel	23	CRC (9-bit)
24	0 (TTC reserved)	24	ECRID(0)	24	control channel	24	CRC (9-bit)
25	0 (TTC reserved)	25	ECRID(1)	25	control channel	25	CRC (9-bit)
26	0 (TTC reserved)	26	ECRID(2)	26	control channel	26	CRC (9-bit)
27	0 (TTC reserved)	27	ECRID(3)	27	control channel	27	CRC (9-bit)
28	0 (TTC reserved)	28	ECRID(4)	28	control channel	28	CRC (9-bit)
29	0 (TTC reserved)	29	ECRID(5)	29	control channel	29	CRC (9-bit)
30	0 (TTC reserved)	30	ECRID(6)	30	control channel	30	CRC (9-bit)
31	0 (TTC reserved)	31	ECRID(7)	31	control channel	31	CRC (9-bit)

Table 2. Combined TTC/Data bit definitions.

3.0 Readout Control (Readout_Ctrl)

The HUB module is obliged to receive the Readout Control (Readout_CTRL) information from the ROD via serial link named Readout_CTRL [2]. The HUB module is the only one module within the shelf which gets the Readout Control data from the ROD. That information is used by the Hub, also fanned out to the rest of the system. The main purpose is to provide resets to all of the data links (Aurora) between the Fex's and the ROD plus HUB module.

3.1 Readout Control - Physical Implementation

The Readout_Ctrl link on the HUB module is implemented with the use of MGT Transceiver GTH), control and diagnostic logic. The Readout_Ctrl link is designed to operate at 6.4 Gbps. When 8b/10b overhead is accounted for, the effective rate is reduced to $6.4 \times 0.8 = 5.12$ Gbps. In order to to control message transmission within a single LHC clock period, the lengh of the message is limited tp 128 bts. The HUB Readout Control FW features one receiver (RX). In order to debug the design, the standard Xilinx diagnostic components are being used to monitor the data flow (as for example like the ILA and VIO). The physical layer is configured with the use of GT wizard.

The physical implementation of the Readout_CTRL links assumes that there are Control Registers on the Tx ROD side, and Shadow Registers on the Rx HUB side. The transmitter side generates the 128 bit message from 4 Control registers: Word_0, Word_1, Word_2, and Word_3. The transmitter side logic is in charge to write control information into these registers for transmission to the modules within the shelf. These registers are continuously transmitted to the HUB which receives the data into a duplicate set of 4 registers referred to as Shadow Registers. Anything written into a Control Register at the transmitter side will appear in the corresponding Shadow register at the receiving side within the following LHC clock. The least significant byte of Word_0 is reserved for the 8b10b Comma character K28.5.



(1/(6.4 Gbps *0.8)) * 128 bits = 2.5 ns = 1/40 MHz

Figure 13. Control and Shadow Register

3.2 Control Bit definition

The bits within the Readout Control words are primarily defined to provide initialization functions for all of the FEX data links.

Comma Character

Bits 7 to 0 of Word_0 contain the Comma character that maintains alignment of the 4 shadow registers with their corresponding Control registers. The chosen character is K28.5 = 0xBC.

Version

The 4-bit value contains the version number of this overall bit assignment.

ROD_BUSY

When active, this signal indicates that the ROD cannot currently accept further data from Fex sources. This signal is fanned-out to the shelf FEX's by the Hub via the Combined_TTC link.

Global_Link_Reset

This single bit is used to reset all of the data (Aurora) links within the shelf. The primary use is in the first initialisation after power-up. The ROD can hold this reset active for an indefinite amount of time. On the trailing edge (deactivation), the eFex's should provide additional timing control for the GTReset and Reset signals on the Aurora interface. This signal is fanned-out to the shelf FEX's by the Hub via the Combined_TTC link.

Channel Up

This reports on whether each slot's Aurora Channel is 'UP' or 'Down'. The information is rebroadcast to each FEX slot in the so that the Aurora transmitter knows if the receiver side of the channel is up. If a channel goes down, the ROD attempt to reset both Rx and Tx ends of the link.

Slot_N_link_reset_M

These signals allow the ROD to reset individual links providing data to it. The active time is indeterminate, and may be very short. On the trailing edge (deactivation), the eFex's should provide additional timing control for the GTReset and Reset signals on the Aurora interface.

Slots 3-8 have 4 resets each. This is to cover the case of jFex where each of 4 processors has its own data link to the ROD. It is expected that eFex boards in these slots will only use the M=0 reset.

Slots 9-14 only have a single reset. These slots will only be populated by eFEX boards which only require one reset.

CRC (9-bit)

CRC is included to provide additional robustness on this link. Erroneous resets could cause loss of data. Choice of polynomial is from <u>https://users.ece.cmu.edu/~koopman/crc/index.html.</u> The chosen polynomial is 0x17d in Koopman format of 0x2fb in explicit+1 format.

3.3 Readout Control - FW development strategy

The HUB Readout Control FW features one receiver (RX). In order to debug the design, the standard Xilinx diagnostic components are being used to monitor the data flow (as for example like the ILA and VIO). The physical layer is configured with the use of GT wizard.

word 0		word 1		word 2		word 3	
bit	OXBC = K28.5	bit		bit		bit	
0	0	0	slot 3 link reset 0	0	0	0	0
1	0	1	slot 3 link reset 1	1	0	1	0
2	1	2	slot 3 link reset 2	2	0	2	0
3	1	3	slot 3 link reset 3	3	0	3	0
4	1	4	slot 4 link reset 0	4	0	4	0
5	1	5	slot 4 link reset 1	5	0	5	0
6	0	6	slot 4 link reset 2	6	0	6	0
7	1	7	slot 4 link reset 3	7	0	7	0
8	version 0	8	slot 5 link reset 0	8	0	8	0
9	version 1	9	slot 5 link reset 1	9	0	9	0
10	version 2	10	slot 5 link reset 2	10	0	10	0
11	version 3	11	slot 5 link reset 3	11	0	11	0
12	0	12	slot 6 link reset 0	12	0	12	0
13	0	13	slot 6 link reset 1	13	0	13	0
14	ROD_BUSY (to all slots)	14	slot 6 link reset 2	14	0	14	0
15	Aurora_Init (all links)	15	slot 6 link reset 3	15	0	15	0
16	slot3 channel up	16	slot 7 link reset 0	16	0	16	0
17	slot4 channel up	17	slot 7 link reset 1	17	0	17	0
18	slot5 channel up	18	slot 7 link reset 2	18	0	18	0
19	slot6 channel up	19	slot 7 link reset 3	19	0	19	0
20	slot7 channel up	20	slot 8 link reset 0	20	0	20	0
21	slot8 channel up	21	slot 8 link reset 1	21	0	21	0
22	slot9 channel up	22	slot 8 link reset 2	22	0	22	0
23	slot10 channel up	23	slot 8 link reset 3	23	0	23	CRC (9-bit)
24	slot11 channel up	24	slot 9 link reset	24	0	24	CRC (9-bit)
25	slot12 channel up	25	slot 10 link reset	25	0	25	CRC (9-bit)
26	slot13 channel up	26	slot 11 link reset	26	0	26	CRC (9-bit)
27	slot14 channel up	27	slot 12 link reset	27	0	27	CRC (9-bit)
28	0	28	slot 13 link reset	28	0	28	CRC (9-bit)
29	0	29	slot 14 link reset	29	0	29	CRC (9-bit)
30	0	30	0	30	0	30	CRC (9-bit)
31	0	31	0	31	0	31	CRC (9-bit)

Table 3: Readout_Ctrl bit assignments.

4.0 Specification for the HUB Safe Configuration

Introduction

During the regular operation, the HUB firmware is obliged to control the group of signals which are wired to the FPGA. These signals are handled on the HUB FPGA by the Safe Configuration component. This piece of firmware is in charge to properly receive the signals and control them by the ILA and VIO component. The HUB Safe Configuration needs to present in any type of HUB configuration.

Logic Analyzer (ILA)

The customizable Integrated Logic Analyzer (ILA) IP core is a logic analyzer core that can be used to monitor the internal signals of a design [4]. The ILA core includes many advanced features of modern logic analyzers, including Boolean trigger equations, and edge transition triggers. Because the ILA core is synchronous to the design being monitored, all design clock constraints that are applied to your design are also applied to the components inside the ILA core.

Virtual Input/Output (VIO)

The LogiCORETM IP Virtual Input/Output (VIO) core is a customizable core that can both monitor and drive internal FPGA signals in real time [5]. The number and width of the input and output ports are customizable in size to interface with the FPGA design. Because the VIO core is synchronous to the design being monitored and/or driven, all design clock constraints that are applied to your design are also applied to the components inside the VIO core. Run time interaction with this core requires the use of the Vivado® logic analyzer feature.

SYSMON

Optionally, the HUB configuration can include the SYSMON (SLR0 and SLR1): Each super logic region: SLR0 and SLR1 has one system monitor to provide for monitoring supply voltages within the SLR. The I2C DRP and JTAG DRP access is limited to the master SLR only (SYSMONE1_X0Y0 for devices with two SLRs) [7]. The system monitors can be placed in the bottom SLR0 (SYSMONE1_X0Y0) and then consecutively in the upper SLR increasing Y locations (SYSMONE1_X0Y1). Monitoring across SLR boundaries is not possible. Temperature, VCCINT, VCCAUX, VCCBRAM measurements are specific to an individual SLR. For the UltraScale FPGAs SYSMONE1, the System Management Wizard provides I2C functionality to the slave SLRs using the DRP port and additional logic. The SYSMON has numerous operating modes that are user-defined by writing to the control registers, which can be accessed through DRP, JTAG or I2C. It is also possible to

initialize these register contents when the SYSMON is instantiated in a design using the block attributes.

No	Signal name	Location and I/O Standards	Components	Direction
0	Logic_Clk_320.64_Mhz_to_FPGA_Dir Logic_Clk_320.64_MHz_to_FPGA_Cmp	PACKAGE_PIN K22 PACKAGE_PIN J22 IOSTANDARD LVDS DIFF_TERM_ADV TERM_100 DQS_BIAS TRUE_EQUALIZATION EQ_LEVEL0	IBUFGDS	IN
1	Logic_Clk_40.08_Mhz_to_FPGA_Dir Logic_Clk_40.08_Mhz_to_FPGA_Cmp	PACKAGE_PIN J24 PACKAGE_PIN H24 IOSTANDARD LVDS DIFF_TERM_ADV TERM_100 DQS_BIAS TRUE EQUALIZATION EQ_LEVEL0	IBUFGDS	IN
2	Ref_4008_Mhz_from_Other_Hub_Dir Ref_4008_Mhz_from_Other_Hub_Cmp	PACKAGE_PIN H23 PACKAGE_PIN G23 IOSTANDARD LVDS DIFF_TERM_ADV TERM_100 DQS_BIAS TRUE EQUALIZATION EQ_LEVEL0	IBUFGDS	IN

3	Ref_4008_MHz_from_FPGA_to_Rec_Dir Ref_4008_MHz_from_FPGA_to_Rec_Cmp	PACKAGE_PIN AV31 PACKAGE_PIN AW31 IOSTANDARD LVDS	Controling only, an VIO component added. A default value set to 0.	OUT
4	PLL_4008_Mhz_Lock_Detect_to_FPGA	PACKAGE_PIN B27 IOSTANDARD LVCMOS18	Monitoring only, an ILA component added.	IN
5	PLL_32064_MHz_Lock_Detect_to_FPGA	PACKAGE_PIN B26 IOSTANDARD LVCMOS18	Monitoring only, an ILA component added.	IN
6	Select_Input_Second_40_Fanout	PACKAGE_PIN A26 IOSTANDARD LVCMOS18	Controling only, an VIO component added. A default value set to 0.	OUT
7	FPGA_SW_A_ATC_LOOP_DET FPGA_SW_B_ATC_LOOP_DET FPGA_SW_C_ATC_LOOP_DET	PACKAGE_PIN AV13 PACKAGE_PIN AT14 PACKAGE_PIN AV15 IOSTANDARD LVCMOS33 SLEW SLOW DRIVE 4	Controling only, an VIO component added. A default value set to 0.	OUT
8	FPGA_SW_A_LOOP_DETECTED FPGA_SW_B_LOOP_DETECTED FPGA_SW_C_LOOP_DETECTED	PACKAGE_PIN AY15 PACKAGE_PIN AU13 PACKAGE_PIN AV16 IOSTANDARD LVCMOS33	Monitoring only, an ILA component added.	IN
9	FPGA_SW_A_MDC FPGA_SW_B_MDC FPGA_SW_C_MDC	PACKAGE_PIN AW13 PACKAGE_PIN AT16 PACKAGE_PIN AY13 IOSTANDARD LVCMOS33 SLEW SLOW DRIVE 4	Controling only, an VIO component added. A default value set to 0.	OUT
10	FPGA_SW_A_MDIO	PACKAGE_PIN AW15	Monitoring only, an ILA	IN

-			1	
	FPGA_SW_B_MDIO FPGA_SW_C_MDIO	PACKAGE_PIN AU16 PACKAGE_PIN AY14 IOSTANDARD LVCMOS33 PULLUP TRUE	component added.	
11	ISO_SLOT_HW_ADRS_0 ISO_SLOT_HW_ADRS_1 ISO_SLOT_HW_ADRS_2 ISO_SLOT_HW_ADRS_3 ISO_SLOT_HW_ADRS_4 ISO_SLOT_HW_ADRS_5 ISO_SLOT_HW_ADRS_6 ISO_SLOT_HW_ADRS_7	PACKAGE_PIN AT12 PACKAGE_PIN AT11 PACKAGE_PIN AU12 PACKAGE_PIN AU11 PACKAGE_PIN AV11 PACKAGE_PIN AW12 PACKAGE_PIN AW11 PACKAGE_PIN AW11 IOSTANDARD LVCMOS33	Monitoring only, an ILA component added.	IN
12	SHELF_ADRS_0_TO_FPGA SHELF_ADRS_1_TO_FPGA SHELF_ADRS_2_TO_FPGA SHELF_ADRS_3_TO_FPGA SHELF_ADRS_4_TO_FPGA SHELF_ADRS_5_TO_FPGA SHELF_ADRS_6_TO_FPGA SHELF_ADRS_7_TO_FPGA	PACKAGE_PIN BB15 PACKAGE_PIN BB14 PACKAGE_PIN BA14 PACKAGE_PIN BB13 PACKAGE_PIN BB12 PACKAGE_PIN BB11 PACKAGE_PIN BA11 PACKAGE_PIN BA11 IOSTANDARD LVCMOS33	Monitoring only, an ILA component added.	IN
13	OVERALL_ADRS_0_TO_RES_NET OVERALL_ADRS_1_TO_RES_NET OVERALL_ADRS_2_TO_RES_NET OVERALL_ADRS_3_TO_RES_NET OVERALL_ADRS_4_TO_RES_NET OVERALL_ADRS_5_TO_RES_NET OVERALL_ADRS_6_TO_RES_NET OVERALL_ADRS_7_TO_RES_NET	PACKAGE_PIN BF25 PACKAGE_PIN BE25 PACKAGE_PIN BF26 PACKAGE_PIN BE27 PACKAGE_PIN BF27 PACKAGE_PIN BE28 PACKAGE_PIN BE29 PACKAGE_PIN BE30 IOSTANDARD LVCMOS18 SLEW SLOW DRIVE 4	Controling only, an VIO component added. A default value set to 0.	OUT
14	HUB_I2C_TO_FPGA_SCL_0 HUB_I2C_TO_FPGA_SDA_0 Hub_I2C_TO_FPGA_SCL_1 Hub_I2C_TO_FPGA_SDA_1	PACKAGE_PIN BE16 PACKAGE_PIN BF16 PACKAGE_PIN BA29 PACKAGE_PIN BB29 IOSTANDARD LVCMOS18	No monitoring.	IN
15	I2C_Buf_1501_ENABLE I2C_Buf_1502_ENABLE I2C_Buf_1503_ENABLE	PACKAGE_PIN BA16 PACKAGE_PIN BA15 PACKAGE_PIN BB16 IOSTANDARD LVCMOS33 SLEW SLOW DRIVE 4	Controling only, an VIO component added. A default value set to 1 for I2C_Buf_1501_ENABLE, others set to 0.	OUT

,		1		
16	Recvr_MiniPOD_INTR_B Trans_MiniPOD_INTR_B	PACKAGE_PIN AR15 PACKAGE_PIN AN16 IOSTANDARD LVCMOS33	Monitoring only, an ILA component added.	IN
17	Recvr_MiniPOD_RESET_B Trans_MiniPOD_RESET_B	PACKAGE_PIN AR14 PACKAGE_PIN AP13 IOSTANDARD LVCMOS33 SLEW SLOW DRIVE 4	Controling only, an VIO component added. A default value set to 1.	OUT
18	Recvr_MiniPOD_SCL Trans_MiniPOD_SCL	PACKAGE_PIN AR12 PACKAGE_PIN AN15 IOSTANDARD LVCMOS33 SLEW SLOW DRIVE 4	Controling only, an VIO component added. A default value set to 0.	OUT
19	Recvr_MiniPOD_SDA Trans_MiniPOD_SDA	PACKAGE_PIN AR13 PACKAGE_PIN AP15 IOSTANDARD LVCMOS33	Monitoring only, an ILA component added.	IN
20	ACCESS_SIGNAL_1_FROM_FPGA ACCESS_SIGNAL_2_FROM_FPGA	PACKAGE_PIN AT30 PACKAGE_PIN AT31 IOSTANDARD LVCMOS18 SLEW SLOW DRIVE 4	Controling only, an VIO component added. A default value set to 0.	OUT
21	HUB_FPGA_LED50_DRV HUB_FPGA_LED51_DRV HUB_FPGA_LED52_DRV	PACKAGE_PIN BF29 PACKAGE_PIN BF30 PACKAGE_PIN BF31 IOSTANDARD LVCMOS18 SLEW SLOW DRIVE 4	Controling only, an VIO component added. A default value set to 0.	OUT
22	Hubs_SMB_Alert_B	PACKAGE_PIN AP16 IOSTANDARD LVCMOS33	Monitoring only, an ILA component added.	IN
23	ALL_HUB_POWER_GOOD_TO_FPGA	PACKAGE_PIN AM16 IOSTANDARD LVCMOS33	Monitoring only, an ILA component added.	IN
24	MGT_FO_EQU_ENB_GRP_1 MGT_FO_EQU_ENB_GRP_2 MGT_FO_EQU_ENB_GRP_3 MGT_FO_EQU_ENB_GRP_4 MGT_FO_EQU_ENB_GRP_5	PACKAGE_PIN C25 PACKAGE_PIN A25 PACKAGE_PIN B25 PACKAGE_PIN A24 PACKAGE_PIN C24	Controling only, an VIO component added. A default value set to 0.	OUT

	MGT_FO_EQU_ENB_GRP_6 MGT_FO_EQU_ENB_GRP_7 MGT_FO_EQU_ENB_GRP_8 MGT_FO_EQU_ENB_GRP_9 MGT_FO_EQU_ENB_GRP_10 MGT_FO_EQU_ENB_GRP_11 MGT_FO_EQU_ENB_GRP_12 MGT_FO_EQU_ENB_GRP_13	PACKAGE_PIN B22 PACKAGE_PIN D20 PACKAGE_PIN C20 PACKAGE_PIN A23 PACKAGE_PIN A21 PACKAGE_PIN A20 PACKAGE_PIN A19 PACKAGE_PIN A18 IOSTANDARD LVCMOS18		
		SLEW SLOW DRIVE 8		
25	TBD_SPARE_LINK_0_Dir TBD_SPARE_LINK_0_Cmp TBD_SPARE_LINK_1_Dir TBD_SPARE_LINK_1_Cmp TBD_SPARE_LINK_2_Dir TBD_SPARE_LINK_2_Cmp TBD_SPARE_LINK_3_Dir TBD_SPARE_LINK_3_Cmp	PACKAGE_PIN AV26 PACKAGE_PIN AW26 PACKAGE_PIN AT27 PACKAGE_PIN AU27 PACKAGE_PIN AY27 PACKAGE_PIN AY28 PACKAGE_PIN AT29 PACKAGE_PIN AU29 IOSTANDARD LVCMOS18SLEW SLOW	Controling only, an VIO component added. A default value set to 0.	OUT
		DRIVE 4		
26	ROD_PRESENT_B_TO_FPGA	PACKAGE_PIN AW27 IOSTANDARD LVCMOS18	Monitoring only, an ILA component added.	IN
27	ROD_Power_Control_2_FPGA ROD_Power_Control_3_FPGA ROD_Power_Control_4_FPGA	PACKAGE_PIN AW28 PACKAGE_PIN AV30 PACKAGE_PIN AV29	Monitoring only, an ILA component added.	IN
		IOSTANDARD LVCMOS18		
28	ROD_Power_Enable ROD_Power_Enable_B	PACKAGE_PIN AR17 PACKAGE_PIN AP17 IOSTANDARD LVCMOS33 SLEW SLOW DRIVE 4	Controling only, an VIO component added. A default value: ROD_Power_Enable set 0 ROD_Power_Enable_B set 1	OUT
29	FPGA_RODs_SMBALERT_B	PACKAGE_PIN BB28 IOSTANDARD LVCMOS18	Monitoring only, an ILA component added.	IN
30	Phys_U21_TXD0 Phys_U21_TXD1 Phys_U21_TXD2 Phys_U21_TXD3 Phys_U21_TX_EN Phys_U21_GTX_CLK Phys_U22_TXD0 Phys_U22_TXD1 Phys_U22_TXD2 Phys_U22_TXD3 Phys_U22_TX_EN	PACKAGE_PIN BA36 PACKAGE_PIN AY35 PACKAGE_PIN BB36 PACKAGE_PIN BA35 PACKAGE_PIN BB34 PACKAGE_PIN BA34 PACKAGE_PIN AR36 PACKAGE_PIN AT36 PACKAGE_PIN AR35 PACKAGE_PIN AT35 PACKAGE_PIN AU34	Controling only, an VIO component added. A default value set to 0.	OUT

	Phys_U22_GTX_CLK	PACKAGE_PIN AT34		
		IOSTANDARD LVCMOS18		
31	Phys_U21_CLK125_LED_MODE Phys_U21_RXD0_MODE0 Phys_U21_RXD1_MODE1 Phys_U21_RXD2_MODE2 Phys_U21_RXD3_MODE3 Phys_U21_RX_DV_CLK125_EN Phys_U21_RX_CLK_PHYAD2 Phys_U22_CLK125_LED_MODE Phys_U22_RXD0_MODE0 Phys_U22_RXD1_MODE1 Phys_U22_RXD2_MODE2 Phys_U22_RXD3_MODE3 Phys_U22_RX_DV_CLK125_EN Phys_U22_RX_CLK_PHYAD2	PACKAGE_PIN AU33 PACKAGE_PIN BC31 PACKAGE_PIN BA32 PACKAGE_PIN BB33 PACKAGE_PIN AY33 PACKAGE_PIN AY33 PACKAGE_PIN AV33 PACKAGE_PIN AV33 PACKAGE_PIN AV35 PACKAGE_PIN AV35 PACKAGE_PIN AV36 PACKAGE_PIN AV32 PACKAGE_PIN AW32 PACKAGE_PIN AW33 IOSTANDARD LVCMOS18	Monitoring only, an ILA component added.	IN
32	Spare_OSC_TO_FPGA_Dir Spare_OSC_TO_FPGA_Cmp	PACKAGE PIN AU28 PACKAGE PIN AV28 IOSTANDARD LVDS DQS_BIAS TRUE	IBUFGDS	IN

Table 4: "Hub Safe Configuration" signal list, including the location and I/O standard, components
which are being used to receive these signals and directionality.

5. Readout Data (Aurora 8b10b)

Figure 14 shows the Hub's distribution of readout data in the context of the cards in the ATCA shelf. The readout data comes from the Node slots and from the FPGA on each Hub module. All of this data flows to both the ROD and to the FPGA on each Hub. The arrangement shown in Figure 14 supports 2 independent streams of readout data. That is, the readout stream processed by the ROD and Hub FPGA on Hub-1 can be independent of the readout stream flowing into Hub-2.

The FEX-HUB receives 6 serial streams of Readout Data from each FEX Module using the Aurora8b10b protocol. Currently the link rate is set to 6.4Gbps. The Aurora implementation for the HUB FPGA will be conducted with the use of Aurora 8b10b IP core (Wizard). The Xilinx Aurora 8B/10B core supports the AMBA® protocol AXI4-Stream user interface [3]. The core implements the Aurora 8B/10B protocol using the high-speed serial transceivers. The Aurora 8B/10B core (Figure 15) is a scalable, lightweight, link-layer protocol for high-speed serial communication. The protocol is open and can be implemented using Xilinx FPGA technology. The protocol is typically used in applications requiring simple, low-cost, high-rate, data channels and is used to transfer data between devices using one or many transceivers. The Aurora8b10b IP core supports: 7 series GTX/GTH, UltraScale GTH, UltraScale+ GTH, GTP transceivers. Officially the Aurora8b10b IP core does not support the GTY transceivers. The HUB FPGA is equipped with two type of MGT transceivers (GTY and GTH) and therefore, two different implementation method will be used. The GTY requires non-standard implementation. That method assumes that the Aurora IP core (wizard) will generate the Aurora 8b10b protocol files, while the GT wizard will be used to configure the physical layer. In the final step, the merging process is foreseen to provide the Aurora8b10b for GTY transceivers.

The Xilinx statement is that there is not really technical reason behind Aurora 8b10b not supporting GTY transceivers. But since GTY transceivers are meant to be targeted for higher line rate, they recommend to use the Aurora 64b66b for better throughput.

Finally, we figured out the method to implement the Aurora8b10b protocol in GTY transceivers. The FW design is based on the Xilinx example. And the method is presented below.

Aurora8b10b IP core configures two parts: link layer (protocol) and physical layer (GT part). In real, the Aurora8b10b core uses the GT wizard to configure the physical layer. Basically, two IP cores are being used to provide full setup. Thus, in order to implement the Aurora8b10b in GTY, the GT wizard needs to be run "manually" to configure the GTY transceivers.



Hub-Module Readout Data Distribution

Figure 14. Illustration of FEX-Hub distribution of high-speed readout data signals.



Figure 15. The Aurora 8b10b overview (Xilinx)

Aurora 8b10b implementation in GTY – recipe (1)

Standard Aurora8b10b IP core (GTH) configures the Physical and Link Layer:

Aurora 8B10B (11.0)	A
Documentation 📄 IP Location 🧔 Switch to Defaults	
Documentation Defaults Show disabled ports +GTO_DRP +CORE_CONTROL +GT_SERIAL_RXUSER_DATA_M_AXI_RX -TX_system_reset CORE_STATUS	Component Name aurora_36106_0 Core Options Shared Logic Physical Layer Lane Width (Bytes) 2 • • Line Rate (Gbps) 5 • • • (0.5 - 6.6) Column Used nght • • Lanes 1 • • Starting GT Quad Quad X0Y3 • Starting GT Quad Quad X0Y3 • Starting GT Lane X0Y12 • [Selected GT X0Y12] GT Refdk Selection MCTREFELKD of Quad X0Y3 • GT Refdk Selection MCTREFELKD of Quad X0Y3 • ButT dk (Metz) 125 • • (6.25 - 200) LinkLayer Dataflow Mode RX-only Simplex • Interface Framing • Flow Control None •
-init_ck_in tx_out_ck -user_ck sys_reset_out -sync_ck -gt_refck1	Scrambler/Descrambler Uttle Endan Support Error Detection CRC Debug and Control Wixado Lab Tools
	Additional transceiver control and status ports

Aurora 8b10b implementation in GTY – recipe (2)

Once the Aurora8b10b core is generated, open IP example Design



Aurora 8b10b implementation in GTY – recipe (3)

Open GT wizard to configure the GT part of the protocol:

mentation 🏀 Presets 🚞 IP Location 🧔 Switch to Defau	lts						
IP Symbol Physical Resources	Component Name gtwizard_	ultrascale_0					
	Basic Physical Reso	ources Optional Features Structural	Options				
t-dick on channels to enable and edit	System						
	Transceiver configur	Trapportium configuration propert CTV_Aurora 98108*					
OuadX0Y2	Transceiver turn						
	transceiver type	dii		•			
CPL	Transmitter			Receiver			
X0Y7	Line rate (Gb/s)	3.125		Line rate (Gb/s)	3.125		
	PLL type	CPLL	Ŧ	PLL type	CPLL	•	
XUY5	QPLL Fractional-	-N options	۲	QPLL Fractiona	I-N options		۲
	Requested refere clock (MHz)	ence 156.25 Calc		Requested refe dock (MHz)	156.25	Calc	
	Resulting fractiona of QPLL feedback div	al part ider /(2^24) = 0		Resulting fraction of QPLL feedback di	uid part vider /(2^24) = 0	8	
	Actual Reference	125	Ŧ	Actual Reference	125	•	
XOYS	Clock (MHz)	0D/10D	-	Clock (MHZ)	90/100		
	Encoding	16	-	Decoding	16	-	
X0Y4	User data width	10	•	User data width	10	-	
QuadX0Y1	Internal data width	20	•	Internal data width	20		
	Buffer	Enable (1)	-	Buffer	Enable (1)		
	TXOUTCLK source	TXOUTCLKPMA	•	RXOUTCLK source	RXOUTCLKPMA	•	~
	Advanced		۲	Advanced			۲
	and	Custom 👻		Insertion loss at I	Vyquist (dB)	14	
	emphasis mode			Equalization mode		Auto 💌	
				When Auto is spe by the Wizard de loss at Nyquist. R the appropriate e	cified, the equalization m pends on the value speci lefer to Xilinx UG576/UG qualization mode for you	ode implemented fied for insertion 578 to determine r system	
				Link coupling		AC 🔻	
Aurora 8b10b implementation in GTY – recipe (4)

Once the GT files are generated, replaced them with the files generated by Aurora8b10b IP core:



Aurora 8b10b implementation in GTY – recipe (5)

Visual inspection needed (design, xdc file, system clock, mgt referene clock):



Aurora 8b10b implementation in GTY – test (1)

ZYNQ Board (GTX) and VCU108 Xilinx Dev Board setup



Image 1: This is the setup which is used to test the Aurora8b10b protocol in GTY transceivers. The ZynQ module (from PANDA experiment) was used to transmit the readout data (Aurora8b10b with GTX transceivers), and the Xilinx module dev board as the receiver (Aurora8b10b with GTY transceivers).

Aurora 8b10b implementation in GTY – test (2)

ZYNQ Board (GTX) and VCU108 Xilinx Dev Board: Links are up and stable

In order to control the Aurora8b10b protocol the VIO components is being used.

Hardware Manager - localhost/xilinx_tcf/Xilinx/	0000183b3a1c01							
Hardware	_ □ ♂ ×	(🔊 hw	_ila_1 x 🕥 hw_vios x				
역 🔀 🖨 📳 🕨 🕨 🖿			hw	<u>vio 1</u>				
Name	Status		Q	Name	Value	Activity	Direction	VIO
	Connected Closed Open N/A Programmed Idle OK	Dashboard Options		Le lane_up_j_i_vio Le tx_channel_up_r_vio Le tx_lock j j vio Le chipscope1.i_vio/probe_out2[2:0] Le gtreset_vio_j Le sysreset_vio_j	(H) 0 • (B) 0 • (B) 0 •		Input Input Output Output Output	hw_vio_1 hw_vio_1 hw_vio_1 hw_vio_1 hw_vio_1 hw_vio_1
<	>							

Hardware Manager - localhost/xilinx_tcf/Digiler	t/210308956281							
Hardware	_ 🗆 🖻 ×		🔊 hw_	ila_1 X 🔊 hw_vios X				
옥 🛣 🖨 🛃 📭 🕨 🕨 🔳			hw	<u>vio 1</u>				
Name	Status		0	Name	Value	Activity	Direction	VIO
🖃 📲 localhost (2)	Connected	0	2	:∿a lane up i i vio	•		Input	hw vio 1
🚊 🖉 🤌 xilinx_tcf/Digilent/210308956281 (1)	Open	tio		····∿ rx_channel_up_r_vio	ŏ		Input	hw_vio_1
Ė·· ♦ xcvu095_0 (3)	Programmed	8	-	™	0		Input	hw_vio_1
📴 SysMon (System Monitor)		ard	 +	🗄 墙 chipscope1.i_vio/probe_out2[2:0]	[H] 0 🔻		Output	hw_vio_1
🔤 hw_ila_1 (chipscope1.i_ila)	🔵 Idle	<u>۾</u>		… ∿a atreset vio i	[B] 0 🔻		Output	hw vio 1

Aurora 8b10b implementation in GTY – test (3)

ZYNQ Board (GTX) and VCU108 Xilinx Dev Board: TX and RX data check OK.

Hardware Manager - localhost/xilinx_tcf/Xilinx/	0000183b3a1c0	1										
Hardware	×	6	🔊 hw	_ila_1 × 🔊 hw_vios ×								
오 🔀 🖨 🖪 📭 🕨 🕨 🔳			Wa	veform - <u>hw_ila_1</u>								
Name	Status		¥	ILA Status:Idle		0						
□· localhost (2) ···· 0 × xilinx_tcf/Digilent/210308956281 (0)	Connected Closed	ions	Ŧ	Name	Value	o		2	1	4		6
	Open N/A	ard Opt	=		1883	1883	0c41	0620	8310	(c188)	60c4	b062
	Programmed	Dashbo		lane_up_ii_r	1							
I hw_ila_1 (chipscope1.i_ila) - 發 hw_vio_1 (chipscope1.i_vio)	OK OK											
٢		>										

Hardware Manager - localhost/xilinx_tcf/Digilen	t/210308956281											
Hardware	_ □ ℓ ×	6	hw_	_ila_1 × 🕲 hw_vios ×								
오 🔀 😂 🛃 📭 🕨 🕨 🔳			Wav	veform - <u>hw_ila_1</u>								
Name	Status		۲	ILA Status:Idle		0						
🖃 📲 localhost (2)	Connected	2		Name	Value							
☐	Open	Ę	•		- Circle	0		2		4		6
⊡· xcvu095_0 (3)	Programmed	Ö	-		1883	(1883)	0c41	0620)	8310	c188)	60c4	b06
📲 🔯 SysMon (System Monitor)		ard		∎-₩ err. count i[0:7]	00	\models						
🛛 📴 hw_ila_1 (chipscope1.i_ila)	🔵 Idle	<u>امْ</u>	9			<u> </u>						
🔤 hw_vio_1 (chipscope 1.i_vio)	OK	ast		🖟 link_reset_ila	0							
🦾 🍘 xilinx_tcf/Xilinx/0000183b3a1c01 (0)	Closed			14 rx_resetdone_i	1							
				₩ frame_err_i	0							
				🕼 soft_err_i	0							
			-	₩ rx_hard_err_i	0							
			0+	₩ tx_lock_i_ila	1							

5.1 Aurora Line Mapping

The Aurora Line Mapping, 4 lines options (option A: 1,2,3,4 and option B: 3,4,5,6) and 6-lane mapping, respectively.

	1,2	2,3,4 opt	tion		3,4,5,6	option			6-Lane		
	lane	quad	rx MGT	lane	quad	rx MGT		lane	quad	rx MGT	+
Slot 3	1	126	1	1	126	1		1	126	10/091	ŕ
	2	126	0	2	126	0		2	126	0	
	3	125	3	3	125	3		3	125	3	
	4	125	2	4	125	2		4	125	2	
	5	125	1	5	125	1		5	125	1	
	6	125	0	6	125	0		6	125	0	
slot 4	1	124	3	1	124	3		1	124	3	
	2	124	2	2	124	2		2	124	2	
	3	128	1	3	128	1		3	128	1	
	4	120	3		120	3			120	3	
	6	127	2	6	127	2		6	127	2	
			-			-				-	
slot 5	1	127	1	1	127	1		1	127	1	
	2	127	0	2	127	0		2	127	0	
	3	126	3	3	126	3		3	126	3	
	4	126	2	4	126	2		4	126	2	
	5	130	1	5	130	1		5	130	1	
	6	130	0	6	130	0		6	130	0	
slot 6	1	129	3	1	129	3	_	1	129	3	
	2	129	2	2	129	2		2	129	2	
	3	129	1	3	129	1		3	129	1	
	4	129	0	4	129	0		4	129	0	
	5	128	3	5	128	3		5	128	3	
	ь	128	2	6	128	2		6	128	2	
slot 7	1	132	3	1	192	2		1	182	3	
3007	2	132	2	2	132	2		2	132	2	
	3	132	1	3	132	1		3	132	1	
	4	132	0	4	132	0		4	132	ō	
	5	131	1	5	131	1		5	131	1	
	6	131	0	6	131	0		6	131	o	
slot 8	1	130	3	1	130	3		1	130	3	
5101 0	2	130	2	2	130	2		2	130	2	
	3	130	1	3	130	1		3	130	1	
	4	130	0	4	130	0		4	130	0	
	5	131	3	5	131	3		5	131	3	
	6	131	2	6	131	2		6	131	2	
slot 9	1	133	1	1	133	1		1	133	1	
	2	133	0	2	133	0		2	133	0	
	3	232	0	3	232	0		3	232	0	
	4	232	1	4	232	1		4	232	1	
	5	232	2	5	232	2		5	232	2	
	0	232	3	0	232	5			2.52		
slot 10	1	233	0	1	233	0		1	233	0	
	2	233	1	2	233	1		2	233	1	
	3	233	2	0	235	2		4	233	3	
	5	229	2	5	229	2		5	229	2	
	6	229	3	6	229	3		6	229	3	
slot 11	1	230	0	1	230	0		1	230	0	
	2	230	1	2	230	1		2	230	2	
	4	230	3	4	230	3		4	230	3	
	5	231	0	5	231	0		5	231	0	
	6	231	1	6	231	1		6	231	1	
									225	_	
slot 12	1	227	2	1	227	2		1	227	2	
	2	227	3	2	227	3		2	227	3	
	4	228	1	4	228	1		4	228	1	
	5	228	2	5	228	2		5	228	2	
	6	228	3	6	228	3		6	228	3	
-1-0.42		225			220			_	220	-	
siot 13	1	229	0	1	229	0		1	229	1	
				1 A A A A A A A A A A A A A A A A A A A							

5.2 Proposed Aurora and Combined_TTC/Data initialization sequence

This is the proposed Aurora and Combined_TTC/Data initialization scheme. This is preliminary model, it will be discussed, and it might be changed (this scheme is proposed by Ed Flaherty).

- Hub configuration
 Hub Asserts PWR_CON1 to power-up the ROD
 ROD asserts PWR_CON2 to indicate Power Good
 After configuration, the ROD asserts PWR_CON3 indicating ready to run
 ROD Power-Up timer is started
- 4) Hub Combined TTC/Data GT reset pulse is asserted
- 5) Hub Combined TTC/Data GT reset pulse is de-asserted
- 6) Aurora reset propagates from Readout_CTRL to COMBINED_TTC
- 7) ROD Power-Up timer is de-asserted.
- 7) All Aurora channel reset timers in Hub, ROD and FEX's start simultaneously
- 8) All Aurora channel reset timers in Hub, ROD and FEX's de-assert simultaneously
- 9) All Aurora receivers should assert Channel-UP simultaneously

Hub ROD PWR-UP handshake signals PWR_CON1: power-on from Hub PWR_CON2: power-good from ROD PWR_CON3: rod ready to run PWR_CON4: reserved – ether direction

Figure 16. Sequence of events for the Aurora and Combined TTC/Data initialization.

-Hub driven signals -ROD driven signa	ls -FEX driven Signals
Hub Config done 1	
ROD PWR-UP (PWR_CON1) 2	
ROD PWR-GOOD (PWR_CON2) 3	
ROD Ready (PWR_CON3) 4	
ROD PWR-ON Timer	7
ROD Readout_CTRL link reset 4	7
Hub combined_ttc GTreset pulse 4 Cttc GT reset timer	
Hub Combined_TTClink reset	7
ROD Aurora channel reset (reset + GT reset)	7 Aurora channel reset timer
Hub Aurora <u>channel reset (reset + GT reset)</u>	7 Aurora channel reset timer 8
FEX Aurora channel reset (reset + GT reset)	7 Aurora channel reset timer 8
FEX Aurora Channel_UP	Flaherty 9

- ROD Power-UP timer
 - Pulse Width not very critical just "long"
 - Currently 32-bit countdown starting from X"3FFFFFFF" @125MHz clock = 8.6 seconds
- Aurora Channel Reset Timer: used at all Rx & Tx interfaces
 - 4 outputs: Tx_reset, Tx_GTReset, Rx_reset, Rx_GTReset
 - Timing critical for all 4 outputs
 - All aurora interfaces should start at the same time (based upon combined_TTC link reset)
 - currently running from 125MHz clock
 - May be better to change to 40MHz clock in future
- Hub GTReset Pulse
 - Pulse Width not very critical, but must be significantly shorter than the ROD Power-UP pulse
 1 sec?

Figure 17. Illustration of Hub/ROD/FEX Aurora initialization sequence (Ed Flahery's Proposal).

6.0 IBERT test.

In order to test the specific MGT channels the IBERT FW was provided for the FTM, ROD and HUB modules. The table describes the list of tests and results.

No	Test description	Result
1	4 MiniPOD Receiver MGT channels	No errors
2	6 lanes of MGT data from all 12 of the FEX slot	No errors
3	Combined_TTC/Data to the 12 FEX slots	No errors
4	Combined_TTC/Data to the ROD on This HUB	No errors
5	Combined_TTC/Data Data to the Other HUB	No errors
6	Combined_TTC/Data Data that was sent out by the Other HUB	No errors
7	Readout Control Data that was sent out by the ROD on This HUB	No errors
8	HUB sends out two lanes of Readout data to the Other HUB	No errors
9	HUB receives two lanes of Readout data from the Other HUB	No errors
10	FPGA on This HUB sends one lane of its readout data to the ROD on This HUB	No errors

6.1 Combined_TTC/ Data to the FEX 3; test@6.4Gbps:

								Vivado 2017	.2					-	•
ile <u>E</u> dit <u>T</u> ools <u>W</u> in	dow La <u>v</u> out	⊻iew <u>H</u> elp	Q+ Quick	Access											
≥ ★ ★ ≥ m	X¢ x	11 😿	Dashboard 👻											Serial I/O Ana	lyzer -
ARDWARE MANAGER - Io	calhost/xilinx_tcf/X	ilinx/000016c	47de501												?
Ecl Console Message	s Serial I/O Li	inks × S	erial I/O Sca	ns											2 _ 6 6
Q ≍ ≑ +															
Name	TX F	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject Error	TX Reset
😑 Ungrouped Links (0)												,			
 Link Group 0 (16) 							Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	1	Inject	Reset
🗞 Link 0	MGT_X0Y0/TX M	IGT_X0Y0/RX	No Link	6.007	3.567	5.938E-1	Reset	PRBS 7-bit ↓	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	1	Inject	Reset
% Link 1	MGT_X0Y1/TX M	IGT_X0Y1/RX	6.413 Gbps	7.383	0E0	1.355E-11	Reset] PRBS 7-bit ↓	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV(1100) 🗸	1	Inject	Reset
💫 Link 2	MGT_X0Y2/TX M	IGT_X0Y2/RX	No Link	6.007	3.567	5.938E-1	Reset	PRBS 7-bit ↓	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	\checkmark	Inject	Reset
💫 Link 3	MGT_X0Y3/TX M	IGT_X0Y3/RX	No Link	6.007	3.567	5.938E-1	Reset] PRBS 7-bit ∨	PRBS 7-bit 🗸	1.67 dB (00111) ∨	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	\checkmark	Inject	Reset
🗞 Link 4	MGT_X0Y4/TX M	IGT_X0Y4/RX	No Link	6.007	3.567	5.938E-1	Reset	PRBS 7-bit ↓	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	1	Inject	Reset
💫 Link 5	MGT_X0Y5/TX M	IGT_X0Y5/RX	No Link	6.007	3.567	5.938E-1	Reset	PRBS 7-bit ↓	PRBS 7-bit 🗸	1.67 dB (00111) ↓	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	Image: A start of the start	Inject	Reset
💫 Link 6	MGT_X0Y6/TX M	IGT_X0Y6/RX	No Link	6.007	3.567	5.938E-1	Reset	PRBS 7-bit ↓	PRBS 7-bit ↓	1.67 dB (00111) ↓	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	~	Inject	Reset
S Link 7	MGT_X0Y7/TX M	IGT_X0Y7/RX	No Link	6.007	3.567	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) ↓	0.68 dB (00011) v	1018 mV (1100) ↓	✓	Inject	Reset
S Link 8	MGT_X0Y8/TX M	IGT_X0Y8/RX	No Link	6.008	3.567	5.938E-1	Reset	PRBS 7-bit V	PRBS 7-bit V	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV (1100) V	 Image: A start of the start of	Inject	Reset
b Link 9	MGT_X0Y9/TX M	IGT_X0Y9/RX	No Link	6.008	3.567	5.938E-1	Reset	PRBS 7-DIT V	PRBS 7-bit V	1.67 dB (00111) ~	0.68 dB (00011) V	1018 mV (1100) ~	~	Inject	Reset
Link 10	MGT_X0Y10/TX M	IGT_X0Y10/RX	No Link	6.008	3.307	5.9366-1	Reset	PRBS 7-bit V	PRBS 7-bit	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV(1100) V	v	Inject	Reset
O LINK 11 9. Link 12	MGT_X011171X M	CT YOVI DRY	No Link	6.009	2.567	5.0305.1	Reset	PRBS 7-bit v	PRBS 7-bit	1.67 dB (00111) v	0.68 dB (00011) v	1018 mV(1100) v	v	Inject	Reset
b Link 12	MGT_X0112/TX M	IGT_X0112/RX	No Link	6.008	3.567	5.938E-1	Reset	PRBS 7-bit	PRBS 7-bit v	1.67 dB (00111) v	0.68 dB (00011) v	1018 mV (1100) v	•	Inject	Reset
a Link 14	MGT_X0Y14/TX M	IGT XOVI 4/BX	No Link	6.008	3.567	5.938E-1	Reset	PBBS 7-bit v	PBBS 7-bit v	1.67 dB (00111) v	0.68 dB (00011) v	1018 mV (1100) v	Z	Inject	Reset
& Link 15	MGT_X0V15/TX M	IGT YOV15/BY	No Link	6.008	3.567	5.938E-1	Reset	PRBS 7-bit	PBBS 7-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (1100) v		Inject	Reset

6.2 Combined_TTC/Data to the FEX 4; test@6.4Gbps:

								Vivado 2017.	2					-	
File Edit Tools Win	dow Lavout	View Helr	Q- Ouick	Access											
	X¢X		Dashboard 🗸										=	Serial I/O Analy	zer
ARDWARE MANAGER - loo	calhost/xilinx to	f/Xilinx/000016	c47de501												?
Tcl Console Message	s Serial I/O	Links × S	erial I/O Sca	ns										?	- 6 6
Q <u>∓</u> ≑ +															
Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject Error	TX Rese
Ungrouped Links (0)										(7
~							Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) ↓	0.68 dB (00011) 🗸	1018 mV (1100) V	✓	Inject	Rese
B Link 0	MGT_X0Y0/TX	MGT_X0Y0/RX	No Link	1.74E13	1.033	5.938E-1	Reset	PRBS 7-bit v	PRBS 7-bit v	1.6/ dB (00111) ↓	0.68 dB (00011) v	1018 mV (1100) ~	Image: A state of the state	Inject	Rese
% Link I	MGT_X0Y1/TX	MGT_X0Y1/RX	6.413 Gbps	1.15/E13	0E0	8.641E-14	Reset	PRBS 7-bit v	PRBS /-bit v	1.67 dB (00111) ~	0.68 dB (00011) V	1018 mV (1100) ~	 Image: A start of the start of	Inject	Rese
EINK 2 Link 2	MGT_X0Y2/TX	MGT_X0Y2/RX	NO LINK	1.74E13	1.033	5.938E-1	Reset	PRBS /-DIT V	PRBS /-DIT V	1.0\ GR (00111) ~	0.68 dB (00011) ~	T018 mA (1100) ~	×	Inject	Rese
EINK 3 0. Link 4	MGT_X0Y3/TX	MGI_X0Y3/RX	NO LINK	1.74E13	1.033	5.938E-1	Reset	PRBS 7-bit V	PRBS 7-bit V	1.67 dB (00111) V	0.68 dB (00011) V	1018 mv (1100) V	 Image: A start of the start of	Inject	Rese
Unk 4 0 Link 5	MGT_X0Y4/TX	MGT_X0Y4/RX	No Link	1.74E13	1.033	5.938E-1	Reset	PRBS 7-DIT V	PRBS /-DIT V	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV (1100) V	×	inject] Rese
b LINK 5	MGT_X0Y5/TX	MGT_X0Y5/RX	NO LINK	1.74E13	1.033	5.938E-1	Reset	PRBS 7-bit V	PRBS 7-Dit V	1.67 dB (00111) V	0.68 dB (00011) 🗸	1018 mV (1100) V	~	Inject	Rese
LINK 0	MGT_X0Y6/TX	MGT_X0Y6/RX	No Link	1.74E13	1.033	5.9386-1	Reset	PRBS 7-bit V	PRBS 7-Dit V	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV (1100) V	~	Inject	Rese
b) LINK 7	MGT_X0Y//TX	MGT_X0Y7/RX	No Link	1.74E13	1.033	5.938E-1	Reset	PRBS 7-bit V	PRBS 7-DIL V	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV (1100) V	~	Inject	Rese
LINK 0	MGT_X0Y8/TX	MGT_X0Y8/RX	No Link	1.74E13	1.033	5.9386-1	Reset	PRBS 7-bit V	PRBS 7-Dil V	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV (1100) V	~	Inject	Rese
b) LINK 9	MGT_X0Y9/1X	MGT_X0Y9/RX	NO LINK	1.74E13	1.033	5.938E-1	Reset	PRBS 7-bit V	PRBS 7-DIL V	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV (1100) V	~	Inject	Rese
Eink 10	MGT_X0Y10/D	MGT_X0Y10/R	No Link	1.74613	1.035	5.937E-1	Reset	PRBS 7-bit V	PRBS 7-Dil V	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV(1100) V	~	Inject	Rese
 Link 12 Link 12 	MGT_X0Y11777	MGT_X0111/R	No Link	1.74613	1.033	5.0205.1	Reset	PRBS 7-bit ++	PRBS 7-bit w	1.67 dB (00111) v	0.68 dB (00011) v	1018 mV(1100) v	v	Inject	Bese
0 LINK 12 9 Link 12	MGT_X0Y12/17	MGT_X0Y12/R	No Link	1.74613	1.035	5.9366-1	Reset	PRBS 7-bit V	PRBS 7-DiL V	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV(1100) V	~	Inject	Rese
 Link 13 Link 14 	MGT_X0Y13/17	MGT_X0T13/R	No Link	1.74612	1.033	5.0205.1	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111) ++	0.68 dB (00011) v	1018 mV(1100) v	v	Inject	Rese
 Link 14 Link 15 	MGT_X0Y14/17	MGT_X0114/R	No Link	1.74613	1.035	5.03051	Reset	PRBS 7-bit v	PRBS 7-bit v	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV(1100) V	~	Inject	Rese
(

6.3 Combined_TTC/Data to the FEX 5; test@6.4Gbps:

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N RX Status BES Errors BER BERT Feest X Patterm TX Pre-Cursor TX Diff Swing DFE Enabled Inject Error TA Reset P Unit 0 MGT_X0Y07X MGT_X0	Q ₹ ≑ +																
Androge Olso North With Weight Cases Personal Market Long and Cases Androge Olso Composition Composition </td <td></td> <td>TX F</td> <td>RX</td> <td>Status</td> <td>Bits</td> <td>Errors</td> <td>BER</td> <td>BERT Reset</td> <td>TX Pattern</td> <td>RX Pattern</td> <td>TX Pre-Cursor</td> <td>TX Post-Cursor</td> <td>TX Diff Swing</td> <td>DFE Enabled</td> <td>Inject Error</td> <td>TX Reset</td> <td>RX</td>		TX F	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject Error	TX Reset	RX
http://widit.com/file.com/	ngrouped Links (0)																
Unk 0 MoT_WOYNK MG_WOYNK MG_WARK 288 1.715 5.938E1 Reast PR85 7bt v PR65 7bt v 167 d8 (0011) v 0.68 d8 (0001) v 1018 mV (1100) v Ø Inject Reset Inject Reset Inject Reset PR65 7bt v 167 d8 (0011) v 0.68 d8 (0001) v 1018 mV (1100) v Ø Inject Reset PR65 7bt v 167 d8 (0011) v 0.68 d8 (0001) v 1018 mV (1100) v Ø Inject Reset PR65 7bt v 167 d8 (0011) v 0.68 d8 (0001) v 1018 mV (1100) v Ø Inject Reset PR65 7bt v 167 d8 (0011) v 0.68 d8 (0001) v 1018 mV (1100) v Ø Inject Reset PR65 7bt v 167 d8 (0011) v 0.68 d8 (0001) v 1018 mV (1100 v Ø Inject Reset PR65 7bt v 167 d8 (0011) v 0.68 d8 (0001) v 1018 mV (1100 v Ø Ø Inject Reset PR65 7bt v 167 d8 (0011) v 0.68 d8 (0001) v 1018 mV (1100 v Ø Ø Inject Reset PR65 7bt v 167 d8 (0011) v 0.68 d8 (0001) v 1018 mV (1100 v Ø Ø Inject Reset PR65 7bt v 167 d8 (0011) v 0.68 d8 (0001) v<	nk Group 0 (16)							Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	1	Inject	Reset	1
Unk1 MGT_2001/RK 643 36ps 243.44 Reset PRES 7-bit PRES 7-bit PRES 7-bit 1.67 dB (00011) 0.68 dB (00011) 0.18 mV(1100 V V Inject Reset Reset PRES 7-bit 1.67 dB (00011) 0.68 dB (00011) 10.8 mV(1100 V V Inject Reset Inject Reset Inject Reset Inject Reset Inject R	, Link 0	MGT_X0Y0/TX M	GT_X0Y0/RX	No Link	2.889	1.715	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	✓	Inject	Reset	1 E
Unk 2 MGT_X0/27/X MGT_X0/27/X <	Link 1	MGT_X0Y1/TX M	GT_X0Y1/RX	6.413 Gbps	2.903	0E0	3.445E-14	Reset	PRBS 7-bit ∨	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸		Inject	Reset	ÎΕ
Unk 3 MGT_X0YTX_MGT_	Link 2	MGT_X0Y2/TX M	GT_X0Y2/RX	No Link	2.889	1.715	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	\checkmark	Inject	Reset	10
Unk 4 MGT_WOYATK	Link 3	MGT_X0Y3/TX M	GT_X0Y3/RX	No Link	2.889	1.715	5.938E-1	Reset	PRBS 7-bit ↓	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB(00011) 🗸	1018 mV (1100) 🗸	\checkmark	Inject	Reset	
Unk 5 MGT_X0Y6/TX MGT_X0Y6/TX MGT_X0Y6/TX MGT_X0Y6/TX MGT_X0Y6/TX MGT_X0Y7/TX	Link 4	MGT_X0Y4/TX M	GT_X0Y4/RX	No Link	2.889	1.715	5.938E-1	Reset	PRBS 7-bit ↓	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	1	Inject	Reset	
Unk 6 MGT_WOYG/TX	Link 5	MGT_X0Y5/TX M	GT_X0Y5/RX	No Link	2.889	1.715	5.938E-1	Reset	PRBS 7-bit ↓	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	\checkmark	Inject	Reset	
Unk 7 MGT_X007/7K MGT_X001/7K	Link 6	MGT_X0Y6/TX M	GT_X0Y6/RX	No Link	2.889	1.715	5.938E-1	Reset	PRBS 7-bit ∨	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV(1100) 🗸	\checkmark	Inject	Reset	
Unk 8 MGT_X009TX, MGT_X0047K, No Unk 2.889 1.715 5.938E-1 Reset PRBS 7-bit > 1.67 db (00111) > 0.69 db (00011) 1018 mV(1100) ✓ Imject Reset Reset Imject Reset	Link 7	MGT_X0Y7/TX M	GT_X0Y7/RX	No Link	2.889	1.715	5.938E-1	Reset	PRBS 7-bit ↓	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB(00011) 🗸	1018 mV(1100) 🗸	\checkmark	Inject	Reset	
Unk 9 MGT_X009/TK_MGT_X0010/RK_N0 Link 2.889 1.715 5.938E-1 Reset PRBS 7-bit v PRBS 7-bit v 1.67 dB (00111) v 0.68 dB (00011) v 1018 mV(1100) v V Inject Reset Inject	Link 8	MGT_X0Y8/TX M	GT_X0Y8/RX	No Link	2.889	1.715	5.938E-1	Reset	PRBS 7-bit ∨	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV(1100) 🗸	\checkmark	Inject	Reset	
Unk 10 MGT_X0Y10/TK_MGT_	Link 9	MGT_X0Y9/TX M	GT_X0Y9/RX	No Link	2.889	1.715	5.938E-1	Reset	PRBS 7-bit ↓	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	\checkmark	Inject	Reset	
Unk 11 MGT_X0Y1_JTXX MGT_X0Y1_JXX NG Unk 2.889 1.715 5.9386-1 Reset PRBS 7-bit v 1.67 dB (00111) v 0.68 dB (00011) v 1018 mV(1100) v V Inject Reset	Link 10	MGT_X0Y10/TX M	GT_X0Y10/RX	No Link	2.889	1.715	5.938E-1	Reset	PRBS 7-bit ∨	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV(1100) 🗸	\checkmark	Inject	Reset	
Unk 12 MGT_X0012/TX_MGT_X0012/TX_M0 Unk 2.889 1.715 5.938E1 Reset PRBS 7-bit v 1.67 dB (00111) v 0.68 dB (00011) v 1018 mV(1100) v V Inject Reset	, Link 11	MGT_X0Y11/TX M	GT_X0Y11/RX	No Link	2.889	1.715	5.938E-1	Reset	PRBS 7-bit ↓	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	\checkmark	Inject	Reset	
Umk 13 MGT_X0013/TK MGT_X0013/TK MG Umk 2.889 1.715 5.938E-1 Reset PR85 7-bit ∨ PR95 7-bit ∨ 1.67 dB (00111) ∨ 0.68 dB (00011) ∨ 1018 mV (1100) ∨ ⊘ Inject Reset Umk 14 MGT_X014/TK MGT_X0115/TK	Link 12	MGT_X0Y12/TX M	GT_X0Y12/RX	No Link	2.889	1.715	5.938E-1	Reset	PRBS 7-bit ↓	PRBS 7-bit 🗸	1.67 dB (00111) ↓	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	\checkmark	Inject	Reset	
Link 14 MGT_X0Y14/RX_MGT_X0Y14/RX_M0 Link 2.889 1.715 5.938E-1 Reset PRBS 7-bit v PABS 7-bit v 0.68 dB (00011) v 1018 mV (1100) v Z Inject Reset Inject Inject Reset Inject Inject Reset Inject	, Link 13	MGT_X0Y13/TX M	GT_X0Y13/RX	No Link	2.889	1.715	5.938E-1	Reset	PRBS 7-bit ↓	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	\checkmark	Inject	Reset	
Unk 15 MGT_X0Y15/TX MGT_X0Y15	Link 14	MGT_X0Y14/TX M	GT_X0Y14/RX	No Link	2.889	1.715	5.938E-1	Reset	PRBS 7-bit ↓	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB(00011) 🗸	1018 mV (1100) 🗸	\checkmark	Inject	Reset	
	Link 15	MGT_X0Y15/TX M	GT_X0Y15/RX	No Link	2.889	1.715	5.938E-1	Reset	PRBS 7-bit ∨	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	\checkmark	Inject	Reset	

6.4 Combined_TTC/Data to the FEX 6; test@6.4Gbps:

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6.5 Combined_TTC/Data to the FEX 7; test@6.4Gbps:

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Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject Error	TX Res
😑 Ungrouped Links (0)													,	
🚳 Link Group 0 (16)							Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	✓	Inject	Rese
💫 Link 0	MGT_X0Y0/TX	MGT_X0Y0/RX	No Link	2.63E13	1.561	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	\checkmark	Inject	Rese
% Link 1	MGT_X0Y1/TX N	MGT_X0Y1/RX	6.413 Gbps	1.984	0E0	5.041E-14	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	✓	Inject	Rese
🗞 Link 2	MGT_X0Y2/TX	MGT_X0Y2/RX	No Link	2.63E13	1.561	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	\checkmark	Inject	Rese
💫 Link 3	MGT_X0Y3/TX	MGT_X0Y3/RX	No Link	2.63E13	1.561	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	\checkmark	Inject	Rese
💫 Link 4	MGT_X0Y4/TX	MGT_X0Y4/RX	No Link	2.63E13	1.561	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) ∨	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	\checkmark	Inject	Rese
💫 Link 5	MGT_X0Y5/TX	4GT_X0Y5/RX	No Link	2.63E13	1.561	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) ↓	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	~	Inject	Rese
b Link 6	MGT_X0Y6/TX	4GT_X0Y6/RX	No Link	2.63E13	1.561	5.938E-1	Reset	PRBS 7-bit V	PRBS 7-bit V	1.67 dB (00111) ↓	0.68 dB (00011) V	1018 mV (1100) ↓	✓	Inject	Rese
S LINK 7	MGT_X0Y7/TX	IGT_X0Y7/RX	No Link	2.63E13	1.561	5.938E-1	Reset	PRBS 7-bit V	PRBS 7-bit V	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV (1100) V	✓	Inject	Rese
LINK 8	MGT_X0Y8/TX	MGT_X0Y8/RX	No Link	2.63513	1.562	5.938E-1	Reset	PRBS 7-bit V	PRBS 7-Dit V	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV(1100) V	✓	Inject	Rese
UIIK 9 Q. Link 10	MGT_X019/1X	MCT_X0Y3.0/DX	No Link	2.03E13	1.562	5.03001	Reset	PRBS 7-bit V	PRBS 7-bit V	1.67 dB (00111) v	0.68 dB (00011) v	1018 mV(1100) V	V	Inject	Rese
Link 10	MGT_X0Y10/1X /	MGT_X0Y10/PO	No Link	2.03E13	1.562	5.9386-1	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV (1100) V	✓	Inject	Rese
& Link 12	MGT_X0Y12/TX I	MGT_X0V12/RV	No Link	2.63E13	1.562	5.938E-1	Reset	PBBS 7-bit v	PBBS 7-bit w	1.67 dB (00111) v	0.68 dB (00011) v	1018 mV (1100) v	×	Inject	Rese
a Link 13	MGT_X0Y13/TX1	MGT_X0Y13/R)	No Link	2.63E13	1.562	5.938E-1	Reset	PRBS 7-bit v	PRBS 7-bit v	1.67 dB (00111) v	0.68 dB (00011) v	1018 mV (1100) v	 Z 	Inject	Bese
Link 14	MGT X0Y14/TX I	MGT X0Y14/RV	No Link	2.63E13	1.562	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) ~	0.68 dB (00011) v	1018 mV (1100) v	<	Inject	Rese
a Link 15	MGT X0Y15/TX I	MGT X0Y15/RV	No Link	2.63E13	1.562	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸		Inject	Rese
δ ₀ Link 10 δ ₀ Link 11 δ ₀ Link 12 δ ₀ Link 13 δ ₀ Link 14 δ ₀ Link 15	MGT_X0Y10/TX 1 MGT_X0Y11/TX 1 MGT_X0Y12/TX 1 MGT_X0Y13/TX 1 MGT_X0Y13/TX 1 MGT_X0Y15/TX 1	4GT_X0Y10/RX 4GT_X0Y11/RX 4GT_X0Y12/RX 4GT_X0Y13/RX 4GT_X0Y14/RX 4GT_X0Y15/RX	: No Link : No Link : No Link (No Link (No Link (No Link	2.63E13 2.63E13 2.63E13 2.63E13 2.63E13 2.63E13	1.562 1.562 1.562 1.562 1.562	5.938E-1 5.938E-1 5.938E-1 5.938E-1 5.938E-1 5.938E-1	Reset Reset Reset Reset Reset Reset	PRBS 7-bit v PRBS 7-bit v PRBS 7-bit v PRBS 7-bit v PRBS 7-bit v PRBS 7-bit v	PRBS 7-bit v PRBS 7-bit v PRBS 7-bit v PRBS 7-bit v PRBS 7-bit v PRBS 7-bit v	1.67 dB (00111) ↓ 1.67 dB (00111) ↓ 1.67 dB (00111) ↓ 1.67 dB (00111) ↓ 1.67 dB (00111) ↓	0.68 dB (00011) ~ 0.68 dB (00011) ~ 0.68 dB (00011) ~ 0.68 dB (00011) ~ 0.68 dB (00011) ~	1018 mV (1100) ~ 1018 mV (1100) ~ 1018 mV (1100) ~ 1018 mV (1100) ~ 1018 mV (1100) ~	V V V V	Inject Inject Inject Inject Inject Inject	

6.6 Combined_TTC/Data to the FEX 8; test@6.4Gbps:

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© Ungrouped Links (0) Index Peaker PRES 7-bit Ind de (00011) 0.66 de (000011) 108 mV (1100) ✓ Index Peaker © Unk Group MGT_XOVD/X	Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject Error	TX Rese
	😑 Ungrouped Links (0)												,			
Builton 0 MGT_20V0/TX_MGT_20V0/T	~							Reset	PRBS 7-bit 🖌	PRBS 7-bit 🖌	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	✓	Inject	Reset
9. Unk1 MGT_2007LW_MGT_2007LW_G432000F 2.4E13 060 4.1064.4 Readt PR857-bit v PR857-bit v 1.67 d6 000111 v 1.08 mV(1100) v V Inject Reset 6. Unk3 MGT_2007LW_MGT_2007LW_MGT_2007LW_M0 LUK 2.38E13 1.418 5.5936-1 Reset PR857-bit v PR857-bit v 1.67 d6 000111 v 0.68 d6 000011 v 1018 mV(1100) v V Inject Reset 6. Unk4 MGT_2007LW_MGT_2004RW_N0 LUK 2.38E13 1.418 5.5936-1 Reset PR857-bit v PR857-bit v 1.67 d6 000111 v 0.68 d8 000011 v 1018 mV(1100) v V Inject Reset 6. Unk6 MGT_2007LW_MGT_2007LW_N0 LUK 2.38E13 1.418 5.5936-1 Reset PR857-bit v PR857-bit v 1.67 d8 000111 v 1018 mV(1100) v V Inject Reset 6. Unk6 MGT_2007LW_MGT_2007RW_N0 LUK 2.38E13 1.418 5.5936-1 Reset PR857-bit v PR857-bit v 1.67 d8 000111 v 1018 mV(1100) v V Inject Reset 6. Unk10 MGT_2007LW_MGT_2007RW_MGT_2007RW_N0 LUK 2.38E13 1.418 5.5936-1 Reset <td< td=""><td>🗞 Link 0</td><td>MGT_X0Y0/TX</td><td>MGT_X0Y0/RX</td><td>No Link</td><td>2.388E13</td><td>1.418</td><td>5.938E-1</td><td>Reset</td><td>PRBS 7-bit 🗸</td><td>PRBS 7-bit 🗸</td><td>1.67 dB (00111) 🗸</td><td>0.68 dB (00011) 🗸</td><td>1018 mV(1100) 🗸</td><td>\checkmark</td><td>Inject</td><td>Reset</td></td<>	🗞 Link 0	MGT_X0Y0/TX	MGT_X0Y0/RX	No Link	2.388E13	1.418	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV(1100) 🗸	\checkmark	Inject	Reset
ibit N2 MCT_20072M: MGT_20072M: NoLLMR 2.38813 1.418 5.59861 Reset PR857-bit v 1.67 d6 (00111) v 0.68 d6 (00011) v 1018 mV(1100) v Ø Impect Reset ibit N4 MGT_20074M: MGT_20074M: NoLLMR 2.38813 1.418 5.59861 Reset PR857-bit v PR857-bit v 1.67 d6 (00111) v 0.68 d6 (00011) v 1018 mV(1100) v Ø Impect Reset ib Link 6 MGT_20074M: MGT_20054M: NoLMK 2.38813 1.418 5.59861 Reset PR857-bit v PR857-bit v 1.67 d6 (00111) v 0.68 d8 (00011) v 1018 mV(1100) v Ø Impect Reset ib Link 6 MGT_20074M: MGT_20054M: NoLMK 2.38811 1.418 5.59861 Reset PR857-bit v PR857-bit v 1.67 d8 (00111) v 0.68 d8 (00011) v 1018 mV(1100) v Ø Impect Reset ib Link 6 MGT_20074M: MGT_20074M: NoLMK 2.38811 1.418 5.59861 Reset PR857-bit v PR857-bit v 1.67 d8 (00111) v 0.68 d8 (00011) v 1018 mV(1100) v Ø Impect Reset ib Link 19 MGT_20074M: MGT_20074M: NoLMK 2.388113	🗞 Link 1	MGT_X0Y1/TX	MGT_X0Y1/RX	6.413 Gbps	2.4E13	0E0	4.168E-14	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV(1100) 🗸	\checkmark	Inject	Reset
Buiki 3 MMT_XOVATX	🗞 Link 2	MGT_X0Y2/TX	MGT_X0Y2/RX	No Link	2.388E13	1.418	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV(1100) 🗸	\checkmark	Inject	Reset
6. Unk4 MGT_X0Y4/TX MGT_X0Y4/TX No Link 2.38613 1.41.8. 5.9381-1 Reset PR85 7.bit > N67 d6 (00111) 0.68 d6 (00011) 1.018 mV(1100) Ø Inject Reset 6. Unk5 MGT_X0Y6/TX MGT_X0Y6/TX No Link 2.38613 1.41.8. 5.9381-1 Reset PR85 7.bit > 1.67 d6 (00111) 0.68 d6 (00011) 1.018 mV(1100) Ø Ø Inject Reset 6. Unk6 MGT_X0Y6/TX MGT_X0Y7/TX MGT_X01L 2.38613 1.41.8. 5.9381-1 Reset PR85 7.bit > 1.67 d6 (00111) 0.68 d6 (00011) 1.018 mV(1100) Ø Ø Inject Reset 6. Unk7 MGT_X0Y7/TX MGT_X0Y7/TX NG Link 2.38613 1.41.8. 5.9381-1 Reset PR85 7.bit > 1.67 d6 (00111) 0.68 d6 (00011) 1.018 mV(1100) Ø Ø Inject Reset 6. Unk9 MGT_X0Y1/TX MGT_X0Y1/TX NGT_N NG Link 2.38813 1.41.8. 5.9381-1 Reset PR85 7.bit PR85 7.bit 1.67 d6 (00111) 0.68 d6 (00011) 1.018 mV(1100) Ø Ø Inject Reset 6. Unk12 MGT_X0Y1/TX MGT_X0Y1/TX MGT_X0Y1/TX MGT_X0Y1/TX NG Link 2.38813 <td< td=""><td>💫 Link 3</td><td>MGT_X0Y3/TX</td><td>MGT_X0Y3/RX</td><td>No Link</td><td>2.388E13</td><td>1.418</td><td>5.938E-1</td><td>Reset</td><td>PRBS 7-bit 🗸</td><td>PRBS 7-bit 🗸</td><td>1.67 dB (00111) 🗸</td><td>0.68 dB (00011) 🗸</td><td>1018 mV (1100) 🗸</td><td>\checkmark</td><td>Inject</td><td>Reset</td></td<>	💫 Link 3	MGT_X0Y3/TX	MGT_X0Y3/RX	No Link	2.388E13	1.418	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	\checkmark	Inject	Reset
Bail Link 5 MGT_XXY5/TX Moluke 2.38813 1.41e 5.3986-1 Reset PR85 7-bit PR85 7-bit< PR85 7	💫 Link 4	MGT_X0Y4/TX	MGT_X0Y4/RX	No Link	2.388E13	1.418	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) ↓	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	\checkmark	Inject	Reset
ib. Unk 6 MGT_X0V9RTX_MGT_X0V12MX 2.388E13 1.418 5.938E-1 Reset PR85 7-bit > 16.7 dB (00111) 0.68 dB (00011) 1018 mV (1100) Ø Inject Reset ib. Unk 7 MGT_X0V9RTX_MGT_X0V12MX 2.388E13 1.418 5.938E-1 Reset PR85 7-bit > 16.7 dB (00111) 0.68 dB (00011) 1018 mV (1100) Ø Inject Reset ib. Unk 8 MGT_X0V9RTX_MGT_X0V12MX 2.388E13 1.418 5.938E-1 Reset PR85 7-bit > 16.7 dB (00111) 0.68 dB (00011) 1018 mV (1100) Ø Inject Reset ib. Unk 10 MGT_X0V9RTX_MGT_X0V12MX N0 Link 2.388E13 1.418 5.938E-1 Reset PR85 7-bit > 1.67 dB (00111) 0.68 dB (00011) 1018 mV (1100) Ø Inject Reset ib. Link 10 MGT_X0V12MX N0 Link 2.388E13 1.418 5.938E-1 Reset PR85 7-bit 1.67 dB (00111) 0.68 dB (00011) 1018 mV (1100) Ø Inject Reset ib. Link 10 MGT_X0V12MX MGT_X0V12MX N0 Link 2.388E13 1.418 5.938E-1 Reset PR85 7-bit 1.67 dB (00111) 0.68 d	💫 Link 5	MGT_X0Y5/TX	MGT_X0Y5/RX	No Link	2.388E13	1.418	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) ↓	0.68 dB (00011) 🗸	1018 mV (1100) v	\checkmark	Inject	Reset
ab. Link 7 MKT_X0Y/7X, MGT_X0Y/RX, MGL LMK 2.388E13 1.418. 5.938E1 Reset PRBS 7-bit V. 167 dB (00111) 0.68 dB (00011) VIII 000 V Inject Reset ab. Link 8 MGT_X0Y9/RX, MGT_X0Y9/RX, No Link 2.388E13 1.418. 5.938E1 Reset PRBS 7-bit V. 167 dB (00111) 0.68 dB (00011) VIII 000 V Inject Reset ab. Link 10 MGT_X0Y1/RX, MGT_X012/RX, No Link 2.388E13 1.418. 5.938E1 Reset PRBS 7-bit V. 167 dB (00111) 0.68 dB (00011) VIII 000 V Inject Reset ab. Link 11 MGT_X0Y1/RX, MGT_X012/RX, No Link 2.388E13 1.418. 5.938E1 Reset PRBS 7-bit V. 167 dB (00111) 0.68 dB (00011) VIII NWT (1000) V Inject Reset ab. Link 11 MGT_X0Y1/RX, MGT_X012/RX, No Link 2.388E13 1.418. 5.938E1 Reset PRBS 7-bit V. 167 dB (00111) 0.68 dB (00011) VIII NWT (1000) V Inject Reset ab. Link 12 MGT_X0Y12/RX, No Link 2.388E13 1.418. 5.938E1 Reset PRBS 7-bit V. 167 dB (00111) <	🗞 Link 6	MGT_X0Y6/TX	MGT_X0Y6/RX	No Link	2.388E13	1.418	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) ↓	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	1	Inject	Reset
b. Link B MST_XOVERX MoT_XOVERX No Link 2.388E13 1.418. 5.938E1 Reset PH85 7bit V 1.67 dB (00111) 0.68 dB (00011) 0.101 mV (1100) V Inject Reset 6. Link 10 MGT_XOVERX No Link 2.388E13 1.418. 5.938E1 Reset PH85 7bit PH85 7bit 1.67 dB (00111) 0.68 dB (00011) 1018 mV (1100) V Inject Reset 6. Link 11 MGT_XOV127X MGT_XOV12RK No Link 2.388E13 1.418. 5.938E1 Reset PH85 7bit 1.67 dB (00111) 0.68 dB (00011) 1018 mV (1100) V Inject Reset 6. Link 12 MGT_XOV127X MGT_XOV12RK No Link 2.388E13 1.418. 5.938E1 Reset PR85 7bit<	S Link 7	MGT_X0Y7/TX	MGT_X0Y7/RX	No Link	2.388E13	1.418	5.938E-1	Reset	PRBS 7-bit v	PRBS 7-bit v	1.67 dB (00111) ↓	0.68 dB (00011) v	1018 mV (1100) ↓	✓	Inject	Reset
ab. Link 10 MGT_XOV9/XX_MGT_XOV9/XX_MGT_XOV Z388E13 1.418. 5.938E1 Reset PH85 7bit V 1.67 dB (00111) 0.168 dB (00011) 0.1018 mV (1100) Ø Inject Reset 8. Link 10 MGT_XOV1/XX MGT_XOV1/RX, No Link 2.388E13 1.418. 5.938E1 Reset PH85 7bit PH85 7bit 1.67 dB (00111) 0.68 dB (00011) 1018 mV (1100) Ø Inject Reset 8. Link 11 MGT_XOV1/XX MGT_XOV1/RX, No Link 2.388E13 1.418. 5.938E1 Reset PH85 7bit 1.67 dB (00111) 0.68 dB (00011) 1018 mV (1100) Ø Inject Reset 8. Link 12 MGT_XOV1/XX MGT_XOV1/RX, No Link 2.388E13 1.418. 5.938E1 Reset PH85 7bit 1.67 dB (00111) 0.68 dB (00011) 1018 mV (1100) Ø Inject Reset 8. Link 13 MGT_XOV1/ATX MGT_XOV1/AT	Link 8	MGT_X0Y8/TX	MGT_X0Y8/RX	No Link	2.388E13	1.418	5.938E-1	Reset	PRBS 7-bit V	PRBS 7-bit V	1.67 dB (00111) ↓	0.68 dB (00011) V	1018 mV (1100) V	 Image: A start of the start of	Inject	Reset
ab. Link 10 MBI_X0V10/X MBI_X0V10/X MBI_X0V10/X MBI_X0V10X 2.38813 1.418. 5.93861 PRes2 PRes 7-bit 1.67 dB (00111) 0.68 dB (00011) 0.101 mV (1100) Ø Inject Resc b, Link 12 MGT_X0V12/X MGT_X0V12/K MG LNK 2.38813 1.418. 5.93861 Resct PRES 7-bit PRES 7-bit 0.67 dB (00111) 0.68 dB (00011) 1018 mV (1100) Ø Inject Resc b, Link 13 MGT_X0V13/X MGT_X0V13/RX No Link 2.38813 1.418. 5.93861 Resct PRES 7-bit PRES 7-bit 0.67 dB (00111) 0.68 dB (00011) 1018 mV (1100) Ø Inject Resc b, Link 13 MGT_X0V13/X MGT_X0V13/RX No Link 2.38813 1.418. 5.93861 Reset PRES 7-bit<	S Link 9	MGT_X0Y9/TX	MGT_X0Y9/RX	NO LINK	2.388E13	1.418	5.938E-1	Reset	PRBS 7-bit V	PRBS 7-bit V	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV (1100) ~	 Image: A start of the start of	Inject	Reset
ab. Link 11 Mol_X0/11/X Mol_X0/11/X Mol_X0/11/X Mol_X0/11/X Mol_X0/11/X Mol_X0/11/X Mol_X0/11/X Mol_X0/11/X Mol_X0/12/X Mol_X0/1	EINK 10	MGT_X0Y10/D	K MGT_X0Y10/R		2.388E13	1.418	5.938E-1	Reset	PRBS 7-Dit V	PRBS 7-Dit V	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV (1100) V	 ✓ 	Inject	Reset
6b Inik 12 Mid_2012/XVMG_V01201X (MC UNK 2.388E13 1.418 5.938E1 Reset PR85 7/bit PR85 7/bit 0.67 dB (00111) 0.68 dB (00011) 0.1018 mV (1100) Ø Inject Reset 6b Link 13 MGT_X0V147K MGT_X0V147K No Link 2.388E13 1.418 5.938E1 Reset PR85 7/bit PR85 7/bit 0.67 dB (00111) 0.68 dB (00011) 0.101 mV (1100) Ø Inject Reset 6b Link 15 MGT_X0V15/TX MGT_X0V15/RX No Link 2.388E13 1.418 5.938E1 Reset PR85 7/bit<	D Link 11	MGT_X0Y117D	K MGT_X0Y11/R	No Link	2.388E13	1.418	5.938E-1	Reset	PRBS 7-Dit V	PRBS 7-Dit V	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV (1100) V	✓	Inject	Reset
Bit Init 13 INST_20113/A Mol JARY, No Link 2.388E11 1.41.6. 5.358E1 Reset PR85 7/bit PR85 7/bit 0.67 dB (00111) 0.108 dB (00011) 0.108 mV (1100) V Inject Reset & Link 15 MGT_X0V15/TX MGT_X0V15/RX No Link 2.388E13 1.418 5.938E-1 Reset PR85 7/bit PR85 7/bit 0.68 dB (00011) 0.108 mV (1100) V Inject Reset & Link 15 MGT_X0V15/TX MGT_X0V15/RX No Link 2.388E13 1.418 5.938E-1 Reset PR85 7/bit<	O LINK 12 O Link 12	MGT_X0Y12/D	K MGT_X0Y12/R	No Link	2.300013	1.410	5.9300-1	Reset	PRBS 7-DiL V	PRBS 7-DiL V	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV(1100) V	4	Inject	Reset
0 0.00121 <	& Link 14	MGT_X0Y14/D	MGT_X0T13/R	No Link	2.388E13	1.418	5.938E-1	Reset	PRBS 7-bit v	PRBS 7-bit v	1.67 dB (00111) v	0.68 dB (00011) v	1018 mV (1100) ~	×	Inject	Reset
	& Link 15	MGT_X0114/17	MGT_X0114/10	No Link	2 388E13	1.418	5 938E-1	Reset	PRBS 7-bit w	PRBS 7-bit w	1.67 dB (00111) v	0.68 dB (00011) v	1018 mV (1100) v		Inject	Reset

6.7 Combined_TTC/Data to the FEX 9; test@6.4Gbps:

Bit wit wit wit wit wit wit wit wit wit w										Vivado	2017.2						-	• ×
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Td Console Messages Serial UO Links x Serial UD Links x Serial UD Links x Serial UD Links x Serial UD Links x Series UD Links Series UD Links Series UD Links	HARDWAR	RE MANAGER -	localhost/xilinx	_tcf/Xilinx/0	00016c47d	e501												? ×
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TX RX Status BEs Errors BER DEFT Reset TX Patterm TX Pre-Cursor TX Drf Swing DFE Enabled Inject Error TX Reset RX Pattern Unix (0) Image: Construction of the state	Q X	♦ +																
Lucks (0) Inc Inc Inc Reset PR85 7bit PR85 7bit L67 dB (0011) 0.08 dB (00011) 1018 mV(1100) Ø Inject Reset Reset MGT_X0YGTX M		TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject Error	TX Reset	RX Reset	RX PLI
0 (10) Met Fest PB8 7 bit v PB8 7 bit v </td <td>Links (0)</td> <td></td> <td>,</td> <td></td> <td>,</td> <td></td> <td></td> <td></td>	Links (0)												,		,			
Mot_zovorzy	0(16)							Reset	PRBS 7-bit ↓	PRBS 7-bit 🗸	1.67 dB(00111) ∨	0.68 dB(00011) 🗸	1018 mV(1100) ∨	1	Inject	Reset	Reset]
Metry ory rurs Metry ory rurs 64.13 0.293 <th0.293< th=""> 0.293 0.293<td></td><td>MGT_X0Y0/TX</td><td>MGT_X0Y0/RX</td><td>No Link</td><td>3.288</td><td>1.952</td><td>5.938E-1</td><td>Reset</td><td>PRBS 7-bit ↓</td><td>PRBS 7-bit 🗸</td><td>1.67 dB(00111) ↓</td><td>0.68 dB(00011) 🗸</td><td>1018 mV(1100) ∨</td><td>\checkmark</td><td>Inject</td><td>Reset</td><td>Reset</td><td>Lockec</td></th0.293<>		MGT_X0Y0/TX	MGT_X0Y0/RX	No Link	3.288	1.952	5.938E-1	Reset	PRBS 7-bit ↓	PRBS 7-bit 🗸	1.67 dB(00111) ↓	0.68 dB(00011) 🗸	1018 mV(1100) ∨	\checkmark	Inject	Reset	Reset	Lockec
MBI_2072/IX M01200 2.287 1.952 5.988+1 Reset PRBS 7-bit v 1.67 dB (00111) v 0.68 dB (00011) v 1018 mV(1100 v V Phget Reset Reset MGT_2074/IX MGT_2074/RK No Link 3.288 1.952 5.938+1 Reset PRBS 7-bit v 1.67 dB (00111) v 0.68 dB (00011) v 1018 mV(1100 v V Phget Reset Reset MGT_2074/IX MGT_2074/RK No Link 3.288 1.952 5.938+1 Reset PRBS 7-bit v 1.67 dB (00111) v 0.68 dB (00011) v 1018 mV(1100 v V Phget Reset Reset MGT_2074/IX MGT_2074/RK No Link 3.288 1.952 5.938+1 Reset PRBS 7-bit v 1.67 dB (00111) v 0.68 dB (00011) v 1018 mV(1100 v V Phget Reset Reset MGT_2077/RK MGT_2074/RK No Link 3.288 1.952 5.938+1 Reset PRBS 7-bit v 1.67 dB (00111) v 0.68 dB (00011) v 1018 mV(1100 v V Phget Reset Reset MGT_2077/RK NGT_2074/RK NGT No Link 3.288 1.952 5.938+1 Reset PRBS 7-bit v 1.67 dB (00111) v 0.68 dB (00011) v		MGT_X0Y1/TX	MGT_X0Y1/RX	6.413 G	2.931	0E0	3.411E	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) ↓	0.68 dB (00011) 🗸	1018 mV (1100) ↓	✓	Inject	Reset	Reset	Lockec
Impl_purpting Impl_pur		MGT_X0Y2/TX	MGT_X0Y2/RX	No Link	3.287	1.952	5.938E-1	Reset	PRBS 7-bit v	PRBS 7-bit v	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV (1100) V	1	Inject	Reset	Reset	
Intel_Unitary		MGT_X0Y3/TX	MGT_X0Y3/RX	No Link	3 288	1.952	5.938E-1	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111) V	0.68 dB (00011)	1018 mV (1100) V	 ✓ 	Inject	Reset	Reset	
Matrix X016/TX Matrix		MGT_X0Y5/TX	MGT X0Y5/RX	No Link	3.288	1.952	5.938E-1	Reset	PRBS 7-bit v	PRBS 7-bit v	1.67 dB (00111) v	0.68 dB (00011) v	1018 mV (1100) ~	<	Inject	Reset	Reset	Locked
MGT_X0Y7/TX MGT_X0Y1/TX		MGT X0Y6/TX	MGT X0Y6/RX	No Link	3.288	1.952	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	 Image: A start of the start of	Inject	Reset	Reset	Lockec
MGT_XOYB/TX_MGT_XOYB/TX_MGLINK 3.288 1.952 5.938E1 Reset PRBS 7-bit v 1.67 dB (00111) v 0.68 dB (00011) v 1018 mV (1100) v V Inject Reset Reset MGT_XOYB/TX_MGT_XOY10/TX_MGT_XOY10/TX_MGT_XOY10/TX_MGT_XOY10/TX_MGT_XOY10/TX_MGT_XOY10/TX_MGT_XOY10/TX_MGT_XOY10/TX_MGT_XOY10/TX_MGT_XOY10/TX_MGT_XOY10/TX_MGT_XOY12/TX_M		MGT_X0Y7/TX	MGT_X0Y7/RX	No Link	3.288	1.952	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) ∨	0.68 dB(00011) 🗸	1018 mV(1100) 🗸	1	Inject	Reset	Reset	Lockec
MGT_X0Y9/RX_MGL_X0Y9/RX_MGUINK 3.288 1.952 5.938E1 Reset PR85 7bit v PR85 7bit v 1.67 dB (00111) v 0.68 dB (00011) v 1018 mV (1100) v Ø Inject Reset Reset MGT_X0Y10/TX_MGT_X0Y10/TX_MBUINK 3.288 1.952 5.938E1 Reset PR85 7bit v PR85 7bit v PR85 7bit v 1.67 dB (00111) v 0.68 dB (00011) v 1018 mV (1100) v Ø Inject Reset Reset MGT_X0Y12/TX_MGT_X0Y12/FX_MGT_X0Y12		MGT_X0Y8/TX	MGT_X0Y8/RX	No Link	3.288	1.952	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB(00111) ↓	0.68 dB(00011) 🗸	1018 mV(1100) 🗸	\checkmark	Inject	Reset	Reset	Lockec
MGT_X0/12/fX_MGT_X0/12/fX_MG 3.288 1.952 5.938E-1 Reset PR85 7-bit v PR85 7-bit v 1.67 dB (00111) v 0.68 dB (00011) v 1018 mV (1100) v V Inject Reset Reset MGT_X0/12/fX_MGT_X0/12/fX		MGT_X0Y9/TX	MGT_X0Y9/RX	No Link	3.288	1.952	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB(00111) ∨	0.68 dB(00011) 🗸	1018 mV(1100) 🗸	\checkmark	Inject	Reset	Reset	Lockec
MGT_X0/11/rK MGT_X0/12/rK Mo Link 3.28a. 1.55 5.938E1 Reset PR85 7-bit > PR85 7-bit 0.68 dB (00011) 1018 mV (1100) Ø Inject Reset Reset MGT_X0/12/rK MGT_X0/12/rK Mo Link 3.28a. 1.952 5.938E1 Reset PR85 7-bit > PR85 7-bit 0.68 dB (00011) 1018 mV (1100) Ø Inject Reset Reset MGT_X0/12/rK MGT_X0/12/rK Mo Link 3.28a. 1.952 5.938E1 Reset PR85 7-bit > 1.67 dB (00111) 0.68 dB (00011) 1018 mV (1100) Ø Inject Reset Reset MGT_X0/12/rK MGT_X0/12/rK Mo Link 3.28a. 1.952 5.938E1 Reset PR85 7-bit 1.67 dB (00111) 0.68 dB (00011) 1018 mV (1100) Ø Inject Reset Reset MGT_X0/12/rK MGT_X0/12/rK Mo Link 3.28a. 1.952 5.938E1 Reset PR85 7-bit 1.67 dB (00111) 0.68 dB (00011) 1018 mV (1100) Ø Ø Inject Reset Reset MGT_X0/12/rK MGT_X0/15/rK MGT_X0/15/rK MGT_X0/15/rK MGT_X0/15/rK MGT_X0/15/rK MGT_X0/15/rK MGT		MGT_X0Y10/TX	MGT_X0Y10/RX	No Link	3.288	1.952	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) ↓	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	\checkmark	Inject	Reset	Reset	Lockec
MGT_XOY12/K MGT_XOY12/K MGT_MGT_XOY12/K MGT_MGT_MGT_XOY12/K MGT_MGT_MGT_MGT_MGT_MGT_MGT_MGT_MGT_MGT_		MGT_X0Y11/TX	MGT_X0Y11/RX	No Link	3.288	1.952	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) ↓	0.68 dB (00011) 🗸	1018 mV (1100) ↓	Image: A state of the state	Inject	Reset	Reset	Lockec
MGT_X0/13/M MGT_X0/13/M MGT_X0/14/M MGT_X0/14/M MGT_X0/15/MX MGT_X0/1		MGT_X0Y12/TX	MGT_X0Y12/RX	No Link	3.288	1.952	5.938E-1	Reset	PRBS 7-bit v	PRBS 7-bit v	1.67 dB (00111) ↓	0.68 dB (00011) V	1018 mV (1100) ~	1	Inject	Reset	Reset	Lockec
MGT_XOVIS/TX_MGT_X		MGT_X0Y13/1X	MGT_X0Y13/RX	No Link	3.200	1.952	5.020E-1	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV (1100) V	✓	Inject	Reset	Reset	
		MGT_X0V15/TX	MGT_X0V15/RX	No Link	3.288	1.952	5.938E-1	Reset	PBBS 7-bit	PBBS 7-bit v	1.67 dB (00111) v	0.68 dB (00011) v	1018 mV (1100) v	·	Inject	Reset	Reset	Locked

6.8 Combined_TTC/Data to the FEX 10; test@6.4Gbps:

Edit Tools Window ★ ★ € ★ ★ WARE MANAGER - localin Console Messages ★ ♦ ★ Ungrouped Links (0) Undrouped Links (0) Undroup 0 (16) & Link 0 MK & Link 2 MK & Link 3 MK	w Layout C C C C C C C C C C C C C C C C C C C	⊻iew Help Xtilinx/000016c Links × S RX	Q- Ou Dashboard 47de501 erial I/O So Status	iick Access										Serial I/O A	vnalyzer
	Serial I/O	⊘ X XIIInx/000016c Links × S RX	Dashboard 47de501 erial I/O S Status	d ↓ cans Bits										🗮 Serial I/O A	nalyzer
WARE MANAGER - localh Console Messages Image: Imag	Serial I/O	Xilinx/0000160 Links × S RX	erial I/O S	cans Bits											
Console Messages ★ ★ ★ te T. T. Ungrouped Links (o) * * b, Link 0 MC % ⊕, Link 1 MC % ⊕, Link 2 MC % ⊕, Link 3 MC %	Serial I/O	Links × S	erial I/O S	cans											
Image: marked bit in the state of	GT_X0Y0/TX	RX	Status	Bits											2 4
Image T. μ Ungrouped Links (o) μ Link Group 0 (16) δ ₀ Link 0 MC δ ₀ Link 1 MC δ ₀ Link 2 MC δ ₀ Link 3 MC δ ₀ Link 4 MC	TX GT_X0Y0/TX GT_X0Y1/TX	RX	Status	Bits											
Ungrouped Links (٥) Unk Group 0 (16) Unk 0 MC Unk 1 MC Unk 2 MC Unk 3 MC Unk 4 MC	GT_X0Y0/TX		Status	1111.0	Errore	DED	PEPT Porot	TV Pattorn	PV Pattorn	TX Bro Cursor	TX Post Cursor	TV Diff Swing	DEE Epobled	Inject Error	TY Poso
Link Group 0 (16) ab Link 0 MC bb Link 1 MC ab Link 2 MC ab Link 3 MC ab Link 4 MC	GT_X0Y0/TX			2.00	LITUIS	DEIX	DEINI Neser	ix rattern	No. Tatteri	TXTTE-Cursor	TXT OSC-CUISO	TX Dill Swing	DIE Ellabled	inject ciroi	IX Nese
Bo Link 0 MC % Link 1 MC Bo Link 2 MC Bo Link 3 MC Bo Link 4 MC	GT_X0Y0/TX						Reset	PRBS 7-bit 🗸	PRBS 7-bit 🐱	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	✓	Inject	Rese
% Link 1 MC 💩 Link 2 MC 💩 Link 3 MC 💩 Link 4 MC	GT YOVL/TY	MGT_X0Y0/RX	No Link	1.58E13	9.384	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	 Image: A start of the start of	Inject	Rese
ab Link 2 MC ab Link 3 MC ab Link 4 MC	01_1012/11	MGT_X0Y1/RX	6.413 G	1.588E13	0E0	6.297E	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	 Image: A start of the start of	Inject	Rese
 δ_b Link 3 M0 δ_b Link 4 M0 	GT_X0Y2/TX	MGT_X0Y2/RX	No Link	1.58E13	9.384	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) ↓	0.68 dB (00011) 🗸	1018 mV(1100) 🗸	\checkmark	Inject	Rese
🗞 Link 4 MC	GT_X0Y3/TX	MGT_X0Y3/RX	No Link	1.58E13	9.384	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	\checkmark	Inject] Rese
	GT_X0Y4/TX	MGT_X0Y4/RX	No Link	1.58E13	9.384	5.938E-1	Reset	PRBS 7-bit ↓	PRBS 7-bit 🗸	1.67 dB (00111) ↓	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	Image: A state of the state	Inject	Rese
S Link 5 MC	GT_X0Y5/TX	MGT_X0Y5/RX	No Link	1.58E13	9.384	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) ↓	0.68 dB (00011) 🗸	1018 mV (1100) 🗸		Inject	Rese
Tink 6 MC	GI_X0Y6/TX	MGF_X0Y6/RX	No Link	1.581E13	9.385	5.938E-1	Reset	PRBS 7-bit V	PRBS 7-bit V	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV (1100) ~	Image: A state of the state	Inject	Rese
S LINK / MC	GT_X0Y7/TX	MGT_X0Y7/RX	No Link	1.581E13	9.385	5.938E-1	Reset	PRBS 7-bit V	PRBS 7-bit V	1.67 dB (00111) V	0.68 dB (00011) ~	1018 mV (1100) V		Inject	Rese
LINK 0 MC		MGT_X0Y8/RX	No Link	1.501613	9.365	5.9386-1	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV (1100) V		Inject	Rese
& Link 10 MC		MGT_X013/KX	No Link	1.581E13	9.385	5.938E-1	Reset	PBBS 7-bit	PBBS 7-bit v	1.67 dB (00111) v	0.68 dB (00011) v	1018 mV (1100) v		Inject	Rese
& Link 11 MC	GT X0Y11/TX	MGT_X0Y11/8X	No Link	1.581E13	9.385	5.938E-1	Reset	PBBS 7-bit v	PBBS 7-bit v	1.67 dB (00111) v	0.68 dB (00011) v	1018 mV (1100) ~	×	Inject	Rese
& Link 12 MC	GT X0Y12/TX	MGT X0Y12/RX	No Link	1.581E13	9.385	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	Image: A state of the state	Inject	Rese
& Link 13 MC	GT_X0Y13/TX	MGT_X0Y1 3/RX	No Link	1.581E13	9.385	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	 Image: A start of the start of	Inject	Rese
🗞 Link 14 MC	GT_X0Y14/TX	MGT_X0Y14/RX	No Link	1.581E13	9.385	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	✓	Inject	Rese
🗞 Link 15 MC	GT_X0Y15/TX	MGT_X0Y15/RX	No Link	1.581E13	9.385	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	~	Inject	Reset
₿ ₀ Link 15 MC	GT_X0Y15/TX	MGT_X0Y15/RX	No Link	1.581E13	9.385	5.938E-1	Reset	PRBS 7-bit ↓	PRBS 7-bit ↓	1.67 dB (00111) ↓	0.68 dB (00011) ~	1018 mV (1100) 🗸	×	Inject] <u>Re</u>

6.9 Combined_TTC/Data to the FEX 11; test@6.4Gbps:

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ile <u>E</u> dit	<u>T</u> ools <u>W</u> ind	dow La <u>y</u>	out <u>V</u> iew	<u>H</u> elp	Q+ Quick Ad	cess										
≥] ← /	• 🖬 🐘	× ¢	<u>%</u>	😹 Das	hboard 👻										📰 Serial I/	0 Analyzer
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Q	≑ +															
x	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject Error	TX Reset	RX Reset	RX PLL Status
						Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	7	Inject	Reset	Reset	
ат хоуолтх	MGT X0Y0/RX	No Link	1.717E10	1.02E10	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 👻	1.67 dB (00111) v	0.68 dB (00011) v	1018 mV (1100) ~	 ✓ 	Inject	Reset	Reset	Locked
T_X0Y1/TX	MGT_X0Y1/RX	6.413 G	1.73E10	0E0	5.78E-11	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	1	Inject	Reset	Reset	Locked
л_хоу2/тх	MGT_X0Y2/RX	No Link	1.782E10	1.058	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB(00111) 🗸	0.68 dB(00011) 🗸	1018 mV(1100) 🗸	1	Inject	Reset	Reset	Locked
т_хоуз/тх	MGT_X0Y3/RX	No Link	1.785E10	1.06E10	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB(00111) 🗸	0.68 dB(00011) 🗸	1018 mV(1100) 🗸	✓	Inject	Reset	Reset	Locked
T_X0Y4/TX	MGT_X0Y4/RX	No Link	1.788E10	1.061	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB(00111) 🗸	0.68 dB(00011) 🗸	1018 mV(1100) 🗸	1	Inject	Reset	Reset	Locked
T_X0Y5/TX	MGT_X0Y5/RX	No Link	1.739E10	1.033	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB(00111) ↓	0.68 dB(00011) 🗸	1018 mV(1100) 🗸	\checkmark	Inject	Reset	Reset	Locked
т_хоү6/тх	MGT_X0Y6/RX	No Link	1.742E10	1.034	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB(00111) ↓	0.68 dB(00011) 🗸	1018 mV (1100) 🗸	1	Inject	Reset	Reset	Locked
f_X0Y7/TX	MGT_X0Y7/RX	No Link	1.745E10	1.036	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) ↓	0.68 dB (00011) 🗸	1018 mV (1100) ~	1	Inject	Reset	Reset	Locked
г_хоүв/тх	MGT_X0Y8/RX	No Link	1.747E10	1.038	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) ↓	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	1	Inject	Reset	Reset	Locked
T_X0Y9/TX	MGT_X0Y9/RX	No Link	1.751E10	1.04E10	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) ↓	0.68 dB (00011) ↓	1018 mV (1100) ~	✓	Inject	Reset	Reset	Locked
T_X0Y10/TX	MGT_X0Y10/RX	No Link	1.129E10	6.706E9	5.938E-1	Reset	PRBS 7-bit V	PRBS 7-bit v	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV (1100) ~	1	Inject	Reset	Reset	Locked
1_X0Y11/1X	MGT_X0Y11/HX	No Link	1.809EI0	1.074	5.938E-1	Reset	PRBS 7-DIL V	PRBS 7-bit v	1.67 dB (00111) V	0.68 dB (00011) 👳	1018 mV (1100) V	v	Inject	Reset	Reset	Locked
T XOV13/TX	MGT_X0112/RX	No Link	1.815E10	1.077	5.938E-1	Reset	PBBS 7-bit v	PBBS 7-bit	1.67 dB (00111)	0.68 dB (00011) v	1018 mV (1100) v	<i>.</i>	Inject	Reset	Reset	Locked
T X0V14/TX	MGT_X0V14/BX	No Link	1.817E10	1.079	5.938E-1	Reset	PBBS 7-bit v	PBBS 7-bit	1.67 dB (00111)	0.68 dB (00011) v	1018 mV (1100) ~	<i>z</i>	Inject	Reset	Reset	Locked
T X0V15/TX	MGT_X0V15/BX	No Link	1.82E10	1.081	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit v	1.67 dB (00111) v	0.68 dB (00011) v	1018 mV (1100) ~		Inject	Reset	Reset	Locked
r_x0v15/Tx	MGT_X0Y15/RX	No Link	1.82E10	1.081	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB(00111) ↓	0.68 dB(00011) 🗸	1018 mV (1100) 🗸	Ø	Inject	Reset	Reset	Locked

7.0 Combined_TTC/Data to the FEX 12; test@6.4Gbps:

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Nume Nume <t< th=""><th></th><th>× a</th><th></th><th>Dashboan</th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th>= Serial I/O A</th><th>analyzer</th></t<>		× a		Dashboan											= Serial I/O A	analyzer
Console Message Serial IO Link x Serial IO Link Serial IO Link X Serial IO Link Serial IO Link x Serial IO Link x Message Serial IO Link K Message Serial IO Link Message Message Me	DWARE MANAGER	albert kiliny to	forilipy/00001.6	c47do501												
Nerses Seraturo Link s Seraturo Santa	DWARE MANAGER -100	an iost/AnniA_tt	.17/11110/000010	C4708301												f
Image N RX RX B18 Errors BER BETR BeeR CAP Pattern RX Percursor TX Ddf Swng DE Enabled Neet Error RA Beer 0 Undrogoet Line	l Console Message	s Serial I/C	DLinks × S	erial I/O S	cans											? _ 0
TX RX Status Bits Errors BER DERT Reset TX Pattern RX Pattern TX Pat-Cursor TX Diff Samp DEF Enabled mject Error TA Beset Jundroupoul Links Mol TX YOV/TX Mol XX Stratus Stratus Base TA PR85 7Abt PR85 7Abt In PR85 7Abt	. <u>₹</u> ≑ +															
Unpropertures Description Reset PR85 7-bit PR85 7-bit< PR85 7-bit PR85 7-bit< PR85 7-bit PR85 7-bit PR85 7-bit PR85 7-bit PR85 7-bit PR85 7-bit< PR85 7-bit PR85 7-bit< PR85 7-bit< PR85 7-bit< PR	me	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject Error	TX Reset
Burk Grup 0.19 MGT 2007/JT. MG	🖴 Ungrouped Links (0)												-			
b. IMO MOT, YOUYTK, MOT, YUNGK, MOLLINK, S-703EL S-70.5E. Reset PRBS 7 het PRBS 7 het PRBS 7 het S 70 d(00111) 0.66 dB (00011) 1.018 mV(1100) V Implet Reset b. Link 2 MGT, YOUYTK, MGT, YUNGK, MOLINK S-703EL S-714. I/002EL Reset PRBS 7 het PRBS 7 het S 708 (00111) 0.66 dB (00011) 1.018 mV(1100) V V Implet Reset b. Link 4 MGT, YOUYTK, MGT, YUNGK, MOLINK S-703EL S-714. I/002EL Reset PRBS 7 het I/RES 7 het	🐵 Link Group 0 (16)							Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	✓	Inject	Reset
Sunk1 MGT_XOU/TX MGT_XOU/TX </td <td>🗞 Link 0</td> <td>MGT_X0Y0/TX</td> <td>MGT_X0Y0/RX</td> <td>No Link</td> <td>5.703E14</td> <td>5.715</td> <td>1.002E-1</td> <td>Reset</td> <td>PRBS 7-bit 🗸</td> <td>PRBS 7-bit 🗸</td> <td>1.67 dB (00111) ↓</td> <td>0.68 dB (00011) 🗸</td> <td>1018 mV(1100) 🗸</td> <td>\checkmark</td> <td>Inject</td> <td>Reset</td>	🗞 Link 0	MGT_X0Y0/TX	MGT_X0Y0/RX	No Link	5.703E14	5.715	1.002E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) ↓	0.68 dB (00011) 🗸	1018 mV(1100) 🗸	\checkmark	Inject	Reset
Ba IMC 2 MOV 2007 X MOT 2007 2007 2007 X MOT 2007 2007 2007 2007 2007 2007 2007 200	🗞 Link 1	MGT_X0Y1/TX	MGT_X0Y1/RX	6.413 G	5.667E14	0E0	1.765E	Reset	PRBS 7-bit ↓	PRBS 7-bit 🗸	1.67 dB (00111) 🗸	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	\checkmark	Inject	Reset
ib. ink 3 MGT_X0Y37K MGT_X0Y37K <td>🗞 Link 2</td> <td>MGT_X0Y2/TX</td> <td>MGT_X0Y2/RX</td> <td>No Link</td> <td>5.703E14</td> <td>5.714</td> <td>1.002E-1</td> <td>Reset</td> <td>PRBS 7-bit 🗸</td> <td>PRBS 7-bit 🗸</td> <td>1.67 dB (00111) ↓</td> <td>0.68 dB (00011) 🗸</td> <td>1018 mV (1100) 🗸</td> <td>1</td> <td>Inject</td> <td>Reset</td>	🗞 Link 2	MGT_X0Y2/TX	MGT_X0Y2/RX	No Link	5.703E14	5.714	1.002E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) ↓	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	1	Inject	Reset
Built 4 MGT_X0Y4/TK MGT_X0Y1/TK <	💫 Link 3	MGT_X0Y3/TX	MGT_X0Y3/RX	No Link	5.703E14	5.714	1.002E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) ↓	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	1	Inject	Reset
Ba. Link S MdT_X0Y5/TX Motile 5.708:11 5.715. 1.002E1 Reset PRBS 7-bit 1.67 dB (0011) 0.68 dB (00011) 1.018 mV (1100) V Imject Reset Ba. Link S MdT_X0Y6/TX MdT_X0Y7/TX MGT_X0Y7/TX MGT_X0Y7/TX NGT_X0Y7/TX NGT_X0Y7/T	🗞 Link 4	MGT_X0Y4/TX	MGT_X0Y4/RX	No Link	5.703E14	5.714	1.002E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) ↓	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	✓	Inject	Reset
Ba. Link 8 MET_XOV6/TX MOT_XOV17/K No Lunk 5.705±1 5.715. 1.002±1 Reset PRBS 7-bit 1.67 dB (00111) 0.68 dB (00011) 1.018 mV (1100) V Imject Reset Ba. Link 7 MCT_XOV7/TX MOT_XOV7/TX MOT_LONK S.705±14 5.715. 1.002±1 Reset PRBS 7-bit 1.67 dB (00111) 0.68 dB (00011) 1.018 mV (1100) V Imject Reset Ba. Link 10 MGT_XOV17/X MGT_XOV10/RX No Lunk 5.703±14 5.715. 1.002±1 Reset PRBS 7-bit<	S Link 5	MGT_X0Y5/TX	MGT_X0Y5/RX	No Link	5.703E14	5.715	1.002E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit 🗸	1.67 dB (00111) ↓	0.68 dB (00011) v	1018 mV (1100) v	Image: A state of the state	Inject	Reset
ab, LINK 2 MGT_X0Y/TX MGT_X0Y/TX MGT_X0Y/TX MC 5./13 1.002-1 Reset PRBS 7-bit v 1.67 dB (00111) v 0.68 dB (00011) v 1.018 mV (1100) v V Inject Reset b, LINK 8 MGT_X0Y9/TX MGT_X0Y9/TX MGT_X0Y9/TX MGT_X0Y9/TX MGT_X0Y9/TX MGT_X0Y9/TX 5.703E14 5.715 1.002E1 Reset PRBS 7-bit v 1.67 dB (00111) v 0.66 dB (00011) v 1.018 mV (1100) v V Inject Reset b, LINK 10 MGT_X0Y10/TX MGT_X0Y10/TX MGT_X0Y10/TX MGT_X0Y10/TX MGT_X0Y12/TX MGT_X0	S Link 6	MGT_X0Y6/TX	MGT_X0Y6/RX	No Link	5.703E14	5.715	1.002E-1	Reset	PRBS 7-bit V	PRBS 7-bit V	1.67 dB (00111) ↓	0.68 dB (00011) V	1018 mV (1100) V	✓	Inject	Reset
Ba. Link 8 Mell 2019/1X Mill 2019/X Moland 5.705-14 5.715. 1.002-1 Hess / PRB 7-bit PRB 7-bit 1.67 dB (00111) 0.068 dB (00011) 1.018 mV (1100) Ø Inject Hesset Ba. Link 9 MMT_X0V107X MGT_X01107K No Link 5.703E14 5.715. 1.002E1 Reset PRB 7-bit PRB 7-bit 0.66 dB (00011) 1.018 mV (1100) Ø Inject Reset Ba. Link 10 MGT_X0V107K MGT_X0V117K NGT_X0V117K NGT	S LINK /	MGT_X0Y7/TX	MGT_X0Y7/RX	No Link	5.703E14	5.715	1.002E-1	Reset	PRBS 7-bit V	PRBS 7-bit V	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV (1100) V	Image: A state of the state	Inject	Reset
Bit Info Mid [V07/IX Mid] V017/IX Mid] V017/IX Mid] V017X M	Link 8	MGT_X0Y8/TX	MGT_X0Y8/RX	NO LINK	5.703E14	5.715	1.002E-1	Reset	PRBS 7-Dit V	PRBS 7-bit V	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV (1100) V	~	Inject	Reset
Bit Int I MRI_001101X MIG_00110X R0 Lunk S.7.0814 S.7.14. L002E1 Reset PRBS 7-bit I.67 dB (00111) O.68 dB (00011) I.18 mV (1000) V Imject Reset Bit Int I MGT_007117X MGT_007137X No Lunk S.703E14 S.714 1.002E1 Reset PRBS 7-bit 1.67 dB (00111) 0.68 dB (00011) I.018 mV (1000) V Imject Reset Bit Int I MGT_007137X MGT_007137X No Lunk S.703E14 S.714 1.002E1 Reset PRBS 7-bit 1.67 dB (00111) 0.68 dB (00011) I.018 mV (1000) V Imject Reset Bit Int I MGT_007147X MGT_007147X No Lunk S.703E14 S.714 1.002E1 Reset PRBS 7-bit I.67 dB (00111) 0.68 dB (00011) I.018 mV (1000) V Imject Reset Bit Link 14 MGT_007147X MGT_007147X No Lunk S.703E14 S.714 1.002E1 Reset PRBS 7-bit I.67 dB (00111) 0.68 dB (00011) I.018 mV (1000) V Imject Reset Bit Link 15 MGT_007147X MGT_007147X NO LUNK S.703E1	b) Link 9	MGT_X0Y9/1X	MGT_X0Y9/RX	NO LINK	5.703E14	5./15	1.002E-1	Reset	PRBS 7-DIL V	PRBS 7-DIL V	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV (1100) V	×	Inject	Reset
66 UN11 MB1_20111/W101_2011 (M101001 J.14 LORDER J PRB5 7-bit 1.67 dB (00111) 0.05 dB (00011) 1.018 mV (1100) J.14 Inject Reset 66 Link 12 MGT_X001_27K MGT_X012/RK No Link 5.705E14 5.714 1.002E1 Reset PRB5 7-bit 1.67 dB (00111) 0.068 dB (00011) 1.018 mV (1100) J.1 Inject Reset 60 Link 12 MGT_X001_27K MGT_X012/RK No Link 5.705E14 5.714 1.002E1 Reset PRB5 7-bit 1.67 dB (00111) 0.68 dB (00011) 1.018 mV (1100) J. Minit Minit Minit Minit 5.703E14 5.714 1.002E1 Reset PRB5 7-bit 1.67 dB (00111) 0.68 dB (00011) 1.018 mV (1100) J. Minit <	Link 10	MGT_X0Y10/1	X MGT_X0Y10/R	No Link	5.703E14	5.715	1.002E-1	Reset	PRBS 7-bit	PRBS 7-bit V	1.67 dB (00111) V	0.68 dB (00011) V	1018 mV(1100) V	v	Inject	Reset
66 biller11 biller121 biller121 biller13 bil	OLINK 11 Q. Link 12	MGT_X0Y11/1	X MGT_X0111/R	No Link	5 702614	5.714	1.002E-1	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111) v	0.68 dB (00011) v	1018 mV(1100) v	¥	Inject	Beset
Bit Indigon 1 and monormal contract Software France Test	6 Link 12	MGT_X0112/15	X MGT_X0112/R	No Link	5.703E14	5.714	1.002E-1	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111) v	0.68 dB (00011) v	1018 mV(1100) v	v	Inject	Reset
Burk 15 MST_X0115/TX MST_X015/TX MST_X015/TX MST_X015/TX MST_X015/TX MST_X0115/TX MST_X0115/	& Link 14	MGT_X0Y14/C	X MGT_X0113/R	No Link	5.703E14	5 714	1.002E-1	Reset	PBBS 7-bit	PBBS 7-bit w	1.67 dB (00111) v	0.68 dB (00011) v	1018 mV (1100) v	×	Inject	Reset
	& Link 15	MGT_X0V15/T	X MGT_X0V15/8	No Link	5.703E14	5.714	1.002E-1	Reset	PBBS 7-bit	PBBS 7-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (1100) v		Inject	Reset

7.1 Combined_TTC/Data to the FEX 13; test@6.4Gbps:

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Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject
😑 Ungrouped Links (0)												-		
 Combined Data to FEX 13 (1) 							Reset	PRBS 7-bit ↓	PRBS 7-bit	✓ 1.67 dB (00111) ✓	0.68 dB(00011) 🗸	1018 mV(1100) 🗸	1	Ir
% Link 1	MGT_X0Y1/TX	MGT_X0Y1/RX	6.413 Gbps	5.5E13	1E0	1.818E-14	Reset	PRBS 7-bit ↓	PRBS 7-bit	✓ 1.67 dB (00111) √	0.68 dB(00011) 🗸	1018 mV(1100) 🗸	 Image: A start of the start of	Ir
 Link Group 1 (15) 							Reset	PRBS 7-bit 🗸	PRBS 7-bit	✓ 1.67 dB (00111) ✓	0.68 dB(00011) 🗸	1018 mV(1100) 🗸	 Image: A start of the start of	l Ir
🗞 Link 16	MGT_X0Y0/TX	MGT_X0Y0/RX	No Link	5.473E13	3.25E13	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit	✓ 1.67 dB (00111) ✓	0.68 dB(00011) 🗸	1018 mV(1100) 🗸	\checkmark	In
🗞 Link 17	MGT_X0Y2/TX	MGT_X0Y0/RX	No Link	6.652E14	4.756E13	7.15E-2	Reset	PRBS 7-bit ∨	PRBS 7-bit	✓ 1.67 dB (00111) √	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	1	Ir
🗞 Link 18	MGT_X0Y3/TX	MGT_X0Y1/RX	No Link	6.651E14	4.749E13	7.14E-2	Reset	PRBS 7-bit ↓	PRBS 7-bit	✓ 1.67 dB (00111) ✓	0.68 dB(00011) 🗸	1018 mV(1100) ↓	1	Ir
🗞 Link 19	MGT_X0Y4/TX	MGT_X0Y2/RX	No Link	5.473E13	3.25E13	5.938E-1	Reset	PRBS 7-bit ↓	PRBS 7-bit	✓ 1.67 dB (00111) √	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	\checkmark	In
🗞 Link 20	MGT_X0Y5/TX	MGT_X0Y2/RX	No Link	6.651E14	4.66E13	7.007E-2	Reset	PRBS 7-bit ↓	PRBS 7-bit	✓ 1.67 dB (00111) ✓	0.68 dB (00011) 🗸	1018 mV (1100) ↓	1	
💫 Link 21	MGT_X0Y6/TX	MGT_X0Y3/RX	No Link	5.473E13	3.25E13	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit	✓ 1.67 dB (00111) √	0.68 dB (00011) v	1018 mV (1100) 🗸	~	In
🐌 Link 22	MGT_X0Y7/TX	MGT_X0Y3/RX	No Link	6.651E14	4.753E13	7.146E-2	Reset	PRBS 7-bit ↓	PRBS 7-bit	✓ 1.67 dB (00111) ✓	0.68 dB (00011) v	1018 mV (1100) ~	Image: A state of the state	lr
🗞 Link 23	MGT_X0Y8/TX	MGT_X0Y4/RX	No Link	5.473E13	3.25E13	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit	✓ 1.67 dB (00111) ✓	0.68 dB (00011) ~	1018 mV (1100) 🗸	~	
💫 Link 24	MGT_X0Y9/TX	MGT_X0Y4/RX	No Link	6.651E14	4.749E13	7.14E-2	Reset	PRBS 7-bit 🗸	PRBS 7-bit	✓ 1.67 dB (00111) ✓	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	1	
🐌 Link 25	MGT_X0Y10/TX	MGT_X0Y5/RX	No Link	5.473E13	3.25E13	5.938E-1	Reset	PRBS 7-bit 🗸	PRBS 7-bit	✓ 1.67 dB (00111) ✓	0.68 dB (00011) ~	1018 mV (1100) 🗸	✓	
S Link 26	MGT_X0Y11/TX	MGT_X0Y5/RX	No Link	6.651E14	4.974E13	7.479E-2	Reset	PRBS 7-bit 🗸	PRBS 7-bit	✓ 1.67 dB (00111) ✓	0.68 dB (00011) v	1018 mV (1100) v	Image: A state of the state	In
6 Link 27	MGT_X0Y12/TX	MGT_X0Y6/RX	No Link	5.473E13	3.25E13	5.938E-1	Reset	PRBS 7-bit V	PRBS 7-bit	✓ 1.67 dB (00111) ✓	0.68 dB (00011) V	1018 mV (1100) V	✓	
S Link 28	MGT_X0Y13/TX	MGT_X0Y6/RX	No Link	6.651E14	4.749E13	7.141E-2	Reset	PRBS 7-bit 🗸	PRBS 7-bit	✓ 1.67 dB (00111) ✓	0.68 dB (00011) v	1018 mV (1100) v	Image: A state of the state	
6 Link 29	MGT_X0Y14/1x	CMGT_X0Y7/RX	NO LINK	5.4/3E13	3.25E13	5.938E-1	Reset	PRBS 7-DIt V	PRBS 7-DIC	✓ 1.67 dB (00111) ✓	0.68 dB (00011) V	1018 mV (1100) V	✓	
🐌 Link 30	MGT_X0Y15/TX	(MGT_X0Y7/RX	No Link	6.651E14	4.018E13	6.041E-2	Reset	PRBS 7-bit 🗸	PRBS 7-bit	✓ 1.67 dB (00111) ✓	0.68 dB (00011) 🗸	1018 mV (1100) 🗸	\checkmark	In
8, Link 30	<u>MGT_X0Y15/7X</u>	(MGT_X0Y7/RX	No Link	6.651E14	4.018E13	6.041E-2	Reset	PRBS7-bit V	PRBS 7-bit	 ↓ 1.67 dB (00111) 	0.68 dB (00011) 🗸	1018 mV (1100) 🗸		

7.2 Combined_TTC/Data to the FEX 14; test@6.4Gbps:

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A mergeware ManAgER -localhost/wilnvg/tox/00016-d7/de501 Ref WARE MANAGER -localhost/wilnvg/tox/00016-d7/de501 Ref Console Mergeware ManAgER -localhost/wilnvg/tox/00016-d7/de501 Ref Console Mergeware ManAgER -localhost/wilnvg/tox/00016-d7/de501 Ref Console Mergeware ManAgER -localhost/wilnvg/tox/00016-d7/de501 Name TX RX Status BER BERT Reset TX Pattern TX Post-Cursor TX Diff Swing DFE Enabled Mergeware ManAgER - local de (00011) 0.66 dB (00011) 1018 mv(1100) ✓ Mergeware ManAgER - localhost/will/mv Reset PR85 7-bit 1.67 dB (00111) 0.66 dB (00011) 1018 mv(1100) ✓ Mergeware ManAgER - localhost/will/mv Reset PR85 7-bit 1.67 dB (00111) 0.66 dB (00011) 1018 mv(1100) ✓ Mergeware ManAgER - local host/will/mv Reset PR85 7-bit <th <="" colspan="2" th=""><th>nject Error</th><th>? _ ć</th></th>	<th>nject Error</th> <th>? _ ć</th>		nject Error	? _ ć
Messages Serial VO Links × Serial VO Scans Q X R Serial VO Links × Serial VO Scans Au X R Status Bits Errors BER BERT Reset TX Pattern TX Pre-Cursor TX Post-Cursor TX Diff Swing DFE Enabled International of the series G Ungrouped Links (0) C RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern TX Pre-Cursor TX Post-Cursor TX Diff Swing DFE Enabled International of the series © Ungrouped Links (0) C Errors BER BERT Reset PRBS 7-bit PRBS 7-bit 1.67 dB (00111) 0.68 dB (00011) 1018 mV (1100) V International of the series International o	nject Error	? — d		
Call Console Messages Serial I/O Links × Serial I/O Scans Q X RX Status Bits Errors BER BERT Reset TX Pattern TX Pre-Cursor TX Post-Cursor TX Diff Swing DFE Enabled In is Ungrouped Links (0) Image: Constraint of the	nject Error	? _ ć		
Q ¥ I TX FX Statu Bits Errors BER BERT Reset TX Pattern FX Pattern TX Pre-Cursor TX Post-Cursor TX Diff Swing DFE Enabled Interpretabled 0 ungrouped Links (0) <td< th=""><td>nject Error</td><td>TX Rese</td></td<>	nject Error	TX Rese		
Name TX RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern TX Per-Cursor TX Post-Cursor TX Diff Swing DFE Enabled D Ungrouped Links(0) 0	nject Error Inject	TX Rese		
Ongrouped Links (iii) Reset PR85 7-bit PR85 7-bit 1.67 dB (00111) 0.68 dB (00011) 1018 mV (1100) Image: Constraint of the constr	Inject			
Bit into 0 MGT_XOVO/TX	inject	Deced		
Built 0 MG_X010/X		Reset		
S LINK I MGI_X011/IX MGI_X011/IX 6.413 G 1.492213 0E0 6.7012 Reset PR657-bit ♥ PR657-bit ♥ 1.67 db (00111) ♥ 0.68 db (00011) ♥ 1018 mV (1100) ♥	inject	Reset		
9. Link 2 NOT YOVOTY NOT YYYYYYYYYYYYYYYYYYYYYYYYYYYYYYYY	Inject	Reset		
	Inject	Reset		
8. LInk 7 MGT X0Y7/TX MGT X0Y7/RX No Link 1.485E13 8.817 5.938E-1 PR85 7-bit y PR85 7-bit y 1.67 d8 (00111) y 0.68 d8 (00011) y 1018 mV (1100) y	Inject	Reset		
& Link 8 MGT X0Y8/TX MGT X0Y8/TX No Link 1.485E13 8.818 5.938E-1 Reset PR85 7-bit v PR85 7-bit v 1.67 d8 (0011) v 0.68 d8 (00011) v 1018 mV (100) v	Inject	Reset		
8. Link 9 MGT X0Y9/TX MGT X0Y9/RX No Link 1.485E13 8.818 5.938E-1 Reset PRBS 7-bit v PRBS 7-bit v 1.67 dB (00111) v 0.68 dB (00011) v 1018 mV (1100) v V	Inject	Reset		
8. Link 10 MGT_X0Y10/TX MGT_X0	Inject	Reset		
🔥 Link 11 MGT_X0Y11/TX MGT_X0Y	Inject	Reset		
🔥 LInk 12 MGT_X0Y12/TX MGT_X0Y12/TX MGT_X0Y12/TX NG LInk 1.485E13 8.818 5.938E-1 Reset PRBS 7-bit 🗸 PRBS 7-bit 🗸 1.67 dB (00111) 🗸 0.68 dB (00011) 🗸 1018 mV (1100) 🗸 📝	Inject	Reset		
🔥 Link 13 MGT_X0Y13/TX MGT_X	Inject	Reset		
δ ₂ Link 14 MGT_X0Y14/TX MGT_X0Y14/RX No Link 1.485E13 8.818 5.938E-1 Reset PRBS 7-bit ∨ PRBS 7-bit ∨ 1.67 dB (00111) ∨ 0.68 dB (00011) ∨ 1018 mV (1100) ∨ 📝	Inject	Reset		
💫 Link 15 ΜGT_X0Y15/TX_MGT_X0	Inject	Reset		

7.3 IBERT Slot no 3 + extra MGT channel tests, tests@6.4Gbps covered the area:

- 4 MiniPOD Receiver MGT channels
- 6 lanes of MGT data from the FEX slot 3
- Combined_TTC/Data to the ROD on This HUB
- Combined_TTC/Data Data to the Other HUB
- Combined_TTC/Data Data that was sent out by the Other HUB
- Readout Control Data that was sent out by the ROD on This HUB
- HUB sends out two lanes of Readout data to the Other HUB
- HUB receives two lanes of Readout data from the Other HUB
- FPGA on This HUB sends one lane of its readout data to the ROD on This HUB

🔍 Applications 👻 Places 👻 🖌 Vivado 2017.2	2 🔻												Sat 16:27	
						Vivado 2	017.2						-	o x
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Tcl Console Messages Serial I/O Links	× Serial I/O	Scans												?_06
Q <u>X</u> ≑ 1														
Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Patt	ern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enable
Ungrouped Links (0)														
✓ IUB: Readout Control Data from This Rod (1)							Reset]	PRBS 7-	bit 🗸				1
🗞 Link 0		MGT_X0Y3/RX	6.413 Gbps	4.179E12	0E0	2.393E-13	Reset]	PRBS 7-	bit 🗸				✓
w lub: MiniPods (4)							Reset]	PRBS 7	bit 🗸				1
% Link 1		MGT_X0Y0/RX	6.413 Gbps	4.179E12	0E0	2.393E-13	Reset]	PRBS 7-	bit 🗸				1
% Link 2		MGT_X0Y1/RX	6.411 Gbps	4.179E12	0E0	2.393E-13	Reset]	PRBS 7	bit 🗸				 Image: A start of the start of
% Link 3		MGT_X0Y2/RX	6.422 Gbps	4.179E12	0E0	2.393E-13	Reset]	PRBS 7-	bit 🗸				1
% Link 4		MGT_X0Y0/RX	6.427 Gbps	4.179E12	0E0	2.393E-13	Reset]	PRBS 7-	bit 🗸				✓
							Reset	PRBS 7-bit	V PRBS 7-	bit 🗸	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000) 🗸	1
% Link 74	MGT_X0Y38/T	X MGT_X0Y38/R	6.413 Gbps	4.179E12	0E0	2.393E-13	Reset	PRBS 7-bit	V PRBS 7-	bit 🗸	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000) 🗸	1
% Link 76	MGT_X0Y39/T	X MGT_X0Y39/R	6.412 Gbps	4.179E12	0E0	2.393E-13	Reset	PRBS 7-bit	V PRBS 7-	bit 🗸	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000) 🗸	
HUB: Combined Data from Other HUB (1)							Reset	1	PRBS 7-	bit 🗸				✓
% Link 2		MGT_X0Y1/RX	6.413 Gbps	4.179E12	0E0	2.393E-13	Reset	1	PRBS 7-	bit 🗸				1
							Reset	1	PRBS 7-	bit 🗸				✓
% Link 0		MGT X0Y4/RX	6.413 Gbps	4.913E11	1E0	2.036E-12	Reset	1	PRBS 7	bit 🗸				
% Link 1		MGT X0Y5/RX	6.413 Gbps	4.913E11	1E0	2.036E-12	Reset	i	PRBS 7-	bit 🗸				1
% Link 2		MGT X0Y6/RX	6.413 Gbps	4.913E11	1E0	2.035E-12	Reset	í	PRBS 7-	bit 🗸				
% Link 3		MGT X0Y7/RX	6.416 Gbps	4.913E11	1E0	2.035E-12	Reset	1	PRBS 7	bit 🗸				
% Link 4		MGT X0Y8/RX	6.391 Gbps	4.913E11	1E0	2.035E-12	Reset	í	PRBS 7-	bit 🗸				
% Link 5		MGT X0Y9/RX	6.416 Gbps	4.913E11	1E0	2.035E-12	Reset	1	PRBS 7	bit 🗸				
Solution of the second seco							Reset	Multiple	PRBS 7-	bit 🗸	Multiple	Multiple	Multiple	V
% Link 93 0	MGT X0Y6/TX	MGT X1Y4/RX	6.400 Gbps	5.103E11	1E0	1.96E-12	Reset	PRBS 7-bit	V PRBS 7-	bit 🗸	0.00 dB (00000) 🗸	6.02 dB (10100) v	846 mV (11000) v	
% Link 94	MGT X0Y6/TX	MGT X1Y5/RX	6.400 Gbps	5.103E11	1E0	1.96E-12	Reset	PRBS 7-bit	V PRBS 7-	bit 🗸	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100) 🗸	
% Link 95	MGT X0Y7/TX	MGT X1Y6/RX	6.400 Gbps	5.103E11	1E0	1.96E-12	Reset	PRBS 7-bit	V PRBS 7-	bit 🗸	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000) 🗸	
% Link 96 0	MGT X0Y7/TX	MGT X1Y7/RX	6.400 Gbps	5.103E11	1E0	1.96E-12	Reset	PRBS 7-bit	V PRBS 7-	bit 🗸	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100) 🗸	1
% Link 97 0	MGT X0Y8/TX	MGT X1Y8/RX	6.400 Gbps	5.103E11	1E0	1.96E-12	Reset	PRBS 7-bit	V PRBS 7-	bit 🗸	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000) 🗸	
% Link 98 0	MGT X0Y8/TX	MGT X1Y9/RX	6.400 Gbps	5.103E11	1E0	1.96E-12	Reset	PRBS 7-bit	V PRBS 7-	bit 🗸	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100) 🗸	
% Link 101		MGT X0Y37/R	6.400 Gbps	5.103E11	0E0	1.96E-12	Reset	1	PRBS 7-	bit 🗸				
% Link 102	MGT X0Y0/TX	MGT X0Y36/R	6.400 Gbps	5.103E11	0E0	1.96E-12	Reset	PRBS 7-bit	V PRBS 7-	bit 🗸	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100) 🗸	
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7.5 IBERT (eye diagram); MiniPods, test@9.6Gbps:



7.6 IBERT Slot no 4, this test@6.4Gbps covered the area:

- 6 lanes of MGT data from the FEX slot 4

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Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	1	RX Pattern	Т	X Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enable
Ungrouped Links (0)															
v lub: Readout Control Data from This Rod (1)							Reset	1	1	PRBS 7-bit	~				
% Link 0		MGT X0Y3/RX	6.413 Gbps	1.537E13	0E0	6.506E-14	Reset	ī		PRBS 7-bit	~				1
Section 4 Sec							Reset	1	1	PRBS 7-bit	~				
% Link 1		MGT X0Y0/RX	6.413 Gbps	1.536E13	0E0	6.508E-14	Reset	ī		PRBS 7-bit	~				1
% Link 2		MGT_X0Y1/RX	6.417 Gbps	1.536E13	0E0	6.508E-14	Reset	1		PRBS 7-bit	~				1
% Link 3		MGT X0Y2/RX	6.413 Gbps	1.536E13	0E0	6.508E-14	Reset	ī	1	PRBS 7-bit	~				
% Link 4		MGT X0Y0/RX	6.413 Gbps	1.536E13	0E0	6.508E-14	Reset	Ĩ		PRBS 7-bit	~				
✓		-					Reset	PRBS 7-bit	~ 1	PRBS 7-bit	~ 0	√ (00000) Bb 00.	6.02 dB (10100) 🗸	846 mV (11000) ↓	
% Link 74	MGT X0Y38/T	X MGT X0Y38/R	6.413 Gbps	1.536E13	0E0	6.509E-14	Reset	PRBS 7-bit	~ 1	PRBS 7-bit	~ 0	.00 dB (00000) ↓	6.02 dB (10100) 🗸	846 mV (11000) 🗸	
% Link 76	MGT X0Y39/T	X MGT X0Y39/R	6.415 Gbps	1.536E13	0E0	6.509E-14	Reset	PRBS 7-bit	~ 1	PRBS 7-bit	~ 0	v (00000) Bb 00.	6.02 dB (10100) 🗸	846 mV (11000) v	
		_					Reset	ī		PRBS 7-bit	~				
% Link 2		MGT X0Y1/RX	6.417 Gbps	1.537E13	0E0	6.505E-14	Reset	1		PRBS 7-bit	~				
 S HUB: Data from FEX 4 (6) 							Reset	1		PRBS 7-bit	~				I
% Link 0		MGT_X0Y2/BX	6,413 Gbps	1.537E13	3E0	1.952E-13	Reset	ī		PRBS 7-bit	~				
S Link 1		MGT X0Y3/BX	6.413 Gbps	1.537E13	3E0	1.952E-13	Reset	1		PRBS 7-bit	~				
% Link 2		MGT_X0Y14/R	6.413 Gbps	1.537E13	3E0	1.952E-13	Reset	ī		PRBS 7-bit	~				
% Link 3		MGT_X0Y15/8	6.413 Gbps	1.537E13	3E0	1.952E-13	Reset	1		PRBS 7-bit	~				
% Link 4		MGT_X0Y16/B)	6.419 Gbps	1.537E13	3E0	1.952E-13	Reset	1	-	PBBS 7-bit	~				
S Link 5		MGT_X0Y17/8	6.415 Gbps	1.537E13	3E0	1.952E-13	Reset	1		PRBS 7-bit	~				
Solution Sector Sect							Reset	Multiple		PRBS 7-bit	V M	lultiple	Multiple	Multiple	
% Link 99 0	MGT X0V9/TX	MGT X1 X1 0/B)	6.400 Gbps	1.193E13	3E0	2.516E-13	Reset	PBBS 7-bit	~ 1	PBBS 7-bit	~ 0	00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000)	
% Link 100.0	MGT YOV9/TY	MGT X1V11/8	6 400 Gbps	1.193E13	3E0	2.516E-13	Reset	PBBS 7-bit	~ 1	PRBS 7-bit	~ 0	00 dB (00000) 🗸	0.00 dB (00000) v	950 mV (1100)	
% Link 101.0	MGT X0V10/	X MGT X1 Y1 2/8)	6.400 Gbps	1.193E13	3E0	2.516E-13	Reset	PBBS 7-bit	~ 1	PBBS 7-bit	~ 0	.00 dB (00000) 🗸	6.02 dB (10100) v	846 mV (11000)	
% Link 102 0	MGT_X0V10/T	X MGT X1 X1 3/8)	6.400 Gbps	1.193E13	3E0	2.516E-13	Reset	PBBS 7-bit	· ·	PRBS 7-bit	v 0	00 dB (00000) 🗸	0.00 dB (00000) v	950 mV (1100)	
% Link 103	MGT_X0Y11/T	X MGT_X1Y14/8)	6.400 Gbps	1.193E13	3E0	2.516E-13	Reset	PBBS 7-bit	÷ 1	PBBS 7-bit	~ 0	.00 dB (00000) 🗸	6.02 dB (10100) v	846 mV (11000)	
% Link 104	MGT_X0V11/T	X MGT_X1114/10	6.400 Gbps	1.193E13	3E0	2.516E-13	Reset	PBBS 7-bit	· ·	PBBS 7-bit	v 0	00 dB (00000)	0.00 dB (00000) v	950 mV (11000)	· Z
% Link 101	MO1_X0111/1	MGT X0X37/8)	6 400 Gbps	1.193E13	0E0	8 385E-14	Reset			PBBS 7-bit	-		0.00 00 (00000) +	550 mv (1100)	×
% Link 102	MGT YOYOTTY	MGT_X0Y26/P)	6 400 Gbps	1 193513	0E0	8 385E-14	Reset	PBBS 7-bit		PBBS 7-bit	× 0	00 dB (00000) 😽	0.00 dB (00000) 😽	950 mV (1100)	
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Link Group: ROD: Data from FEX_4 and 2 Links from HU	JB														
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7.7 IBERT (eye diagram); FEX slot 4, test@6.4 Gbps:



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7.8 IBERT Slot no 5, this test@6.4Gbps covered the area:

- 6 lanes of MGT data from the FEX slot 5

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Name	TX	BX	Status	Bits	Errors	BEB	BERT Reset	TX Pattern	RX P	attern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DEE Enable
Ungrouped Links (0)														
✓ S HUB: Readout Control Data from This Rod (1)							Reset	1	PRBS	57-bit √				
% Link 0		MGT X0Y3/RX	6.413 Gbps	1.951E13	0E0	5.127E-14	Reset	í	PRBS	57-bit √				
V & HUB: MiniPods (4)							Reset	1	PRBS	57-bit √				
% Link 1		MGT X0Y0/RX	6.413 Gbps	1.949E13	0E0	5.13E-14	Reset	í	PRBS	5.7-bit √				
% Link 2		MGT X0Y1/RX	6.413 Gbps	1.95E13	0E0	5.129E-14	Reset	i	PRBS	57-bit √				
% Link 3		MGT X0Y2/RX	6.413 Gbps	1.949E13	0E0	5.131E-14	Reset	i	PRBS	5.7-bit √				
Sh Link 4		MGT X0Y0/BX	6.413 Gbps	1.949E13	0E0	5.131E-14	Reset	i	PRBS	57-bit 🗸				
✓ ♣ HUB: Other Hub RO (2)							Reset	PRBS 7-bit	V PRBS	5 7-bit √	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000) 🗸	
% Link 74	MGT X0Y38/D	MGT X0Y38/R	6.408 Gbps	8.247E12	0E0	1.213E-13	Reset	PRBS 7-bit	V PRBS	57-bit √	0.00 dB (00000) 🗸	6.02 dB (10100) v	846 mV (11000) v	
% Link 76	MGT X0Y39/D	MGT X0Y39/8	6.413 Gbps	8.247E12	0E0	1.213E-13	Reset	PRBS 7-bit	V PRBS	s 7-bit ∨	0.00 dB (00000) v	6.02 dB (10100) v	846 mV (11000) v	
							Reset	1	PRBS	57-bit 🗸				
% Link 2		MGT_X0Y1/BX	6,415 Gbps	8.242E12	0E0	1.213E-13	Reset	1	PRBS	5.7-bit ∨				
Solution of the second seco							Reset	1	PRBS	5 7-bit 🗸				
Sh Link 0		MGT X0YL0/B)	6.413 Gbps	8.255E12	1E0	1.211E-13	Reset	i	PRBS	57-bit 🗸				
S Link 1		MGT X0Y11/8	6.413 Gbps	8.255E12	1E0	1.211E-13	Reset	1	PRBS	s 7-bit ∨				
% Link 2		MGT X0Y12/B	6.413 Gbps	8.255E12	1E0	1.211E-13	Reset	1	PBBS	5.7-bit 🗸				
% Link 3		MGT_X0Y13/80	6.411 Gbps	8.255E12	1E0	1.211E-13	Reset	1	PRBS	s 7-bit ∨				
S Link 4		MGT X0Y24/B	6.413 Gbps	8.255E12	1E0	1.211E-13	Reset	1	PBBS	5.7-bit 🗸				
% Link 5		MGT_X0Y25/80	6.413 Gbps	8.255E12	1E0	1.211E-13	Reset	1	PRBS	s7-bit ∨				
							Reset	Multiple	PRBS	s 7-bit 🗸	Multiple	Multiple	Multiple	
% Link 105	MGT X0Y12/D	MGT X1 Y1 6/80	6.400 Gbps	8.276E12	1E0	1.208E-13	Reset	PRBS 7-bit	V PRBS	57-bit √	0.00 dB (00000) v	6.02 dB (10100) v	846 mV (11000) v	
% Link 106	MGT X0Y12/D	MGT X1 Y1 7/8)	6.400 Gbps	8.276E12	1E0	1.208E-13	Reset	PRBS 7-bit	V PRBS	s 7-bit 🗸	0.00 dB (00000) V	0.00 dB (00000) 🗸	950 mV (1100) v	
% Link 107	MGT_X0Y13/D	MGT X1Y18/8	6.400 Gbps	8.276E12	1E0	1.208E-13	Reset	PRBS 7-bit	V PRBS	57-bit 🗸	0.00 dB (00000) v	6.02 dB (10100) v	846 mV (11000) v	
% Link 108	MGT_X0Y13/D	(MGT_X1Y19/8)	6.400 Gbps	8.275E12	1E0	1.208E-13	Reset	PRBS 7-bit	V PRBS	s 7-bit ∨	0.00 dB (00000) v	0.00 dB (00000) v	950 mV (1100) v	
% Link 109	MGT X0Y14/D	MGT X1 Y20/8	6.400 Gbps	8.275E12	1E0	1.208E-13	Reset	PBBS 7-bit	V PBBS	5.7-bit 🗸	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000) ~	
% Link 110	MGT X0V14/T	(MGT_X1 V21/B)	6.400 Gbps	8.275E12	1E0	1.208E-13	Reset	PBBS 7-bit	V PRB	5.7-bit 🗸	0.00 dB (00000) v	0.00 dB (00000) v	950 mV (1100)	
% Link 101		MGT_X0Y37/B)	6.400 Gbps	8.256E12	0E0	1.208E-13	Reset]	PRBS	s 7-bit 🗸				
% Link 102	MGT X0Y0/TX	MGT_X0X36/B)	6.400 Gbps	8.275E12	0E0	1.208E-13	Reset	PBBS 7-bit	V PBB	5.7-bit 🗸	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100)	
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7.9 IBERT Slot no 6, this test@6.4Gbps covered the area:

- 6 lanes of MGT data from the FEX slot 6

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Ungrouped Links (0)														-	
							Reset			PRBS 7-bit	~				1
% Link 0		MGT_X0Y3/RX	6.413 Gbps	3.682E14	0E0	2.716E-15	Reset			PRBS 7-bit	~				1
							Reset			PRBS 7-bit	~				1
% Link 1		MGT_X0Y0/RX	6.402 Gbps	3.682E14	0E0	2.716E-15	Reset			PRBS 7-bit	~				1
% Link 2		MGT_X0Y1/RX	6.404 Gbps	3.682E14	0E0	2.716E-15	Reset			PRBS 7-bit	~				1
% Link 3		MGT_X0Y2/RX	6.413 Gbps	3.682E14	0E0	2.716E-15	Reset]		PRBS 7-bit	~				1
🗞 Link 4		MGT_X0Y0/RX	6.413 Gbps	3.682E14	0E0	2.716E-15	Reset			PRBS 7-bit	~				1
							Reset	PRBS 7-bit	~	PRBS 7-bit	~	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV(11000) ↓	1
% Link 74	MGT_X0Y38/T	X MGT_X0Y38/RX	6.412 Gbps	3.682E14	0E0	2.716E-15	Reset	PRBS 7-bit	\sim	PRBS 7-bit	~	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000) 🗸	1
No. Link 76	MGT_X0Y39/T	X MGT_X0Y39/RX	6.413 Gbps	3.682E14	0E0	2.716E-15	Reset	PRBS 7-bit	~	PRBS 7-bit	~	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000) 🗸	1
							Reset			PRBS 7-bit	~				1
% Link 2		MGT_X0Y1/RX	6.413 Gbps	3.682E14	0E0	2.716E-15	Reset			PRBS 7-bit	~				1
4 4 HUB: Data from FEX_6 (6)							Reset			PRBS 7-bit	~				1
% Link 0		MGT_X0Y20/RX	6.413 Gbps	3.632E14	0E0	2.753E-15	Reset			PRBS 7-bit	~				1
% Link 1		MGT_X0Y21/RX	6.413 Gbps	3.632E14	0E0	2.753E-15	Reset			PRBS 7-bit	~				1
% Link 2		MGT_X0Y22/RX	6.413 Gbps	3.632E14	0E0	2.753E-15	Reset			PRBS 7-bit	~				1
% Link 3		MGT_X0Y23/RX	6.413 Gbps	3.632E14	0E0	2.753E-15	Reset			PRBS 7-bit	~				1
% Link 4		MGT_X0Y19/RX	6.413 Gbps	3.632E14	0E0	2.753E-15	Reset	7		PRBS 7-bit	~				1
% Link 5		MGT_X0Y18/RX	6.413 Gbps	3.632E14	0E0	2.753E-15	Reset	1		PRBS 7-bit	~				1
% ROD: Data from FEX_6 and 2 Links from H							Reset	Multiple		PRBS 7-bit	~	Multiple	Multiple	Multiple	1
% Link 111	MGT_X0Y15/T	X MGT_X1Y22/RX	6.400 Gbps	3.632E14	0E0	2.753E-15	Reset	PRBS 7-bit	~	PRBS 7-bit	~	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV(11000) ↓	1
% Link 112	MGT_X0Y15/T	X MGT_X1Y23/RX	6.400 Gbps	3.632E14	0E0	2.753E-15	Reset	PRBS 7-bit	~	PRBS 7-bit	~	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100) 🗸	1
-	MGT X0Y16/T	X MGT_X1Y24/RX	6.400 Gbps	3.632E14	0E0	2.753E-15	Reset	PRBS 7-bit	\sim	PRBS 7-bit	~	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV(11000) 🗸	1
% Link 113			6.400 Gbps	3.632E14	0E0	2.753E-15	Reset	PRBS 7-bit	~	PRBS 7-bit	~	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100) ∽	1
% Link 113 % Link 114	MGT_X0Y16/T	X MGT_X1Y25/RX	and a second sec				-	-		DDDD DLU					
୍ତ୍ତି Link 113 ୧୦ Link 114 ୧୦ Link 115	MGT_X0Y16/T MGT_X0Y17/T	X MGT_X1Y25/RX X MGT_X1Y26/RX	6.400 Gbps	3.632E14	0E0	2.753E-15	Reset	PRBS 7-bit	~	PRBS /-DIt	~	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000) ↓	1
֊ Աink 113 Գ Link 114 Գ Link 115 Գ Link 116	MGT_X0Y16/T MGT_X0Y17/T MGT_X0Y17/T	X MGT_X1Y25/RX X MGT_X1Y26/RX X MGT_X1Y27/RX	6.400 Gbps 6.400 Gbps	3.632E14 3.632E14	0E0 0E0	2.753E-15 2.753E-15	Reset	PRBS 7-bit PRBS 7-bit	~	PRBS 7-bit PRBS 7-bit	~	0.00 dB (00000) v 0.00 dB (00000) v	6.02 dB (10100) v 0.00 dB (00000) v	846 mV (11000) ↓ 950 mV (1100) ↓	1
ବ୍ଧ Link 113 ବ୍ୟୁ Link 114 ବ୍ୟୁ Link 115 ବ୍ୟୁ Link 116 ବ୍ୟୁ Link 101	MGT_XOY16/T MGT_XOY17/T MGT_XOY17/T	X MGT_X1Y25/RX X MGT_X1Y26/RX X MGT_X1Y27/RX MGT_X0Y37/RX	6.400 Gbps 6.400 Gbps 6.400 Gbps	3.632E14 3.632E14 3.632E14	0E0 0E0 0E0	2.753E-15 2.753E-15 2.753E-15	Reset Reset Reset	PRBS 7-bit PRBS 7-bit	~	PRBS 7-bit PRBS 7-bit PRBS 7-bit	* * *	0.00 dB (00000) ~ 0.00 dB (00000) ~	6.02 dB (10100) ↓ 0.00 dB (00000) ↓	846 mV (11000) ↓ 950 mV (1100) ↓	✓ ✓ ✓

8.0 IBERT Slot no 7, this test@6.4Gbps covered the area:

- 6 lanes of MGT data from the FEX slot 7

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						Reset	PRBS 7-bit	PRBS 7	bit 🗸	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100)	~	2
	MGT X0Y3/BX	6.417 Gbps	2.102E13	0E0	4.757E-14	Reset	PBBS 7-bit	PBBS 7	bit 🗸	0.00 dB (00000) ~	0.00 dB (00000) 🗸	950 mV (1100)	~	
						Reset	PBBS 7-bit	PBBS 7	bit 🗸	0.00 dB (00000)	Multiple	Multiple		
	MGT X0Y0/PY	6.413 Gbps	2.276E13	050	4.394E-14	Reset]	PBBS 7	bit 🛩					
	MGT YOV1/PV	6.413 Ghps	2.276E13	050	4.394E-14	Reset	PBBS 7-bit	PRBS 7	bit 😔	0.00 dB (00000) 🐱	0.00 dB (00000) 🛩	950 mV (1100)	~	
	MGT YOY2/PY	6.425 Ghps	2 276613	050	4 304E-14	Reset	PRBS 7-bit	PRBS 7	hit w	0.00 dB (00000) v	0.00 dB (00000)	950 mV (1100)	-	
	MGT_X0T2/RX	6.417 Chos	2.270E13	050	4.3946-14	Reset	DDDC 7 hit	PDDC 7	bit 🗸	0.00 dB (00000) 👳	6.00 dB (00000) V	930 mV (1100)	~	
	MG1_X010/KX	0.417 Obps	2.270015	020	4.5540-14	Reset	PRPS 7 bit	. DDDC 7	hit	0.00 dB (00000) ++	6.02 dB (10100) v	846 mV(11000)	×	¥
		C 400 Chas	0.10510	050	4.5.665.1.4	Reset	PRBS 7-DIL	PR85 /		0.00 dB (00000) 🗸	6.02 dB (10100) V	846 mV (11000)	~	¥
_X0Y38/1X	MGT_X0Y38/RX	6.409 Gbps	2.19E13	OEU	4.500E-14	Reset	PRBS 7-DIL	PRBS /		0.00 dB (00000) 🗸	6.02 dB (10100) V	846 mV (11000)	~	2
_X0Y39/1X	MG1_X0Y39/HX	6.404 Gbps	2.128E13	OEU	4./E-14	Reset	PRBS 7-DIt	PRBS 7	DIT 🗸	0.00 dB (00000) V	6.02 dB (10100) V	846 mV (11000)	~	~
						Reset	PRBS 7-DIC	PRBS 7	DIT 🗸	0.00 dB (00000) ~	6.02 dB (10100) V	846 mV (11000)	~	~
r_xoy1/tx	MGT_X0Y1/RX	6.413 Gbps	2.016E13	0E0	4.961E-14	Reset	PRBS 7-bit	PRBS 7	bit 🗸	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000)	~	~
						Reset]	PRBS 7	bit 🗸					~
	MGT_X0Y32/RX	6.413 Gbps	2.131E13	0E0	4.692E-14	Reset]	PRBS 7	bit 🗸					4
	MGT_X0Y33/RX	6.409 Gbps	2.131E13	0E0	4.692E-14	Reset]	PRBS 7	bit 🗸					1
	MGT_X0Y34/RX	6.393 Gbps	2.131E13	0E0	4.692E-14	Reset]	PRBS 7	bit 🗸					4
	MGT_X0Y35/RX	6.427 Gbps	2.131E13	0E0	4.692E-14	Reset]	PRBS 7	bit 🗸					1
	MGT_X0Y28/RX	6.413 Gbps	2.131E13	0E0	4.692E-14	Reset]	PRBS 7	bit 🗸					V
	MGT_X0Y29/RX	6.422 Gbps	2.131E13	0E0	4.692E-14	Reset]	PRBS 7	bit 🗸					1
						Reset	Multiple	PRBS 7	bit 🗸	Multiple	Multiple	Multiple		1
	MGT_X1Y28/RX	6.400 Gbps	2.136E13	0E0	4.681E-14	Reset	PRBS 7-bit	PRBS 7	bit 🗸	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100)	~	1
- X0Y21/TX	MGT X1Y29/RX	6.400 Gbps	2.136E13	0E0	4.681E-14	Reset	PRBS 7-bit	PRBS 7	bit 🗸	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000)	~	1
- x0y21/tx	MGT X1Y30/RX	6.400 Gbps	2.136E13	0E0	4.681E-14	Reset	PRBS 7-bit	PRBS 7	bit 🗸	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100)	~	1
X0Y22/TX	MGT X1Y31/RX	6.400 Gbps	2.136E13	0E0	4.681E-14	Reset	PRBS 7-bit	PRBS 7	bit 🗸	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000)	~	2
- x0y22/TX	MGT X1Y32/BX	6.400 Gbps	2.136E13	0E0	4.681E-14	Reset	PRBS 7-bit	PRBS 7	bit 🗸	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100)	~	2
X0Y23/TX	MGT X1Y33/BX	6.400 Gbps	2.136E13	0E0	4.681E-14	Reset	PRBS 7-bit	PRBS 7	bit 🗸	0.00 dB (00000) 🗸	6.02 dB (10100) v	846 mV (11000)	~	2
	MGT Y0Y37/BY	6.400 Gbps	2.136E13	0E0	4.681E-14	Reset	1	PBBS 7	bit 🗸					
-			2 1 26 5 1 2	0E0	4.681E-14	Reset	PBBS 7-bit	PRBS 7	hit v	0.00 dB (00000) ++	0.00 40 (00000)	050 m)/(1100)		
	rial 1/0 1 2013/7 2010/7 2013/	RX RX MGT_X0Y3/RX MGT_X0Y3/RX MGT_X0Y3/RX MGT_X0Y3/RX X0Y3/TX MGT_X0Y3/RX X0Y3/RX MGT_X0Y3/RX X0Y3/RX MGT_X0Y3/RX X0Y3/RX MGT_X0Y3/RX X0Y3/RX MGT_X0Y3/RX X0Y2/X/K MGT_X1Y3/RX X0Y2/X/K MGT_X1Y3/RX X0Y2/X MGT_X1Y3/RX X0Y2/X MGT_X1Y3/RX </th <th>Frial I/O Scans RX Status RX Status X0Y3/TX MGT_X0Y3/RX 6.417 Gbps MGT_X0Y3/RX 6.413 Gbps X0Y1/TX MGT_X0Y3/RX 6.413 Gbps X0Y2/TX MGT_X0Y3/RX 6.425 Gbps X0Y2/TX MGT_X0Y3/RX 6.425 Gbps X0Y3/RX MGT_X0Y3/RX 6.426 Gbps X0Y3/RX MGT_X0Y3/RX 6.404 Gbps X0Y1/TX MGT_X0Y3/RX 6.427 Gbps MGT_X0Y3/RX 6.403 Gbps MGT_X0Y3/RX MGT_X0Y3/RX 6.422 Gbps MGT_X0Y3/RX MGT_X0Y3/RX 6.422 Gbps MGT_X0Y3/RX MGT_X0Y3/RX 6.422 Gbps MGT_X0Y2/RX MGT_X0Y2/RX 6.422 Gbps MGT_X0Y2/RX MGT_X0Y2/RX 6.422 Gbps MGT_X0Y2/RX MGT_X0Y2/RX 6.422 Gbps MGT_X0Y2/RX MGT_X0Y2/RX 6.422 Gbps MGT_X0Y2/RX X0Y2/T/X MGT_X1Y2/RX 6.400 Gbps X0Y2/T/X MGT_X1Y3/RX 6.400 Gbps X0Y2/T/X MGT_X1Y3/RX</th> <th>RX Status Bits RX Status Bits x0Y3/TX MGT_X0Y3/RX 6.417 Gbps 2.102E13 x0Y3/TX MGT_X0Y3/RX 6.413 Gbps 2.276E13 x0Y1/TX MGT_X0Y3/RX 6.413 Gbps 2.276E13 x0Y2/TX MGT_X0Y3/RX 6.426 Gbps 2.276E13 x0Y2/TX MGT_X0Y3/RX 6.426 Gbps 2.276E13 x0Y3/RX MGT_X0Y3/RX 6.406 Gbps 2.19E13 x0Y3/RX MGT_X0Y3/RX 6.404 Gbps 2.12E13 x0Y1/TX MGT_X0Y3/RX 6.413 Gbps 2.131E13 MGT_X0Y3/RX 6.404 Gbps 2.131E13 2.131E13 MGT_X0Y3/RX 6.403 Gbps 2.131E13 2.131E13 MGT_X0Y3/RX 6.402 Gbps 2.131E13 2.131E13 MGT_X0Y3/RX 6.400 Gbps 2.131E13 2.131E13 MGT_X0Y3/RX 6.400 Gbps 2.136E13 2.136E13 X0Y2/RX MGT_X1Y3/RX 6.400 Gbps 2.136E13 X0Y2/RX MGT_X1Y3/RX 6.400 Gbps</th> <th>RX Status Bits Errors X0Y3/TX MGT_X0Y3/RX 6.417 Gbps 2.102E13 0E0 MGT_X0Y3/RX 6.417 Gbps 2.102E13 0E0 X0Y3/TX MGT_X0Y3/RX 6.413 Gbps 2.276E13 0E0 X0Y3/TX MGT_X0Y3/RX 6.413 Gbps 2.276E13 0E0 X0Y3/TX MGT_X0Y3/RX 6.425 Gbps 2.276E13 0E0 X0Y3/TX MGT_X0Y3/RX 6.426 Gbps 2.19E13 0E0 X0Y3/TX MGT_X0Y3/RX 6.404 Gbps 2.128E13 0E0 X0Y3/TX MGT_X0Y3/RX 6.403 Gbps 2.131E13 0E0 X0Y1/TX MGT_X0Y3/RX 6.413 Gbps 2.131E13 0E0 MGT_X0Y3/RX 6.403 Gbps 2.131E13 0E0 0E0 0MGT_X0Y3/RX 6.413 Gbps 2.131E13 0E0 MGT_X0Y3/RX 6.427 Gbps 2.131E13 0E0 0E0 0MGT_X0Y2/RX 6.427 Gbps 2.131E13 0E0 0X072/RX 0E0 X0Y2/RX 6.422 Gbps 2.131E13 0E0</th> <th>RX Status Bits Errors BER X0Y3/TX MGT_X0Y3/RX 6.417 Gbps 2.102E13 0E0 4.757E-14 X0Y3/TX MGT_X0Y3/RX 6.417 Gbps 2.102E13 0E0 4.394E-14 X0Y1/TX MGT_X0Y3/RX 6.413 Gbps 2.276E13 0E0 4.394E-14 X0Y2/TX MGT_X0Y3/RX 6.425 Gbps 2.276E13 0E0 4.394E-14 X0Y2/TX MGT_X0Y3/RX 6.425 Gbps 2.276E13 0E0 4.394E-14 X0Y3/RX MGT_X0Y3/RX 6.425 Gbps 2.19E13 0E0 4.566E-14 X0Y3/RX MGT_X0Y3/RX 6.404 Gbps 2.19E13 0E0 4.692E-14 X0Y1/TX MGT_X0Y3/RX 6.403 Gbps 2.131E13 0E0 4.692E-14 MGT_X0Y3/RX 6.403 Gbps 2.131E13 0E0 4.692E-14 MGT_X0Y3/RX 6.402 Gbps 2.131E13 0E0 4.692E-14 MGT_X0Y3/RX 6.402 Gbps 2.131E13 0E0 4.692E-14 MGT_X0Y2/RX 6.402 Gbps</th> <th>RX Status Bits Errors BER BERT Reset X0Y3/TX MGT_X0Y3/RX 6.417 Gbps 2.102E13 0E0 4.757E-14 Reset X0Y3/TX MGT_X0Y3/RX 6.413 Gbps 2.102E13 0E0 4.757E-14 Reset X0Y1/TX MGT_X0Y3/RX 6.413 Gbps 2.276E13 0E0 4.394E-14 Reset X0Y1/TX MGT_X0Y3/RX 6.425 Gbps 2.276E13 0E0 4.394E-14 Reset X0Y2/TX MGT_X0Y3/RX 6.425 Gbps 2.276E13 0E0 4.394E-14 Reset X0Y2/TX MGT_X0Y3/RX 6.425 Gbps 2.276E13 0E0 4.394E-14 Reset X0Y3/RX MGT_X0Y3/RX 6.413 Gbps 2.19E13 0E0 4.566E-14 Reset X0Y1/TX MGT_X0Y3/RX 6.413 Gbps 2.19E13 0E0 4.692E-14 Reset X0Y1/TX MGT_X0Y3/RX 6.400 Gbps 2.131E13 0E0 4.692E-14 Reset MGT_X0Y3/RX 6.492 Gbps 2.131E13 0E</th> <th>RX Status Bits Errors BER BERT Reset TX Pattern X0Y3/TX MGT_X0Y3/RX 6.417 Gbps 2.102E13 0E0 4.757E-14 PR8s PR85 7-bit X0Y3/TX MGT_X0Y3/RX 6.413 Gbps 2.276E13 0E0 4.94E-14 PR8s PR85 7-bit X0Y1/TX MGT_X0Y0/RX 6.413 Gbps 2.276E13 0E0 4.94E-14 Reset PR85 7-bit X0Y2/TX MGT_X0Y0/RX 6.425 Gbps 2.276E13 0E0 4.94E-14 Reset PR85 7-bit X0Y2/TX MGT_X0Y0/RX 6.425 Gbps 2.276E13 0E0 4.94E-14 Reset PR85 7-bit X0Y3/TX MGT_X0Y3/RX 6.426 Gbps 2.19E13 0E0 4.56E-14 Reset PR85 7-bit X0Y3/R/X MGT_X0Y3/RX 6.403 Gbps 2.19E13 0E0 4.961E-14 Reset PR85 7-bit X0Y3/R/X MGT_X0Y3/RX 6.403 Gbps 2.13E13 0E0 4.692E-14 Reset PR85 7-bit X0Y3/R/X 6.403 Gbps<</th> <th>RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern X0Y3/TX MGT_X0Y3/RX 6.417 Gbps 2.102E13 0E0 4.757E-14 Reset PRBS 7-bit P PRBS 7-bit</th> <th>RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern X0Y3/TX MGT_X0Y3/RX 6.417 Gbps 2.102E13 0E0 4.757E14 Reset PR85 7-bit > PR85 7-bit ><th>RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern TX Pre-Cursor x0Y3/TX MGT_X0Y3/RX 6.417 Gbps 2.102E13 0E0 4.757E14 Reset PR85 7-bit > 0.00 dB (00000) > MGT_X0Y3/RX 6.413 Gbps 2.276E13 0E0 4.394E14 Reset PR85 7-bit > 0.00 dB (00000) > X0Y3/TX MGT_X0Y3/RX 6.423 Gbps 2.276E13 0E0 4.394E14 Reset PR85 7-bit > 0.00 dB (00000) > X0Y2/TX MGT_X0Y3/RX 6.423 Gbps 2.276E13 0E0 4.394E14 Reset PR85 7-bit > 0.00 dB (00000) > X0Y2/TX MGT_X0Y3/RX 6.425 Gbps 2.276E13 0E0 4.394E14 Reset PR85 7-bit > 0.00 dB (00000) > X0Y3/RX 6.425 Gbps 2.276E13 0E0 4.394E14 Reset PR85 7-bit > 0.00 dB (00000) > X0Y3/RX 6.403 Gbps 2.19E13 0E0 4.566E144 Reset PR85 7-bi</th><th>RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern TX Pre-Cursor TX Post-Cursor x0Y3/TX MGT_X0Y3/RX 6.417 Gbps 2.102E13 0E0 4.757E14 Reset PR85 7-bit > 0.00 dB (00000) > 0.00 dB (000000) > 0.00 dB (000</th><th>RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern TX Pre-Cursor TX Post-Cursor TX Diff Swing x0Y3/TX MGT_X0Y3/R0 6.417 Gbps 2.102E13 OE0 4.757E14 Reset PRBS 7-bit > PRBS 7-bit > 0.00 dB (00000) 0.00 dB (00000) 0.00 dB (00000) 950 mV (1100) MGT_X0Y3/RX 6.417 Gbps 2.102E13 OE0 4.394E14 Reset PRBS 7-bit > PRBS 7-bit > 0.00 dB (00000) 0.00 dB (00000) 950 mV (1100) WGT_X0Y3/RX 6.413 Gbps 2.276E13 OE0 4.394E14 Reset PRBS 7-bit > PRBS 7-bit > 0.00 dB (00000) 0.00 dB (00000) 950 mV (1100) X0Y1/TX MGT_X0Y3/RX 6.425 Gbps 2.276E13 OE0 4.394E14 Reset PRBS 7-bit > PRBS 7-bit > 0.00 dB (00000) 0.00 dB (00000) 0.00 dB (00000) 6.02 dB (1010) \$46 mV (11000) X0Y3/RX A6.17 Gbps 2.19E13 OE0 4.56E14 Reset PRBS 7-bit > PRBS 7-bit 0.00 dB (000000) 6.02 dB (10</th><th>Prial I/O Scans Prial I/O Scans TX Pattern TX Pattern TX Pre-Cursor TX Polt-Cursor TX Diff Swing <</th></th>	Frial I/O Scans RX Status RX Status X0Y3/TX MGT_X0Y3/RX 6.417 Gbps MGT_X0Y3/RX 6.413 Gbps X0Y1/TX MGT_X0Y3/RX 6.413 Gbps X0Y2/TX MGT_X0Y3/RX 6.425 Gbps X0Y2/TX MGT_X0Y3/RX 6.425 Gbps X0Y3/RX MGT_X0Y3/RX 6.426 Gbps X0Y3/RX MGT_X0Y3/RX 6.404 Gbps X0Y1/TX MGT_X0Y3/RX 6.427 Gbps MGT_X0Y3/RX 6.403 Gbps MGT_X0Y3/RX MGT_X0Y3/RX 6.422 Gbps MGT_X0Y3/RX MGT_X0Y3/RX 6.422 Gbps MGT_X0Y3/RX MGT_X0Y3/RX 6.422 Gbps MGT_X0Y2/RX MGT_X0Y2/RX 6.422 Gbps MGT_X0Y2/RX MGT_X0Y2/RX 6.422 Gbps MGT_X0Y2/RX MGT_X0Y2/RX 6.422 Gbps MGT_X0Y2/RX MGT_X0Y2/RX 6.422 Gbps MGT_X0Y2/RX X0Y2/T/X MGT_X1Y2/RX 6.400 Gbps X0Y2/T/X MGT_X1Y3/RX 6.400 Gbps X0Y2/T/X MGT_X1Y3/RX	RX Status Bits RX Status Bits x0Y3/TX MGT_X0Y3/RX 6.417 Gbps 2.102E13 x0Y3/TX MGT_X0Y3/RX 6.413 Gbps 2.276E13 x0Y1/TX MGT_X0Y3/RX 6.413 Gbps 2.276E13 x0Y2/TX MGT_X0Y3/RX 6.426 Gbps 2.276E13 x0Y2/TX MGT_X0Y3/RX 6.426 Gbps 2.276E13 x0Y3/RX MGT_X0Y3/RX 6.406 Gbps 2.19E13 x0Y3/RX MGT_X0Y3/RX 6.404 Gbps 2.12E13 x0Y1/TX MGT_X0Y3/RX 6.413 Gbps 2.131E13 MGT_X0Y3/RX 6.404 Gbps 2.131E13 2.131E13 MGT_X0Y3/RX 6.403 Gbps 2.131E13 2.131E13 MGT_X0Y3/RX 6.402 Gbps 2.131E13 2.131E13 MGT_X0Y3/RX 6.400 Gbps 2.131E13 2.131E13 MGT_X0Y3/RX 6.400 Gbps 2.136E13 2.136E13 X0Y2/RX MGT_X1Y3/RX 6.400 Gbps 2.136E13 X0Y2/RX MGT_X1Y3/RX 6.400 Gbps	RX Status Bits Errors X0Y3/TX MGT_X0Y3/RX 6.417 Gbps 2.102E13 0E0 MGT_X0Y3/RX 6.417 Gbps 2.102E13 0E0 X0Y3/TX MGT_X0Y3/RX 6.413 Gbps 2.276E13 0E0 X0Y3/TX MGT_X0Y3/RX 6.413 Gbps 2.276E13 0E0 X0Y3/TX MGT_X0Y3/RX 6.425 Gbps 2.276E13 0E0 X0Y3/TX MGT_X0Y3/RX 6.426 Gbps 2.19E13 0E0 X0Y3/TX MGT_X0Y3/RX 6.404 Gbps 2.128E13 0E0 X0Y3/TX MGT_X0Y3/RX 6.403 Gbps 2.131E13 0E0 X0Y1/TX MGT_X0Y3/RX 6.413 Gbps 2.131E13 0E0 MGT_X0Y3/RX 6.403 Gbps 2.131E13 0E0 0E0 0MGT_X0Y3/RX 6.413 Gbps 2.131E13 0E0 MGT_X0Y3/RX 6.427 Gbps 2.131E13 0E0 0E0 0MGT_X0Y2/RX 6.427 Gbps 2.131E13 0E0 0X072/RX 0E0 X0Y2/RX 6.422 Gbps 2.131E13 0E0	RX Status Bits Errors BER X0Y3/TX MGT_X0Y3/RX 6.417 Gbps 2.102E13 0E0 4.757E-14 X0Y3/TX MGT_X0Y3/RX 6.417 Gbps 2.102E13 0E0 4.394E-14 X0Y1/TX MGT_X0Y3/RX 6.413 Gbps 2.276E13 0E0 4.394E-14 X0Y2/TX MGT_X0Y3/RX 6.425 Gbps 2.276E13 0E0 4.394E-14 X0Y2/TX MGT_X0Y3/RX 6.425 Gbps 2.276E13 0E0 4.394E-14 X0Y3/RX MGT_X0Y3/RX 6.425 Gbps 2.19E13 0E0 4.566E-14 X0Y3/RX MGT_X0Y3/RX 6.404 Gbps 2.19E13 0E0 4.692E-14 X0Y1/TX MGT_X0Y3/RX 6.403 Gbps 2.131E13 0E0 4.692E-14 MGT_X0Y3/RX 6.403 Gbps 2.131E13 0E0 4.692E-14 MGT_X0Y3/RX 6.402 Gbps 2.131E13 0E0 4.692E-14 MGT_X0Y3/RX 6.402 Gbps 2.131E13 0E0 4.692E-14 MGT_X0Y2/RX 6.402 Gbps	RX Status Bits Errors BER BERT Reset X0Y3/TX MGT_X0Y3/RX 6.417 Gbps 2.102E13 0E0 4.757E-14 Reset X0Y3/TX MGT_X0Y3/RX 6.413 Gbps 2.102E13 0E0 4.757E-14 Reset X0Y1/TX MGT_X0Y3/RX 6.413 Gbps 2.276E13 0E0 4.394E-14 Reset X0Y1/TX MGT_X0Y3/RX 6.425 Gbps 2.276E13 0E0 4.394E-14 Reset X0Y2/TX MGT_X0Y3/RX 6.425 Gbps 2.276E13 0E0 4.394E-14 Reset X0Y2/TX MGT_X0Y3/RX 6.425 Gbps 2.276E13 0E0 4.394E-14 Reset X0Y3/RX MGT_X0Y3/RX 6.413 Gbps 2.19E13 0E0 4.566E-14 Reset X0Y1/TX MGT_X0Y3/RX 6.413 Gbps 2.19E13 0E0 4.692E-14 Reset X0Y1/TX MGT_X0Y3/RX 6.400 Gbps 2.131E13 0E0 4.692E-14 Reset MGT_X0Y3/RX 6.492 Gbps 2.131E13 0E	RX Status Bits Errors BER BERT Reset TX Pattern X0Y3/TX MGT_X0Y3/RX 6.417 Gbps 2.102E13 0E0 4.757E-14 PR8s PR85 7-bit X0Y3/TX MGT_X0Y3/RX 6.413 Gbps 2.276E13 0E0 4.94E-14 PR8s PR85 7-bit X0Y1/TX MGT_X0Y0/RX 6.413 Gbps 2.276E13 0E0 4.94E-14 Reset PR85 7-bit X0Y2/TX MGT_X0Y0/RX 6.425 Gbps 2.276E13 0E0 4.94E-14 Reset PR85 7-bit X0Y2/TX MGT_X0Y0/RX 6.425 Gbps 2.276E13 0E0 4.94E-14 Reset PR85 7-bit X0Y3/TX MGT_X0Y3/RX 6.426 Gbps 2.19E13 0E0 4.56E-14 Reset PR85 7-bit X0Y3/R/X MGT_X0Y3/RX 6.403 Gbps 2.19E13 0E0 4.961E-14 Reset PR85 7-bit X0Y3/R/X MGT_X0Y3/RX 6.403 Gbps 2.13E13 0E0 4.692E-14 Reset PR85 7-bit X0Y3/R/X 6.403 Gbps<	RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern X0Y3/TX MGT_X0Y3/RX 6.417 Gbps 2.102E13 0E0 4.757E-14 Reset PRBS 7-bit P PRBS 7-bit	RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern X0Y3/TX MGT_X0Y3/RX 6.417 Gbps 2.102E13 0E0 4.757E14 Reset PR85 7-bit > PR85 7-bit > <th>RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern TX Pre-Cursor x0Y3/TX MGT_X0Y3/RX 6.417 Gbps 2.102E13 0E0 4.757E14 Reset PR85 7-bit > 0.00 dB (00000) > MGT_X0Y3/RX 6.413 Gbps 2.276E13 0E0 4.394E14 Reset PR85 7-bit > 0.00 dB (00000) > X0Y3/TX MGT_X0Y3/RX 6.423 Gbps 2.276E13 0E0 4.394E14 Reset PR85 7-bit > 0.00 dB (00000) > X0Y2/TX MGT_X0Y3/RX 6.423 Gbps 2.276E13 0E0 4.394E14 Reset PR85 7-bit > 0.00 dB (00000) > X0Y2/TX MGT_X0Y3/RX 6.425 Gbps 2.276E13 0E0 4.394E14 Reset PR85 7-bit > 0.00 dB (00000) > X0Y3/RX 6.425 Gbps 2.276E13 0E0 4.394E14 Reset PR85 7-bit > 0.00 dB (00000) > X0Y3/RX 6.403 Gbps 2.19E13 0E0 4.566E144 Reset PR85 7-bi</th> <th>RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern TX Pre-Cursor TX Post-Cursor x0Y3/TX MGT_X0Y3/RX 6.417 Gbps 2.102E13 0E0 4.757E14 Reset PR85 7-bit > 0.00 dB (00000) > 0.00 dB (000000) > 0.00 dB (000</th> <th>RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern TX Pre-Cursor TX Post-Cursor TX Diff Swing x0Y3/TX MGT_X0Y3/R0 6.417 Gbps 2.102E13 OE0 4.757E14 Reset PRBS 7-bit > PRBS 7-bit > 0.00 dB (00000) 0.00 dB (00000) 0.00 dB (00000) 950 mV (1100) MGT_X0Y3/RX 6.417 Gbps 2.102E13 OE0 4.394E14 Reset PRBS 7-bit > PRBS 7-bit > 0.00 dB (00000) 0.00 dB (00000) 950 mV (1100) WGT_X0Y3/RX 6.413 Gbps 2.276E13 OE0 4.394E14 Reset PRBS 7-bit > PRBS 7-bit > 0.00 dB (00000) 0.00 dB (00000) 950 mV (1100) X0Y1/TX MGT_X0Y3/RX 6.425 Gbps 2.276E13 OE0 4.394E14 Reset PRBS 7-bit > PRBS 7-bit > 0.00 dB (00000) 0.00 dB (00000) 0.00 dB (00000) 6.02 dB (1010) \$46 mV (11000) X0Y3/RX A6.17 Gbps 2.19E13 OE0 4.56E14 Reset PRBS 7-bit > PRBS 7-bit 0.00 dB (000000) 6.02 dB (10</th> <th>Prial I/O Scans Prial I/O Scans TX Pattern TX Pattern TX Pre-Cursor TX Polt-Cursor TX Diff Swing <</th>	RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern TX Pre-Cursor x0Y3/TX MGT_X0Y3/RX 6.417 Gbps 2.102E13 0E0 4.757E14 Reset PR85 7-bit > 0.00 dB (00000) > MGT_X0Y3/RX 6.413 Gbps 2.276E13 0E0 4.394E14 Reset PR85 7-bit > 0.00 dB (00000) > X0Y3/TX MGT_X0Y3/RX 6.423 Gbps 2.276E13 0E0 4.394E14 Reset PR85 7-bit > 0.00 dB (00000) > X0Y2/TX MGT_X0Y3/RX 6.423 Gbps 2.276E13 0E0 4.394E14 Reset PR85 7-bit > 0.00 dB (00000) > X0Y2/TX MGT_X0Y3/RX 6.425 Gbps 2.276E13 0E0 4.394E14 Reset PR85 7-bit > 0.00 dB (00000) > X0Y3/RX 6.425 Gbps 2.276E13 0E0 4.394E14 Reset PR85 7-bit > 0.00 dB (00000) > X0Y3/RX 6.403 Gbps 2.19E13 0E0 4.566E144 Reset PR85 7-bi	RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern TX Pre-Cursor TX Post-Cursor x0Y3/TX MGT_X0Y3/RX 6.417 Gbps 2.102E13 0E0 4.757E14 Reset PR85 7-bit > 0.00 dB (00000) > 0.00 dB (000000) > 0.00 dB (000	RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern TX Pre-Cursor TX Post-Cursor TX Diff Swing x0Y3/TX MGT_X0Y3/R0 6.417 Gbps 2.102E13 OE0 4.757E14 Reset PRBS 7-bit > PRBS 7-bit > 0.00 dB (00000) 0.00 dB (00000) 0.00 dB (00000) 950 mV (1100) MGT_X0Y3/RX 6.417 Gbps 2.102E13 OE0 4.394E14 Reset PRBS 7-bit > PRBS 7-bit > 0.00 dB (00000) 0.00 dB (00000) 950 mV (1100) WGT_X0Y3/RX 6.413 Gbps 2.276E13 OE0 4.394E14 Reset PRBS 7-bit > PRBS 7-bit > 0.00 dB (00000) 0.00 dB (00000) 950 mV (1100) X0Y1/TX MGT_X0Y3/RX 6.425 Gbps 2.276E13 OE0 4.394E14 Reset PRBS 7-bit > PRBS 7-bit > 0.00 dB (00000) 0.00 dB (00000) 0.00 dB (00000) 6.02 dB (1010) \$46 mV (11000) X0Y3/RX A6.17 Gbps 2.19E13 OE0 4.56E14 Reset PRBS 7-bit > PRBS 7-bit 0.00 dB (000000) 6.02 dB (10	Prial I/O Scans TX Pattern TX Pattern TX Pre-Cursor TX Polt-Cursor TX Diff Swing <

8.1 IBERT Slot no 8, this test@6.4Gbps covered the area:

- 6 lanes of MGT data from the FEX slot 8

				Vivado 2	017.2					-	•
Help Q+ Quick Access											
Dashboard 👻										🔛 Serial I/O Ana	ilyzer
10299A57644											?
Serial I/O Scans											? _ 🖓
TX RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Ena
					Reset	1	PRBS 7-bit 🗸				6
MGT X0Y3	RX 6.413 Gbps	1.858E13	0E0	5.383E-14	Reset	1	PRBS 7-bit 🗸				
					Reset	ĩ	PRBS 7-bit 🗸				
MGT X0Y0	RX 6.420 Gbps	3.519E13	0E0	2.842E-14	Reset	1	PRBS 7-bit 🗸				
MGT X0Y1	RX 6.413 Gbps	3.519E13	0E0	2.842E-14	Reset	ĩ	PRBS 7-bit 🗸				
MGT X0Y2	RX 6.413 Gbps	3.519E13	0E0	2.842E-14	Reset	1	PRBS 7-bit 🗸				
MGT X0Y0	RX 6.410 Gbps	3.519E13	0E0	2.842E-14	Reset	í	PRBS 7-bit 🗸				
					Reset	PRBS 7-bit	PRBS 7-bit 🗸	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000) 🗸	
мот хоузвлх мот хоуз	3/RX 6.413 Gbps	6.292E13	0E0	1.589E-14	Reset	PRBS 7-bit	PRBS 7-bit 🗸	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000) v	
MGT X0Y39/TX MGT X0Y3	RX 6.421 Gbps	6.292E13	0E0	1.589E-14	Reset	PRBS 7-bit	PRBS 7-bit 🗸	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000) ∨	
					Reset	1	PRBS 7-bit 🗸				
MGT X0Y1	RX 6.413 Gbps	6.292E13	0E0	1.589E-14	Reset	1	PRBS 7-bit 🗸				
					Reset	1	PBBS 7-bit				6
MGT X0Y2	0.424 Gbps	1.864E13	2E0	1.073E-13	Reset	1	PRBS 7-bit v				6
MGT X0Y2	7/RX 6.413 Gbps	1.864E13	2E0	1.073E-13	Reset	1	PRBS 7-bit 🗸				
MGT X0Y3	VBX 6.404 Gbps	1.864E13	2E0	1.073E-13	Reset	1	PBBS 7-bit				6
MGT X0V3	/BX 6.416 Gbps	1.864E13	2E0	1.073E-13	Reset]	PBBS 7-bit				0
MGT X0Y3	VBX 6.400 Gbps	1.864E13	2E0	1.073E-13	Reset	1	PBBS 7-bit				6
MGT X0V3	/BX 6.413 Gbps	1.864E13	2E0	1.073E-13	Reset]	PBBS 7-bit				
	field of the output				Reset	Multiple	PBBS 7-bit	Multiple	Multiple	Multiple	6
MGT X0V23/TX MGT X1V3	1/BX 6.400 Gbps	1.865E13	2E0	1.072E-13	Reset	PBBS 7-bit	PBBS 7-bit	0.00 dB (00000) v	0.00 dB (00000) v	950 mV (1100)	
MGT_X0Y24/TX_MGT_X1V3	ARX 6.400 Ghns	1.865E13	2F0	1.072E-13	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	6.02 dB (10100)	846 mV (11000)	6
MGT X0Y24/TX MGT X1Y3	0.400 Gbps	1.865E13	2E0	1.072E-13	Reset	PBBS 7-bit	PBBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (1100)	6
MGT X0V25/TX MGT X1V3	7/8X 6 400 Gbps	1.865E13	2E0	1.072E-13	Reset	PBBS 7-bit	PBBS 7-bit	0.00 dB (00000) v	6.02 dB (10100)	846 mV (11000)	
MGT_X0Y25/TX_MGT_X1Y3	R/RX 6.400 Ghos	1.865E13	2E0	1.072E-13	Reset	PBBS 7-bit	PBBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (1100)	6
MGT_X0V26/TX_MGT_X1V2	ARX 6.400 Ghos	1.865E13	200	1.072E-13	Reset	PBBS 7-bit	PBBS 7-bit	0.00 dB (00000)	6.02 dB (10100)	846 mV (11000)	0
101_10120,1X M01_X110	7/8X 6.400 Ghns	1.865E13	050	5.362E-14	Reset]	PBBS 7-bit				6
MINT XIIY 4	not onlog oppo	10000110	020	5.0002211	neset			0.00.45 (00000)			
	Q- Oulck Access Dashboard + 10299A57644 C Serial I/O Scans TX RX MGT_X0Y2/ MGT_X0Y2/ MGT_X0Y3/ MGT_X0Y3/ MGT_X0Y3/ MGT_X0Y3/ MGT_X0Y3/ MGT_X0Y3/ MGT_X0Y3/ MGT_X0Y3/ MGT_X0Y3//X MGT_X0Y3//X MGT_X0Y3//X MGT_X0Y3//X MGT_X0Y3//X MGT_X0Y3//X MGT_X0Y3//X MGT_X0Y2//X MGT_X	Beip Q- Ouick Access Dashboard → 10299A57644 IO299A57644 IO299A57644 TX RX Status TX RX Status MGT_X0Y3/RX 6.413 Gbps MGT_X0Y3/RX 6.410 Gbps MGT_X0Y3/RX 6.4	Bashboard ~ Dashboard ~ 10299A57644 C Serial I/O Scans TX RX Status Bits MGT_X0Y3/RX 6.413 Gbps 3.519E13 MGT_X0Y3/RX 6.413 Gbps 3.519E13 MGT_X0Y0/RX 6.413 Gbps 3.519E13 MGT_X0Y0/RX 6.413 Gbps 3.519E13 MGT_X0Y3/RX 6.413 Gbps 6.529213 MGT_X0Y3/RX 6.413 Gbps 6.292E13 MGT_X0Y3/RX 6.424 Gbps 6.292E13 MGT_X0Y1/RX 6.413 Gbps 1.684E13 MGT_X0Y3/RX 6.424 Gbps 1.684E13 MGT_X0Y3/RX 6.413 Gbps 1.684E13 MGT_X0Y3/RX 6.413 Gbps 1.684E13 MGT_X0Y3/RX 6.424 Gbps 1.684E13 MGT_X0Y3/RX 6.416 Gbps 1.684E13 MGT_X0Y3/RX 6.416 Gbps 1.684E13 MGT_X0Y3/RX 6.400 Gbps 1.685E13 MGT_X0Y3/RX 6.400 Gbps 1.685E13 MGT_X0Y3/RX 6.400 Gbps 1.685E13 <td>Bashboard - Dasbboard - 10299A57644 C Serial I/O Scans TX RX Status Bits Errors MGT_X0Y3/RX 6.413 Gbps 3.858E13 OEO MGT_X0Y0/RX 6.420 Gbps 3.519E13 OEO MGT_X0Y0/RX 6.413 Gbps 3.519E13 OEO MGT_X0Y0/RX 6.413 Gbps 3.519E13 OEO MGT_X0Y3/RX 6.413 Gbps 3.519E13 OEO MGT_X0Y3/RX 6.413 Gbps 3.519E13 OEO MGT_X0Y3/RX 6.413 Gbps 6.292E13 OEO MGT_X0Y3/RX 6.413 Gbps 6.292E13 OEO MGT_X0Y3/RX 6.413 Gbps 6.292E13 OEO MGT_X0Y3/RX 6.413 Gbps 1.864E13 2EO MGT_X0Y3/RX 6.414 Gbps 1.864E13 2EO MGT_X0Y3/RX 6.413 Gbps 1.864E13 2EO MGT_X0Y3/RX 6.413 Gbps 1.864E13 2EO MGT_X0Y3/RX 6.413 Gbps 1.864E13 2EO</td> <td>RX Status Bits Errors BER MGT_X0Y3/RX 6.413 Gbps 3.519E13 0E0 3.392E14 MGT_X0Y3/RX 6.413 Gbps 3.519E13 0E0 2.842E14 MGT_X0Y3/RX 6.413 Gbps 6.292E13 0E0 1.599E14 MGT_X0Y3/RX 6.413 Gbps 6.292E13 0E0 1.599E14 MGT_X0Y3/RX 6.413 Gbps 1.864E13 2E0 1.075E13 MGT_X0Y3/RX 6.413 Gbps 1.864E13 2E0 1.075E13 MGT_X0Y3/RX 6.413 Gbps 1.864E13 2E0 1.075E13 MGT_X0Y3/RX 6.413 Gbps 1.864E13 2E0 1</td> <td>Norman Norman Norman Belp Qr Outck Access Control Access Control Access 10299457644 Control Access Control Access Control Access TX RX Status Bits Errors BER BERT Reset MGT_X0Y3RK 6.413 Gbps 3.519E13 OEO 2.842E-14 Reset MGT_X0Y0RK 6.413 Gbps 3.519E13 OEO 2.842E-14 Reset MGT_X0Y3RK 6.413 Gbps 6.292E13 OEO 1.599E-14 Reset MGT_X0Y3RK 6.413 Gbps 6.292E13 OEO 1.599E-14 Reset MGT_X0Y3RK 6.413 Gbps 1.694E13 2EO 1.073E-13 Reset MGT_X0Y3RK 6.413 Gbps 1.864E13 2EO</td> <td>RX Status Bits Errors BER BERT Peset TX Pattern MGT_X0Y3RX 6.413 Gbps 3.519E13 0E0 5.383E-14 Reset Reset</td> <td>RX Status Bits Errors BER EERT Reset TX Pattern RX Pattern MGT_X0Y307X 6.413 Gbps 1.859E13 0E0 5.393E14 Reset PR85 7-bit PR85</td> <td>RX Status Bits Errors BER EERT TX Pattern RX Pattern X Pre-Cursor TX RX Status Bits Errors BER EERT TX Pattern RX Pattern X Pre-Cursor MGT_X0Y3/RX 6.413 Gbps 1.859E13 OE0 5.383E14 Reset PR85 7-bit > MGT_X0Y0/RX 6.413 Gbps 3.519E13 OE0 2.842E14 Reset PR85 7-bit > MGT_X0Y0/RX 6.413 Gbps 3.519E13 OE0 2.842E14 Reset PR85 7-bit > MGT_X0Y0/RX 6.413 Gbps 3.519E13 OE0 2.842E14 Reset PR85 7-bit > MGT_X0Y0/RX 6.413 Gbps 3.519E13 OE0 2.842E14 Reset PR85 7-bit > O.00 dB (00000) N MGT_X0Y3/RX 6.413 Gbps 3.519E13 OE0 2.842E14 Reset PR85 7-bit > 0.00 dB (00000) N MGT_X0Y3/RX 6.413 Gbps 5.292E13 OE0 1.598</td> <td>R Status Bts Errors BER BERT Reset XP Past 5-bit X X Pro-Cursor X Post-Cursor V Rt Status Bts Errors BER BERT Reset X Pattern X Pro-Cursor X Post-Cursor MGT_X0Y3/RX 6.413 Gbps 1.858E13 GEO Sage14 Reset PPBS 7-bit > MGT_X0Y0/RX 6.420 Gbps 5.19E13 GEO 2.442E14 Reset PPBS 7-bit > MGT_X0Y0/RX 6.413 Gbps 3.519E13 GEO 2.442E14 Reset PPBS 7-bit > MGT_X0Y0/RX 6.413 Gbps 3.519E13 GEO 2.442E14 Reset PPBS 7-bit > MGT_X0Y0/RX 6.413 Gbps 3.519E13 GEO 2.442E14 Reset PPBS 7-bit > GEO GEO 2442E14 Reset PPBS 7-bit > GEO 44101001 K GEO 4</td> <td>Normal Substrate Status Bits First REF REF PRES The Pres<!--</td--></td>	Bashboard - Dasbboard - 10299A57644 C Serial I/O Scans TX RX Status Bits Errors MGT_X0Y3/RX 6.413 Gbps 3.858E13 OEO MGT_X0Y0/RX 6.420 Gbps 3.519E13 OEO MGT_X0Y0/RX 6.413 Gbps 3.519E13 OEO MGT_X0Y0/RX 6.413 Gbps 3.519E13 OEO MGT_X0Y3/RX 6.413 Gbps 3.519E13 OEO MGT_X0Y3/RX 6.413 Gbps 3.519E13 OEO MGT_X0Y3/RX 6.413 Gbps 6.292E13 OEO MGT_X0Y3/RX 6.413 Gbps 6.292E13 OEO MGT_X0Y3/RX 6.413 Gbps 6.292E13 OEO MGT_X0Y3/RX 6.413 Gbps 1.864E13 2EO MGT_X0Y3/RX 6.414 Gbps 1.864E13 2EO MGT_X0Y3/RX 6.413 Gbps 1.864E13 2EO MGT_X0Y3/RX 6.413 Gbps 1.864E13 2EO MGT_X0Y3/RX 6.413 Gbps 1.864E13 2EO	RX Status Bits Errors BER MGT_X0Y3/RX 6.413 Gbps 3.519E13 0E0 3.392E14 MGT_X0Y3/RX 6.413 Gbps 3.519E13 0E0 2.842E14 MGT_X0Y3/RX 6.413 Gbps 6.292E13 0E0 1.599E14 MGT_X0Y3/RX 6.413 Gbps 6.292E13 0E0 1.599E14 MGT_X0Y3/RX 6.413 Gbps 1.864E13 2E0 1.075E13 MGT_X0Y3/RX 6.413 Gbps 1.864E13 2E0 1.075E13 MGT_X0Y3/RX 6.413 Gbps 1.864E13 2E0 1.075E13 MGT_X0Y3/RX 6.413 Gbps 1.864E13 2E0 1	Norman Norman Norman Belp Qr Outck Access Control Access Control Access 10299457644 Control Access Control Access Control Access TX RX Status Bits Errors BER BERT Reset MGT_X0Y3RK 6.413 Gbps 3.519E13 OEO 2.842E-14 Reset MGT_X0Y0RK 6.413 Gbps 3.519E13 OEO 2.842E-14 Reset MGT_X0Y3RK 6.413 Gbps 6.292E13 OEO 1.599E-14 Reset MGT_X0Y3RK 6.413 Gbps 6.292E13 OEO 1.599E-14 Reset MGT_X0Y3RK 6.413 Gbps 1.694E13 2EO 1.073E-13 Reset MGT_X0Y3RK 6.413 Gbps 1.864E13 2EO	RX Status Bits Errors BER BERT Peset TX Pattern MGT_X0Y3RX 6.413 Gbps 3.519E13 0E0 5.383E-14 Reset Reset	RX Status Bits Errors BER EERT Reset TX Pattern RX Pattern MGT_X0Y307X 6.413 Gbps 1.859E13 0E0 5.393E14 Reset PR85 7-bit PR85	RX Status Bits Errors BER EERT TX Pattern RX Pattern X Pre-Cursor TX RX Status Bits Errors BER EERT TX Pattern RX Pattern X Pre-Cursor MGT_X0Y3/RX 6.413 Gbps 1.859E13 OE0 5.383E14 Reset PR85 7-bit > MGT_X0Y0/RX 6.413 Gbps 3.519E13 OE0 2.842E14 Reset PR85 7-bit > MGT_X0Y0/RX 6.413 Gbps 3.519E13 OE0 2.842E14 Reset PR85 7-bit > MGT_X0Y0/RX 6.413 Gbps 3.519E13 OE0 2.842E14 Reset PR85 7-bit > MGT_X0Y0/RX 6.413 Gbps 3.519E13 OE0 2.842E14 Reset PR85 7-bit > O.00 dB (00000) N MGT_X0Y3/RX 6.413 Gbps 3.519E13 OE0 2.842E14 Reset PR85 7-bit > 0.00 dB (00000) N MGT_X0Y3/RX 6.413 Gbps 5.292E13 OE0 1.598	R Status Bts Errors BER BERT Reset XP Past 5-bit X X Pro-Cursor X Post-Cursor V Rt Status Bts Errors BER BERT Reset X Pattern X Pro-Cursor X Post-Cursor MGT_X0Y3/RX 6.413 Gbps 1.858E13 GEO Sage14 Reset PPBS 7-bit > MGT_X0Y0/RX 6.420 Gbps 5.19E13 GEO 2.442E14 Reset PPBS 7-bit > MGT_X0Y0/RX 6.413 Gbps 3.519E13 GEO 2.442E14 Reset PPBS 7-bit > MGT_X0Y0/RX 6.413 Gbps 3.519E13 GEO 2.442E14 Reset PPBS 7-bit > MGT_X0Y0/RX 6.413 Gbps 3.519E13 GEO 2.442E14 Reset PPBS 7-bit > GEO GEO 2442E14 Reset PPBS 7-bit > GEO 44101001 K GEO 4	Normal Substrate Status Bits First REF REF PRES The Pres </td

8.2 IBERT Slot no 9, this test@6.4Gbps covered the area:

- 6 lanes of MGT data from the FEX slot 9

						Vivado 2	017.2							-	
File Edit Teels Window Lowert View	Holp Q+ (Juick Access													
		ed											== Serial I/O	Anaha	or
•, • ~ • • • × * * * * *	¢ Dashboa												= Senariyo	Arranyz	.ei
ARDWARE MANAGER - localhost/xilinx_tcf/Digilent/2	210299A57644														?
Tcl Console Messages Serial I/O Links	× Serial I/O	Scans												?	_ 8 0
Q ≚ ≑ +															
Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern		RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing		DFE Ena
Ungrouped Links (0)															
HUB: Readout Control Data from This Rod (1)							Reset	PRBS 7-bit	~	PRBS 7-bit 🗸	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100)	~	
% Link 0	MGT X0Y3/TX	MGT X0Y3/RX	6.413 Gbps	7.748E11	0E0	1.291E-12	Reset	PRBS 7-bit	~	PRBS 7-bit 🗸	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100)	~	
							Reset	PRBS 7-bit		PRBS 7-bit 🗸	0.00 dB (00000)	Multiple	Multiple		
% Link 1		MGT X0Y0/RX	6.413 Gbps	3.398E13	0E0	2.943E-14	Reset	í		PRBS 7-bit ~					
% Link 2	MGT X0Y1/TX	MGT X0Y1/RX	6.413 Gbps	3.398E13	0E0	2.943E-14	Reset	PRBS 7-bit	~	PRBS 7-bit v	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100)	~	J
% Link 3	MGT X0Y2/TX	MGT X0Y2/BX	6.422 Gbps	3.398E13	0E0	2.943E-14	Reset	PBBS 7-bit	~	PRBS 7-bit v	0.00 dB (00000)	0.00 dB (00000) 🗸	950 mV (1100)	~	5
% Link 4	MGT X0Y0/TX	MGT_X0Y0/BX	6.410 Gbps	3.398E13	0E0	2.943E-14	Reset	PBBS 7-bit	~	PBBS 7-bit v	0.00 dB (00000)	6.02 dB (10100) v	846 mV (11000)		6
v line Hub R0 (2)							Reset	PBBS 7-bit	-	PBBS 7-bit	0.00 dB (00000)	6.02 dB (10100)	846 mV (11000)		
% Link 74	MGT YOV28/D	MGT YOV28/P	6 413 Ghns	3 398E13	OEO	2 943E-14	Reset	PBBS 7-bit	÷	PBBS 7-bit	0.00 dB (00000)	6.02 dB (10100) ~	846 mV (11000)		
S Link 74	MGT X0Y20/D	MGT YOV20/P	6 417 Gbps	3 276E13	0E0	3.053E-14	Reset	PRBS 7-bit	Ť.	PRBS 7-bit	0.00 dB (00000)	6.02 dB (10100) w	846 mV (11000)		
	MOT_X0133/17	(0.417 0005	5.270215	020	5.0552 14	Reset	PBBS 7-bit	÷	PBBS 7-bit	0.00 dB (00000)	6.02 dB (10100) v	846 mV (11000)	÷	
Solution of the second se	MCT YOVE TY	MCT YOVE DY	6 416 Ghoc	2 20051 2	050	2 0425 14	Reset	PPPC 7 bit	×	PPPS 7 bit	0.00 dB (00000)	6.02 dB (10100) ++	846 mV (11000)	¥	
- Click 2	MG1_X011/1X	MG1_X011/KX	0.410 0005	5.550215	OLU	2.9436-14	Reset	1 1103 7-010	×	PRBS 7-bit v	0.00 dB (00000) 0	0.02 dB (10100) 0	840 110 (11000)	Ŷ	
 Stick 9 		MCT YOY22/D	6 400 Ghos	2 02251 2	150	25426.14	Reset	1		PPPS 7-bit					
9 Link 0		MGT_X0132/R0	6 412 Gbps	2.022013	150	3.5456-14	Reset	1		PPBC 7 bit					
-5 LINK 9		MGT_X0133/R0	6 412 Obps	2.022013	100	3.3436-14	Reset	1		PRBS 7-bit V					
-5 LINK 10		MGT_X0T34/R0	6.413 Gbps	2.022013	100	3.3436-14	Reset	1		PRBS 7-bit V					
S LINK 11		MGT_X0Y35/R0	6.413 Gbps	2.023E13	160	3.543E-14	Reset	1		PRBS 7-Dit V					
% LINK 12		MGT_X0Y36/R0	6.413 Gbps	2.823E13	160	3.543E-14	Reset	1		PRBS 7-DIL V					
S LINK 13		MG1_X0Y37/PO	6.413 Gbps	2.823E13	TEU	3.543E-14	Reset			PRBS 7-Dit V					
WD: Data from FEX_9 and 2 Links from H							Reset	Multiple		PRBS 7-DIE V	Multiple	Multiple	Multiple		
% Link 92	MGT_X1Y38/T	CMGT_X0Y30/R	6.400 Gbps	1.375E13	TEO	7.275E-14	Reset	PRBS 7-bit	~	PRBS 7-bit V	0.00 dB (00000) V	0.00 dB (00000) V	269 mV (0000)	~	
% Link 96	MGT_X0Y2/TX	MGT_X0Y31/R	6.400 Gbps	1.375E13	1E0	7.275E-14	Reset	PRBS 7-bit	~	PRBS 7-bit V	0.00 dB (00000) V	6.02 dB (10100) V	846 mV (11000)	~	
% Link 97	MGT_X0Y3/TX	MGT_X0Y32/R	6.400 Gbps	1.374E13	1E0	7.276E-14	Reset	PRBS 7-bit	~	PRBS 7-bit v	0.00 dB (00000) V	6.02 dB (10100) v	846 mV (11000)	~	4
% Link 98	MGT_X0Y4/TX	MGT_X0Y33/R	6.400 Gbps	1.374E13	1E0	7.276E-14	Reset	PRBS 7-bit	~	PRBS 7-bit 🗸	0.00 dB (00000) ~	6.02 dB (10100) 🗸	846 mV (11000)	~	-
% Link 99	MGT_X0Y4/TX	MGT_X0Y34/RX	6.400 Gbps	1.374E13	1E0	7.276E-14	Reset	PRBS 7-bit	~	PRBS 7-bit 🗸	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100)	~	ų
% Link 100	MGT_X0Y5/TX	MGT_X0Y35/R	6.400 Gbps	4.485E11	1E0	2.229E-12	Reset	PRBS 7-bit	~	PRBS 7-bit 🗸	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000)	~	-
% Link 94		MGT_X0Y37/R	6.400 Gbps	1.374E13	0E0	7.276E-14	Reset			PRBS 7-bit 🗸					-
% Link 95	MGT_X0Y0/TX	MGT_X0Y36/R	6.400 Gbps	1.374E13	0E0	7.276E-14	Reset	PRBS 7-bit	~	PRBS 7-bit 🗸	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100)	~	¥

8.3 IBERT Slot no 10, this test@6.4Gbps covered the area:

- 6 lanes of MGT data from the FEX slot 10

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me	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern		RX Pattern		TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enable
🖴 Ungrouped Links (0)															
🐵 HUB: Readout Control Data from This Rod (1)							Reset			PRBS 7-bit	\sim				1
% Link 0		MGT_X0Y3/RX	6.413 Gbps	1.118E13	0E0	8.948E-14	Reset			PRBS 7-bit	\sim				1
4 HUB: MiniPods (4)							Reset			PRBS 7-bit	\sim				1
% Link 1		MGT_X0Y0/RX	6.415 Gbps	5.36E13	0E0	1.866E-14	Reset			PRBS 7-bit	~				1
% Link 2		MGT_X0Y1/RX	6.413 Gbps	5.36E13	0E0	1.866E-14	Reset			PRBS 7-bit	~				1
% Link 3		MGT X0Y2/RX	6.415 Gbps	5.36E13	0E0	1.866E-14	Reset	1		PRBS 7-bit	~				1
% Link 4		MGT X0Y0/RX	6.413 Gbps	5.36E13	0E0	1.866E-14	Reset	ī		PRBS 7-bit	~				1
HUB: Other Hub R0 (2)							Reset	PRBS 7-bit	~	PRBS 7-bit	~	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000) 🗸	1
% Link 74	MGT X0Y38/TX	MGT X0Y38/RX	6.413 Gbps	8.133E13	0E0	1.23E-14	Reset	PRBS 7-bit	~	PRBS 7-bit	~	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000) 🗸	~
% Link 76	MGT X0Y39/TX	MGT X0Y39/RX	6.413 Gbps	8.133E13	0E0	1.23E-14	Reset	PRBS 7-bit	~	PRBS 7-bit	~	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000) 🗸	1
HUB: Combined Data from Other HUB (1)							Reset	ĩ		PRBS 7-bit	~				✓
% Link 2		MGT X0Y1/RX	6.416 Gbps	8.134E13	0E0	1.229E-14	Reset	ī		PRBS 7-bit	~				<
% HUB: Data from FEX 10 (6)							Reset			PRBS 7-bit	¥				✓
% Link 0		MGT X0Y22/BX	6.413 Gbps	1.115E13	4E0	3.588E-13	Reset			PRBS 7-bit	~				
S Link 1		MGT X0Y23/BX	6.416 Gbps	1.115E13	4E0	3.588E-13	Reset	1		PRBS 7-bit	~				
% Link 2		MGT X0V36/BX	6.413 Gbps	1.115E13	4E0	3.588E-13	Reset	i		PBBS 7-bit	~				2
% Link 3		MGT X0V37/BX	6.413 Gbns	1.115E13	4E0	3.588E-13	Reset	1		PBBS 7-bit	÷				Z
S Link 4		MGT X0V38/BX	6.413 Gbps	1.115E13	4E0	3.588E-13	Reset	i		PBBS 7-bit	~				2
% Link 5		MGT_X0Y39/BX	6.423 Gbps	1.115E13	4E0	3.588E-13	Reset	1		PBBS 7-bit	Ū				· ·
BOD: Data from EEX 10 and 2 Links from H			or the only o				Reset	Multiple		PBBS 7-bit		Multiple	Multiple	Multiple	Z
% Link 68	MGT YOVLATY	MGT YOV24/PV	6.400 Ghns	1 124E13	4E0	3 56E-13	Reset	PBBS 7-bit	~	PBBS 7-bit	÷	0.00 dB (00000) v	0.00 dB (00000) v	269 mV (0000)	
% Link 69	MGT_X0114/TX	MGT_X0Y25/PX	6.400 Gbps	1 124613	4E0	3 56E-13	Reset	PRBS 7-bit		PRBS 7-bit		0.00 dB (00000) v	0.00 dB (00000) v	269 mV (0000)	•
9 Link 70	MGT_X0115/TX	MGT_X0125/RX	6.400 Gbps	1 1 2461 2	450	2.565.12	Reset	PPPS 7-bit		PDDC 7.bit		0.00 dB (00000) ++	0.00 dB (00000) ++	269 mV (0000) ++	v Z
6 Link 70	MGT_X0110/1X	MGT_X0720/RA	6.400 Gbps	1.124613	4E0	2.565.12	Reset	PRPS 7 bit	· · ·	PPPC 7 bit		0.00 dB (00000) ++	0.00 dB (00000) ++	269 mV (0000) ++	¥
S Link 71	MGT_X0117/1X	MGT_X0727/RX	6.400 Gbps	1.124013	40	3.502-13	Reset	PRBS 7-bit	×	DDDC 7 bit	×	0.00 dB (00000) 👽	0.00 dB (00000) 👳	269 mV (0000) V	¥
9 Link 72	MGT_X0V10/TX	MCT_X0Y20/RX	6.400 Gbps	1 1 24E1 2	4E0	2.565.12	Reset		~	PDDC 7 bit	~	0.00 dB (00000) V	0.00 dB (00000) ++	269 mV (0000) V	×
O LINE / J		MGT YOV27/PV	6.400 Gbps	1 1 2461 2	460	9 001E-14	Reset		*	PDDC 7.6#	×	0.00 ub (00000) V	5.55 db (00000) V	200 110 (0000) 0	✓
9 Link 101		MG1_X0137/RX	0.400 Gbps	1.124013	050	0.9015-14	Reset			DDDC 7 ka	~	0.00.40(00000)	0.00 dB (00000)	050	✓
% Link 101	MCT YOYO TY	MCT YOURS DY	6 400 Ghrc		· · · · · · · · · · · · · · · · · · ·									A STILLING A CONTRACT OF A CON	

8.4 IBERT Slot no 11, this test@6.4Gbps covered the area:

- 6 lanes of MGT data from the FEX slot 11

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	RX	Status	Bits	Errors	BEB	BERT Reset	TX Pattern		RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing		DEE Enak
						Reset	PRBS 7-bit	~	PRBS 7-bit 🗸	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100)	~	1
оүзлтх	MGT X0Y3/RX	6.411 Gbps	9.448E12	0E0	1.058E-13	Reset	PRBS 7-bit	~	PRBS 7-bit 🗸	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100)	~	1
						Reset	PRBS 7-bit		PRBS 7-bit 🗸	0.00 dB (00000)	Multiple	Multiple		1
	MGT X0Y0/RX	6.413 Gbps	5.51E13	0E0	1.815E-14	Reset	i		PRBS 7-bit 🗸					1
0Y1/TX	MGT X0Y1/RX	6.409 Gbps	5.51E13	0E0	1.815E-14	Reset	PRBS 7-bit	~	PRBS 7-bit 🗸	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100)	~	
0Y2/TX	MGT X0Y2/RX	6.413 Gbps	5.51E13	0E0	1.815E-14	Reset	PRBS 7-bit	~	PRBS 7-bit 🗸	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100)	~	
оуолтх	MGT X0Y0/BX	6.413 Gbps	5.913E13	0E0	1.691E-14	Reset	PRBS 7-bit	~	PRBS 7-bit 🗸	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000)	~	
						Reset	PRBS 7-bit	~	PRBS 7-bit 🗸	0.00 dB (00000) ~	0.00 dB (00000) 🗸	950 mV (1100)	~	
0V24/TX	MGT X0Y24/BX	6.416 Gbps	4.173E13	3E0	7.189E-14	Reset	PBBS 7-bit	~	PBBS 7-bit v	0.00 dB (00000) v	0.00 dB (00000) v	950 mV (1100)	~	
0Y25/TX	MGT_X0Y25/BX	6.413 Gbps	4.173E13	3E0	7.189E-14	Reset	PRBS 7-bit	~	PRBS 7-bit 🗸	0.00 dB (00000) v	0.00 dB (00000) v	950 mV (1100)	~	
0У26/ТХ	MGT X0Y26/BX	6.403 Gbps	4.173E13	3E0	7.189E-14	Reset	PBBS 7-bit	~	PBBS 7-bit v	0.00 dB (00000) v	0.00 dB (00000) v	950 mV (1100)	~	
0727/17	MGT_X0Y27/8X	6.403 Gbps	4.173E13	3E0	7.189E-14	Reset	PBBS 7-bit	Ĵ	PBBS 7-bit v	0.00 dB (00000) v	0.00 dB (00000) v	950 mV (1100)	Ū.	
0У28/ТУ	MGT YOV28/BY	6 413 Ghns	4 173E13	3E0	7 189E-14	Reset	PBBS 7-bit	-	PBBS 7-bit	0.00 dB (00000) ~	0.00 dB (00000) v	950 mV (1100)		7
02000	MGT YOY20/RY	6 402 Gbps	4 173E13	3E0	7 189E-14	Reset	PBBS 7-bit	÷.	PBBS 7-bit	0.00 dB (00000) ×	0.00 dB (00000) v	950 mV (1100)	÷.	
						Reset	PBBS 7-bit	-	PBBS 7-bit	0.00 dB (00000) v	6.02 dB (10100) v	846 mV (11000)		
ovae my	MGT YOV20/PV	6 413 Ghns	6 111E13	050	1.636E-14	Reset	PBBS 7-bit	÷	PBBS 7-bit	0.00 dB (00000) ~	6.02 dB (10100) v	846 mV (11000)		
0720/17	MGT_X0Y20/RV	6 413 Gbps	6111613	0E0	1.6365-14	Reset	PRBS 7-bit	Ť.	PRBS 7-bit	0.00 dB (00000) w	6.02 dB (10100) v	846 m)/ (11000)		
0133/17	MG1_X0133/10	0.415 0005	0.1111210	020	1.0302 14	Reset	PPPS 7-bit		PPPS 7-bit	0.00 dB (00000) ++	6.02 dB (10100) +	846 mV (11000)	*	
	MCT YOVE IDV	6 412 Ghos	5 026512	050	1 6995 14	Beset	PPPC 7 bit	×	PPPS 7 bit	0.00 dB (00000) ++	6.02 dB (10100) ++	846 mV(11000)	×	¥
011/1X	MG1_X011/KX	0.413 Obbs	5.520215	OLU	1.0000-14	Reset	Multiple	~	PRBS 7-bit	Multiple	Multiple	Multiple	~	
1 VO TV	MCT YOVI O/DY	6 400 Ghos	2 95 261 2	150	2 506E 14	Beset	DDDC 7. hit		PPPS 7-bit 4	0.00.dR (00000) ++	0.00.48 (00000) **	269 m)/ (0000)		¥
110/17	MGT_X0118/RA	6 400 Gbps	2.052010	150	3.500E-14	Reset	PPPC 7 bit	×	PRBS 7-bit v	0.00 dB (00000) ++	0.00 dB (00000) ++	269 mV (0000)	~	¥
1 11 2/14	MGT_X0Y20/PX	6 400 Gbps	2.052010	150	2 5065-14	Reset	PPPS 7-bit	×	PPPS 7-bit	0.00 dB (00000) ++	0.00 dB (00000) ++	269 mV (0000)	*	
1113/18	MGT_X0Y21/RX	6 400 Gbps	2.052010	150	2 506E 14	Reset	PPPC 7 bit	~	PPPS 7 bit	0.00 dB (00000) ++	0.00 dB (00000) ++	269 mV (0000)	×	¥
1117/18	MGT_X0121/RA	6.400 Gbps	2.052013	100	3.5000-14	Reset	PRBS 7-bit	×	PRBS 7-bit v	0.00 dB (00000) V	0.00 dB (00000) 💠	269 mV (0000)	~	
1 120/18	MGT_X0T22/R0	6 400 Gbps	2.032013	100	2 506E 1 4	Reset	DDDC 7 HH	~	DDDC 7 hit	0.00 dB (00000) V	0.00 dB (00000) V	269 mV (0000)	~	
1123/18	MGT_XUY23/RX	6.400 Gbps	2.052013	150	3.500E-14	Reset	FRBS 7-DIL	~	PRBS 7-Dit V	0.00 dB (00000) 🗸	0.00 dB (00000) 🗢	269 mV (0000)	~	~
	MGL XUY37/RX	6.400 Gbps	2.913E13	UEU	1.691E-14	Reset]		PRBS 7-DIL V		0.00.45 (00000)	050		¥
	0Y3/TX 0Y1/TX 0Y2/TX 0Y0/TX 0Y26/TX 0Y26/TX 0Y26/TX 0Y26/TX 0Y26/TX 0Y26/TX 0Y38/TX 0Y39/TX 0Y39/TX 0Y39/TX 0Y39/TX 1Y1/TX 1Y1/TX 1Y1/TX 1Y1/TX 1Y1/TX	RX WGT_X0V3/RX WGT_X0V3/RX WGT_X0V3/RX V12/TX MGT_X0V3/RX V02/TX MGT_X0V2/RX V02/TX VGT_X0X VGT_X0X	PX Status 0Y3/TX MGT_X0Y3/RX 6.411 Gbps MGT_X0Y0/RX 6.413 Gbps VI/TX MGT_X0Y1/RX 6.413 Gbps 0Y1/TX MGT_X0Y1/RX 6.413 Gbps 0Y0/TX MGT_X0Y2/RX 6.413 Gbps 0Y0/TX MGT_X0Y2/RX 6.413 Gbps 0Y24/TX MGT_X0Y3/RX 6.413 Gbps 0Y38/TX MGT_X0Y3/RX 6.413 Gbps 0Y1/TX MGT_X0Y1/RX 6.400 Gbps 1Y12/TX MGT_X0Y1/RX 6.400 Gbps 1Y12/TX MGT_X0Y2/RX 6.400 Gbps 1Y207X MGT_X0Y2/RX 6.400 Gbps 1Y207X MGT_X0Y2/RX 6.400 Gbps	RX Status Bits 0Y3/TX MGT_X0Y3/RX 6.411 Gbps 5.51E13 0Y1/TX MGT_X0Y0/RX 6.413 Gbps 5.51E13 0Y1/TX MGT_X0Y0/RX 6.413 Gbps 5.51E13 0Y1/TX MGT_X0Y2/RX 6.413 Gbps 5.51E13 0Y0/TX MGT_X0Y2/RX 6.413 Gbps 5.51E13 0Y2/TX MGT_X0Y2/RX 6.413 Gbps 5.51E13 0Y2/TX MGT_X0Y2/RX 6.413 Gbps 5.51E31 0Y2/TX MGT_X0Y2/RX 6.413 Gbps 4.173E13 0Y2/FIX MGT_X0Y2/RX 6.413 Gbps 4.173E13 0Y2/FIX MGT_X0Y2/RX 6.413 Gbps 4.173E13 0Y2/FIX MGT_X0Y2/RX 6.413 Gbps 6.111E13 0Y2/FIX MGT_X0Y3/RX 6.413 Gbps 6.111E13 0Y3/FIX MGT_X0Y3/RX 6.413 Gbps 6.111E13 0Y3/FIX MGT_X0Y1/RX 6.400 Gbps 2.852E13 1Y1/FIX MGT_X0Y2/RX 6.400 Gbps 2.852E13 1Y1/FIX MGT_X0Y2/RX	RX Status Bits Errors 0Y3/TX MGT_X0Y3/RX 6.411 Gbps 9.44812 0.00 MGT_X0Y0/RX 6.413 Gbps 5.51E13 0.00 0Y3/TX MGT_X0Y0/RX 6.413 Gbps 5.51E13 0.00 0Y3/TX MGT_X0Y0/RX 6.413 Gbps 5.51E13 0.00 0Y3/TX MGT_X0Y2/RX 6.413 Gbps 5.913E13 0.00 0Y2/TX MGT_X0Y2/RX 6.413 Gbps 5.913E13 0.00 0Y2/TX MGT_X0Y2/RX 6.413 Gbps 4.173E13 3.00 0Y2/TX MGT_X0Y2/RX 6.413 Gbps 6.111E13 0.00 0Y3/TX MGT_X0Y3/RX 6.413 Gbps 6.111E13 0.00 0Y3/TX MGT_X0Y1/RX 6.400 Gbps 2.852E13 1.00 0Y1/TX	RX Status Bits Errors BER 0Y3/TX MGT_X0Y3/RX 6.411 Gbps 9.446112 0.00 1.058613 MGT_X0Y0/RX 6.413 Gbps 5.51613 0.00 1.815614 0Y1/TX MGT_X0Y0/RX 6.409 Gbps 5.51613 0.00 1.815614 0Y0/TX MGT_X0Y0/RX 6.416 Gbps 5.91813 0.00 1.815614 0Y0/TX MGT_X0Y0/RX 6.416 Gbps 5.91813 0.00 1.691614 0Y2/TX MGT_X0Y2/RX 6.413 Gbps 4.173613 360 7.189614 0Y2/TX MGT_X0Y2/RX 6.403 Gbps 4.173613 360 7.189614 0Y2/TX MGT_X0Y2/RX 6.403 Gbps 4.173613 360 7.189614 0Y2/TX MGT_X0Y2/RX 6.403 Gbps 4.173613 360 7.189614 0Y2/TX MGT_X0Y2/RX 6.413 Gbps 6.11613 060 1.636614 0Y2/TX MGT_X0Y2/RX 6.413 Gbps 6.11613 060 1.636614 0Y2/TX	RX Status Bits Errors BER BERT Reset 0Y3/TX MGT_X0Y3/RX 6.411 Gbps 9.44612 0.6661 1.656414 Reset MGT_X0Y3/RX 6.413 Gbps 5.51613 060 1.815614 Reset MGT_X0Y3/RX 6.409 Gbps 5.51613 060 1.815614 Reset 0Y1/TX MGT_X0Y3/RX 6.416 Gbps 5.51613 060 1.615614 Reset 0Y0/TX MGT_X0Y3/RX 6.416 Gbps 5.51613 060 1.615614 Reset 0Y2/TX MGT_X0Y2/RX 6.413 Gbps 5.913613 060 1.691614 Reset 0Y2/TX MGT_X0Y2/RX 6.403 Gbps 4.173613 360 7.189614 Reset 0Y2/TX MGT_X0Y2/RX 6.403 Gbps 4.173613 360 7.189614 Reset 0Y2/TX MGT_X0Y2/RX 6.413 Gbps 6.111613 060 1.636614 Reset 0Y2/TX MGT_X0Y2/RX 6.413 Gbps 6.111613 0601 1.636614	RX Status Bits Errors BER BERT Reset TX Pattern 0/3/TX MGT_X0/3/RX 6.411 Gbps 9.44812 0.00 1.056121 Reset PR85 7-bit MGT_X0/3/RX 6.413 Gbps 5.51E13 0C0 1.815E-14 Reset PR85 7-bit V0/1/TX MGT_X0/0/RX 6.413 Gbps 5.51E13 0C0 1.815E-14 Reset PR85 7-bit 0/0/1/X MGT_X0/0/RX 6.413 Gbps 5.51E13 0C0 1.815E-14 Reset PR85 7-bit 0/0/1/X MGT_X0/0/RX 6.413 Gbps 5.913E13 0C0 1.815E-14 Reset PR85 7-bit 0/0/2/X MGT_X0/2/4/RX 6.416 Gbps 4.173E13 3E0 7.189E-14 Reset PR85 7-bit 0/2/2/X MGT_X0/2/4/RX 6.413 Gbps 4.173E13 3E0 7.189E-14 Reset PR85 7-bit 0/2/2/X MGT_X0/2/4/RX 6.413 Gbps 6.111E13 0E0 1.68E-14 Reset PR85 7-bit 0/2/2/X MGT_X0/2/4/RX <t< th=""><th>RX Status Bits Errors BER BERT Reset TX Pattern 0'3/TX MGT_X0'3/RX All Gbps All Gbps All Gbps Pass Pass PBS 7-bit > MGT_X0'3/RX All Gbps S-51E13 OEO 1.015E-14 Reset PBS 7-bit > MGT_X0'0/RX 6.413 Gbps S-51E13 OEO 1.015E-14 Reset PBS 7-bit > 0Y/TX MGT_X0'0/RX 6.413 Gbps S-51E13 OEO 1.015E-14 Reset PBS 7-bit > 0Y/TX MGT_X0'0/RX 6.413 Gbps S.51E13 OEO 1.051E-14 Reset PBS 7-bit > 0Y/TX MGT_X0'2/RX 6.413 Gbps 5.1213 OEO 1.051E-14 Reset PBS 7-bit > 0Y/ZM MGT_X0'2/RX 6.413 Gbps 4.172E13 GEO 7.189E-14 Reset PBS 7-bit > 0Y/ZM MGT_X0'2/RX 6.403 Gbps 4.172E13 GEO 7.189E-14 Reset PBS 7-bit</th><th>RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern 0'3/TX MGT_X0Y3/RX All Gbps All Gbps All Gbps Pass Pass<!--</th--><th>RX Status Bits Errors BERT BERT Reset TX Pattern RX Pattern Patt</th><th>RX Status Bits Errors BERT Mester TX Patterm RX Patterm TX Patterm PRBS 7-bit 0.00 dB (00000) 0.00</th><th>RX Staus Bits Errors BER BERT Reset TX Pattern RX Pattern RX Pattern TX Post-Cursor PX Post-C</th><th>RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern RX Pattern TX Post-Cursor Status 0'3/TX MGT_X0Y3/RX All Gbps All Gbps All Gbps All Gbps Solar Obs Solar Obs Solar Obs Solar Obs Solar Obs Solar Obs Solar Solar Solar Solar Solar All Solar All Solar Solar All Solar Solar Solar Solar Solar Solar Solar Solar Solar Solar</th></th></t<>	RX Status Bits Errors BER BERT Reset TX Pattern 0'3/TX MGT_X0'3/RX All Gbps All Gbps All Gbps Pass Pass PBS 7-bit > MGT_X0'3/RX All Gbps S-51E13 OEO 1.015E-14 Reset PBS 7-bit > MGT_X0'0/RX 6.413 Gbps S-51E13 OEO 1.015E-14 Reset PBS 7-bit > 0Y/TX MGT_X0'0/RX 6.413 Gbps S-51E13 OEO 1.015E-14 Reset PBS 7-bit > 0Y/TX MGT_X0'0/RX 6.413 Gbps S.51E13 OEO 1.051E-14 Reset PBS 7-bit > 0Y/TX MGT_X0'2/RX 6.413 Gbps 5.1213 OEO 1.051E-14 Reset PBS 7-bit > 0Y/ZM MGT_X0'2/RX 6.413 Gbps 4.172E13 GEO 7.189E-14 Reset PBS 7-bit > 0Y/ZM MGT_X0'2/RX 6.403 Gbps 4.172E13 GEO 7.189E-14 Reset PBS 7-bit	RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern 0'3/TX MGT_X0Y3/RX All Gbps All Gbps All Gbps Pass Pass </th <th>RX Status Bits Errors BERT BERT Reset TX Pattern RX Pattern Patt</th> <th>RX Status Bits Errors BERT Mester TX Patterm RX Patterm TX Patterm PRBS 7-bit 0.00 dB (00000) 0.00</th> <th>RX Staus Bits Errors BER BERT Reset TX Pattern RX Pattern RX Pattern TX Post-Cursor PX Post-C</th> <th>RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern RX Pattern TX Post-Cursor Status 0'3/TX MGT_X0Y3/RX All Gbps All Gbps All Gbps All Gbps Solar Obs Solar Obs Solar Obs Solar Obs Solar Obs Solar Obs Solar Solar Solar Solar Solar All Solar All Solar Solar All Solar Solar Solar Solar Solar Solar Solar Solar Solar Solar</th>	RX Status Bits Errors BERT BERT Reset TX Pattern RX Pattern Patt	RX Status Bits Errors BERT Mester TX Patterm RX Patterm TX Patterm PRBS 7-bit 0.00 dB (00000) 0.00	RX Staus Bits Errors BER BERT Reset TX Pattern RX Pattern RX Pattern TX Post-Cursor PX Post-C	RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern RX Pattern TX Post-Cursor Status 0'3/TX MGT_X0Y3/RX All Gbps All Gbps All Gbps All Gbps Solar Obs Solar Obs Solar Obs Solar Obs Solar Obs Solar Obs Solar Solar Solar Solar Solar All Solar All Solar Solar All Solar Solar Solar Solar Solar Solar Solar Solar Solar Solar

8.5 IBERT Slot no 12, this test@6.4Gbps covered the area:

- 6 lanes of MGT data from the FEX slot 12

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Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	F	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE En
Ungrouped Links (0)														
							Reset	1	P	PRBS 7-bit 🗸				
% Link 0		MGT X0Y3/RX	6.413 Gbps	5.682E14	0E0	1.76E-15	Reset	ĩ	P	PRBS 7-bit 🗸				
- 🚯 HUB: MiniPods (4)							Reset	ĩ	P	PRBS 7-bit ↓				
% Link 1		MGT X0Y0/RX	6.413 Gbps	5.69E14	0E0	1.758E-15	Reset	ĩ	P	PRBS 7-bit 🗸				
% Link 2		MGT X0Y1/RX	6.416 Gbps	5.69E14	0E0	1.758E-15	Reset	í	P	PRBS 7-bit 🗸				
% Link 3		MGT X0Y2/RX	6.403 Gbps	5.69E14	0E0	1.758E-15	Reset	i	P	PRBS 7-bit 🗸				
% Link 4		MGT X0Y0/BX	6.410 Gbps	5.69E14	0E0	1.758E-15	Reset	i	P	PRBS 7-bit 🗸				
WHUB: Other Hub RO (2)							Reset	PRBS 7-bit	V P	PRBS 7-bit 🗸	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000) 🗸	
% Link 74	MGT X0Y38/T		6.410 Gbps	5.68E14	0E0	1.76E-15	Reset	PBBS 7-bit	- P	PBBS 7-bit	0.00 dB (00000) v	6.02 dB (10100) 🗸	846 mV (11000)	
9 Link 76	MGT X0V39/T	MGT YOV39/R	6.413 Gbps	5.68E14	0E0	1.761E-15	Reset	PBBS 7-bit	U P	PBBS 7-bit	0.00 dB (00000) v	6.02 dB (10100)	846 mV (11000)	
HUB: Combined Data from Other HUB (1)			Contro onpo				Reset	1	P	PBBS 7-bit				
9 Link 2		MGT YOVL/RY	6.416 Gbps	5.68E14	OEO	1 76E-15	Reset	1	P	PBBS 7-bit				
HUB: Data from FEX 12 (6)		MOT_XOT1/100	0.410 0000	5.00214	020	1.702.15	Reset	1	P	PBBS 7-bit				
S Link 0		MGT YOVI 4/P	6 413 Ghns	5.673E14	2E0	3 526E-15	Reset	1	P	PBBS 7-bit				
S Link 1		MGT_X0114/10	6 410 Gbps	5.673E14	2E0	3 526E-15	Reset	-		PRBS 7-bit				
S Link 2		MGT_X0115/R	6.410 Gbps	5.672614	200	2 5265-15	Reset	1		PPRS 7-bit				
% Link 3		MGT_X0110/R	6.416 Gbps	5.673E14	2E0	3.526E-15	Reset	1	P	PRBS 7-bit				
S Link 4		MGT_X0117/R	6 410 Gbps	5.672E14	200	2 5265-15	Reset	1	-	PRES 7-bit				
To Link 4		MGT_X0118/R	6.419 Gbps	5.073E14	200	3.3202-13	Reset	1	-	-R837-bit 🗸				
 BOD, Data from EEV 10 and 0 links from U. 		MG1_X0Y19/H	0.410 Obbs	5.673E14	260	3.526E-15	Reset		-	-R857-bit 🗸	Marchine La	Marchine Inc.	Markin In	
 We have a set of the set of the			6 400 Char	5 604514	050	0.5105.15	Reset	Multiple	P	RBS 7-DIL V	Multiple	Multiple	Multiple	
S LINK 56	MGT_X0Y4/TX	MGT_X0Y12/R	6.400 Gbps	5.684E14	2E0	3.519E-15	Reset	PRBS 7-Dit	V P	PRBS 7-Dit V	0.00 dB (00000) V	6.02 dB (10100) V	846 mV (11000) V	
No Link 57	MGT_X0Y4/1X	MGT_X0Y13/R	6.400 Gbps	5.664E14	2E0	3.519E-15	Reset	DDDC 7 F*	V P	noszikit	0.00 dB (00000) V	0.00 dB (00000) V	950 mV (1100) V	
% LINK 38	MGT_X0Y5/TX	MGT_X0Y14/R	6.400 Gbps	5.684E14	2E0	3.519E-15	Keset	PRBS 7-DIT	× P	rkssi/-bit ∨	0.00 dB (00000) ~	0.00 dB (00000) V	269 mV (0000) V	
% LINK 59	MGT_X0Y5/TX	MGT_X0Y15/R	6.400 Gbps	5.684E14	2E0	3.519E-15	Reset	PRBS 7-bit	V P	-RBS /-bit v	0.00 dB (00000) V	6.02 dB (10100) V	846 mv (11000) V	
S LINK 60	MGT_X0Y6/TX	MGT_X0Y16/R	6.400 Gbps	5.684E14	2E0	3.519E-15	Reset	PRBS 7-DIt	~ P	-RBS /-DIT V	0.00 dB (00000) V	0.00 dB (00000) V	269 mV (0000) V	
% LINK 61	MGT_X0Y7/TX	MGT_X0Y17/R	6.400 Gbps	5.684E14	2E0	3.519E-15	Reset	PRBS /-bit	✓ P	rk⊌S /-bit ∨	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	269 mV (0000) 🗸	
% LINK 101		MGT_X0Y37/R	6.400 Gbps	5.684E14	0E0	1.759E-15	Reset]	P	rk⊌S 7-bit ∨				
S LINK 102	MGT_X0Y0/TX	MGT_X0Y36/R	6.400 Gbps	5.684E14	OEO	1.759E-15	Reset	PRBS 7-bit	~ P	PRBS 7-bit 🗸	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100) V	

8.6 IBERT Slot no 13, this test@6.4Gbps covered the area:

- 6 lanes of MGT data from the FEX slot 13

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ile <u>E</u> dit <u>T</u> ools <u>W</u> indow Layout <u>V</u> iew <u>H</u>	elp <u>Q- Quid</u>	k Access														
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ARDWARE MANAGER - localhost/xilinx_tcf/Digilent/21	0299A57644															
Fcl Console Messages Serial I/O Links ×	Serial I/O Sc	ans													?	_ 0
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Name	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern		RX Pattern		TX Pre-Cursor	TX Post-Cursor	TX Diff Swing		DFE Enabled	
🕒 Ungrouped Links (0)																
 HUB: FEX_slot_13 (10) 						Reset	PRBS 7-bit	\sim	PRBS 7-bit	~	0.00 dB (00000) 🗸	Multiple 🗸	Multiple	~	· 🗸	
% Link 0	MGT_X0Y0/RX	6.413 Gbps	5.708E13	0E0	1.752E-14	Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (1100)0) ~	· 🗸	
% Link 1	MGT_X0Y0/RX	6.427 Gbps	5.708E13	0E0	1.752E-14	Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100)) ~	· 🗸	
% Link 3	MGT_X0Y1/RX	6.413 Gbps	5.708E13	0E0	1.752E-14	Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	0.00 dB (00000) ~	950 mV (1100)) ~	, 🗸	
% Link 5	MGT_X0Y2/RX	6.413 Gbps	5.708E13	0E0	1.752E-14	Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100)) ~	/	
% Link 9	MGT_X0Y4/RX	6.410 Gbps	5.708E13	1E0	1.752E-14	Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100)) ~	, 🗸	
% Link 11	MGT_X0Y5/RX	6.413 Gbps	5.708E13	1E0	1.752E-14	Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100)) ~	· 🗸	
% Link 13	MGT_X0Y6/RX	6.409 Gbps	5.708E13	1E0	1.752E-14	Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100)) ~	/	
% Link 15	MGT_X0Y7/RX	6.413 Gbps	5.708E13	1E0	1.752E-14	Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100)) ~	· 🗸	
% Link 41	MGT_X0Y20/RX	6.413 Gbps	5.708E13	1E0	1.752E-14	Reset	PRBS 7-bit	\mathbf{v}	PRBS 7-bit	~	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100)) 🗸	1 🗹	
% Link 43	MGT_X0Y21/RX	6.413 Gbps	5.708E13	1E0	1.752E-14	Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100)) ~	· 🗸	
						Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	Multiple 🗸	Multiple	~	, 🗸	
% Link 86	MGT_X0Y6/RX	6.400 Gbps	5.735E13	1E0	1.744E-14	Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (1100)0) ~	, 🗸	
% Link 87	MGT_X0Y7/RX	6.400 Gbps	5.735E13	1E0	1.744E-14	Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100)) ~	/	
% Link 88	MGT_X0Y8/RX	6.400 Gbps	5.735E13	1E0	1.744E-14	Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	269 mV (0000	n) ~	/	
% Link 89	MGT_X0Y9/RX	6.400 Gbps	5.735E13	1E0	1.744E-14	Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (1100)0) ~	· 🗸	
% Link 90	MGT_X0Y10/RX	6.400 Gbps	5.735E13	1E0	1.744E-14	Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	269 mV (0000	n) ~	/	
% Link 91	MGT_X0Y11/RX	6.400 Gbps	5.735E13	1E0	1.744E-14	Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (1100)0) ~	, 🖌	
w ROD: Hub Readout AL_0 to This ROD (1)						Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	269 mV (0000	n) ~	· 🗸	
% Link 161	MGT_X0Y37/RX	6.400 Gbps	5.7E13	1E0	1.754E-14	Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	269 mV (0000)) ~	, 🖌	
						Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	Multiple v	Multiple	~	/	
% Link 167	MGT_X0Y39/RX	6.413 Gbps	1.532E13	1E0	6.528E-14	Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	269 mV (0000	n) ~	/	
% Link 168	MGT_X0Y38/RX	6.416 Gbps	1.528E13	1E0	6.546E-14	Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (1100)0) ~	/	
Sombined_Data_From_Other_Hub (1)						Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	269 mV (0000	n) ~	/	
% Link 170	MGT_X0Y1/RX	6.413 Gbps	5.388E13	1E0	1.856E-14	Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	269 mV (0000)) ~	, 🗸	
% Transmitter_HUB_Readout_AL_to_Other_HUB (2)						Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (1100)0) ~	· 🗸	
🗞 Link 171	MGT_X0Y0/RX	No Link	8.707E12	4.11E12	4.72E-1	Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (1100)0) ~	, 🗸	
🗞 Link 172	MGT_X0Y1/RX	No Link	8.689E12	4.367E12	5.026E-1	Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (1100)0) 🗸	· 🗸	
System 2 - State - Sta						Reset	PRBS 7-bit	\sim	PRBS 7-bit	~	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (1100)0) ~	, 🖉	
🗞 Link 173	MGT_X0Y2/RX	No Link	5.732E13	2.846E13	4.965E-1	Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (1100	10) v	· 🗸	
System 2 - State - Combined_Data_to_FEX_13 (1) System 2 - State -						Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100	n ~	/	
🐌 Link 174	MGT_X0Y2/RX	No Link	5.618E13	2.798E13	4.981E-1	Reset	PRBS 7-bit	\sim	PRBS 7-bit	\sim	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100	n) ~	· 🗸	

8.7 IBERT Slot no 14, this test@6.4Gbps covered the area:

- 6 lanes of MGT data from the FEX slot 14

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TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern		TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enat
						Reset	1	PRBS 7-bit	~				1
	MGT X0Y3/RX	6.413 Gbps	7.051E12	0E0	1.418E-13	Reset	1	PRBS 7-bit	~				1
						Reset	1	PRBS 7-bit	~				
	MGT X0Y0/RX	6.411 Gbps	7.243E12	0E0	1.381E-13	Reset	ī	PRBS 7-bit	~				1
	MGT X0Y1/RX	6.413 Gbps	7.243E12	0E0	1.381E-13	Reset	i i	PRBS 7-bit	~				1
	MGT X0Y2/RX	6.409 Gbps	7.243E12	0E0	1.381E-13	Reset	1	PRBS 7-bit	~				1
	MGT X0Y0/RX	6.405 Gbps	7.243E12	0E0	1.381E-13	Reset	i i	PRBS 7-bit	~				1
						Reset	PRBS 7-bit	 PRBS 7-bit 	~	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000) ↓	1
MGT X0Y38/T	X MGT X0Y38/R	6.413 Gbps	3.497E13	0E0	2.859E-14	Reset	PRBS 7-bit	 PRBS 7-bit 	~	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000) 🗸	1
MGT X0Y39/T	X MGT X0Y39/R	6.414 Gbps	3.497E13	0E0	2.859E-14	Reset	PRBS 7-bit	PRBS 7-bit	~	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000) ↓	1
						Reset	ī	PRBS 7-bit	~				1
	MGT X0Y1/RX	6.413 Gbps	3.498E13	0E0	2.859E-14	Reset	ī	PRBS 7-bit	~				1
						Reset	1	PRBS 7-bit	~				1
	MGT X0Y8/RX	6.410 Gbps	1.249E13	2E0	1.602E-13	Reset	ĩ	PRBS 7-bit	~				1
	MGT X0Y9/RX	6.413 Gbps	1.249E13	2E0	1.602E-13	Reset	1	PRBS 7-bit	~				1
	MGT X0Y10/R	6.404 Gbps	1.249E13	2E0	1.602E-13	Reset	ĩ	PRBS 7-bit	~				1
	MGT X0Y11/R	6.413 Gbps	1.249E13	2E0	1.602E-13	Reset	1	PRBS 7-bit	~				1
	MGT X0Y12/R	6.413 Gbps	1.249E13	2E0	1.602E-13	Reset	ī	PRBS 7-bit	\sim				1
	MGT X0Y13/R	6.413 Gbps	1.249E13	2E0	1.602E-13	Reset	ī	PRBS 7-bit	~				1
						Reset	Multiple	PRBS 7-bit	~	Multiple	Multiple	Multiple	1
MGT X0Y0/TX	MGT X0Y0/RX	6.400 Gbps	7.261E12	2E0	2.755E-13	Reset	PRBS 7-bit	PRBS 7-bit	~	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	269 mV (0000) v	1
MGT X0Y1/TX	MGT X0Y1/RX	6.400 Gbps	7.261E12	2E0	2.755E-13	Reset	PRBS 7-bit	 PRBS 7-bit 	~	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	269 mV (0000) ↓	1
MGT X0Y2/TX	MGT X0Y2/RX	6.400 Gbps	7.261E12	2E0	2.755E-13	Reset	PRBS 7-bit	 PRBS 7-bit 	\sim	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	269 mV (0000) ↓	1
MGT_X0Y2/TX	MGT_X0Y3/RX	6.400 Gbps	7.261E12	2E0	2.755E-13	Reset	PRBS 7-bit	PRBS 7-bit	~	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000) ↓	1
MGT X0Y3/TX	MGT X0Y4/RX	6.400 Gbps	7.261E12	2E0	2.755E-13	Reset	PRBS 7-bit	 PRBS 7-bit 	\sim	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	269 mV (0000) ↓	1
MGT_X0Y3/TX	MGT_X0Y5/RX	6.400 Gbps	7.261E12	2E0	2.755E-13	Reset	PRBS 7-bit	 PRBS 7-bit 	~	0.00 dB (00000) 🗸	6.02 dB (10100) 🗸	846 mV (11000) 🗸	1
	MGT X0Y37/R	6.400 Gbps	7.261E12	0E0	1.377E-13	Reset	ī	PRBS 7-bit	~				1
	NOT YOURCED	6 400 Ghns	7.261E12	0E0	1.377E-13	Reset	PRBS 7-bit	 PRBS 7-bit 	~	0.00 dB (00000) 🗸	0.00 dB (00000) 🗸	950 mV (1100)	
	Serial I/O TX 4GT_X0Y38/T 4GT_X0Y39/T 4GT_X0Y39/T 4GT_X0Y1/TX 4GT_X0Y1/TX 4GT_X0Y3/TX 4GT_X0Y3/TX	Serial I/O Scans TX RX MGT_X0V3/RX MGT_X0V3/RX MGT_X0V3/RX MGT_X0V1/RX MGT_X0V3/RX MGT_X0V3/RX MGT_X0V3/RX MGT_X0V3/RX MGT_X0V3/RX MGT_X0V3/RX MGT_X0V3/RX MGT_X0V3/RX MGT_X0V3/RX MGT_X0V3/RX MGT_X0V3/RX MGT_X0V3/RX MGT_X0V1/RX MGT_X0V1/RX MGT_X0V1/RX MGT_X0V1/RX MGT_X0V1/RX MGT_X0V1/RX MGT_X0V1/RX MGT_X0V1/RX MGT_X0V1/RX MGT_X0V1/RX MGT_X0V1/RX MGT_X0V0/RX MGT_X0V1/RX MGT_X0V0/RX MGT_X0V2/RX MGT_X0V2/RX MGT_X0V2/RX MGT_X0V2/RX MGT_X0V2/RX MGT_X0V2/RX MGT_X0V2/RX MGT_X0V2/RX MGT_X0V2/RX MGT_X0V2/RX	Serial I/O Scans TX RX Status MGT_X0Y3/RX 6.413 Gbps MGT_X0Y1/RX 6.413 Gbps MGT_X0Y1/RX 6.413 Gbps MGT_X0Y1/RX 6.413 Gbps MGT_X0Y2/RX 6.409 Gbps MGT_X0Y0/RX 6.413 Gbps MGT_X0Y0/RX 6.413 Gbps MGT_X0Y3/RX 6.413 Gbps MGT_X0Y3/RX 6.413 Gbps MGT_X0Y3/RX 6.413 Gbps MGT_X0Y1/RX 6.400 Gbps MGT_X0Y2/RX 6.400 Gbps	Serial I/O Scans TX RX Status BIts MGT_X0Y3/RX 6.413 Gbps 7.051E12 MGT_X0Y3/RX 6.413 Gbps 7.051E12 MGT_X0Y3/RX 6.413 Gbps 7.243E12 MGT_X0Y1/RX 6.413 Gbps 7.243E12 MGT_X0Y1/RX 6.413 Gbps 7.243E12 MGT_X0Y3/RX 6.403 Gbps 7.243E12 MGT_X0Y3/RX 6.403 Gbps 7.243E12 MGT_X0Y3/RX 6.413 Gbps 3.497E13 MGT_X0Y3/RX 6.413 Gbps 3.497E13 MGT_X0Y1/RX 6.413 Gbps 1.249E13 MGT_X0Y1/RX 6.404 Gbps 1.249E13 MGT_X0Y1/RX 6.400 Gbps 7.261E12 MGT_X0Y1/RX 6.400 Gbps 7.261E12 MGT_X0Y3/RX 6.400 Gbps 7.261E12 MGT_X0Y3/RX	Serial VO Scans RX Status Bits Errors MGT_X0Y3/PX 6.413 Gbps 7.051E12 0E0 MGT_X0Y0/PX 6.411 Gbps 7.243E12 0E0 MGT_X0Y0/PX 6.413 Gbps 7.243E12 0E0 MGT_X0Y0/PX 6.405 Gbps 7.243E12 0E0 MGT_X0Y0/PX 6.405 Gbps 7.243E12 0E0 MGT_X0Y3/PX 6.405 Gbps 7.243E12 0E0 MGT_X0Y3/PX 6.405 Gbps 7.243E12 0E0 MGT_X0Y3/PX 6.413 Gbps 3.497E13 0E0 MGT_X0Y1/PX 6.413 Gbps 3.497E13 0E0 MGT_X0Y1/PX 6.413 Gbps 1.249E13 2E0 MGT_X0Y1/PX 6.400 Gbps 7.261E12 2E0 MGT_X0Y1/PX 6.400 Gbps 7.261E12 2E0 MGT_X0Y1/PX 6.400 G	Serial I/O Scans Status Bits Errors BER TX RX Status Bits Errors BER MGT_X0Y3/RX 6.413 Gbps 7.03E12 0E0 1.418E13 MGT_X0Y1/RX 6.413 Gbps 7.243E12 0E0 1.381E-13 MGT_X0Y1/RX 6.413 Gbps 7.243E12 0E0 1.381E-13 MGT_X0Y3/RX 6.413 Gbps 7.243E12 0E0 1.381E-13 MGT_X0Y3/RX 6.413 Gbps 7.243E12 0E0 1.381E-13 MGT_X0Y3/RX 6.413 Gbps 3.497E13 0E0 2.859E-14 MGT_X0Y3/RX 6.413 Gbps 3.497E13 0E0 2.859E-14 MGT_X0Y3/RX 6.413 Gbps 3.497E13 0E0 2.859E-14 MGT_X0Y1/RX 6.413 Gbps 1.249E13 2E0 1.602E-13 MGT_X0Y1/RX 6.413 Gbps 1.249E13 2E0 1.602E-13 MGT_X0Y1/RX 6.413 Gbps 1.249E13 2E0 1.602E-13 MGT_X0Y1/RX 6.404 Gbps 1.249E13 <t< td=""><td>Serial I/O Scans Status Bits Errors BER BERT Reset TX RX Status Bits Errors BER BERT Reset MGT_X0Y3/RX 6.413 Gbps 7.051E12 0E0 1.418E13 Reset MGT_X0Y3/RX 6.413 Gbps 7.243E12 0E0 1.381E-13 Reset MGT_X0Y1/RX 6.413 Gbps 7.243E12 0E0 1.381E-13 Reset MGT_X0Y1/RX 6.413 Gbps 7.243E12 0E0 1.381E-13 Reset MGT_X0Y0/RX 6.413 Gbps 7.243E12 0E0 1.381E-13 Reset MGT_X0Y0/RX 6.413 Gbps 3.497E13 0E0 2.859E-14 Reset MGT_X0Y3/RX 6.413 Gbps 3.497E13 0E0 2.859E-14 Reset MGT_X0Y3/RX 6.413 Gbps 1.49E13 2E0 1.602E-13 Reset MGT_X0Y1/RX 6.413 Gbps 1.49E13 2E0 1.602E-13 Reset MGT_X0Y1/RX 6.413 Gbps 1.249E13 2E0 1.602E-13</td><td>Serial VO Scans RX Status Bits Errors BER BERT Reset TX Pattern MGT_X073/RX 6.413 Gbps 7.051E12 0E0 1.418E-13 Reset Reset MGT_X073/RX 6.413 Gbps 7.243E12 0E0 1.381E-13 Reset Reset MGT_X070/RX 6.413 Gbps 7.243E12 0E0 1.381E-13 Reset Reset</td><td>Serial VO Scans RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern MGT_X0Y3/RX 6.413 Gbps 7.051E12 0E0 1.418E-13 Reset PR85 7-bit MGT_X0Y3/RX 6.413 Gbps 7.243E12 0E0 1.381E-13 Reset PR85 7-bit MGT_X0Y0/RX 6.413 Gbps 7.243E12 0E0 1.381E-13 Reset PR85 7-bit MGT_X0Y0/RX 6.403 Gbps 7.243E12 0E0 1.381E-13 Reset PR85 7-bit MGT_X0Y0/RX 6.403 Gbps 7.243E12 0E0 1.381E-13 Reset PR85 7-bit MGT_X0Y0/RX 6.403 Gbps 7.243E12 0E0 1.381E-13 Reset PR85 7-bit MGT_X0Y0/RX 6.413 Gbps 3.497E13 0E0 2.859E-14 Reset PR85 7-bit PR85 7-bit</td><td>Serial VO Scans RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern MGT_X0Y3/RX 6.413 Gbps 7.051E12 0E0 1.418E-13 Reset PR85 7-bit > MGT_X0Y3/RX 6.413 Gbps 7.051E12 0E0 1.418E-13 Reset PR85 7-bit > MGT_X0Y0/RX 6.413 Gbps 7.248E12 0E0 1.381E-31 Reset PR85 7-bit > MGT_X0Y0/RX 6.403 Gbps 7.248E12 0E0 1.381E-31 Reset PR85 7-bit > MGT_X0Y0/RX 6.403 Gbps 7.248E12 0E0 1.381E-31 Reset PR85 7-bit > MGT_X0Y0/RX 6.403 Gbps 7.249E12 0E0 1.381E-31 Reset PR85 7-bit > MGT_X0Y0/RX 6.413 Gbps 3.497E13 0E0 2.859E-14 Reset PR85 7-bit > MGT_X0Y0/RX 6.413 Gbps 1.249E13 2E0 1.602E-13 Reset PR85 7-bit > MGT_X0Y1/RX</td><td>Serial VO Scans RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern TX Pre-Cursor MGT_X0Y3/RX 6.413 Gbps 7.051E12 0E0 1.418E-13 Reset YPR85 7-bit > MGT_X0Y3/RX 6.413 Gbps 7.24E12 0E0 1.381E-31 Reset PR85 7-bit > MGT_X0Y0/RX 6.413 Gbps 7.24E12 0E0 1.381E-31 Reset PR85 7-bit > MGT_X0Y0/RX 6.403 Gbps 7.24E12 0E0 1.381E-31 Reset PR85 7-bit > MGT_X0Y0/RX 6.403 Gbps 7.24E12 0E0 1.381E-31 Reset PR85 7-bit > 0.00 dB (00000) > MGT_X0Y0/RX 6.403 Gbps 7.24F12 0E0 2.859E-14 Reset PR85 7-bit > 0.00 dB (00000) > MGT_X0Y3/RX MGT_X0Y3/RX 6.413 Gbps 3.49F13 0E0 2.859E-14 Reset PR85 7-bit > 0.00 dB (00000) > MGT_X0Y3/RX 6.413 Gbps 1.49E13</td><td>Serial VO Scans RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern TX Pre-Cursor TX Post-Cursor MGT_X0Y3/RX 6.413 Gbps 7.051E12 OEO 1.418E-13 Reset PR85 7-bit ></td><td>Serial VO Scans FX Status Bits Errors BER BERT Reset TX Pattern RX Pattern TX Pre-Cursor TX Post-Cursor TX Post-Cursor TX Diff Swing MGT_X0Y3/RX 6.413 Gbps 7.051E12 0E0 1.418E13 Reset PR85 7-bit ></td></t<>	Serial I/O Scans Status Bits Errors BER BERT Reset TX RX Status Bits Errors BER BERT Reset MGT_X0Y3/RX 6.413 Gbps 7.051E12 0E0 1.418E13 Reset MGT_X0Y3/RX 6.413 Gbps 7.243E12 0E0 1.381E-13 Reset MGT_X0Y1/RX 6.413 Gbps 7.243E12 0E0 1.381E-13 Reset MGT_X0Y1/RX 6.413 Gbps 7.243E12 0E0 1.381E-13 Reset MGT_X0Y0/RX 6.413 Gbps 7.243E12 0E0 1.381E-13 Reset MGT_X0Y0/RX 6.413 Gbps 3.497E13 0E0 2.859E-14 Reset MGT_X0Y3/RX 6.413 Gbps 3.497E13 0E0 2.859E-14 Reset MGT_X0Y3/RX 6.413 Gbps 1.49E13 2E0 1.602E-13 Reset MGT_X0Y1/RX 6.413 Gbps 1.49E13 2E0 1.602E-13 Reset MGT_X0Y1/RX 6.413 Gbps 1.249E13 2E0 1.602E-13	Serial VO Scans RX Status Bits Errors BER BERT Reset TX Pattern MGT_X073/RX 6.413 Gbps 7.051E12 0E0 1.418E-13 Reset Reset MGT_X073/RX 6.413 Gbps 7.243E12 0E0 1.381E-13 Reset Reset MGT_X070/RX 6.413 Gbps 7.243E12 0E0 1.381E-13 Reset Reset	Serial VO Scans RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern MGT_X0Y3/RX 6.413 Gbps 7.051E12 0E0 1.418E-13 Reset PR85 7-bit MGT_X0Y3/RX 6.413 Gbps 7.243E12 0E0 1.381E-13 Reset PR85 7-bit MGT_X0Y0/RX 6.413 Gbps 7.243E12 0E0 1.381E-13 Reset PR85 7-bit MGT_X0Y0/RX 6.403 Gbps 7.243E12 0E0 1.381E-13 Reset PR85 7-bit MGT_X0Y0/RX 6.403 Gbps 7.243E12 0E0 1.381E-13 Reset PR85 7-bit MGT_X0Y0/RX 6.403 Gbps 7.243E12 0E0 1.381E-13 Reset PR85 7-bit MGT_X0Y0/RX 6.413 Gbps 3.497E13 0E0 2.859E-14 Reset PR85 7-bit PR85 7-bit	Serial VO Scans RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern MGT_X0Y3/RX 6.413 Gbps 7.051E12 0E0 1.418E-13 Reset PR85 7-bit > MGT_X0Y3/RX 6.413 Gbps 7.051E12 0E0 1.418E-13 Reset PR85 7-bit > MGT_X0Y0/RX 6.413 Gbps 7.248E12 0E0 1.381E-31 Reset PR85 7-bit > MGT_X0Y0/RX 6.403 Gbps 7.248E12 0E0 1.381E-31 Reset PR85 7-bit > MGT_X0Y0/RX 6.403 Gbps 7.248E12 0E0 1.381E-31 Reset PR85 7-bit > MGT_X0Y0/RX 6.403 Gbps 7.249E12 0E0 1.381E-31 Reset PR85 7-bit > MGT_X0Y0/RX 6.413 Gbps 3.497E13 0E0 2.859E-14 Reset PR85 7-bit > MGT_X0Y0/RX 6.413 Gbps 1.249E13 2E0 1.602E-13 Reset PR85 7-bit > MGT_X0Y1/RX	Serial VO Scans RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern TX Pre-Cursor MGT_X0Y3/RX 6.413 Gbps 7.051E12 0E0 1.418E-13 Reset YPR85 7-bit > MGT_X0Y3/RX 6.413 Gbps 7.24E12 0E0 1.381E-31 Reset PR85 7-bit > MGT_X0Y0/RX 6.413 Gbps 7.24E12 0E0 1.381E-31 Reset PR85 7-bit > MGT_X0Y0/RX 6.403 Gbps 7.24E12 0E0 1.381E-31 Reset PR85 7-bit > MGT_X0Y0/RX 6.403 Gbps 7.24E12 0E0 1.381E-31 Reset PR85 7-bit > 0.00 dB (00000) > MGT_X0Y0/RX 6.403 Gbps 7.24F12 0E0 2.859E-14 Reset PR85 7-bit > 0.00 dB (00000) > MGT_X0Y3/RX MGT_X0Y3/RX 6.413 Gbps 3.49F13 0E0 2.859E-14 Reset PR85 7-bit > 0.00 dB (00000) > MGT_X0Y3/RX 6.413 Gbps 1.49E13	Serial VO Scans RX Status Bits Errors BER BERT Reset TX Pattern RX Pattern TX Pre-Cursor TX Post-Cursor MGT_X0Y3/RX 6.413 Gbps 7.051E12 OEO 1.418E-13 Reset PR85 7-bit >	Serial VO Scans FX Status Bits Errors BER BERT Reset TX Pattern RX Pattern TX Pre-Cursor TX Post-Cursor TX Post-Cursor TX Diff Swing MGT_X0Y3/RX 6.413 Gbps 7.051E12 0E0 1.418E13 Reset PR85 7-bit >
Config ver	HUB FW features	Status											
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1	Readout Control (Readout_Ctrl) data from the ROD; Combined_TTC/Data to This ROD; Combined_TTC/Data to FEX 3.	Done											
2	Readout Control (Readout_Ctrl) data from the ROD; Combined_TTC/Data to This ROD; Combined_TTC/Data to FEX 3, Readout data from FEX 3 (Aurora8b10b)	In progress											
3	Readout Control (Readout_Ctrl) data from the ROD; Combined_TTC/Data to This ROD, Combined to FEX 3, Readout data from FEX 3 (Aurora8b10b);	waiting											
4	Readout Control (Readout_Ctrl) data from the ROD; Combined_TTC/Data to This ROD, Combined_TTC/Data to FEX 3, Readout data from the FEX 3 (Aurora 8b10b); Readout data from FEX 13 (Aurora8b10b)	waiting											
5	Readout Control (Readout_Ctrl) data from the ROD; Combined_TTC/Data to This ROD; Combined_TTC/data to FEX 3, Readout data from FEX 3 (Aurora 8b10b); Readout data from FEX 13 (Aurora8b10b); Combined_TTC/Data to Other HUB	waiting											
6	Readout Control (Readout_Ctrl) data from the ROD; Combined_TTC/Data to This ROD; Combined_TTC/data to FEX 3, Readout data from FEX 3 (Aurora 8b10b); Readout data from FEX 13 (Aurora8b10b); Combined_TTC/Data to Other HUB; Readout AL_0 data to This ROD; Readout AL_1 data to This ROD	waiting											
7	Readout Control (Readout_Ctrl) data from the ROD; Combined_TTC/Data to This ROD; Combined_TTC/data to FEX 3, Readout data from FEX 3 (Aurora 8b10b); Readout data from FEX 13 (Aurora8b10b); Combined_TTC/Data to Other HUB; Readout AL_0 data to This ROD; Readout AL_1 data to This ROD; Readout AL_0 data to Other HUB; Readout AL_1 data to Other HUB;	waiting											
8	Readout Control (Readout_Ctrl) data from the ROD; Combined_TTC/Data to This ROD; Combined_TTC/data all FEXs, Readout data from all FEXs (Aurora 8b10b); Combined_TTC/Data to Other HUB; Readout AL_0 data to This ROD; Readout AL_1 data to This ROD; Readout AL_0 data to Other HUB; Readout AL_1 data to Other HUB;	waiting											
9	Readout Control (Readout_Ctrl) data from the ROD; Combined_TTC/Data to This ROD; Combined_TTC/data all FEXs, Readout data from all FEXs (Aurora 8b10b); Combined_TTC/Data to Other HUB; Readout AL_0 data to This ROD; Readout AL_1 data to This ROD; Readout AL_0 data to Other HUB; Readout AL_1 data to Other HUB; IPBus component	waiting											

9.0 HUB FW development plans (this list is in progress)

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