FEX System
ATCA Hub Module: Overview & Hardware Description

Hub Team
Michigan State University

Hub Final Design Review
March 20, 2018

Plan for Today's Review

- This Talk: Overview of the Hub prototype module
  - Status of hardware & firmware
  - Overview of core functions & their implementation

- Next Talk: Hub hardware tests
  - Description of completed tests
  - Plans for further testing

- Last Talk: Hub firmware overview
  - Current status
  - Development plans

Hub Team

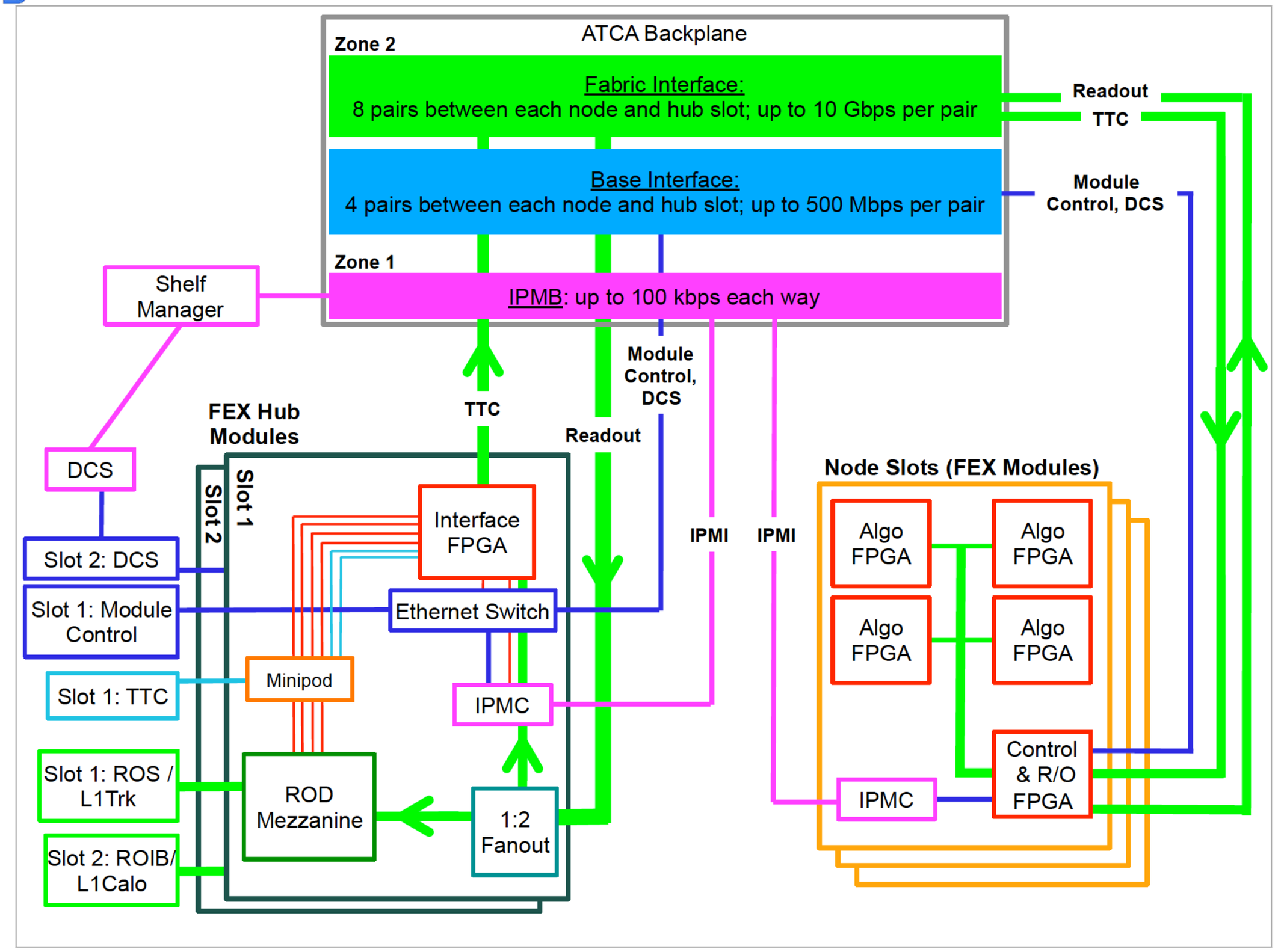
- Many years of experience on the team
  - Dan Edmunds
  - Philippe Laurens
  - Yuri Ermoline
  - Pawel Plucinski
  - Brian Ferguson
  - Spencer Lee

Review Documentation

- Hub hardware specification
  - Updated description of core function implementation
    - Several features not concrete at Preliminary Design Review
  - Detailed descriptions of hardware design
    - Appendices dedicated to each design aspect
  - Summary of Hub test results
    - Details of test plan, description of further planned tests

- Hub firmware specification
  - Description of firmware requirements
    - Overview of interfaces and future needs
  - Details of FW implementation
    - Focus on external interfaces

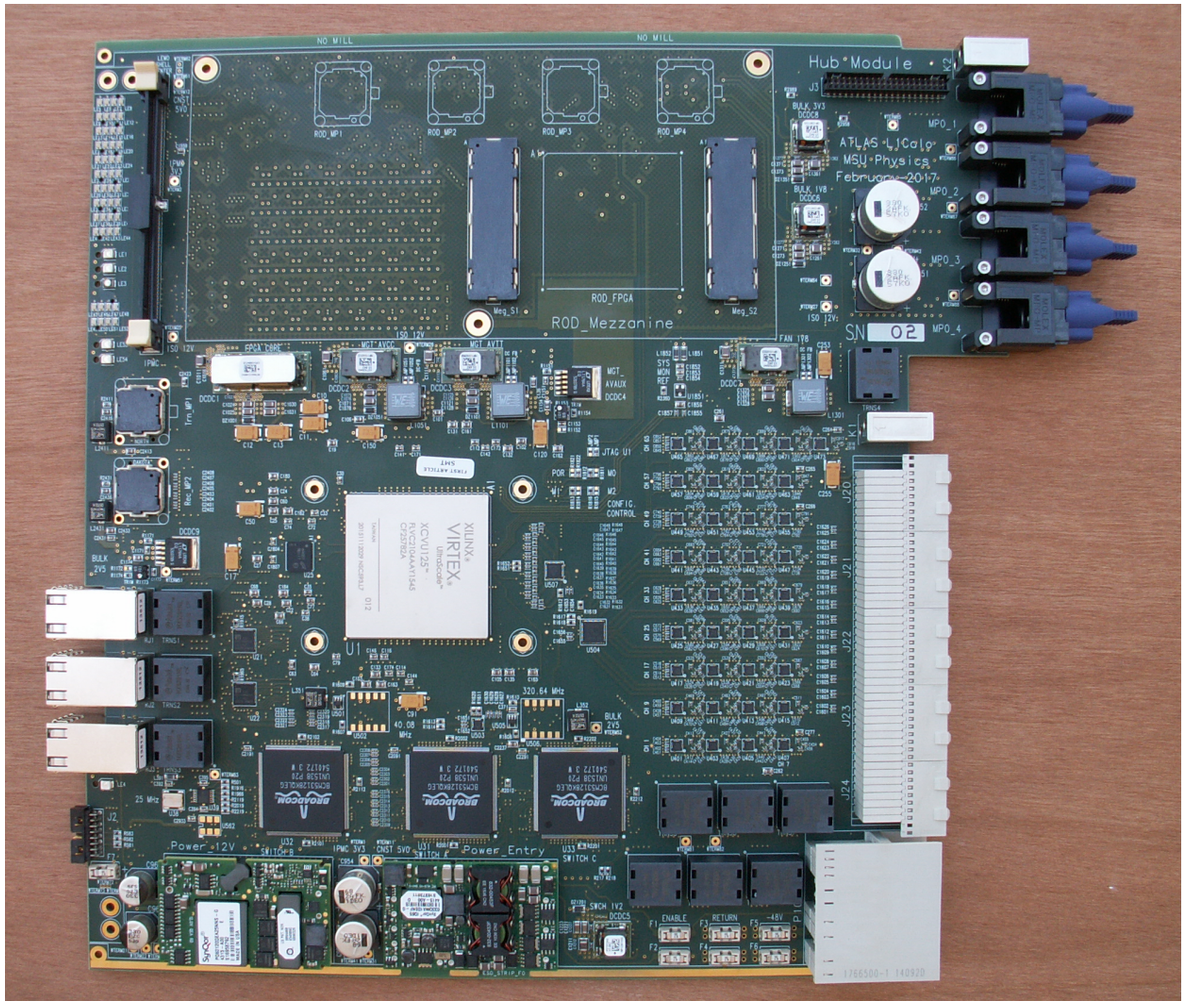
FEX Hub Role in L1Calo

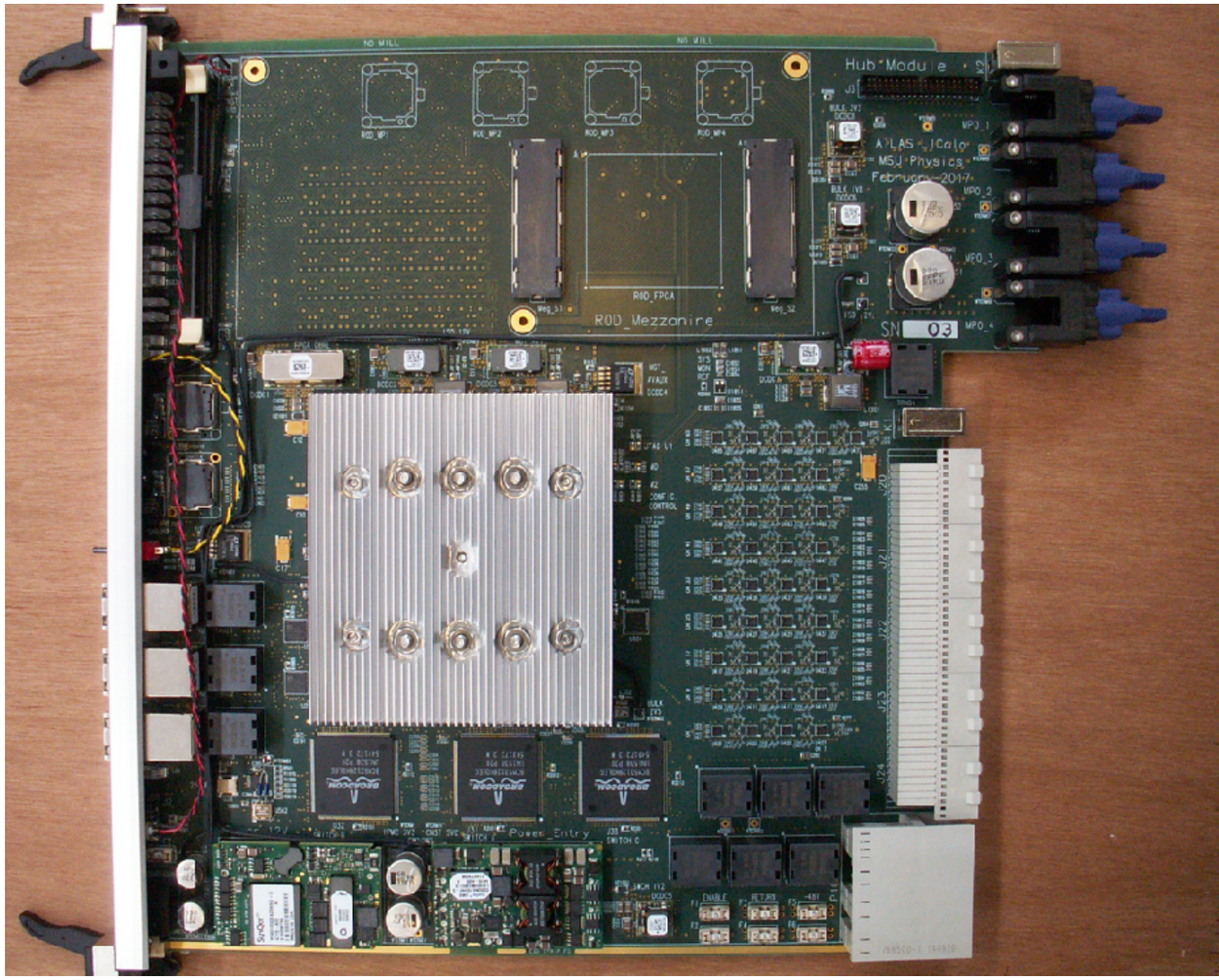


Hub Prototype Card

Primary Hub components

- 74 1:2 ON-Semi high-speed fanout chips
- 2 MEG-Array connectors for ROD interface
- 3 BroadCom 8-port GbE switches
- 1 Xilinx Virtex Ultrascale FPGA (XCVU125)
- 2 Avago MiniPOD opto-electrical modules





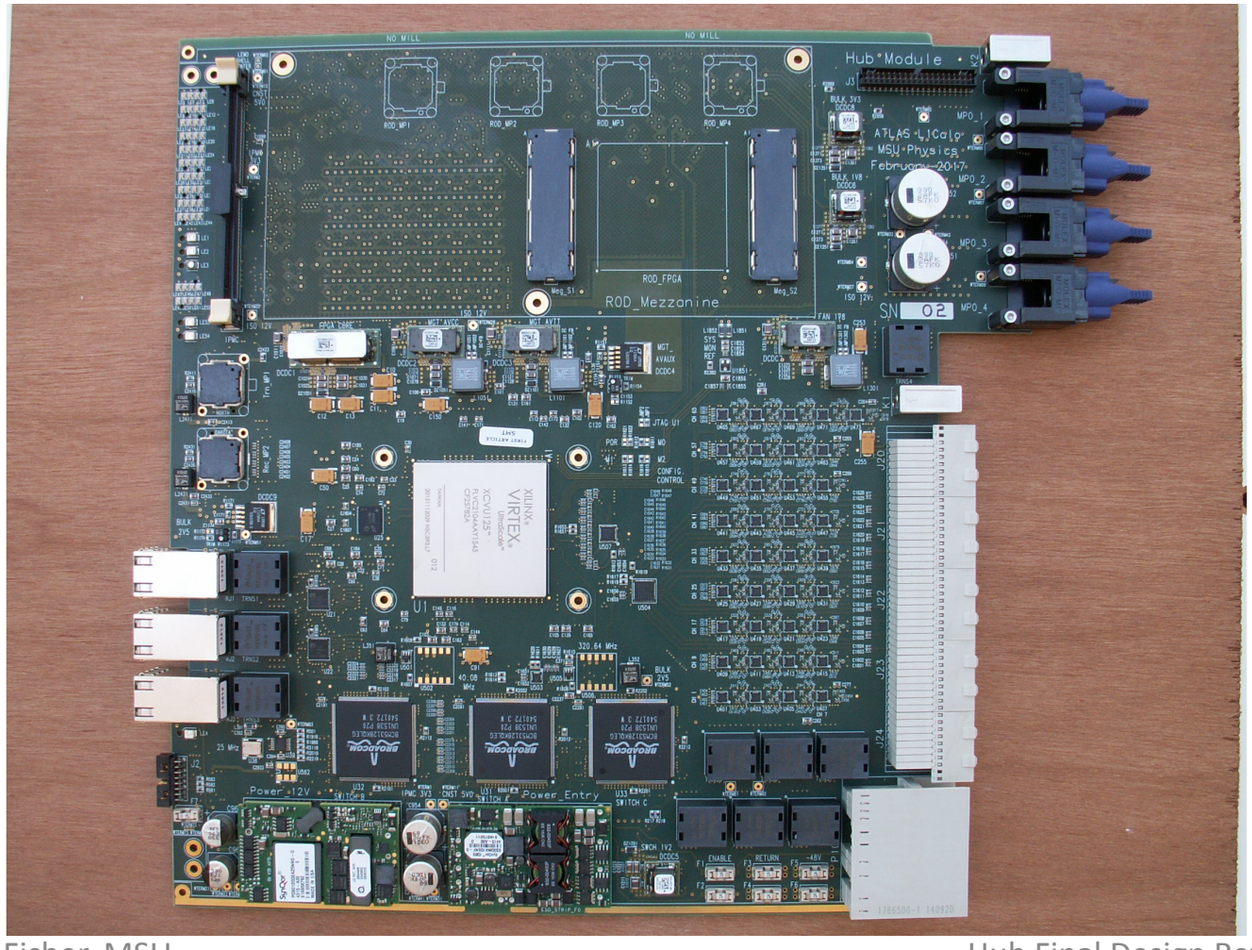
Hub Prototype Status

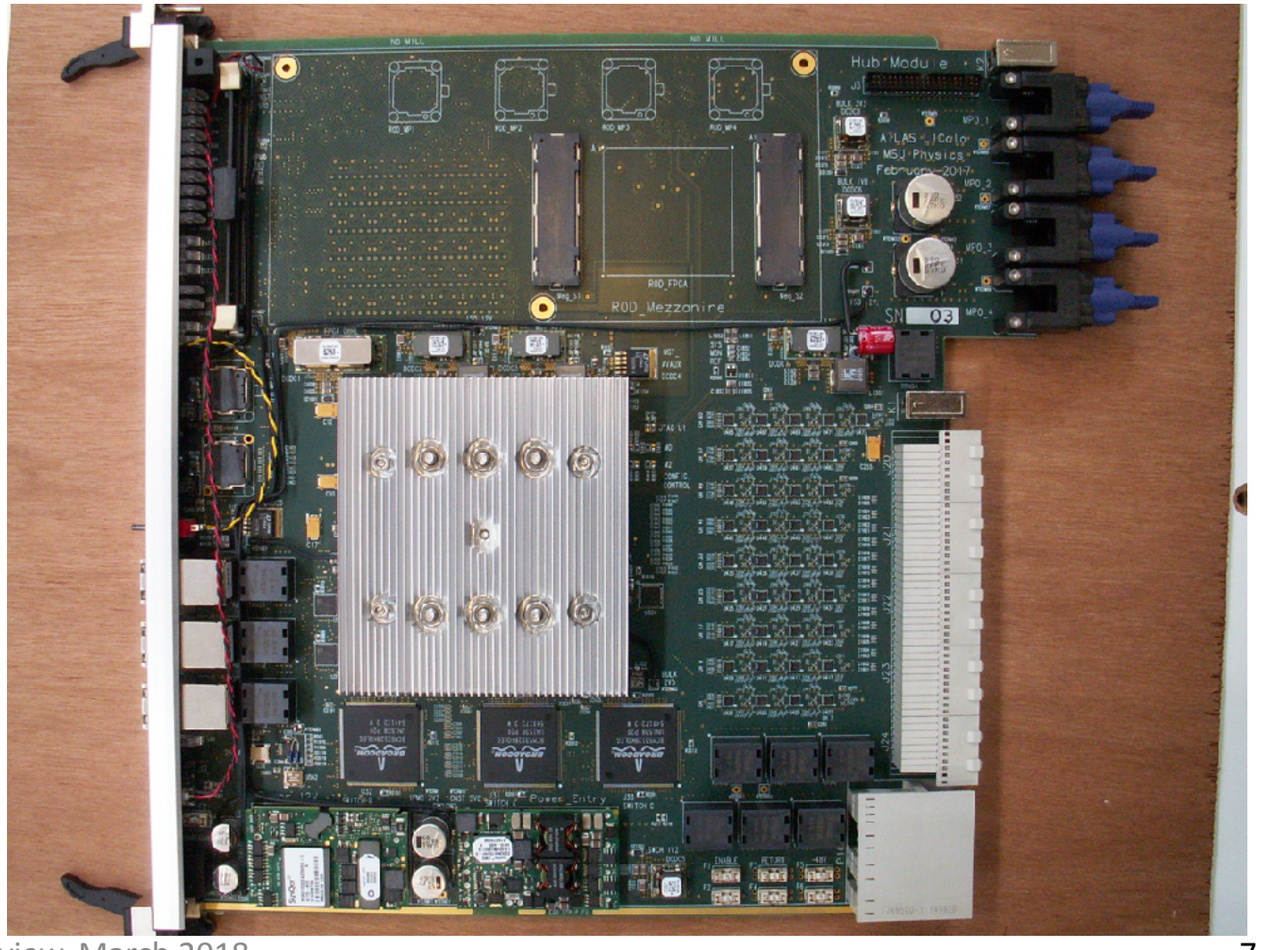
9 Hub prototypes delivered to MSU May 24

- 8 cards with FPGA, 1 without FPGA
- Electrical/power tests/connectivity passed without issues

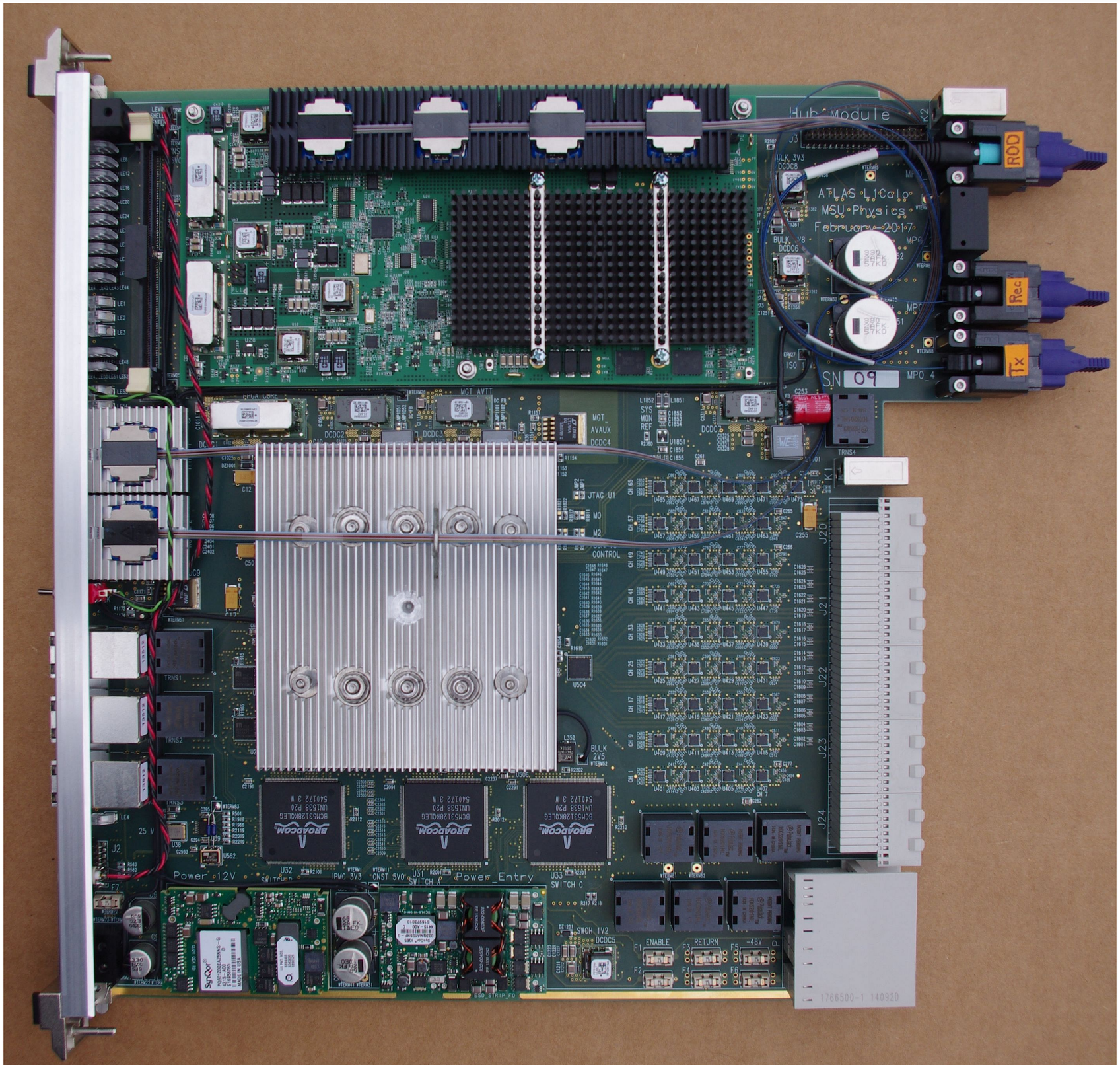
8 Hub prototypes have been gone through final assembly

- No issues, moved directly to configuration and I/O tests
- Tests at MSU with ROD, FEX Test Module
- Tests at Cambridge with ROD

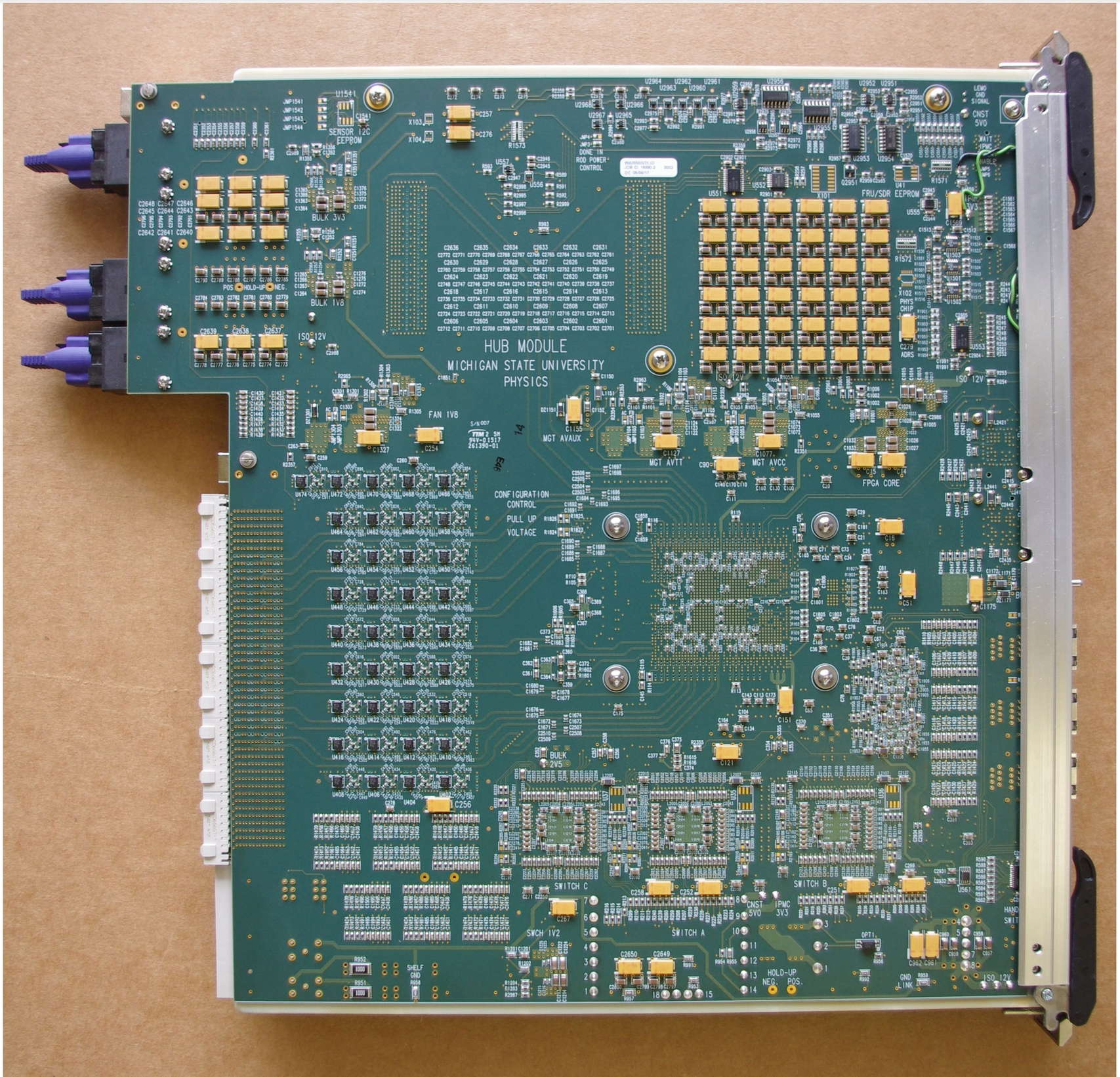




Hub + ROD Prototypes



Hub + ROD Prototypes



Hub Firmware Status

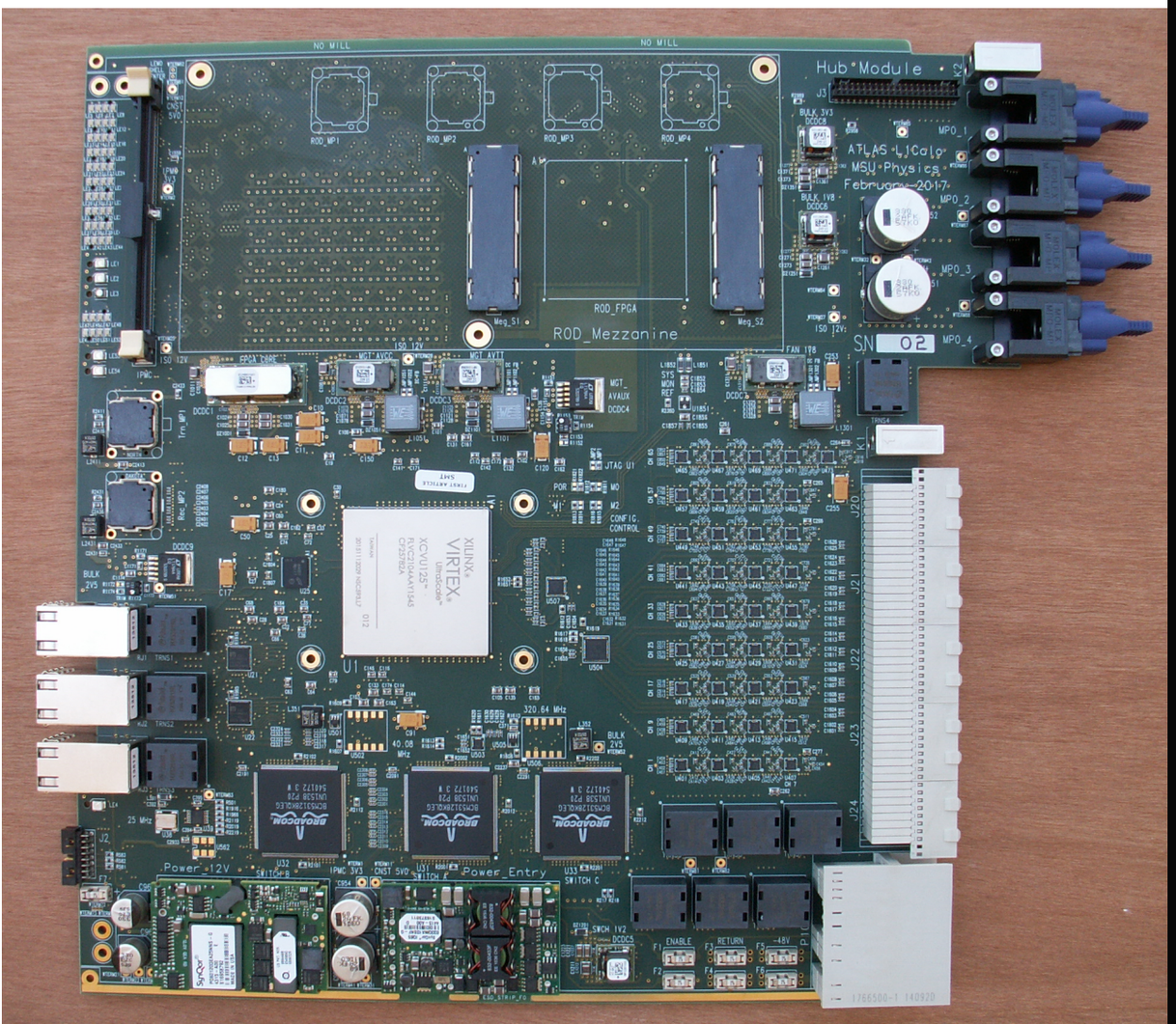
Hub firmware is being developed and debugged

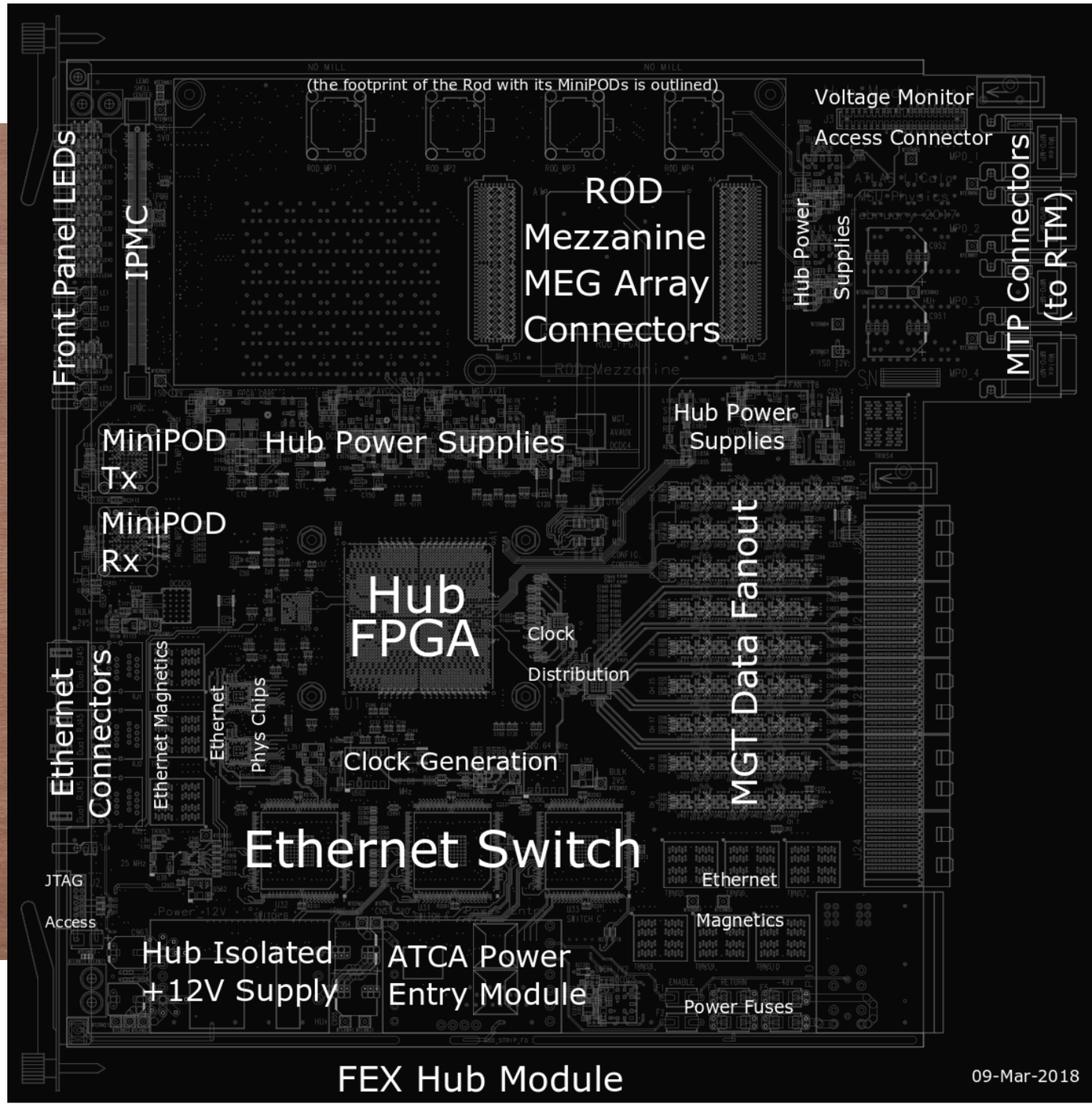
- Core FW for testing and validation largely complete
- FW to support core functions has been demonstrated

Primary firmware requirements

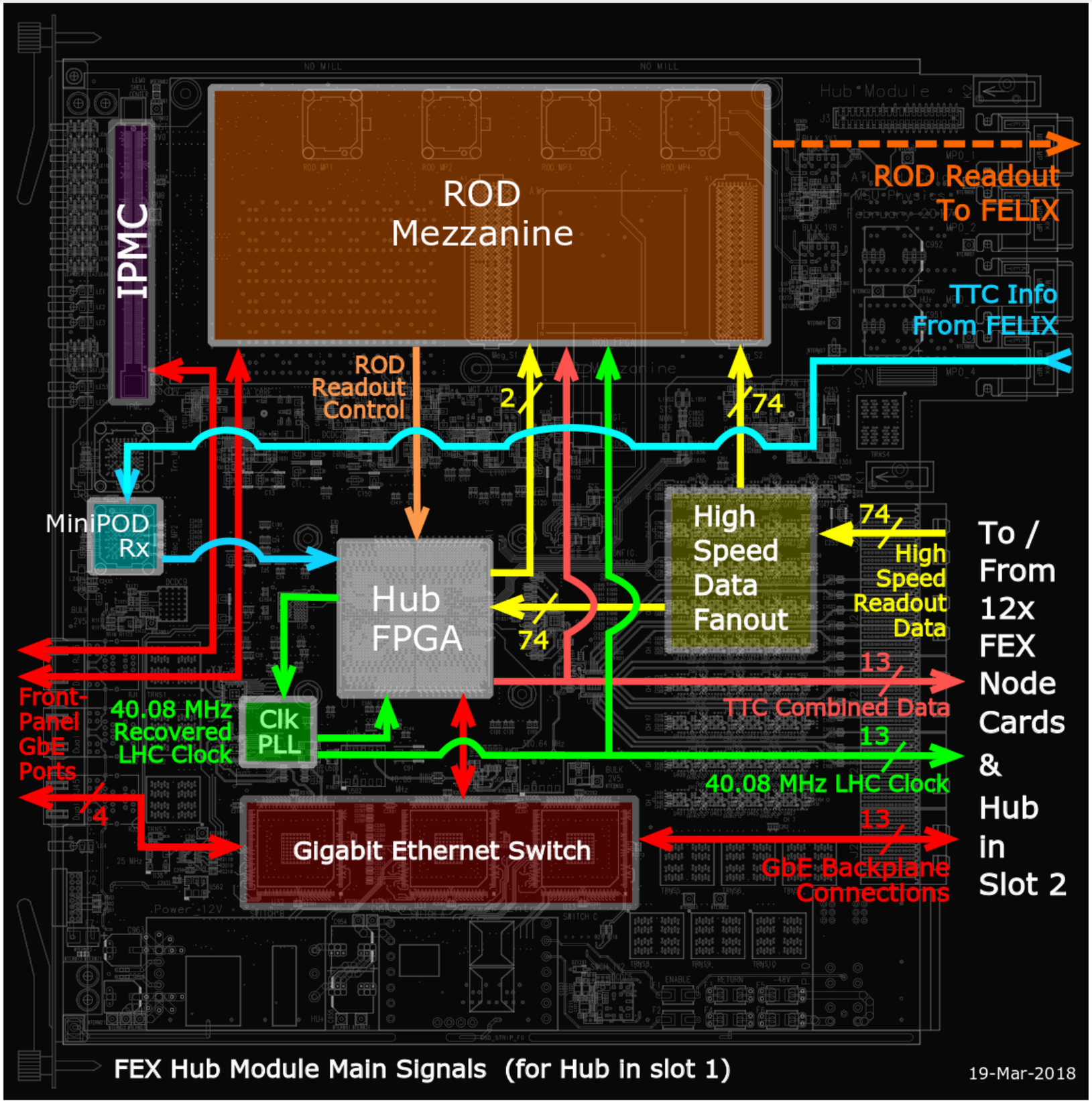
- TTC clock and data distribution
  - ✳ Combined TTC + ROD control signals
  - ✳ ROD/Hub power and data readout synchronization
- Ethernet interfaces
  - ✳ IPbus demonstrated with 2 MACs and PHY chips
- Hub-Hub and Hub-ROD general interfaces

Hub Functions





Hub Functions

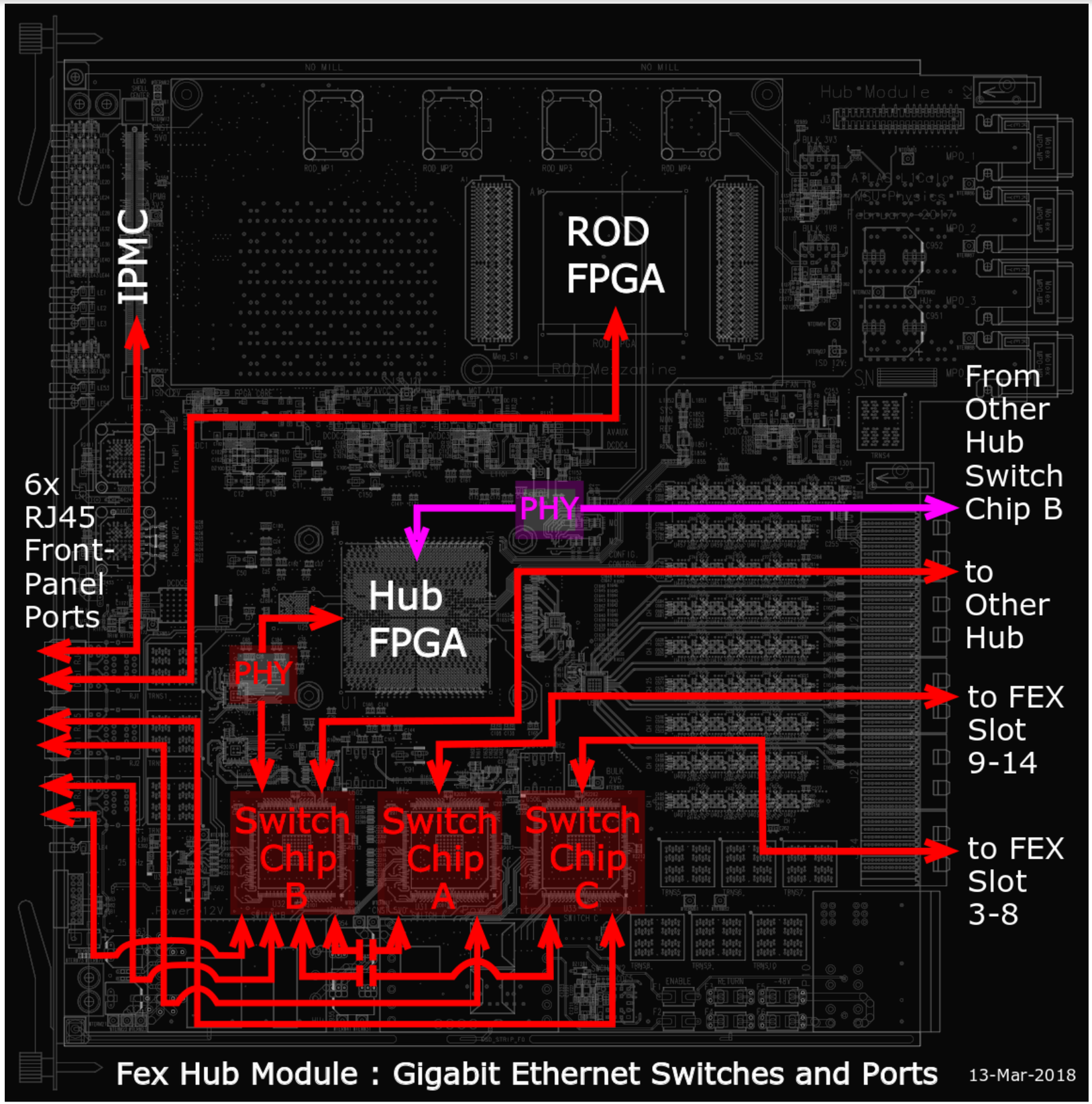


Hub Ethernet Switch

- ❖ Hub GbE switch is implemented using 3 switch chips
  - Broadcom BCM53128
    - Unmanaged, 8 ports, 10/100/1000 Base-T
  - After interconnects, yields an 18-port switch for each Hub

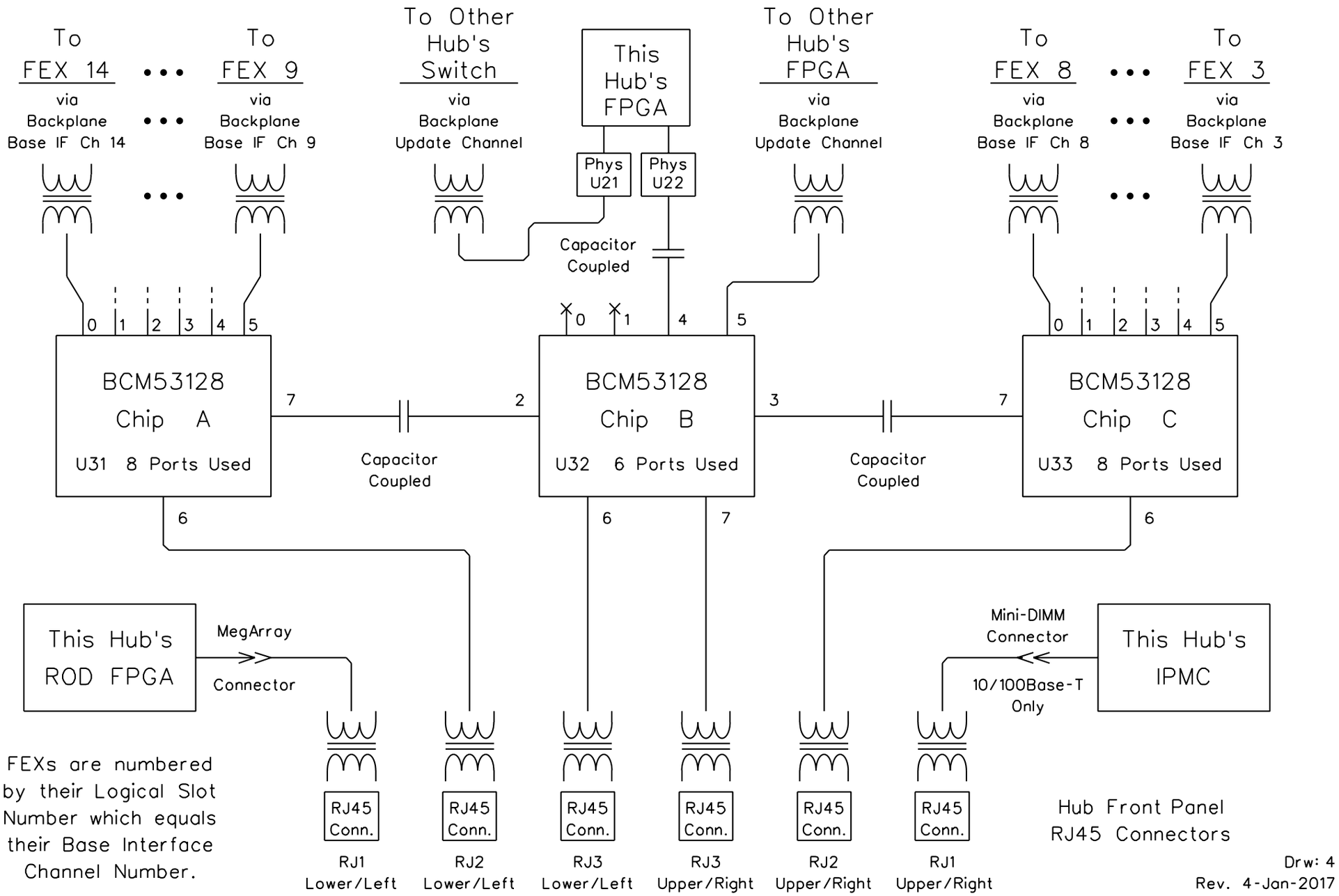
- Backplane: 12 connections to the "FEX Node" modules in this crate via the Base Channel Fabric;
- Backplane: 1 connection to the Ultrascale FPGA on the other Hub via the Update Channel Interface;
- Direct: 1 connection to the Ultrascale FPGA on this Hub;
- Front-Panel: 1 connection for an "up-link";
- Front-Panel: 1 connection for the ROD on this Hub (or IPMC on the other Hub);
- Front-Panel: 1 connection for the ROD on the other Hub (or IPMC on this Hub);
- Front-Panel: 1 spare connection;

Ethernet Switch



Ethernet Switch

Hub-Module All Ethernet Connections



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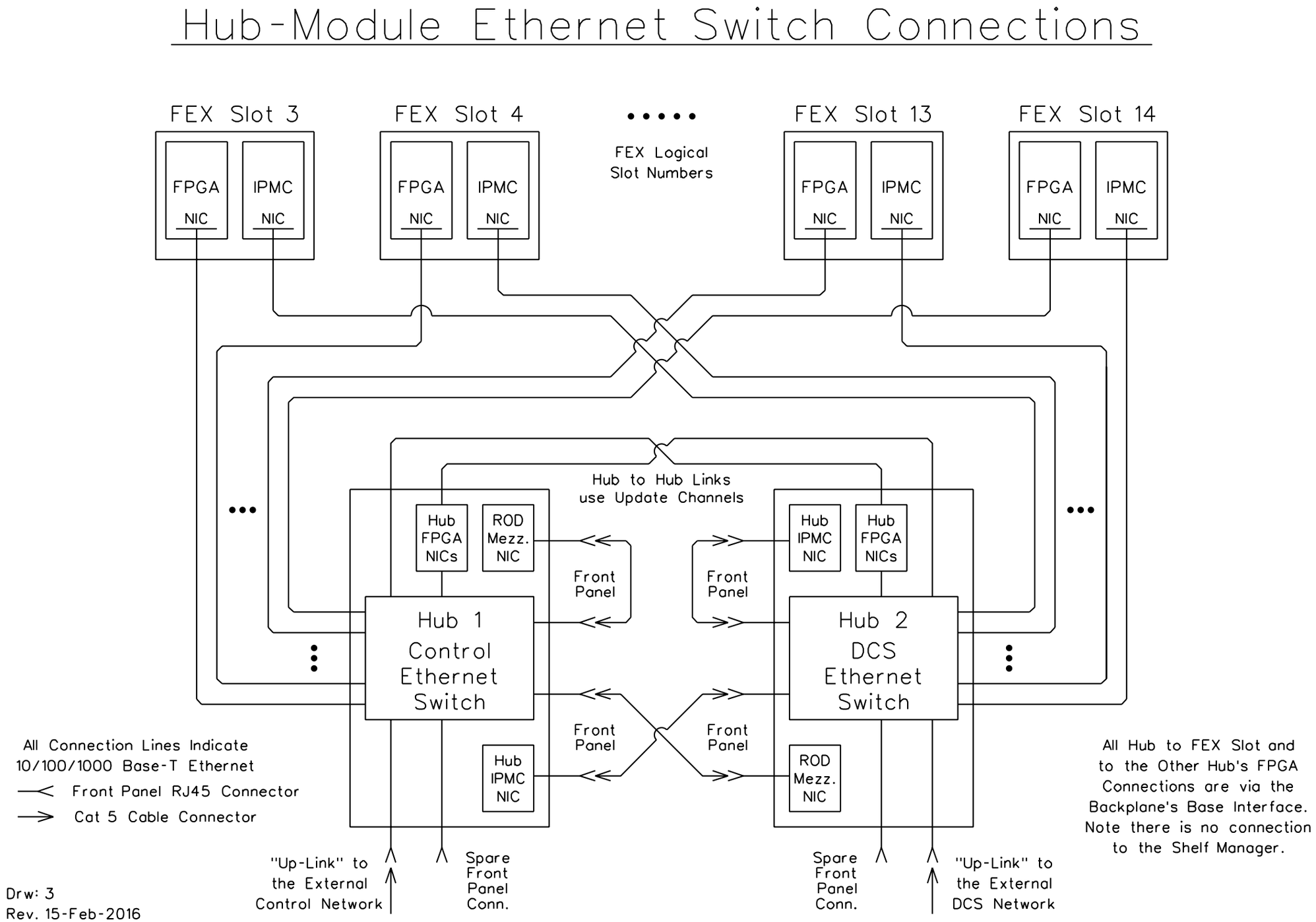

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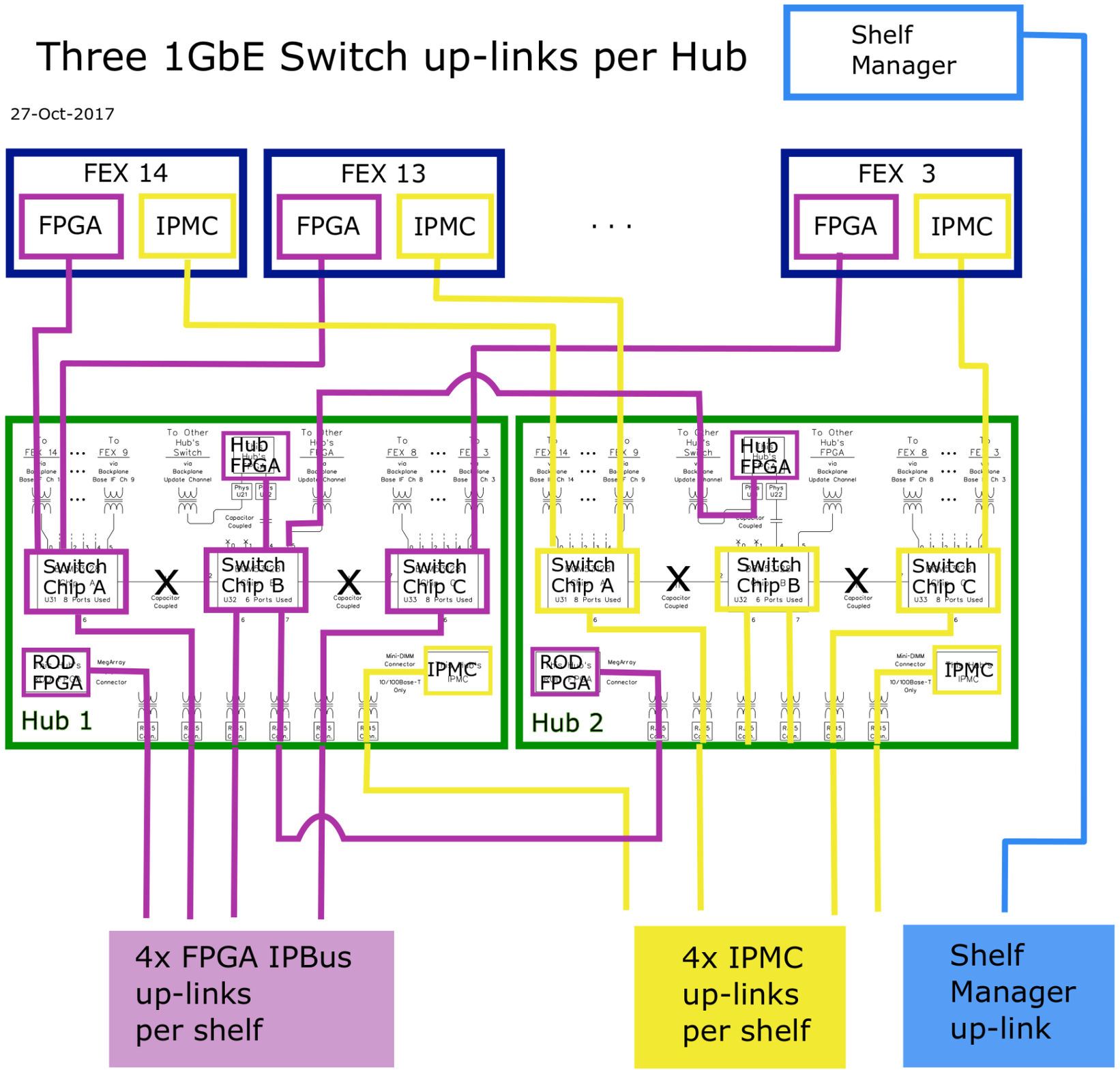

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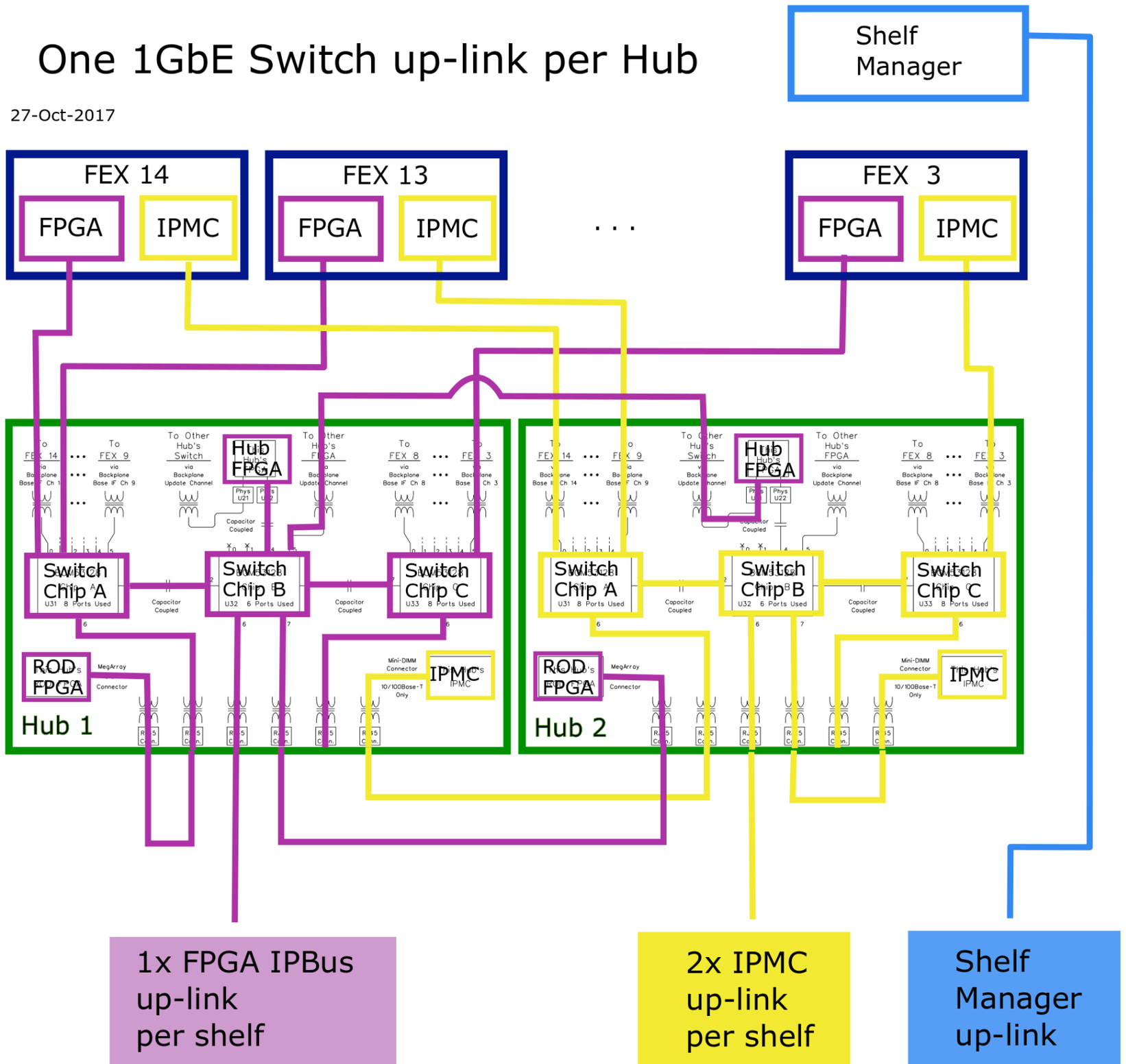
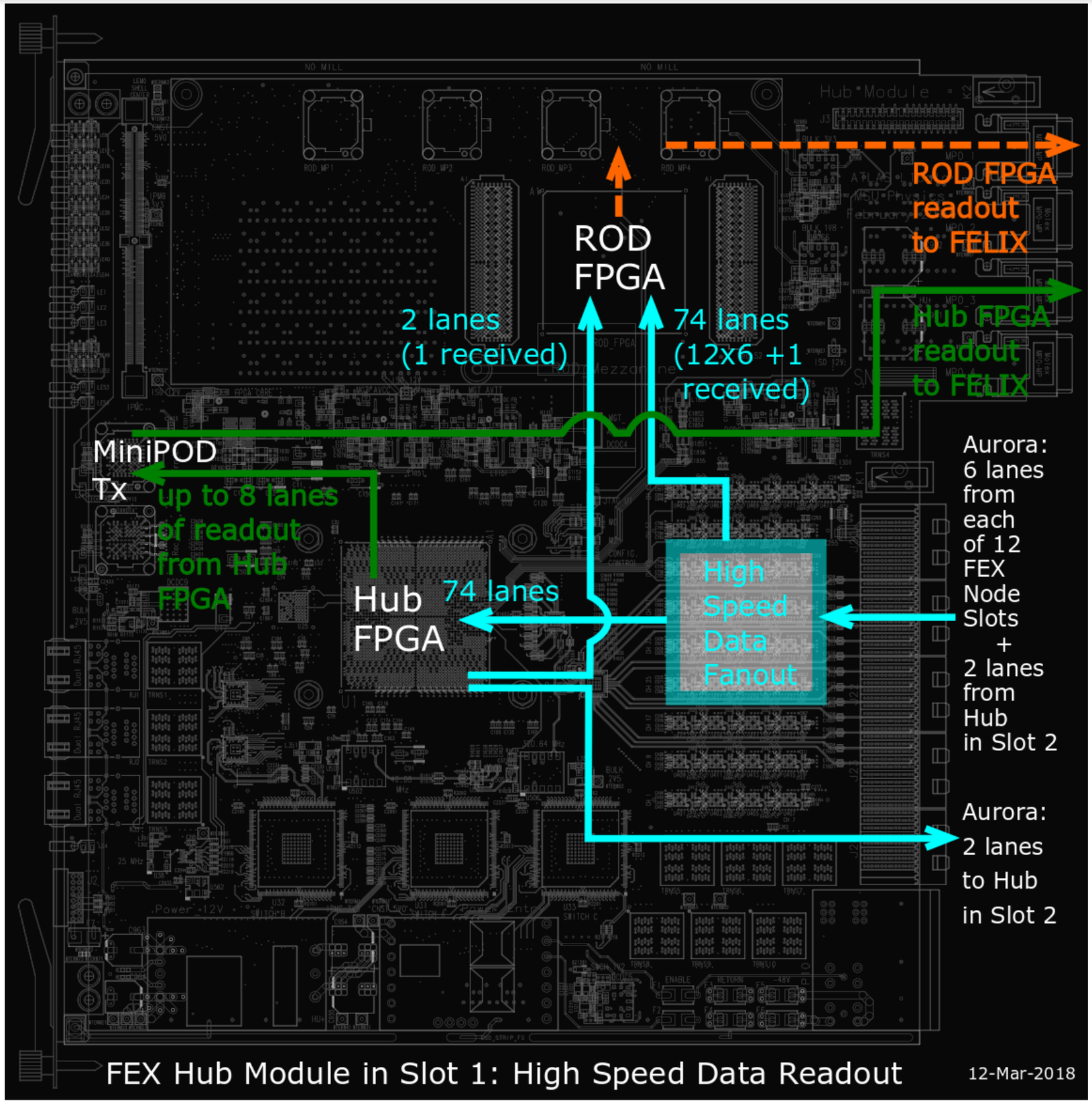


High-Speed Data Paths

- Readout data
  - 6 lanes from each FEX slot
    - Each FEX/L1Topo design will utilize these somewhat differently
  - 2 lanes from the other Hub (true for both Hub slots)
    - This is a non-standard use of the Update Channel
  - Total of 74 lanes received from the Fabric interface
  - Each of these 74 lanes is duplicated via 1:2 fanout
    - ON-Semi NB7VQ14M chips: 37 each on front/back of Hub PCB
    - One copy each to the Hub and ROD FPGAs
      - Current ROD design only implements 1 of 2 Hub readout lanes
        - Due to limitation in MGT availability, could be added if S-Link MiniPODs aren't ultimately required.

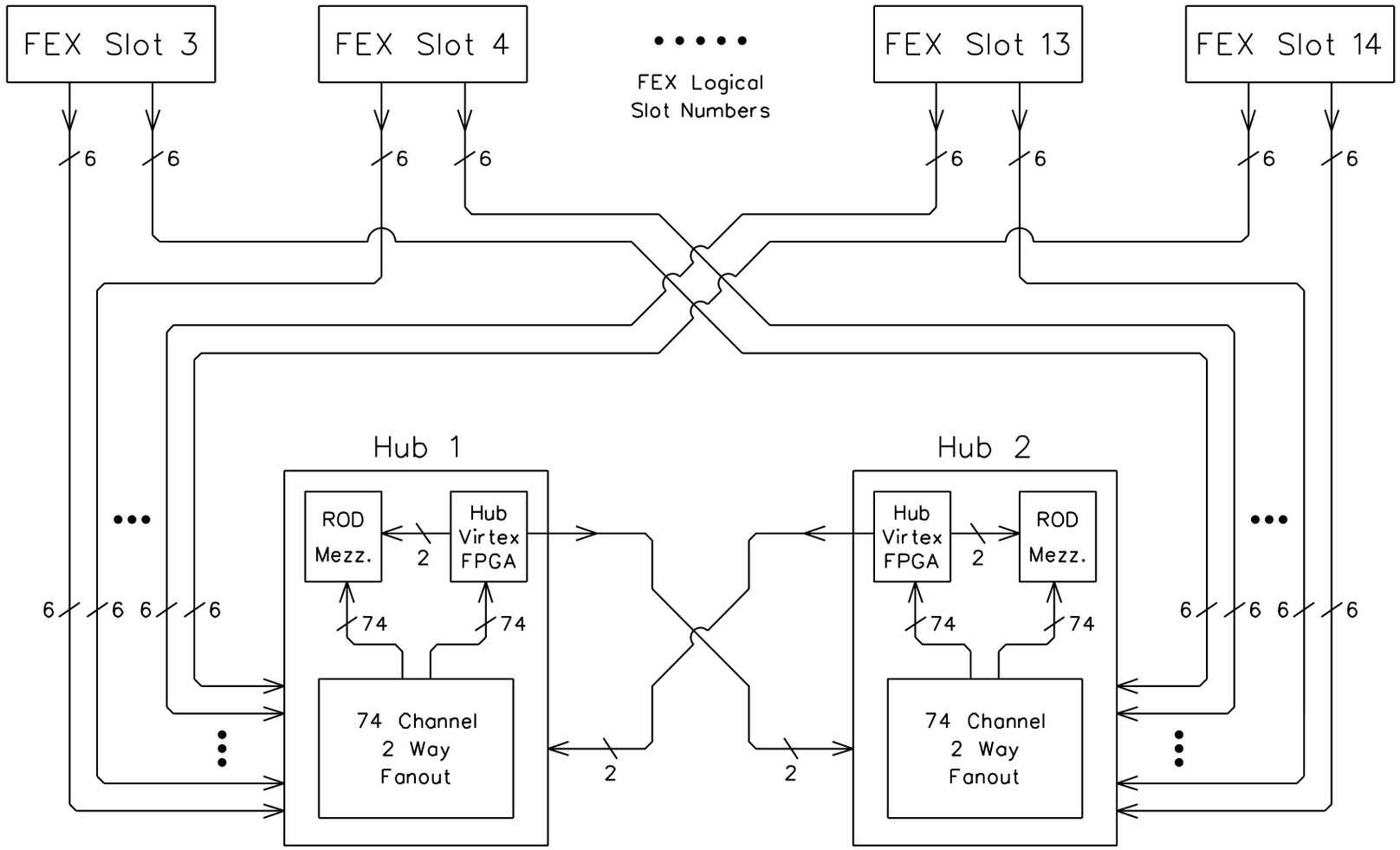
- Optical signals
  - 8 free MGTs on the Hub are routed to a MiniPOD transmitter
    - Optical signals routed out via Zone-3
    - Contingency for future use cases

High-Speed Data Paths



High-Speed Data Paths

Hub-Module Readout Data Distribution



Each line indicates six Fabric Interface Channels carrying FEX Slot Readout Data to the ROD's and to the Hub-Module's Virtex FPGAs

Hub to Hub Links use the Fabric Interface.

The FEX Slot Readout Data on each Fabric Interface Channel is received by an MGT Transceiver on both the ROD's and the Hub-Module's Virtex FPGAs.

Drw: 2 Rev. 15-Feb-2016

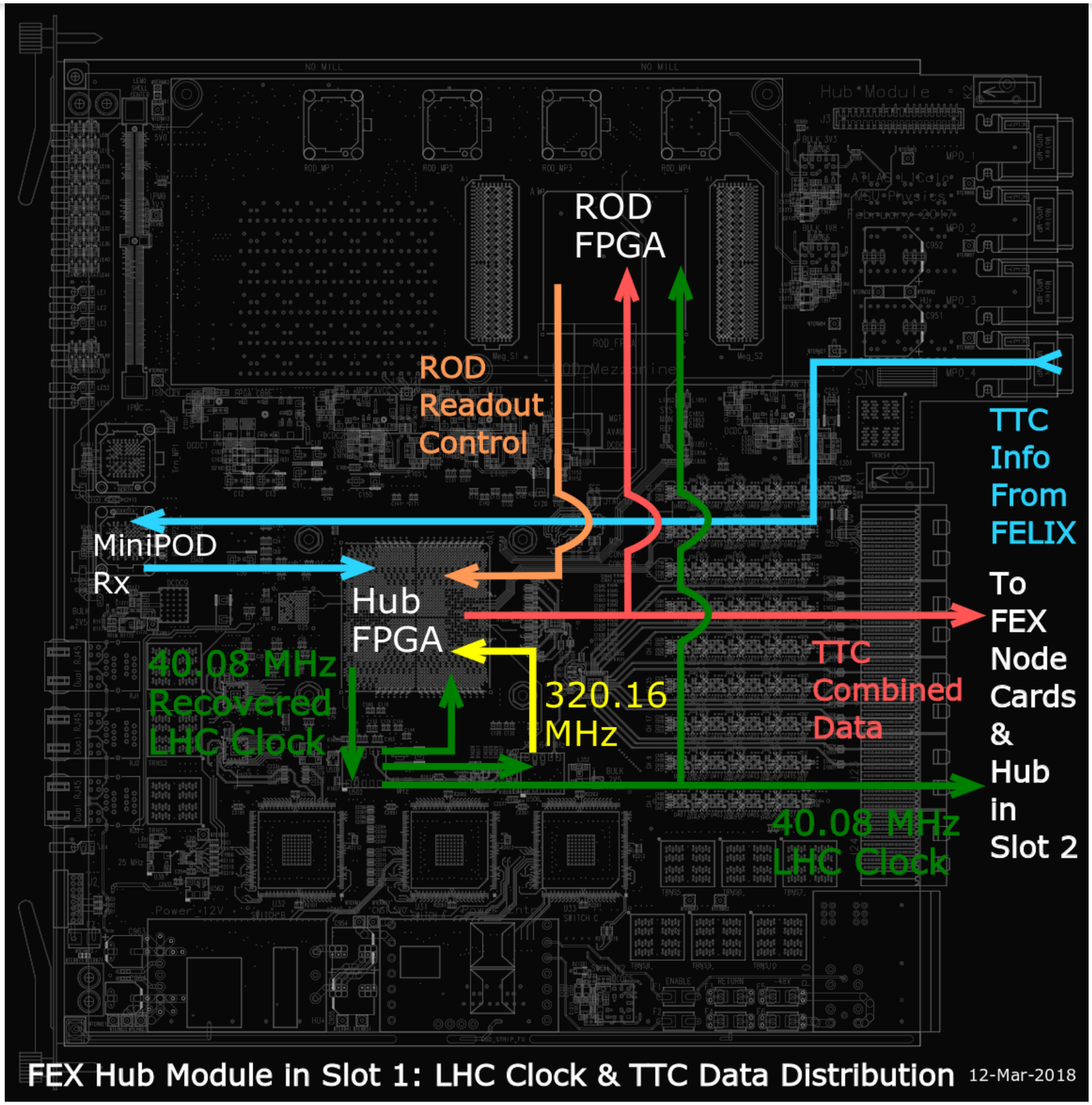
Combined TTC Paths

- TTC signal received optically via MiniPOD from FELIX
  - TTC signal received on Hub FPGA, where it is decoded
    - Current TTC payload not fully defined, but there is no Hub limitation

- Combined data signal
  - Hub receives readout control signal from ROD-1 (slot 1)
    - Readout control from ROD-2 delivered to Hub-1 via Hub-2
  - TTC data and ROD data are combined in Hub FPGA
    - Signals sent to each FEX, both RODs and other Hub

- LHC reference clock
  - Recovered clock transferred to Hub PLL circuit (clock selector)
    - Clock distributed to ROD/FEX/Hub

Combined TTC Paths



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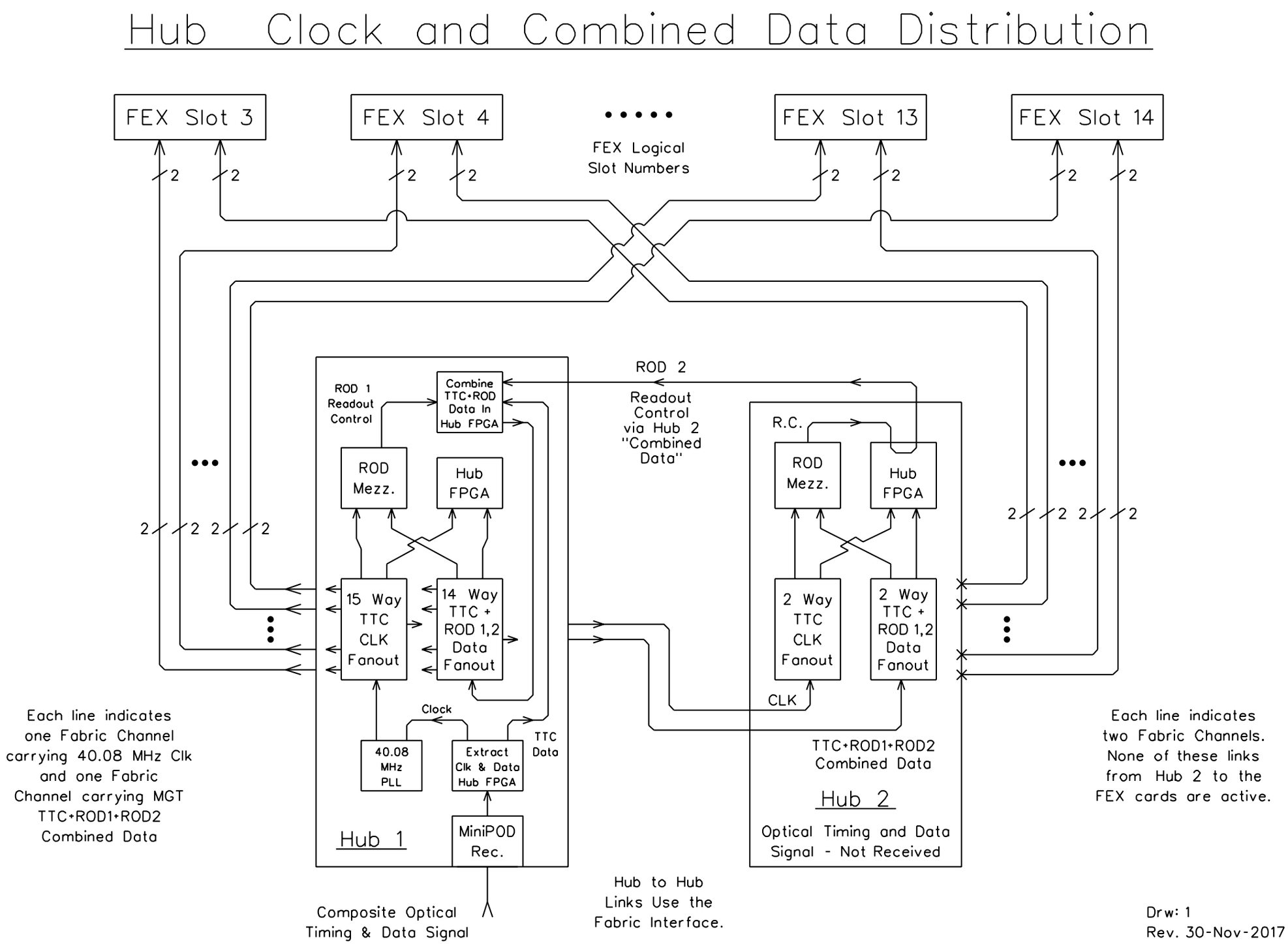
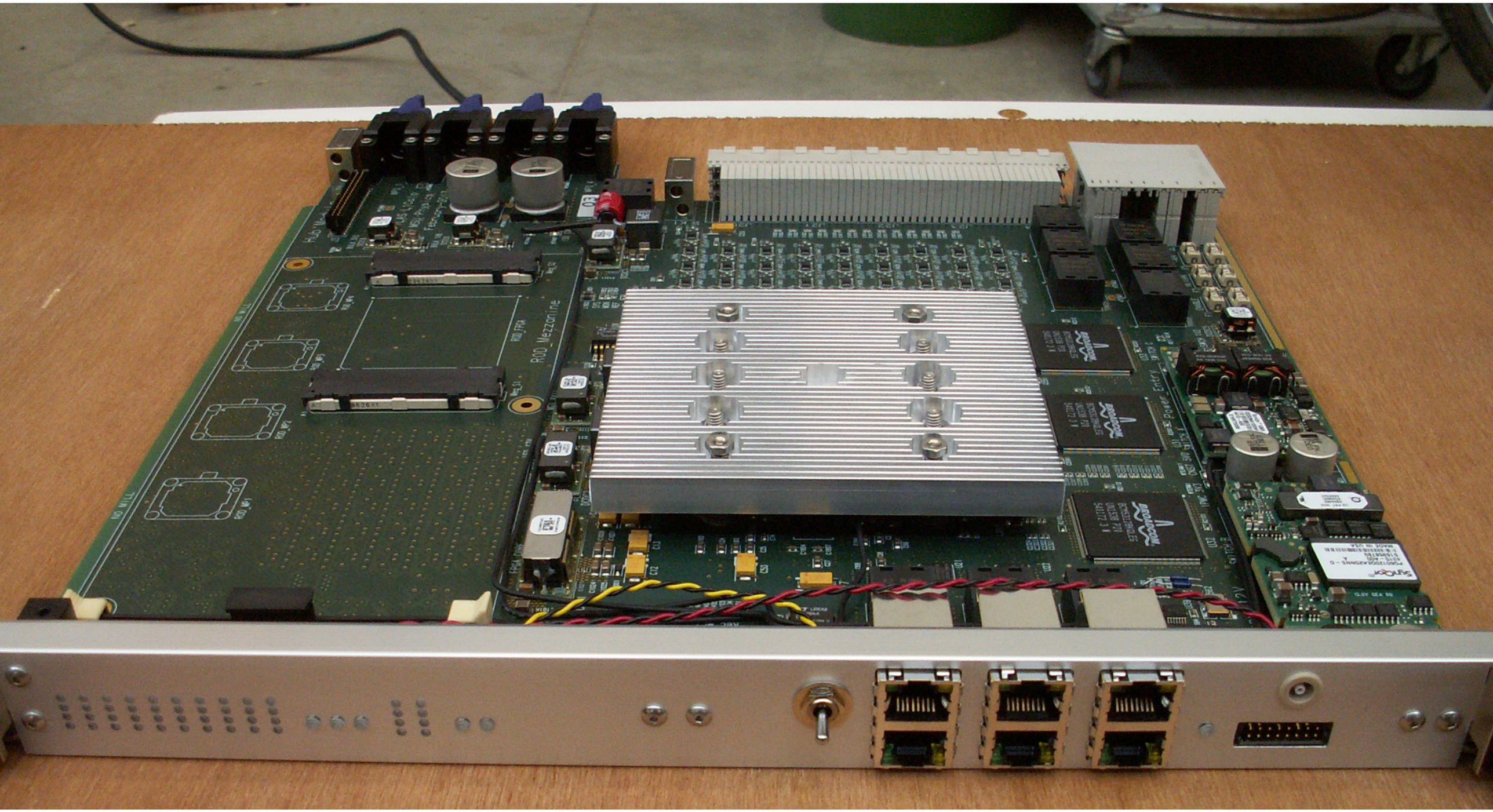


Hub Front Panel



Hub Front Panel

LEDs for each GbE connection:
Each FEX slot, both connections on each Hub, connections between switch chips.

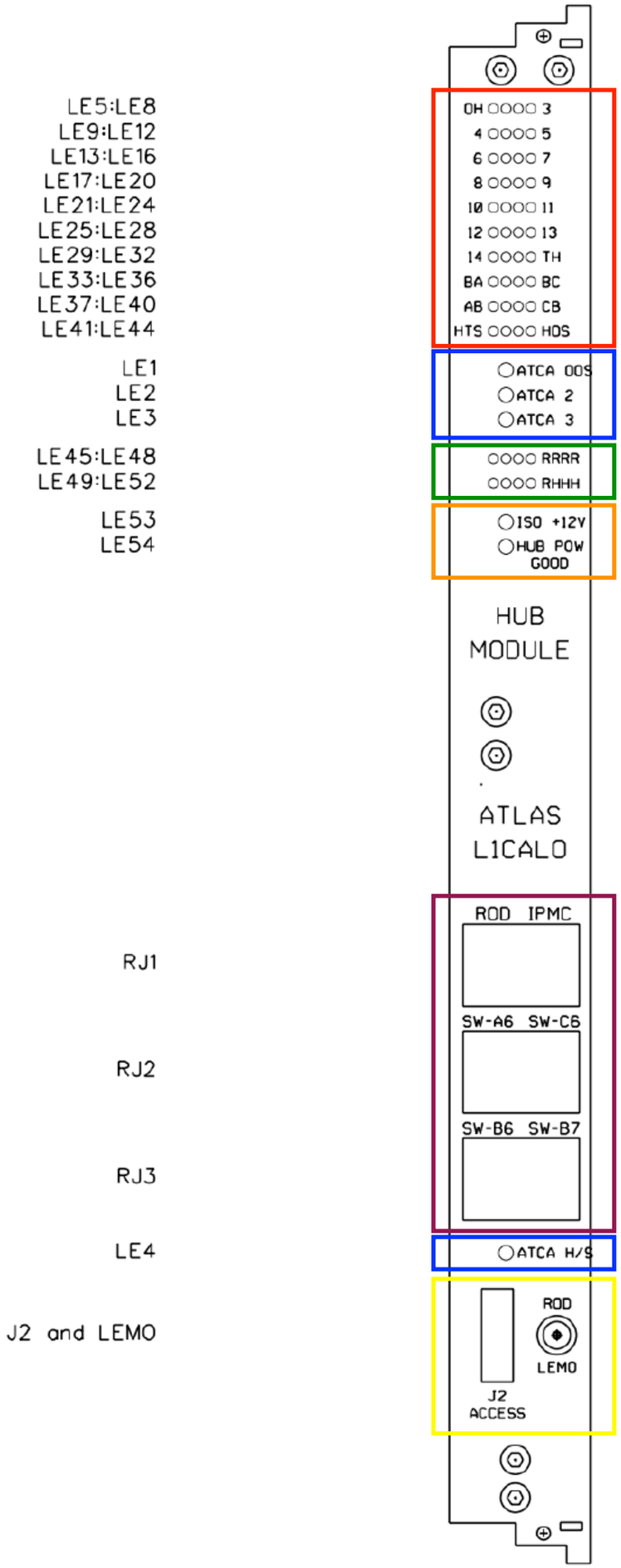
ATCA-required LEDs for IPMC

5 ROD-defined LEDs, 3 Hub “spare” LEDs

Hub power indicators

RJ45 protrusions

LEMO and JTAG/I2C protrusions



Summary

- Implementation of Hub core functionality summarized
  - Hub prototype module includes all required functions to support L1Calo operations.
    - Support for ROD mezzanine
    - GbE switch
    - TTC reception and transmission
    - FEX readout data delivery to ROD/Hub
  - Additional “lifeboat” features implemented using free resources
    - 8x MiniPOD transmitter lanes
    - Hub-Hub and Hub-ROD MGT links

- Next presentation will cover tests of the Hub prototype modules
  - Each of the functions described here have been tested thus far.