

1 **Technical Specification**

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3
4 **ATLAS Level-1 Calorimeter Trigger Upgrade**

5
6 **FEX System Switch Module (FEX Hub)**
7 **Prototype**

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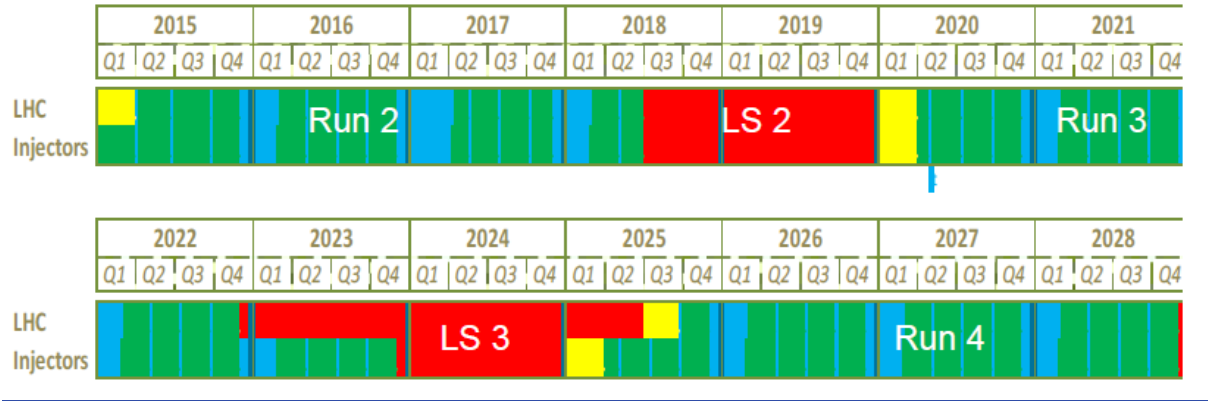
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230 1 Conventions

231 The following conventions are used in this document:

- 232 • The term “Hub” or “FEX-Hub” is used to refer to the Phase-I L1Calo FEX system
233 ATCA switch (hub) module in the rest of this document.
- 234 • The L1Calo FEX system Readout Driver (ROD) mezzanine is referred to as the
235 “Hub-ROD” or just “ROD” in this document.
- 236 • FEX-Hub modules can be physically located in logical slots 1 or 2. The
237 convention for the remainder of this document is to refer to these different
238 modules as Hub-1 and Hub-2, respectively. Likewise the ROD modules in logical
239 slots 1 or 2 are referred to as ROD-1 and ROD-2.
- 240 • The convention in this document will be that Hub-1 is the receiver of the TTC
241 signal from the upstream FELIX system, and thus is responsible for distributing
242 these signals to the FEX, ROD and Hub-2 recipients.
- 243 • A programmable parameter is defined as one that can be altered under computer
244 control, for example between runs, not on an event-by-event basis. Changing such
245 a parameter does not require a re-configuration of any firmware.
- 246 • Where multiple options are given for a link speed, for example, the readout links
247 of the FEX modules are specified as running ≤ 6.4 Gb/s, this indicates that the link
248 speed has not yet been fully defined. Once it is defined, that link will run at a
249 single speed.
- 250 • In accordance with the ATCA convention, a crate of electronics is here referred to
251 as a shelf.
- 252 • [Figure 1](#) explains the timeline for ATLAS running and shutdowns: Phase-I
253 upgrades will be installed before the end of long shutdown LS 2; Phase-II
254 upgrades will be installed before the end of LS 3.
- 255 • The term “*buffer*” is used to mean electrical reception and re-transmission of
256 signals (possibly with fan-out), but without any storage or memory function. The
257 terms “*storage buffer*”, “*FIFO*”, “*Dual Port RAM*” et al. are used where storage is
258 involved.



259
260
261

Figure 1: LHC shutdown and run schedule.

262 **2 Related Documents**

- 263 [1.1] ATLAS TDAQ System Phase-I Upgrade Technical Design Report,
264 CERN-LHCC-2013-018,
265 <http://cds.cern.ch/record/1602235/files/ATLAS-TDR-023.pdf>
- 266 [1.2] L1Calo Phase-I eFEX Specification,
267 <https://twiki.cern.ch/twiki/pub/Atlas/LevelOneCaloUpgradeModules/>
- 268 [1.3] L1Calo Phase-I jFEX Specification,
269 <https://twiki.cern.ch/twiki/pub/Atlas/LevelOneCaloUpgradeModules/>
- 270 [1.4] L1Calo gFEX Specification,
271 <https://twiki.cern.ch/twiki/pub/Atlas/LevelOneCaloUpgradeModules/>
- 272 [1.5] L1Calo Phase-1 ROD Specification ,
273 <https://twiki.cern.ch/twiki/pub/Atlas/LevelOneCaloUpgradeModules/>
- 274 [1.6] L1Calo Phase-I Optical plant Specification,
275 <https://twiki.cern.ch/twiki/pub/Atlas/LevelOneCaloUpgradeModules/>
- 276 [1.7] ATCA Short Form Specification,
277 http://www.picmg.org/pdf/picmg_3_0_shortform.pdf
- 278 [1.8] PICMG 3.0 Revision 3.0 AdvancedTCA Base Specification, *access controlled*,
279 <http://www.picmg.com/>
- 280 [1.9] P. Moreira, A. Marchioro, and K. Kloukinas, The GBT, a Proposed Architecture for
281 Multi-Gb/s Data Transmission in High Energy Physics, 2007.
282 <https://espace.cern.ch/GBT-Project/Papers/paperMoreiraGBT.doc>
- 283 [1.10] Development of an ATCA IPMI controller mezzanine board to be used in the
284 ATCA developments for the ATLAS Liquid Argon upgrade,
285 <http://cds.cern.ch/record/1395495/files/ATL-LARG-PROC-2011-008.pdf>
- 286 [1.11] IPbus Protocol,
287 https://svnweb.cern.ch/trac/cactus/export/trunk/doc/ipbus_protocol_v2_0.pdf
- 288 [1.12] Front-End Link Exchange (Felix),
289 <https://edms.cern.ch/document/13111772/1>
- 290 [1.13] MEG-Array Connectors,
291 [https://cdn.amphenol-](https://cdn.amphenol-icc.com/media/wysiwyg/files/documentation/datasheet/boardwiredtoboard/bwb_meg_array_mezzanine.pdf)
292 [icc.com/media/wysiwyg/files/documentation/datasheet/boardwiredtoboard/bwb_meg](https://cdn.amphenol-icc.com/media/wysiwyg/files/documentation/datasheet/boardwiredtoboard/bwb_meg_array_mezzanine.pdf)
293 [array_mezzanine.pdf](https://cdn.amphenol-icc.com/media/wysiwyg/files/documentation/datasheet/boardwiredtoboard/bwb_meg_array_mezzanine.pdf)
- 294 [1.14] ATLAS L1Calo System-Level Specifications,
295 <https://edms.cern.ch/document/1492098/1>

- 296 [1.15] Spencer Lee, Hub Gigabit Ethernet test description,
297 [https://web.pa.msu.edu/hep/atlas/l1calo/hub/specification/2_final_design_review/H](https://web.pa.msu.edu/hep/atlas/l1calo/hub/specification/2_final_design_review/Hub_GbE_Test_Report_v0_1.pdf)
298 [ub_GbE_Test_Report_v0_1.pdf](https://web.pa.msu.edu/hep/atlas/l1calo/hub/specification/2_final_design_review/Hub_GbE_Test_Report_v0_1.pdf)
- 299 [1.16] Hub firmware specification,
300 [https://web.pa.msu.edu/hep/atlas/l1calo/hub/specification/2_final_design_review/H](https://web.pa.msu.edu/hep/atlas/l1calo/hub/specification/2_final_design_review/HUB_FW_Spec_FDR_03_12_2018.pdf)
301 [UB_FW_Spec_FDR_03_12_2018.pdf](https://web.pa.msu.edu/hep/atlas/l1calo/hub/specification/2_final_design_review/HUB_FW_Spec_FDR_03_12_2018.pdf)

302 **3 Introduction**

303 This document describes the ATCA switch module (FEX-Hub) of the ATLAS Level-1
304 Calorimeter Trigger Processor (L1Calo) system [1.1] . The FEX-Hub is one of several
305 modules being designed to upgrade L1Calo, providing the increased discriminatory
306 power necessary to maintain trigger efficiency as the LHC luminosity is increased
307 beyond that for which ATLAS was originally designed.

308 The function of the FEX-Hub module is to provide common communications functions
309 for the FEX ATCA shelves including the routing of FEX readout data, network
310 communications to and from FEX modules and distribution of clock and control signals.

311 The FEX-Hub modules will be installed in L1Calo during the long shutdown LS2, as part
312 of the Phase-1 upgrade, and will operate during Run 3. They will remain in the system
313 after the Phase-2 upgrade in LS3, and will operate during Run 4, at which time they will
314 form part of L0Calo. The following sections provide overviews of L1Calo in Run 3 and
315 L0Calo in Run 4.

316 This is a specification for the production FEX-Hub module. This final version will
317 deliver the required functionality for the L1Calo FEX system. This specification further
318 describes possible use cases not critical to the core Hub functionality that represent
319 fallback options for the L1Calo (L0Calo) readout system if needed.

320 This document is arranged as follows. The front portion of the document introduces the
321 L1Calo system, the plans for its upgrade and the upgrade evolutions. Next, a descriptive
322 overview of the FEX-Hub module is provided, describing the primary specifications for
323 its functionality within the L1Calo trigger system, including system interfaces and the
324 implementation of the FEX-Hub itself. Finally, there are two appendices that enter into
325 the details of how the FEX-Hub module has been designed and built, which provide an
326 official reference on the “as built” FEX-Hub specification.

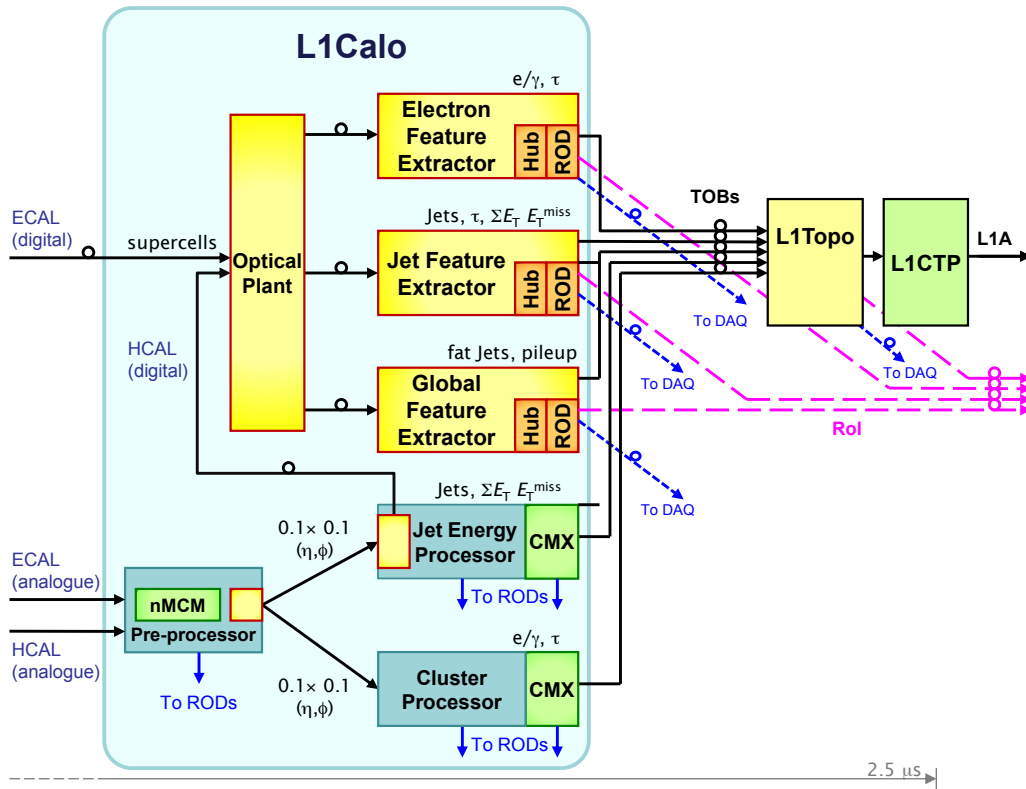
327 **3.1 L1Calo Overview**

328 **3.1.1 Overview of the L1Calo System in Phase I (Run 3)**

329 In Run 3, L1Calo contains three subsystems installed prior to LS2, as shown in [Figure 2](#)
330 (see document [1.1]):

- 331 • The Pre-processor, which receives shaped analog pulses from the ATLAS
332 calorimeters, digitises and synchronises them, identifies the bunch-crossing from
333 which each pulse originated, scales the digital values to yield transverse energy (E_T),
334 and prepares and transmits the data to the following processor stages;

- 335 • The Cluster Processor (CP) subsystem (comprising Cluster Processing Modules
336 (CPMs) and Common Merger Extended Modules (CMXs)) which identifies isolated
337 e/γ and τ candidates;
- 338 • The Jet/Energy Processor (JEP) subsystem (comprising Jet-Energy Modules (JEMs)
339 and Common Merger Extended Modules (CMXs)) which identifies energetic jets and
340 computes various local energy sums.



341

342 **Figure 2:** The L1Calo system in Run 3. *Components installed during LS2 are shown in*
343 *yellow/orange*

344 Additionally, L1Calo contains the following three subsystems installed as part of the
345 Phase-I upgrade in LS2:

- 346 • The electromagnetic Feature Extractor eFEX subsystem, comprising eFEX modules
347 and FEX-Hub modules, the latter carrying Readout Driver (ROD) daughter cards.
348 The eFEX subsystem identifies isolated e/γ and τ candidates, using data of finer
349 granularity than is available to the CP subsystem.
- 350 • The jet Feature Extractor (jFEX) subsystem, comprising jFEX modules, and Hub
351 modules with ROD daughter cards. The jFEX subsystem identifies energetic jets and
352 computes various local energy sums, using data of finer granularity than that
353 available to the JEP subsystem.
- 354 • The global Feature Extractor (gFEX) subsystem, which is a single, stand-alone
355 module. The gFEX subsystem identifies calorimeter trigger features requiring the
356 complete calorimeter data.

357 • An updated Level-1 Topological Processing subsystem (L1Topo), comprising
358 L1Topo modules, and Hub modules with ROD daughter cards. The L1Topo
359 subsystem applies topological selection and threshold criteria on trigger objects
360 derived from the calorimeter and muon detector systems.
361

362 In Run 3, the Liquid Argon Calorimeter provides L1Calo both with analog signals (for
363 the CP and JEP subsystems) and with digitized data (for the FEX subsystems). From the
364 hadronic calorimeters, only analog signals are received. These are digitized on the Pre-
365 processor, transmitted electrically to the JEP, and then transmitted optically to the FEX
366 subsystems. Initially at least, the eFEX and jFEX subsystems will operate in parallel with
367 the CP and JEP subsystems. Once the performance of the FEX subsystems has been
368 validated, the CP sub system will be removed, and the JEP used only to provide hadronic
369 data to the FEX subsystems.

370 The optical signals from the JEP and LDPS electronics are sent to the FEX subsystems
371 via an optical plant. This performs two functions. First, it separates and reforms the fibre
372 bundles, changing the mapping from that employed by the LDPS and JEP electronics to
373 that required by the FEX subsystems. Second, it provides any additional fan-out of the
374 signals necessary to map them into the FEX modules where this cannot be provided by
375 the calorimeter electronics.

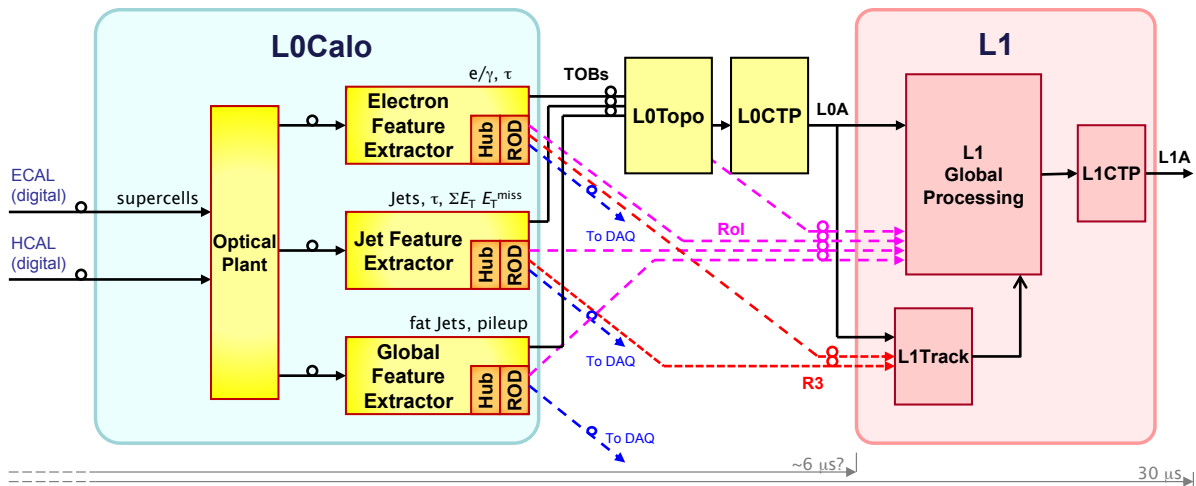
376 The outputs of the FEX subsystems (plus CP and JEP) comprise Trigger Objects (TOBs):
377 data structures which describe the location and characteristics of candidate trigger
378 objects. The TOBs are transmitted optically to the Level-1 Topological Processor
379 (L1Topo), which merges them over the system and executes topological algorithms, the
380 results of which are transmitted to the Level-1 Central Trigger Processor (CTP).

381 The eFEX, jFEX, gFEX and L1Topo subsystems comply with the ATCA standard. The
382 eFEX subsystem comprises two shelves each of 12 eFEX modules. The jFEX subsystem
383 comprises a single ATCA shelf holding 6 jFEX modules. The gFEX subsystem
384 comprises a single ATCA shelf holding a single gFEX module. The L1Topo subsystem
385 comprises a single ATCA shelf housing up to four L1Topo modules, each of which
386 receives a copy of all data from all FEX modules. All L1Calo processing modules
387 produce Region of Interest (RoI) and DAQ readout on receipt of a Level-1 Accept signal
388 from the CTP. RoI information is sent both to the High-Level Trigger (HLT) and the
389 DAQ system, while the DAQ data goes only to the DAQ system. In the FEX and L1Topo
390 subsystems, these data are transmitted by each FEX or L1Topo module via the shelf
391 backplane to two Hub modules (with the exception of the gFEX, which requires no
392 Hub/ROD). Each of these buffers the data and passes a copy to their ROD daughter
393 board. The RODs perform the processing needed to select and transmit the RoI and DAQ
394 data in the appropriate formats; it is likely that the required tasks will be partitioned

395 between the two RODs. Additionally, the Hub modules provide distribution and
 396 switching of the TTC signals and control and monitoring networks.

397 **3.1.2 Overview of the L1Calo System in Phase-II (Run 4)**

398 The Phase-II upgrade will be installed in ATLAS during LS3. At this point, substantial
 399 changes will be made to the trigger electronics. All calorimeter input to L1Calo from the
 400 electromagnetic and hadronic calorimeters will migrate to digital format, the structure of
 401 the hardware trigger will change to consist of two levels, and a Level-1 Track Trigger
 402 (L1Track) will be introduced and will require TOB seeding. The Pre-processor, CP and
 403 JEP subsystems will be removed, and the FEX subsystems, with modified firmware, will
 404 be relabelled to form the L0Calo system in a two stage (Level-0/Level-1) real-time
 405 trigger, as shown in Figure 3. Hence, the FEX subsystems must be designed to meet both
 406 the Phase-I and Phase-II upgrade requirements. The main additional requirements are to
 407 provide real-time TOB data to L1Track, and to accept Phase-II timing and control signals
 408 including Level-0 Accept (LOA) and Level-1 Accept. Additional calorimeter trigger
 409 processing will be provided by a new L1Calo trigger stage.



410 **Figure 3:** The L0/L1Calo system in Run 4. The new Level-1 system is shown in red and
 411 pink. Other modules (yellow /orange) are adapted from the previous system to form the
 412 new L0Calo.

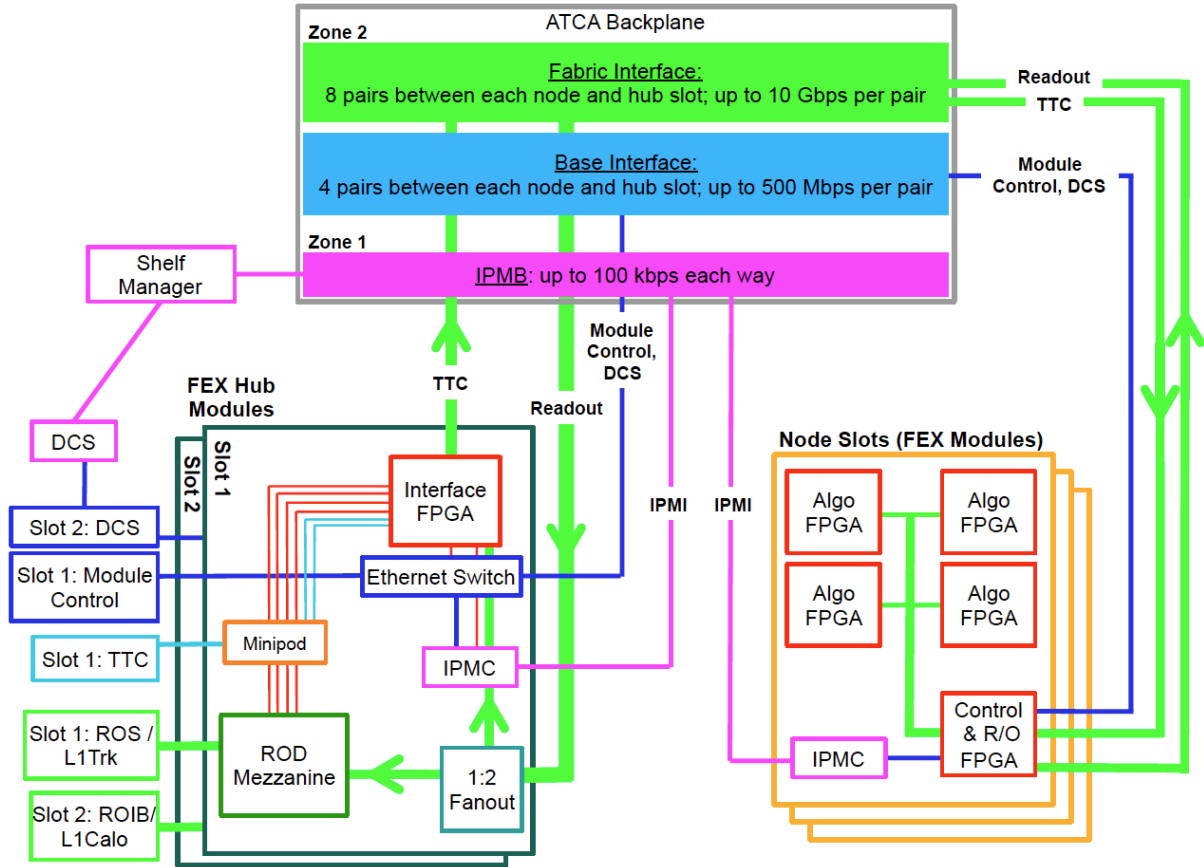
413 **3.2 FEX-Hub Module Overview**

414 The FEX-Hub module is an integral part of the L1Calo system. Its primary functions are
 415 to support FEX system readout, provide switching functionality for module control and
 416 DCS IPbus networks and to distribute timing and control signals to the FEX modules.
 417 **Figure 4** shows a sketch of the Hub modules within the FEX ATCA shelves. There are
 418 to be two Hub modules per shelf. Both Hub modules will receive multi-gigabit FEX data
 419 over the ATCA Fabric Interface, which will be fanned out to a ROD mezzanine on the

420 Hub and to the Hub's own FPGA. This high-speed data path will include two data
421 channels from the other Hub module. The Hub module in logical slot 1 will provide
422 switching capability for a network that routes module control signals on the base
423 interface, while the Hub in logical slot 2 will provide switching for a network that routes
424 DCS information. The Hub module in slot 1 will further receive TTC information from
425 the FELIX system, and these signals will be decoded and fanned out to the FEX modules,
426 ROD modules and also to the Hub in slot 2. The fanned-out TTC control data stream will
427 be interleaved with ROD-to-FEX communications including, for example, back-pressure
428 signals.

429 The Hub module has connections to the other slots in the ATCA shelf over three distinct
430 electrical interfaces, as illustrated in **Figure 4**. ATCA backplane Zone-2 consists of the
431 Fabric Interface and the Base Interface. The Fabric Interface provides 8 differential pairs
432 (channels) from each node slot to each Hub slot (8 to Hub-1 and 8 to Hub-2). There are a
433 total of 8 Fabric Interface channels between Hub-1 and Hub-2 (not 16 total). The Fabric
434 Interface pairs have a nominal bandwidth specification of 10 Gbps / channel. The Base
435 Interface provides 4 differential pairs between each node slot and each Hub slot. There
436 are a total of 4 Base Interface channels between Hub-1 and Hub-2. The Base Interface
437 lines have a nominal bandwidth specification of 500 Mbps / channel, suitable for Gbps
438 Ethernet protocol. Finally, ATCA backplane Zone-1 provides each node and Hub slot
439 with a connection to the Intelligent Platform Management Bus (IPMB) with a total
440 bandwidth of 100 kbps. The Hub module will provide MPO connectors in the ATCA
441 Zone-3 region, which will allow for the routing of fiber-optic cables to/from the
442 MiniPODs on the Hub and ROD modules.

443 The L1Calo FEX-Hub system will consist of eight modules. There will be two eFEX
444 shelves, one jFEX shelf and one L1Topo shelf, each hosting two Hub modules.



445

446 **Figure 4:** Illustration of the functions of FEX-Hub modules within the FEX trigger
 447 system, emphasizing the data paths through the ATCA backplane.

448

449 **4 FEX-Hub Module Functionality**

450 This section describes the functionality required for the FEX-Hub module within the
451 L1Calo FEX trigger system. Details of the implementation of these functions will be
452 described in Section 6 of this document. **Figure 5** illustrates the overall layout of the Hub
453 module, including the outline of the ROD mezzanine card. In this figure, all of the
454 primary functions and features of the Hub module are annotated for reference.

455 **4.1 Support of the ROD Mezzanine Card**

456 The FEX-Hub physically holds the ROD Mezzanine Card and provides electrical
457 connections to it through two 400 pin MEG-Array connectors [1.13].

458 **4.2 FEX and FEX-Hub Readout Data Distribution**

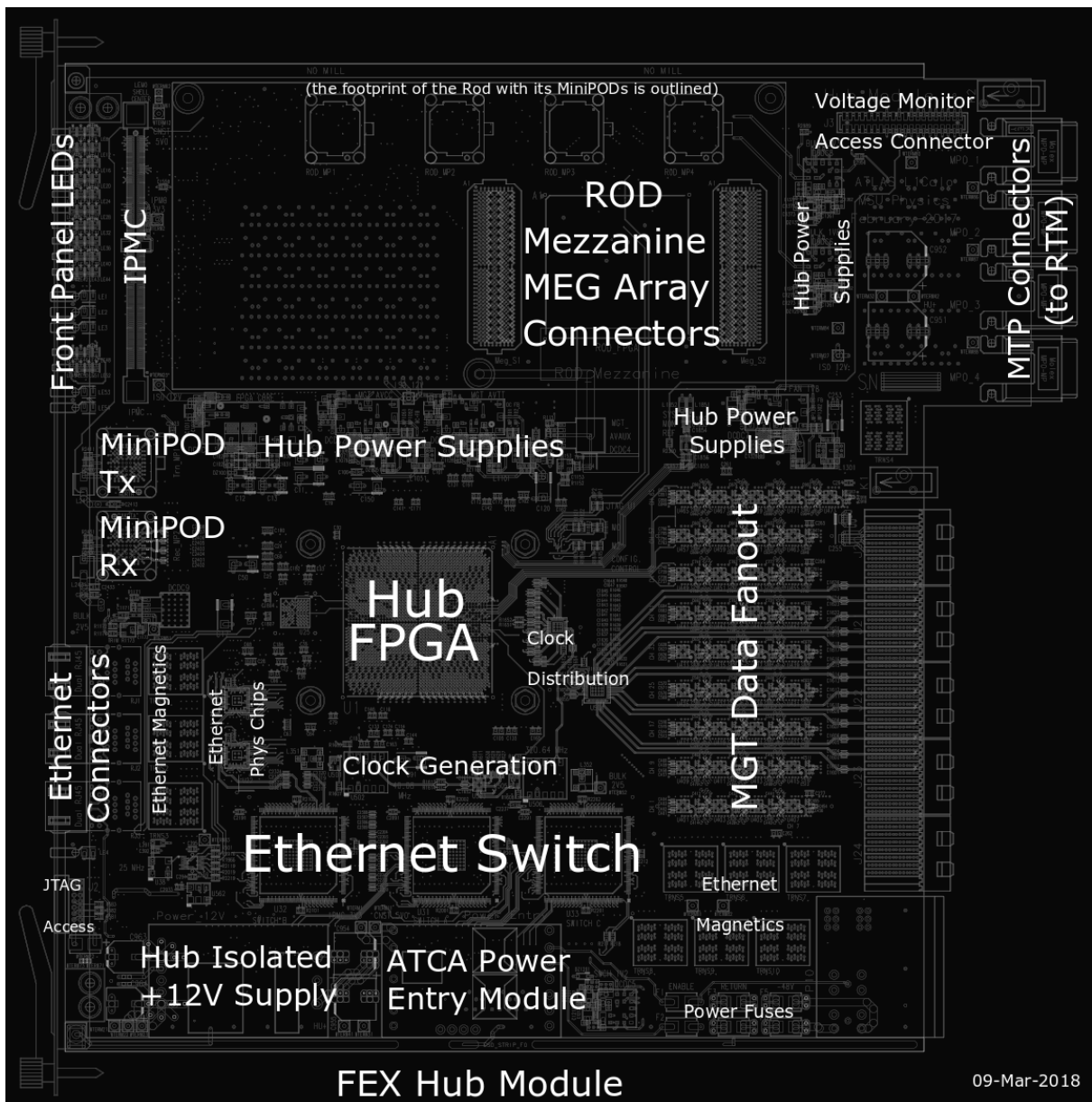
459 The FEX-Hub receives over the Fabric Interface 6 serial streams of Readout Data from
460 each FEX Module. Each FEX-Hub also receives over the Fabric Interface 2 serial
461 streams of Readout Data from the other FEX-Hub in the ATCA shelf. These 74 high-
462 speed serial streams pass through a 1:2 fan-out on the FEX-Hub. One copy of each
463 stream is sent to the ROD mezzanine and one copy is sent to the Hub's own FPGA. The
464 Hub FPGA also sends 2 serial streams with its own Readout Data to its own ROD. Each
465 ROD thus receives a total of 76 high speed Readout Data streams: 6 streams from each
466 FEX, 2 streams from the local Hub FPGA and 2 streams from the other Hub's Hub
467 FPGA. The data rate per readout stream will be 10 Gbps or less.

468 **4.3 TTC Clock and Data Stream Distribution**

469 The FEX-Hub in Slot 1 uses a 12-channel MiniPOD optical receiver to receive TTC
470 signals from the upstream FELIX system. The FEX-Hub receives two types of TTC
471 signals: a copy of the LHC clock and TTC control data. These signals are fanned out to
472 each FEX module, to the local ROD, to the local Hub FPGA and to the FEX-Hub in Slot
473 2 (including its ROD). The LHC clock is directly forwarded without any processing on
474 the FEX-Hub. The TTC control data will be merged with additional control information
475 coming from the ROD module from each FEX-Hub before being fanned out. The FEX-
476 Hub uses two ports from the Fabric Interface Channel to each Node Slot to fan out these
477 two signals to each FEX. These two TTC and control signals sent to the FEX plus the 6
478 Readout Data streams received from each FEX use all 8 signals pairs of each Fabric
479 Channel connecting one FEX to the FEX-Hub, albeit with an unconventional port
480 direction usage.

481 The FEX-Hub in Slot 2 does receive the TTC information from FELIX directly, but
482 receives the TTC Clock and the TTC/ROD readout control stream from the FEX-Hub in

483 Slot 1. The FEX-Hub in Slot 2 sends any required ROD readout control data generated
 484 by its own ROD to the FEX-Hub in Slot 1 for inclusion in the combined TCC/ROD
 485 readout control data stream.



486

487 **Figure 5:** Annotated layout of Hub (+ROD outline) with primary functions noted.

488 **4.4 Ethernet Network Switch**

489 The FEX-Hub hosts an un-managed 10/100/1000 Base-T switch to provide
 490 the following 18 Gigabit Ethernet connections:

491

- 492 • Backplane: 12 connections to the "FEX Node" modules in this crate via the Base
493 Channel Fabric;
- 494 • Backplane: 1 connection to the Ultrascale FPGA on the other Hub via the Update
495 Channel Interface;
- 496 • Direct: 1 connection to the Ultrascale FPGA on this Hub;
- 497 • Front-Panel: 1 connection for an "up-link";
- 498 • Front-Panel: 1 connection for the ROD on this Hub (or IPMC on the other Hub);
- 499 • Front-Panel: 1 connection for the ROD on the other Hub (or IPMC on this Hub);
- 500 • Front-Panel: 1 spare connection;

501

502 This Ethernet switch functionality is implemented in hardware with three interconnected
503 8-port switch chips.

504 The FEX-Hub module circuit board can be modified to disconnect these three switch
505 chips and provide a higher aggregate bandwidth capacity as described in Section 5.

506 **4.5 Slow Control**

507 An IPBus interface is provided for high-level, functional control of the FEX-Hub module.
508 This allows, for example, any firmware parameters to be set, modes of operation to be
509 controlled and monitoring data to be read.

510 **4.6 Connections to the IPMB**

511 The FEX-Hub maintains a connection to the Intelligent Platform Management Bus
512 (IPMB) via an IPM Controller (IPMC) located on the Hub module. Communications
513 between monitorable targets on the Hub, including the ROD mezzanine, are managed via
514 an I2C Bus on the Hub module.

515 **4.7 Power Supplies**

516 The FEX-Hub provides all of the normal ATCA redundant power input, power isolation,
517 and power control from the Shelf Manager via an IPMC card. Bulk +12 Volt power is
518 provided to the ROD Mezzanine Card. Control signals are sent from the Hub to the ROD
519 and Status signals are returned from the ROD to manage the ROD's own power up
520 sequence. DC/DC converters are used to provide the power rails for the Hub itself.

521 **4.8 Extended Use Cases**

522 The FEX-Hub module is intended to be used in the L1Calo and L0Calo trigger systems
523 through Run 4. As such, future use cases in which the Hub may need to augment the
524 capacity of the FEX-Hub-ROD readout path have been identified. This extra
525 functionality is being implemented on the FEX-Hub so long as it does not complicate the
526 core Hub functions and design. These extra Hub functions are as follows:

- 527 • The Hub main FPGA receives a fanned-out copy of all high-speed FEX data being
528 sent to the ROD mezzanine card, allowing at a minimum the monitoring of FEX data.
529 This feature can also support Hub commissioning and diagnostics, as it further
530 provides a Fabric Interface connection to the other Hub module.
- 531 • The Hub main FPGA provides additional MGT links to the ROD mezzanine, which
532 will be instrumented on the ROD if sufficient input MGT links are available.
533 Similarly, MGT links from the ROD to the Hub main FPGA are defined on the HUB-
534 ROD interface.
- 535 • External data output paths from the Hub main FPGA are provided electrically via
536 Ethernet and optically via one MiniPOD transmitter. The MiniPOD socket and
537 routings are implemented by default, but the MiniPOD transmitter is only installed if
538 required.
- 539 Together, this Hub functionality can provide supplemental trigger processing if required.
540 However, all of this functionality could instead be ignored or disabled with no negative
541 impact on the Hub core functions.

542 **4.9 Commissioning and Diagnostic Facilities**

543 The FEX-Hub module provides sufficient Hub-to-Hub electrical connections over the
544 Fabric Interface, Base Interface and front-panel connections to commission and perform
545 standalone diagnostic tests of the Ethernet switching functions, a subset of Fabric
546 Interface high-speed data paths and TTC clock/data distribution using either one or two
547 FEX-Hub modules.

548 Full commissioning and diagnostics will require a mated Hub+ROD, as well as a data
549 source/sink for the node slots (eg, the FEX Test Module or Hub Test Module). The Hub
550 testing and commissioning plan is discussed in greater detail in Section 8.

551 **4.10 Environment Monitoring**

552 The Hub monitors the voltage and current of every power rail on the board. It also
553 monitors the temperatures of FPGAs, of the MiniPOD transmitters (if installed), and of
554 other areas of dense logic. Where possible, this is done using sensors embedded in the
555 relevant devices themselves. Where this is not possible, discrete sensors are used. The
556 voltage and temperature data are collected by the IPMC, via an I2C bus. From there, they
557 are transmitted via Ethernet to the ATLAS DCS system. The Hub hardware also allows
558 these data to be transmitted to the DCS via IPMB and the ATCA Shelf Controller, but it
559 is not foreseen that ATLAS will support this route.

560 **4.11 ATCA Form Factor**

561 The FEX-Hub module is an ATCA module, conforming to the PICMG® 3.0 Revision 3.0
562 specification. The FEX-Hub is only capable of supporting a Dual-Star 14-slot (not 16)
563 ATCA shelf. Within the L1calo system some of the Fabric Interface and Update
564 Interface Channel ports are not used according to their conventional ATCA manner, as
565 described in the technical detail appendices, see Sections 15 and 17.

566 **5 Interfaces to Other L1Calo Modules**

567 The FEX-Hub module has mechanical and electrical connections to three other module
568 types within the L1Calo trigger system: the Hub-ROD Mezzanine card, the
569 eFEX/jFEX/L1Topo modules and the other Hub module when used in a shelf with two
570 Hubs. This section describes and illustrates the electrical connections between these
571 modules.

572 **5.1 TTC Clock and Data Stream Interfaces**

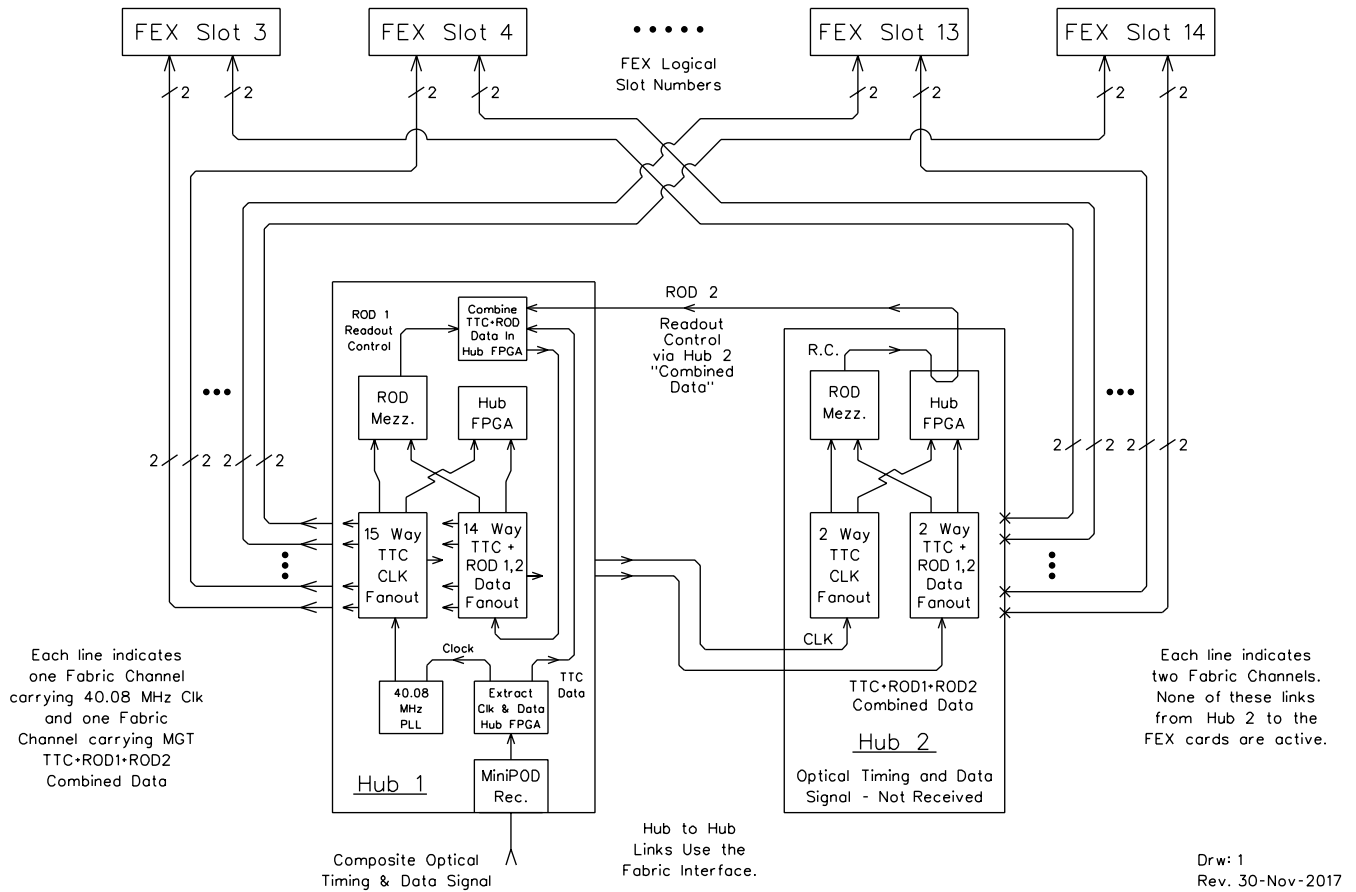
573 **Figure 6** shows the Hub's distribution of the TTC Clock and Data signals in the context
574 of the other cards in the ATCA shelf. The composite TTC signal is received by a
575 MiniPOD receiver on the Hub-1 card. The TTC Clock is fanned out from the Hub-1 card
576 to all other modules in the shelf (including Hub-2) over the Fabric Interface. The TTC
577 Data is combined with the back data from both ROD-1 and ROD-2 on Hub-1 and this
578 combined data stream is also fanned out from the Hub-1 module over the Fabric
579 Interface. When a second Hub is used as shown in **Figure 6**, no TTC information is sent
580 from Hub-2 to any of the Node slots, as the corresponding Fabric Interface ports are not
581 driven on Hub-2. The Hub-1 and Hub-2 cards are identical printed circuit boards and
582 could support independent fan-out of clock and data streams from both Hubs if that were
583 desired in the future. Each Node slot has access to both the Hub-1 and the Hub-2 TTC
584 clock and data streams. L1calo shelves are however currently explicitly defined to
585 provide and use the TTC clock and data information fanned out from Hub-1 only.

586 **5.2 High-Speed Readout Data Interfaces**

587 **Figure 7** shows the Hub's distribution of readout data in the context of the cards in the
588 ATCA shelf. The readout data comes from the Node slots and from the FPGA on each
589 Hub module. All of this data flows to both the ROD and to the FPGA on each Hub. The
590 arrangement shown in **Figure 7** supports 2 independent streams of readout data. That is,
591 the readout stream processed by the ROD and Hub FPGA on Hub-1 can be
592 independent of the readout stream flowing into Hub-2.

593 The Hub's high-speed readout data path as described at the level of the Hub board is
594 illustrated in **Figure 19**, which can be found in the section describing the Hub PCB
595 layout (**Section 6.11**) and in greater detail in the technical detail appendices (**Section 15**).

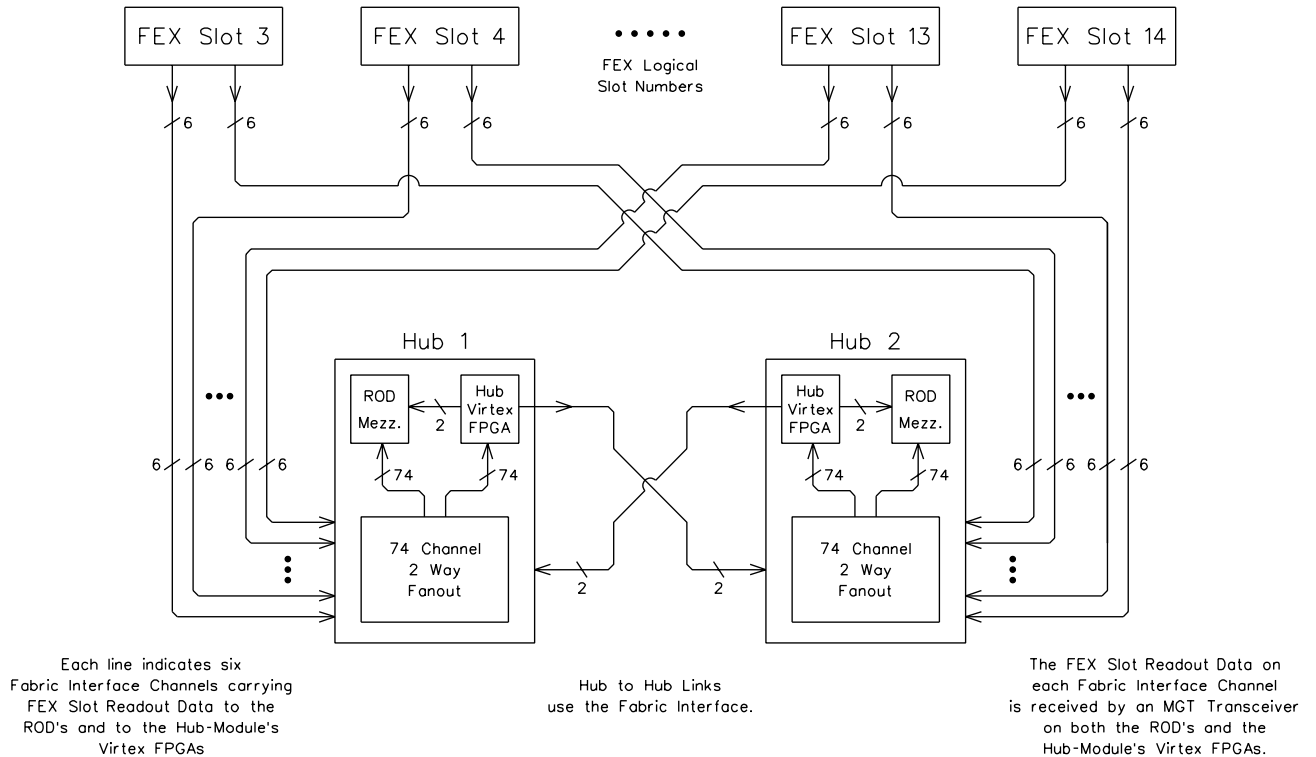
Hub Clock and Combined Data Distribution



596

597 **Figure 6:** Illustration of FEX-Hub distribution of TTC clock and control data stream
598 signals.

Hub-Module Readout Data Distribution



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599

600 **Figure 7:** Illustration of FEX-Hub distribution of high-speed readout data signals.

601

602 **5.3 Ethernet Network Interfaces**

603 **Figure 8** shows the Hub's Base Interface Ethernet Switch in the context of the other cards
 604 in the ATCA shelf. As shown in **Figure 8** the switch on Hub-1 is used to handle all
 605 connections to the IPbus Control network and the switch on Hub-2 is used to handle all
 606 connections to the IPMC/DCS network. Operation with only a Hub-1 in the shelf is
 607 possible but does not provide a Base Interface Ethernet connection to the IPMCs in the

608

609 Node slots. In this situation the Node slot IPMCs can use their IPMB connection to the
 610 Shelf Manager and pass monitoring data to the DCS network.

611 The Gigabit Ethernet switch functionality is implemented in hardware with three
 612 interconnected Broadcom BCM53128 8-port switch chips.

613 When these three switch Chips are left interconnected one up-link connection per Hub is
 614 used to connect the L1calo crate to the rest of the network. The available aggregate
 615 bandwidth for the whole shelf is 1 Gbps over each of the Hub1 and Hub 2 networks. The
 616 corresponding connectivity at the level of one typical L1Calo shelf is depicted in **Figure**
 617 **9**.

618 The FEX-Hub module circuit board can be modified to sever the inter-connections
 619 between these three switch chips. This modification increases the aggregate bandwidth

Hub-Module Ethernet Switch Connections

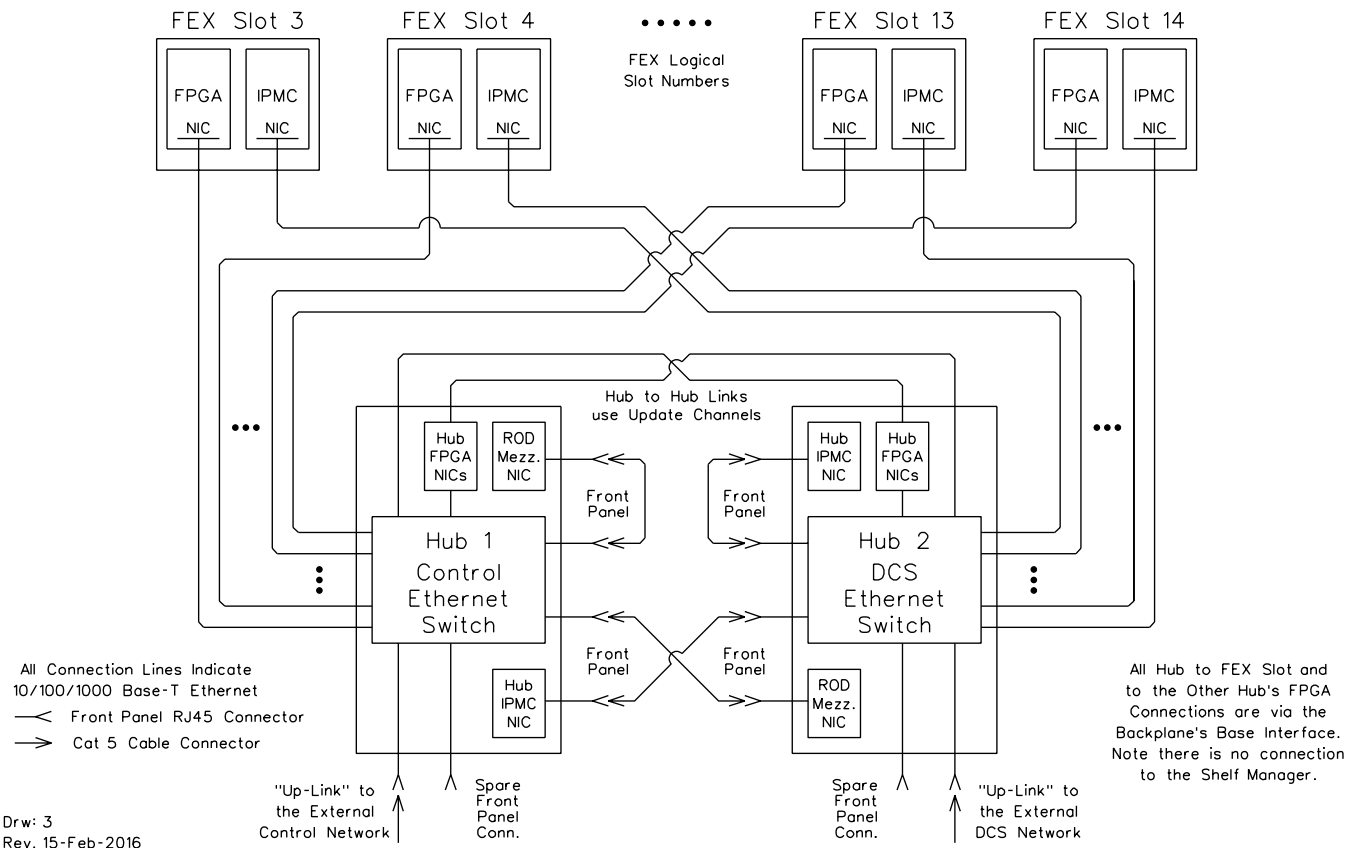
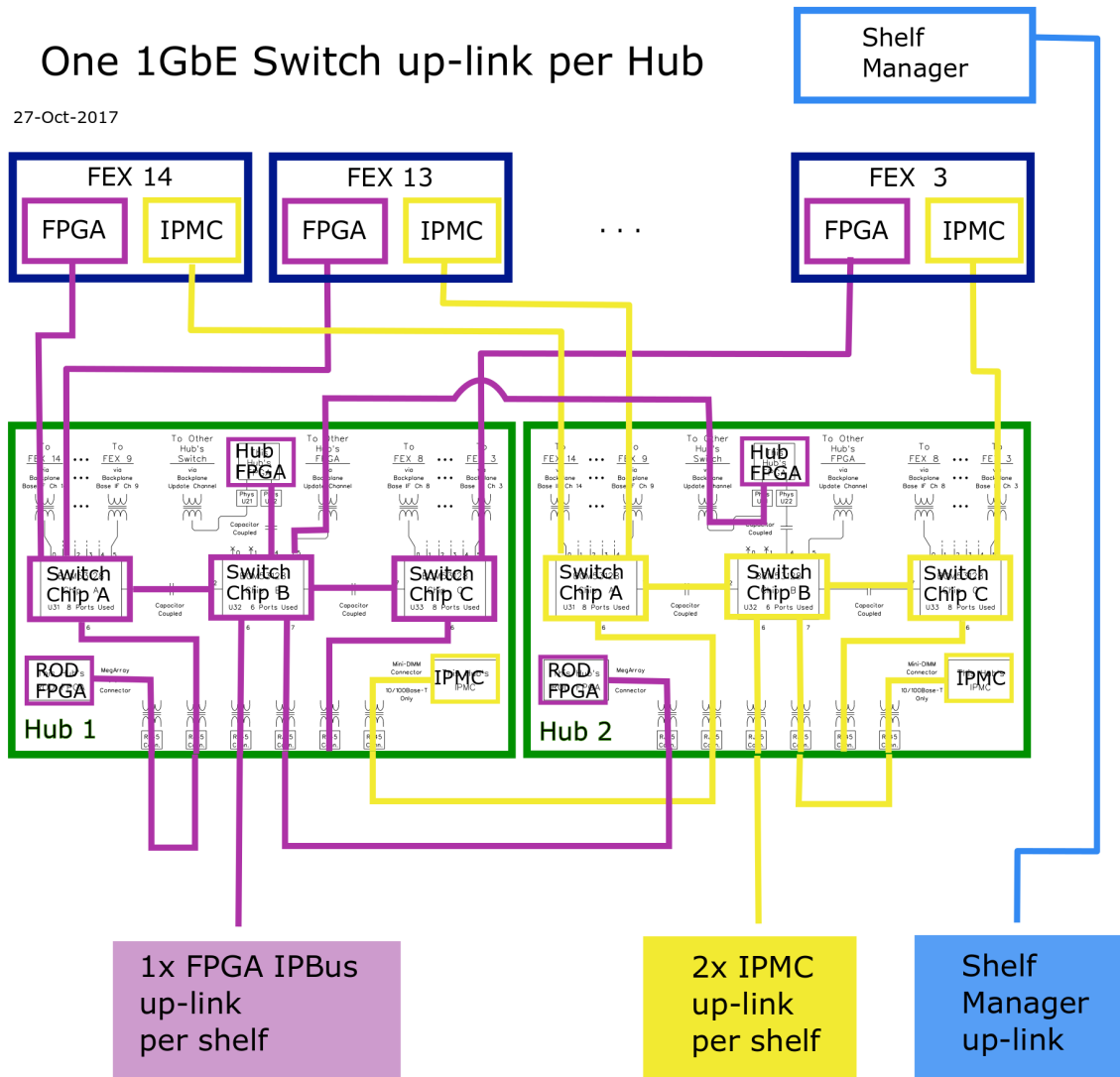


Figure 8: Circuit diagram for the Hub Ethernet switch.

620 capacity. In particular, the aggregate bandwidth is then doubled for the FEX node slots.
 621 Four up-link connections per Hub are then required to connect the 11calo crate to the rest
 622 of the network. The corresponding connectivity at the level of one typical 11calo crate is
 623 depicted in **Figure 10**.



624

625

Figure 9: Hub Ethernet switch configuration with one uplink per shelf.

626

637 **5.4.1.1 Base Interface**

638 The 2 ports of Base Channel 1 (4 pairs of differential signals) of the base interface are
639 used to provide a Gigabit Ethernet connection to be used by the FEX module for its IPbus
640 port.

641 The usage of the ports on this channel follows the ATCA PICMG 3.0 specification for
642 1000BASE-T Ethernet.

643 **5.4.1.2 Fabric Interface**

644 The ports of the Fabric Interface Channel 1 are not used according to the ATCA
645 convention and notation.

646 The 4 ports of Fabric Channel 1 (8 pairs of differential signals) are defined by ATCA as 4
647 transmitting and 4 receiving pairs.

648 Hub-1 is instead transmitting on only 2 of these pairs and receiving readout data from the
649 FEX on the other 6 pairs

650 **5.4.1.3 Hub-1 Module signals as Seen from a FEX Module**

651 The FEX modules receive the LHC clock on the receive signal pair of Fabric Interface
652 Channel 1 port 0. (Note: this clock is received via MiniPOD on Hub-1). This signal is
653 meant to be received as a logic clock and not as data stream. It is not driven by an FPGA
654 MGT Transceiver on the HUB and is not meant to be received by an MGT on a FEX.

655 The FEX modules receive the combined TTC and ROD control data stream on the
656 receive signal pair of Fabric Interface Channel 1 port 1. Note: the TTC control
657 information is provided via the TTC signals sent by FELIX and received on Hub-1. The
658 two RODs on Hub-1 and Hub-2 may need to also send control information to the FEXs.
659 This optional ROD control is merged with the TTC control data stream according to a
660 format to be determined.

661 The FEX modules send their primary readout data streams 0-3 destined to the ROD on
662 Hub-1 on the transmit signal pair of Fabric Interface Channel 1 port 0-3. The FEX
663 module is SENDING its secondary readout data streams 4-5 destined to the ROD on
664 Hub-1 on the RECEIVE signal pair of Fabric Interface Channel 1 port 2-3 which means it
665 is using these two ports in the opposite direction from their conventional usage and
666 ATCA naming.

667 **5.4.2 Interface with Hub-2**

668 Hub-2 resides in logical slot 2 and hosts the IPMC network. Hub-2 does not receive the
669 TTC signal from FELIX via its MiniPOD receiver.

670 *5.4.2.1 Base Interface*

671 The 2 ports of Base Channel 2 (4 pairs of differential signals) of the base interface are
672 used to provide a Gigabit Ethernet connection to be used by the FEX module for its
673 IPMC.

674 The usage of the ports on this channel follows the ATCA PICMG 3.0 specification for
675 1000BASE-T Ethernet.

676 *5.4.2.2 Fabric Interface*

677 The ports of Fabric Interface channel 2 are not used according to the ATCA convention
678 and notation.

679 The 4 ports of Fabric Channel 2 (8 pairs of differential signal) are defined by ATCA as 4
680 transmitting and 4 receiving pairs.

681 Hub-2 is instead transmitting nothing on 2 of these pairs and receiving readout data from
682 the FEX on the other 6 pairs.

683 *5.4.2.3 Hub-2 Module Signals as Seen from a FEX Module*

684 The receive signal pair of Fabric Interface Channel 2 port 0 is unused on FEX modules.
685 The receive signal pair of Fabric Interface Channel 2 port 1 is also unused on FEX
686 modules.

687 The FEX modules send their primary readout data streams 0-3 destined to the ROD on
688 Hub-2 on the transmit signal pair of Fabric Interface Channel 2 port 0-3.

689 The FEX module is SENDING its secondary readout data streams 4-5 destined to the
690 ROD on Hub-2 on the RECEIVE signal pair of Fabric Interface Channel 2 port 2-33
691 which means it is using these two ports in the opposite direction from their conventional
692 usage and ATCA naming.

693 **5.5 Hub Interface to the ROD Mezzanine**

694 Two 400 pin MEG-Array connectors interface the ROD Mezzanine to the FEX-Hub.
695 This section identifies the signals carried through these connectors. A more detailed
696 description of these HUB-ROD connections is given in the technical appendices,
697 **Sections 26, 19 and 18**. An illustration of how the signals are organized in the MEG-
698 Array connectors is shown in **Figure 11**, which emphasizes the relative use of ground
699 and signal pins for the high-speed data lines. This figure is for illustration only and the
700 technical specification appendices should be used for the mapping.

701 Note: both the Ultrascale FPGA used on the FEX-Hub and the Virtex-7 FPGA used on
702 the ROD offer a maximum of 80 MultiGigabit Transceivers (MGT) i.e. 80 Transmitter

703 ports and 80 MGT Receiver ports. The limit on the number of MGT Receivers has been
704 the main limiting factor in the compromises reached in the design of both the Hub-FEX
705 and the ROD.

706 **5.5.1 MGT Differential Inputs to ROD from Hub**

707 These differential signals are connected to MGT Receiver on the ROD FPGA.

- 708 • 12x6 = 72 serial streams of Readout Data from the FEX modules
- 709 • 2x serial streams of Readout Data from the local HUB FPGA
- 710 • 2x serial streams of Readout Data from the other HUB FPGA
- 711 • 1x serial stream of combined TTC and ROD control data stream

712 **5.5.2 MGT Differential Outputs from ROD to Hub**

- 713 • 1x serial stream of ROD Readout Control information

714 This signal needs to be merged with the TTC control data stream by the HUB FPGA of
715 the FEX-Hub in slot 1.

716 A copy of this combined TTC and ROD control data stream is sent to the ROD FPGA
717 from both FEX-Hub in Slot 1 and Slot 2.

718 **5.5.3 Other signals between ROD and Hub**

- 719 • LHC Clock
 - 720 ○ 1x Differential signal pair
- 721 • Geographic Address
 - 722 ○ 8x signals coming from the Hub FPGA
 - 723 The HUB FPGA determines this System Geographic Address by combining
 - 724 the J10 Hardware Address pins with the Shelf Address retrieved from the
 - 725 Shelf Manager by the IPMC. The shelf and slot addressing scheme for this 8-
 - 726 bit address needs to be defined.
- 727 • IPbus port
 - 728 ○ 4x Bi-directional Signal Pairs forming a 1000BASE-T Gigabit Ethernet
 - 729 connection.
- 730 • Sensor I2C Bi-directional Bus

- 731 ○ 2x I2C Signals (Clock and Data) connected to the IPMC
- 732 • JTAG access
- 733 ○ 4x JTAG Signals
- 734 • Power Supply Connections
- 735 ○ +12V bulk power is made available to the ROD
- 736 • Power Control signals: 4 single-ended bidirectional signals nominally used as
- 737 ○ 2x Power Control Signals to the ROD
- 738 ○ 2x Power Status Signals from the ROD
- 739 • Control and Status
- 740 ○ 5x ROD-specified LEDs
- 741 ○ 2x Phy LEDs
- 742 ○ 1x Lemo
- 743 ○ 4x spare bidirectional differential pairs
- 744 ○ 1x ROD present

Hub - ROD Pinout

S2

	A	B	C	D	E	F	G	H	J	K
1	G	G	G	G	G	G	G	LA1	LA2	G
2	G	HRD1	G	G	G	G	G	LA3	LA4	G
3	G	G	G	G	HRD0	G	G	LA5	LA6	G
4	G	71	G	G	G	G	G	LA7	LA8	G
5	G	G	G	G	70	G	G	G	G	G
6	G	69	G	G	G	G	G	HRD3	G	G
7	G	G	G	G	68	G	G	G	G	G
8	G	67	G	G	G	G	G	HRD2	G	G
9	G	G	G	G	66	G	G	G	G	G
10	G	65	G	G	G	G	G	RSV	RSV	G
11	G	G	G	G	64	G	G	G	G	G
12	G	63	G	G	G	G	G	RSV	RSV	G
13	G	G	G	G	62	G	G	G	G	G
14	G	61	G	G	G	G	G	RSV	RSV	G
15	G	G	G	G	60	G	G	G	G	G
16	G	59	G	G	G	G	G	RSV	RSV	G
17	G	G	G	G	58	G	G	G	G	G
18	G	57	G	G	G	G	G	RSV	RSV	G
19	G	G	G	G	56	G	G	G	G	G
20	G	55	G	G	G	G	G	RSV	G	G
21	G	G	G	G	54	G	G	G	G	G
22	G	53	G	G	G	G	G	RSV	G	G
23	G	G	G	G	52	G	G	G	G	G
24	G	51	G	G	G	G	G	TCK	TMS	G
25	G	G	G	G	50	G	G	TDI	TDO	G
26	G	49	G	G	G	G	G	PC1	PC2	G
27	G	G	G	G	48	G	G	PC3	PC4	G
28	G	47	G	G	G	G	G	G	G	G
29	G	G	G	G	46	G	G	SPARE_R2H3	G	G
30	G	45	G	G	G	G	G	G	G	G
31	G	G	G	G	44	G	G	SPARE_R2H2	G	G
32	G	43	G	G	G	G	G	G	G	G
33	G	G	G	G	42	G	G	SPARE_R2H1	G	G
34	G	41	G	G	G	G	G	SPARE_R2H0	G	G
35	G	G	G	G	40	G	G	G	G	G
36	G	39	G	G	G	G	G	G	G	G
37	G	G	G	G	38	G	G	G	G	G
38	G	37	G	G	G	G	G	RRC	G	G
39	G	G	G	G	36	G	G	G	G	G
40	G	G	G	G	G	G	G	G	G	G

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Notes
(1) Differential Signal polarities are as shown.
(2) The Signal pins are available for the other ROD-Hub signals

0 - 71 = FEX_DATA
s = no connect
TxRx = Gigabit Ethernet Magnetics
LAn = Location Address 1-8
RRc = ROD_READOUT_CONTROL
SPARE_R2H = SPARE R2H MGT LINK
LHC_CLK = LHC Clock from Hub
PCn = Power Control 1-4
RP = Rod_Present
RSV - reserved for testing
HRD = HUB_READOUT_DATA
SMBA = SMB Alert

S1

	A	B	C	D	E	F	G	H	J	K
1	V	LED-0	LED-1	G	G	G	G	G	G	G
2	V	LED-Y	LED-R	G	G	G	G	TTC	G	G
3	V	LED-B	LED-G	G	35	G	G	G	G	G
4	V	Lemo-0	Lemo-1	G	G	G	G	34	G	G
5	V	G	G	G	33	G	G	G	G	G
6	V	RSV	RSV	G	G	G	G	32	G	G
7	V	G	G	G	31	G	G	G	G	G
8	V	RSV	RSV	G	G	G	G	30	G	G
9	V	G	G	G	29	G	G	G	G	G
10	V	RSV	RSV	G	G	G	G	28	G	G
11	V	G	G	G	27	G	G	G	G	G
12	V	RSV	RSV	G	G	G	G	26	G	G
13	V	G	G	G	25	G	G	G	G	G
14	V	RSV	RSV	G	G	G	G	24	G	G
15	V	G	G	G	23	G	G	G	G	G
16	V	TBD_LINK3	G	G	G	G	G	22	G	G
17	V	G	G	G	21	G	G	G	G	G
18	V	TBD_LINK2	G	G	G	G	G	20	G	G
19	V	G	G	G	19	G	G	G	G	G
20	V	TBD_LINK1	G	G	G	G	G	18	G	G
21	V	G	G	G	17	G	G	G	G	G
22	V	TBD_LINK0	G	G	G	G	G	17	G	G
23	V	G	G	G	16	G	G	G	G	G
24	V	s	s	G	G	G	G	15	G	G
25	V	SCL0	SDAO	G	G	G	G	14	G	G
26	V	G	G	G	13	G	G	G	G	G
27	V	SMBA	s	G	12	G	G	G	G	G
28	V	G	G	G	11	G	G	G	G	G
29	V	TxRxA_P	TxRxA_N	G	10	G	G	G	G	G
30	V	G	G	G	9	G	G	G	G	G
31	V	TxRxB_P	TxRxB_N	G	8	G	G	G	G	G
32	V	G	G	G	7	G	G	G	G	G
33	V	TxRxC_P	TxRxC_N	G	6	G	G	G	G	G
34	V	G	G	G	5	G	G	G	G	G
35	V	TxRxD_P	TxRxD_N	G	4	G	G	G	G	G
36	V	G	G	G	3	G	G	G	G	G
37	V	s	RP	G	2	G	G	G	G	G
38	V	G	G	G	1	G	G	G	G	G
39	V	LHC_CLK	G	G	0	G	G	G	G	G
40	V	G	G	G	G	G	G	G	G	G

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Figure 11: Illustration of the ROD/Hub MEG-Array connector pin usage, illustrating signal and ground designations. This diagram is not intended for signal mapping, and the final mapping is provided in the technical appendices.

746 **5.6 Hub Interfaces to Second Hub Modules**

747 **5.6.1 Base Interface**

748 The Base Channel 1 is reserved for the Shelf Manager Controller and is unused.

749 The Base Channel 2 port (4 pairs of differential signals) is not currently allocated.

750 **5.6.2 Fabric Interface**

751 The Fabric Interface channel 1 is used according to the ATCA convention and notation
752 with one caveat for Hub-2: Hub-2 is transmitting nothing on 2 of its transmitter pairs.

753 **5.6.3 Hub-2 usage of the Fabric Interface connection to Hub-1**

754 Hub-2 is receiving the LHC clock on the receiving signal pair of Fabric Interface Channel
755 1 port 0.

756 Hub-2 is receiving the combined TTC and ROD control data stream on the receiving
757 signal pair of Fabric Interface Channel 1 port 1.

758 Hub-2 is sending on the transmitting signal pair of Fabric Interface Channel 1 port 0-1 its
759 readout data streams 1-2 destined to the ROD on Hub-1.

760 **5.6.3.1 Hub-1 usage of the Fabric Interface connection to Hub-2**

761 The receiving signal pair of Fabric Interface Channel 1 port 0 is unused on Hub-1.

762 Hub-1 is receiving on the receive signal pair of Fabric Interface Channel 1 port 1 the
763 ROD Readout control information from the ROD on Hub-2.

764 Hub-1 is sending on the transmit signal pair of Fabric Interface Channel 1 port 0-1 its
765 readout data streams 1-2 destined to the ROD on Hub-2.

766 **5.6.4 Update Channel Interface**

767 The 5 ports of the Update Channel (10 pairs of differential signal) are defined by ATCA
768 as 5 transmitting and 5 receiving pairs. The first 4 ports of the Update Channel Interface
769 are not used according to this ATCA convention and notation. The 5th port of the Update
770 Channel Interface is not currently allocated.

771 The 4 Transmit pairs of Update Channel port 0-4 form one Gigabit Ethernet link and are
772 connected to a Switch port of the local Hub. The 4 Receive pairs of Update Channel port
773 0-4 form another Gigabit Ethernet link and are connected to the Hub FPGA on the local
774 Hub.

775 Note: the exact pin assignment of each port to the four 1000BASE-T signal pairs will be
776 specified later while this assignment is internal to Hub operation only (no other L1Calo
777 modules are affected).

778 This Hub-to-Hub connection allows the Hub FPGA on Hub-2 to connect to the IPbus
779 Network serviced by the Ethernet switch on Hub-1.

780 The Hub FPGA on Hub-1 is directly connected to the IPbus Network switch on Hub-1
781 and can simply ignore this additional Ethernet port that would connect it to the IPMC
782 Network serviced by the Ethernet switch on Hub-2.

783 **6 Hub Implementation Details**

784 This section describes the details of how the FEX-Hub functionality has been
785 implemented for the prototype module, which is also the intended implementation for the
786 final production module. The prototype FEX-Hub module is shown in **Figure 12** and
787 **Figure 13**, wherein the ROD mezzanine card has been mounted to illustrate the
788 anticipated final form of the Hub+ROD pairing.

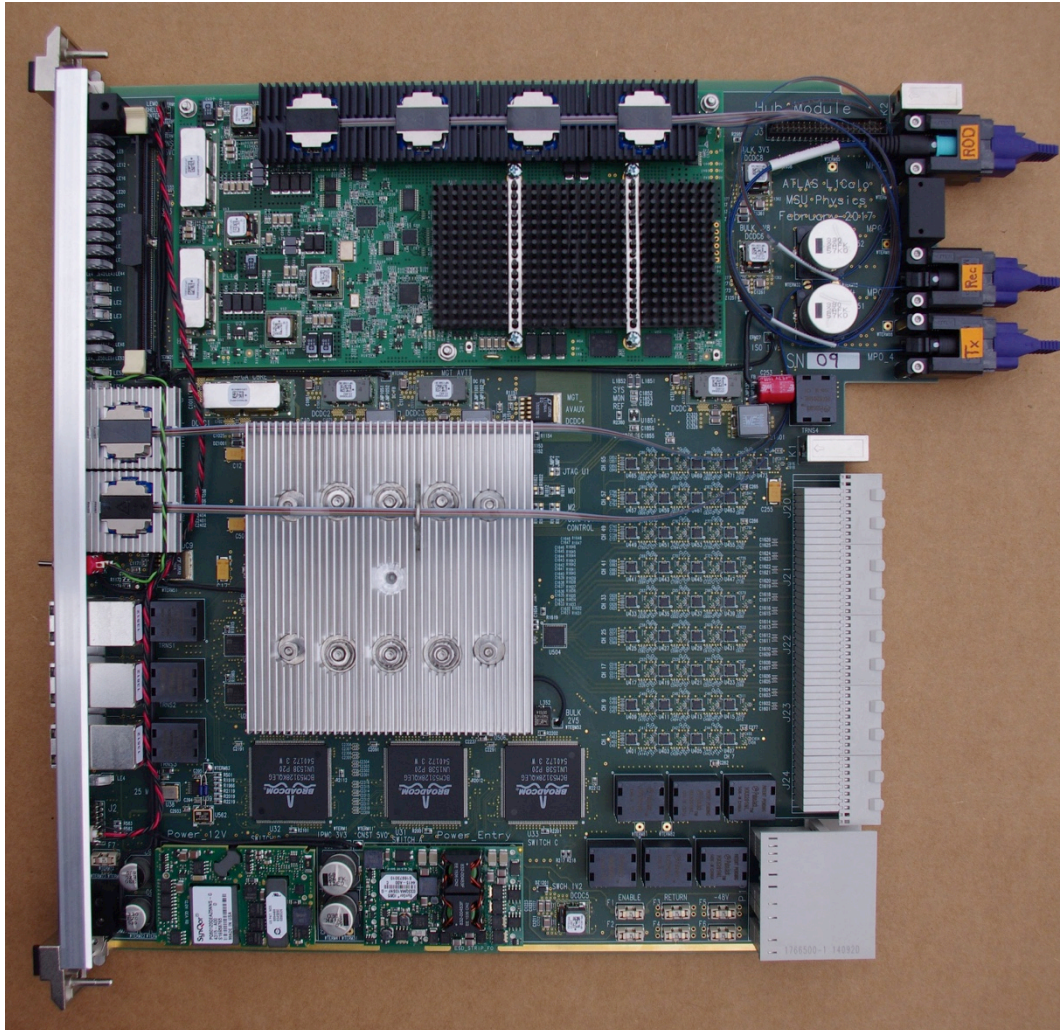
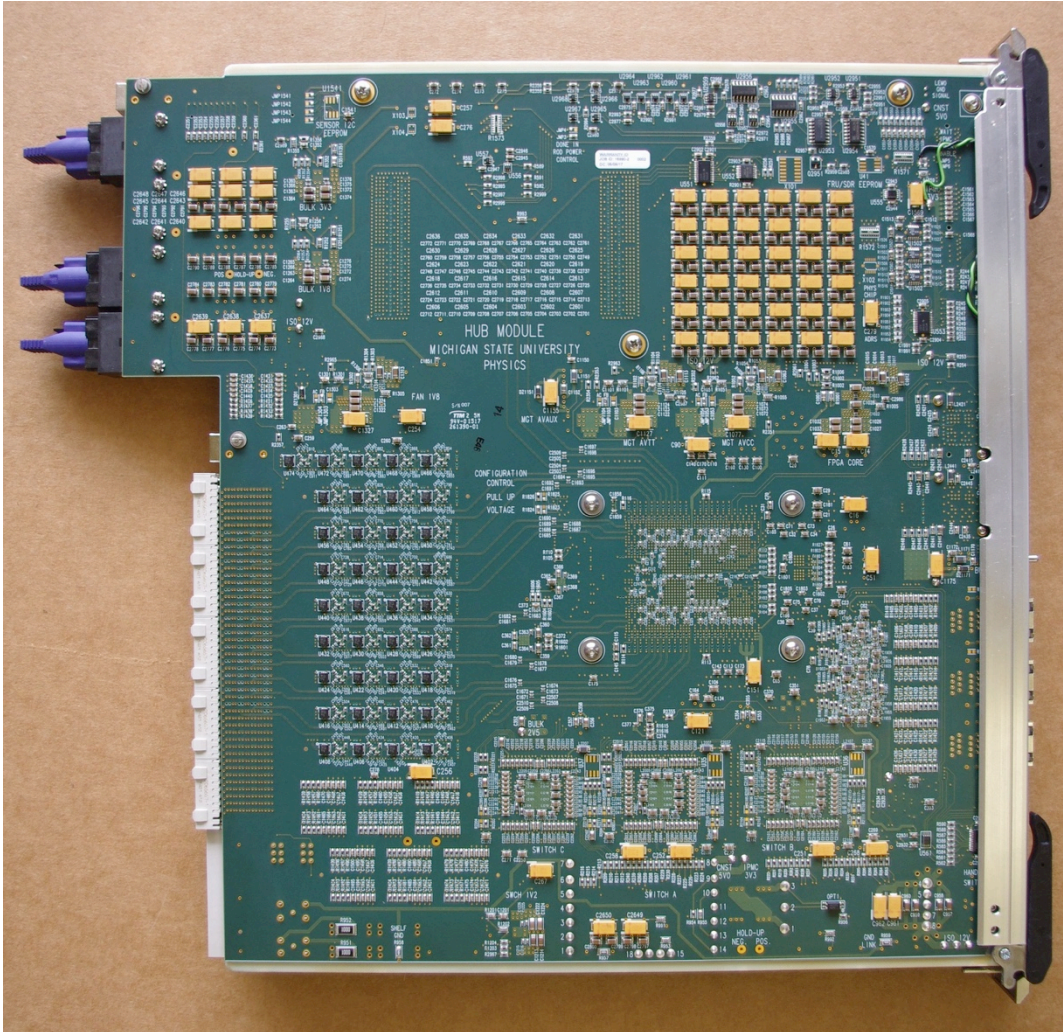


Figure 12: Prototype FEX-Hub module with ROD mezzanine mounted, as viewed from the front of the module.



789

790 **Figure 13:** Prototype FEX-Hub module, as viewed from the back of the module.

791 **6.1 Physical Layout**

792 The FEX-Hub module is implemented as a size 6 HP ATCA card, with the L1Calo-
 793 specified bump-out in Zone 3 to accommodate the L1Calo RTM. An annotated
 794 illustration of the physical layout can be found in **Figure 5**.

795 The Hub holds the ROD mezzanine card. The ROD is located near the top edge of the
 796 Hub and runs from the Hub's front panel edge for 200 mm towards the Hub's backplane
 797 edge. In the direction along the front panel the ROD runs for 100 mm.

798 The Hub and ROD are electrically connected by two 400 pin MEG-Array connectors. A
 799 short 4mm stack height is used so that the Hub and ROD PCBs are quite close to each
 800 other. The component sides of the Hub and ROD both face in the same direction. The
 801 intent is to keep the path of the high-speed differential signals from the Hub to the ROD

802 as short as possible and to give the maximum available height for the MiniPODs and
803 other components on the ROD.

804 The Hub and ROD are mechanically connected to each other using standoffs. The Hub
805 holds the fiber-optic pig-tail cables and connectors that run from Zone 3 on the Hub to
806 the MiniPOD devices on the ROD.

807 The primary components on the Hub card are a Xilinx Ultrascale FPGA, three Broadcom
808 GbE switches (with associated PHY chips and RJ45 connectors), 74 ON-Semi 1:2 fanout
809 chips.

810 The Hub includes heat sinks for its FPGA, and for its MiniPODs. Along its backplane
811 edge the FEX-Hub uses the Zone 1 P10 connector, the full complement of Zone 2
812 connectors (J20 through J24), and 4 MPO connectors in Zone 3.

813 **6.2 Readout Signal Distribution**

814 The FEX-Hub receives readout data on 6 channels of the Fabric Interface from each of
815 the 12 node slots in the shelf. This is 72 channels of high-speed readout data from the
816 FEX node slots. In addition the Ultrascale FPGA on the other FEX-Hub provides 2
817 Fabric Interface channels of readout data. This makes a total of 74 channels of readout
818 data from other slots in the shelf. The FPGA on the FEX-Hub holding the ROD also
819 provides 2 GTH channels of readout data. Thus a total of 74 GTH receivers on the ROD
820 are required to field the readout data from all sources in the shelf.

821 The readout data from the backplane is received by the Hub with On-Semi 2-way fan-out
822 chips that have built-in termination.

823 One output from these fan-out chips runs to 74 MGT inputs on the FEX-Hub's Ultrascale
824 FPGA. The other output from these fan-out chips is routed through the 2 Meg-Array
825 connectors to the ROD mezzanine card.

826 The pinout of the Meg-Array connectors to the ROD has been designed to provide
827 optimum signal fidelity for these high-speed differential signals. The intent is to provide
828 a clean, uniform, and short route for the traces on the ROD that connect the Meg-Array
829 pins to its GTH transceiver inputs. On the ROD the Meg-Array connectors are located
830 adjacent to the edges of its Ultrascale FPGA that hold the MGT transceivers.

831 Additional details can be found in the technical appendices (Section 15).

832 **6.3 Timing and Trigger Control Distribution**

833 In normal operation Hub #1 uses a MiniPOD to receive an optical link from FELIX that
834 contains the LHC Reference Clock and the TTC Data Stream. Logic in the Hub's FPGA

835 separates the LHC Reference Clock from this composite signal and sends it to the
836 reference input of a 40.0787 MHz quartz crystal based Phase Locked Loop. The
837 composite control information is combined with data flow control signals from the two
838 ROD modules in the shelf.

839 The FEX-Hub distributes the TTC Clock and the TCC Data Stream to 15 different
840 objects that use these signals. The objects that use these TTC signals are: 12 ATCA
841 Node Slots, the ROD mezzanine card on this Hub, this Hub's own Ultrascale FPGA, and
842 finally distribution of these TTC signals to the other Hub module.

843 **6.3.1 Clock Distribution**

844 Distribution of the TTC Clock by the Hub is purely by fan-out. Note that the Hub will
845 provide a 40.08 MHz clock signal even when it is not receiving a composite TTC input
846 signal.

847 The specified “pull range” of of this PLL is +/- 40 ppm minimum which gives them an
848 operating range of 40.077097 MHz to 40.080303 MHz. This operating range covers all
849 conditions of operating temperature, supply voltage, and aging. The operating range of
850 these PLLs is wider than the frequency range specified in FELIX Requirement
851 2.3.5: “The FE systems shall operate in the BC clock frequency range 40.078886 MHz to
852 40.078973 MHz during proton runs (at 6.5 TeV) and in the range 40.078422 MHz to
853 40.078970 MHz during heavy ion runs (at 6.5 TeV)”.

854 The clean output of the Hub’s 40.0787 MHz PLL is fanned out to the following loads:

- 855 • as an AC coupled LVDS reference clock to the ROD on this Hub,
- 856 • as a logic clock to the FPGA on this Hub,
- 857 • as a reference clock to the 320.6296 MHz PLL on this Hub,
- 858 • as an AC coupled LVDS reference clock over the backplane to the Hub Module
859 #2 in this shelf,
- 860 • as an AC coupled LVDS reference clock over the backplane to the 12 FEX cards
861 in this shelf

862 In normal operation Hub Module #2 receives its reference clock over the backplane just
863 like the 12 FEX cards. Hub Module #2 does not receive an optical link from FELIX with
864 the LHC Reference Clock. In Hub Module #2 the backplane reference clock is sent to
865 the reference input of its 40.0787 MHz PLL. From there the clean 40 MHz clock signal is
866 fanned out to the following loads:

- 867 • as an AC coupled LVDS reference clock to the ROD on this Hub,

- 868 • as a logic clock to the FPGA on this Hub,
- 869 • as a reference clock to the 320.6296 MHz PLL on this Hub

870 **6.3.2 Control Signal Distribution**

871 Distribution of the TTC Data Stream by the Hub is more complicated than what's
872 required for the clock signal. As shown in the TTC Distribution drawing the TTC Data
873 Stream is mixed with the "back data" coming from both the ROD on Hub-1 and the ROD
874 on Hub-2. A small part of the logic available in the Hub-1 Virtex FPGA is used to
875 combine these 3 data streams.

876 Fabric Interface Channels are used to carry the TTC Clock and the combined Data
877 Stream from Hub-1 to the Node Slots and from Hub-1 to Hub-2. When the Hubs are
878 used this way all Node slots receive both their TTC Clock and the combined Data Stream
879 from the Fabric Interface channels to Hub-1. Note that the PCB traces on both Hubs are
880 the same so that distribution of TTC Data combined with back data from the ROD on
881 Hub-1 on one set of Fabric channels while separately distributing TTC Data combined
882 with back data from the ROD on Hub-2 on another set of Fabric channels is possible.

883 We assume that extraction of the information that a given object requires from the
884 combined TTC plus ROD Data Stream will be performed by FPGA firmware in that
885 object. Further we assume that all objects will receive the combined Data Stream using a
886 MGT Transceiver.

887 As noted the Hub module that holds receives the TTC signal will distribute the TTC
888 Clock and combined Data Stream signals to the other Hub. This connection is necessary
889 to supply these signals to the ROD and Ultrascale FPGA on the other Hub. The physical
890 path to carry these signals from the Hub that receives the FELIX TTC signal to the other
891 Hub is a pair of Fabric Interface channels that run between the Hubs.

892 Note that only the Fabric Interface channels from the Hub that receives the TTC signals
893 from FELIX are actually active. The TTC Fabric Interface channels from the other Hub
894 (Hub-2) are tied Low by that Hub.

895 **6.4 Base Interface Switch**

896 Each FEX-Hub provides a 10/100/1000 Base-T Ethernet switch with 19 ports that are
897 connected to the following:

- 898 • 1 connection to the front panel i.e. the "up-link";
- 899 • 1 connection to the ROD (or IPMC) on this Hub;

- 900 • 1 connection to the ROD (or IPMC) on the other Hub;
- 901 • 1 connection to this Hub's Virtex FPGA;
- 902 • 1 connection to the other Hub's Virtex FPGA;
- 903 • 1 connection to the Shelf Manager;
- 904 • 1 spare front panel connection;
- 905 • 12 connections to the "Node" boards in this shelf.

906 This Hub switch is implemented using 3 Broadcom BCM53118 devices. These 8 port
907 switches include the PHY interface to the BASE-T network connections. Besides
908 providing the advantage of build in PHY interface the BCM53118 can be operated as
909 either a simple unmanaged switch or if managed it can provide advanced switch features.
910 The intent is to provide a prototype Hub switch that is easy for everyone to use but that
911 has advanced features available via remote management if needed.

912 The prototype Hub module has 6 RJ45 Ethernet connectors on its front panel: 4
913 connectors to its switch, one to the Hub ROD and one to the Hub IPMC. The 4 switch
914 connections are normally used for: the up-link to the external network, two ports for
915 connections to either both Hub RODs or both Hub IPMCs (depending on whether this is
916 Hub-1 or Hub-2), and a spare front panel Ethernet connection.

917 The point of having these connections accessible via front panel RJ45 connectors is to
918 make the prototype Hub easy to use in various test setups where either one or two Hubs
919 may be used. The RJ45 connections to the Hub also allow the switch to be tested without
920 any other ATCA cards in the system.

921 **6.5 Hub FPGA**

922 The main Hub FPGA is a large Xilinx Ultrascale device: the XCVU125-1FLVC2104I.

923 This is speed grade “1”, i.e. the normal common slowest speed grade and it is the
924 “Industrial” temperature range which is the common temp range for most of these
925 UltraScale parts.

926 This part has: 40 GTH Transceivers and 40 GTY Transceivers. These are spread across 2
927 Super Logic Regions (SLRs) with 20 of each kind of transceiver in each SLR.

928 This part has 7 HP Select I/O Banks with 52 I/O signals in each. 4 of the HP banks are in
929 SLR #0 and 3 of the HP banks are in SLR #1.

930 This part also has 2 HR Select I/O Banks with 26 I/O signals in each. Both of the HR
931 banks are in SLR #0. The Hub Module uses both of the HR Banks for 3V3 I/O and it
932 uses most of the signals in these Banks.

933 More details are available in the technical description of the Hub FPGA implementation.

934 **6.6 The IPM Controller**

935 For the purposes of monitoring and controlling the power, cooling and interconnections
936 of a module, the ATCA specification defines a low-level hardware management service
937 based on the Intelligent Platform Management Interface standard (IPMI). The Intelligent
938 Platform Management (IPM) Controller is that portion of a module (in this case, the
939 FEX-Hub) that provides the local interface to the shelf manager via the IPMI bus. It is
940 responsible for the following functions:

- 941 • interfacing to the shelf manager via dual, redundant Intelligent Platform Management
942 Buses (IPMBs); it receives messages on all enabled IPMBs and alternates
943 transmissions on all enabled IPMBs;
- 944 • negotiating the Hub power budget with the shelf manager and powering the Payload
945 hardware only once this is completed;
- 946 • managing the operational state of the Hub, handling activations and deactivations,
947 hot-swap events and failure modes;
- 948 • implementing electronic keying, enabling only those backplane interconnects that are
949 compatible with other modules in shelf, as directed by shelf manager;
- 950 • providing to the Shelf Manager hardware information, such as the module serial
951 number and the capabilities of each port on backplane;
- 952 • collecting, via an I2C bus, data on voltages and temperatures from sensors on the
953 Hub, and sending these data, via IPBus, to the main Hub FPGA;
- 954 • driving the BLUE LED, LED1, LED2 and LED3.

955 The Hub uses the IPMC mezzanine produced by LAPP as the IPM Controller [1.9]. The
956 form factor of this mezzanine is DDR3 VLP Mini-DIMM.

957 **6.7 Power Supplies and Management**

958 The power design and power management on the FEX-Hub conform to the full ATCA
959 PICMG® specification (issue 3.0, revision 3.0). Details of the FEX-Hub power system
960 are given in Section 28, and a summary description is provided here.

961 A SynQor IQ65033QMA10SNF-G (10A, 300W) power entry module provides -48V dual
962 redundant input power distribution and 3.3V/5.0V isolated management power for IPMC
963 and its auxiliary circuitry. From the power entry module filtered power, monitored by the
964 IPMC, flows to the input of an Isolated +12 Volt converter. This converter makes the
965 Isolated +12 Volt power that operates everything on the Hub Module except for the
966 power supervision circuits and the IPMC mezzanine card. The Isolated +12 Volt power
967 is provided by a SynQor PQ60120QEA25NNS-G 12V 25A 300 Watt quarter-brick
968 module. Higher current modules are available if needed.

969 By default, on power up, the management power for the IMPC is on. The payload power
970 is disabled by the IPMC until it has successfully negotiated power-up rights with the
971 ATCA Shelf Manager. To enable bench-top diagnosis, a toggle switch is provided to
972 bypass the IPMC. This switch will be disabled for the FEX-Hub modules when they are
973 ready for installation.

974 Details of the Hub power configuration and management can be found in the technical
975 appendices, Section 28.

976 The total power consumption of the FEX-Hub is estimated to be approximately 65W,
977 measured using a FPGA configuration that enables all MGTs operating at their maximum
978 anticipated line rates. Thus, this estimate does not account for any future power
979 consumption by algorithms running in the Hub FPGA fabric.

980 **6.8 Thermal Management**

981 The ATLAS-standard ATCA shelf uses vertical airflow with water chillers sandwiched
982 between shelves. The cooling capacity in ATLAS Point 1 is 400W per slot (front space),
983 which is well above the estimated FEX-Hub power consumption. A high thermal-
984 conductivity aluminium heat-sinks is used for the main FPGA, and heat sinks are fitted
985 for the MiniPOD electro-optical transceivers (if fitted). Finally, the ROD mezzanine is
986 allocated 100W of the total cooling budget, and will manage/monitor the temperature of
987 its FPGA and MiniPODs.

988 **6.9 Front-Panel Layout**

989 The FEX-Hub includes an extruded aluminum ATCA front panel with an EMC
990 gasket. The front panel insertion extraction handles actuate a PCB mounted micro-switch
991 for the hot-swap function.

992 Penetrations through the front panel include those for the standard ATCA LEDs, those
993 for the RJ45 Ethernet connections, LEDs for each of the Hub GbE links to the ROD and
994 backplane, JTAG connection, a LEMO connection to the ROD, five that are required for
995 the ROD mezzanine card and three spare (functions so far unspecified) Hub specific

996 LEDs. Further, the prototype Hub module has a front-panel toggle switch to control the
997 power-on sequence, which will be removed for the production Hub modules.

998 The Hub prototype module front panel silk screen is shown in **Figure 14**.

Hub Module
Front Panel
Draft
Silk
Screen

LE5:LE8
LE9:LE12
LE13:LE16
LE17:LE20
LE21:LE24
LE25:LE28
LE29:LE32
LE33:LE36
LE37:LE40
LE41:LE44

LE1
LE2
LE3

LE45:LE48
LE49:LE52

LE53
LE54

RJ1

RJ2

RJ3

LE4

J2 and LEMO



999

1000

Figure 14: Hub prototype front panel silk screen.

Switch port to OtherHub Link green LED #5	Activity yellow LED #6	Switch port to FEX 3 Link green LED #7	Activity yellow LED #8	ATCA Mandatory: Failure (IPMC Socket pin #104) Red LED #1
Switch port to FEX 4 Link green LED #9	Activity yellow LED #10	Switch port to FEX 5 Link green LED #11	Activity yellow LED #12	ATCA Optional: TBD (IPMC Socket pin #105) Green LED #2
Switch port to FEX 6 Link green LED #13	Activity yellow LED #14	Switch port to FEX 7 Link green LED #15	Activity yellow LED #16	ATCA Optional: TBD (IPMC Socket pin #106) Red LED #3
Switch port to FEX 8 Link green LED #17	Activity yellow LED #18	Switch port to FEX 9 Link green LED #19	Activity yellow LED #20	Driven by ROD FPGA ConfigDone Green LED #45
Switch port to FEX 10 Link green LED #21	Activity yellow LED #22	Switch port to FEX 11 Link green LED #23	Activity yellow LED #24	PowerGood Green LED #46
Switch port to FEX 12 Link green LED #25	Activity yellow LED #26	Switch port to FEX 13 Link green LED #27	Activity yellow LED #28	SMB_Alert Red LED #47
Switch port to FEX 14 Link green LED #29	Activity yellow LED #30	Hub FPGA Link green LED #31	Activity yellow LED #32	GP Blue LED #48
Switch B port 2 (to A) Link green LED #33	Activity yellow LED #34	Switch B port 3 (to C) Link green LED #35	Activity yellow LED #36	From ROD Run Blue LED #49
Switch A port 7 (to B) Link green LED #37	Activity yellow LED #38	Switch C port 7 (to B) Link green LED #39	Activity yellow LED #40	Driven by Hub FPGA TBD Green LED #50
Hub FPGA Phys Chip conx to this Hub's Switch Link green LED #41	Activity yellow LED #42	Hub FPGA Phys Chip conx to other Hub's Switch Link green LED #43	Activity yellow LED #44	TBD Yellow LED #51
				TBD Red LED #52
				Hub Module Isolated +12V present green LED #53
				Hub Module Power Good green LED #54
				RJ1 left/lower ROD Mezzanine Link green LED #57
				Activity yellow LED #58
				RJ1 right/upper IPMC, but no LED signal from PHY made available green LED #55
				Activity yellow LED #56
				RJ2 left/lower Switch A Port 6 Link green LED #61
				Activity yellow LED #62
				RJ2 right/upper Switch C Port 6 Link green LED #59
				Activity yellow LED #60
				RJ3 left/lower Switch B Port 6 Link green LED #65
				Activity yellow LED #66
				RJ3 right/upper Switch B Port 7 Link green LED #63
				Activity yellow LED #64
				ATCA Mandatory: Hot Swap (IPMC Socket pin #103) Blue LED #4

1001

1002

1003

Figure 15: Description of Hub front panel LED definitions.

1004 **6.9.1 Front Panel LEDs**

1005 A description of the LED definitions is given in **Figure 15**. Further details of the Hub
1006 LEDs are given in the technical specification Appendix, **Section 24**.

1007 **6.10 Rear Inputs and Outputs**

1008 **6.10.1 ATCA Zone 1**

1009 This interface is configured according to the ATCA standard. The connections include

- 1010 • dual, redundant -48V power supplies,
- 1011 • hardware address,
- 1012 • IPMB ports A and B (to the ATCA Shelf Manager),
- 1013 • shelf ground,
- 1014 • logic ground.

1015 See the ATCA specification for further details [1.7] .

1016 **6.10.2 ATCA Zone 2**

1017 All Zone 2 connections are described in detail in Section 5 and the technical appendices
1018 (Sections 15, 0 and 17). These include:

- 1019 • Eight Fabric Interface channels to each node slot:
 - 1020 ○ One copy of the 40.08 MHz LHC clock (Hub Tx),
 - 1021 ○ One copy of the combined TTC/Hub-ROD1_CTRL high-speed serial link
1022 (Hub Tx),
 - 1023 ○ Six lanes of high-speed FEX readout data serial links (Hub Rx)
- 1024 • Gigabit Ethernet links in the Base Interface to/from each node slot.

1025 **6.10.3 ATCA Zone 3**

1026 The ATCA Zone 3 houses four Molex MTP backplane connectors, which will connect
1027 directly to the L1Calo Rear Transition Module (RTM). Note that, here the FEX-Hub
1028 violates the standard ATCA form factor, in that the front board protrudes through Zone 3
1029 into the rear space of the ATCA shelf. All L1Calo ATCA modules conform to this
1030 modified standard [1.14] .

1031 **6.11 FEX-Hub PCB**

1032 **Figure 5** illustrates the layout of the main components on the FEX-Hub. **Figure 17**,
1033 **Figure 18** and **Figure 19** illustrate the Gigabit Ethernet switch implementation, the core
1034 TTC distribution and high-speed data distribution on the Hub module, respectively. The
1035 remainder of this section describes the PCB layout of the Hub module.

1036 The Hub printed circuit board is a standard size ATCA card with the RAL specified
 1037 “bump out” in the Zone 3 area to accommodate up to 4 MPT optical connectors for use
 1038 with a Rear Transition Module.

1039 There are 22 copper are in the Hub PCB, used in the following way:

1040

PCB Layer	Layer Type Function	Controlled Impedance
1	Signal Traces	100 Ohm Diff
2	Ground Plane Upper Type	
3	Signal Traces	100 Ohm Diff
4	Ground Plane Upper Type	
5	Signal Traces	100 Ohm Diff
6	Ground Plane Upper Type	
7	Signal Traces	100 Ohm Diff
8	Ground Plane Middle Type	
9	Power Fills and Signals	100 Ohm Diff
10	Ground Plane	Middle Type
11	Power Fills	
12	Power Fills	
13	Ground Plane	Middle Type
14	Power Fills and Signals	100 Ohm Diff
15	Ground Plane Middle Type	
16	Signal Traces	100 Ohm Diff
17	Ground Plane	Lower Type
18	Signal Traces	100 Ohm Diff
19	Ground Plane Lower Type	
20	Signal Traces	100 Ohm Diff
21	Ground Plane Lower Type	
22	Signal Traces	100 Ohm Diff

1041

1042 The stack-up of the Hub card is shown in **Figure 16**.

Layer	Calc Thickness	Primary Stack	Description	Dk / Df
Layer - 1	0.0127 0.0508		Taiyo 4000-BN 1/2oz Sig (Std Plt)	3.90 / 0.0330
Layer - 2	0.0965 0.0152	1080HRC	FR408HR	3.42 / 0.0098
Layer - 3	0.1270 0.0152	0.0050 (1-2116)	FR408HR 1/2oz Sig	3.77 / 0.0089
Layer - 4	0.1422 0.0152	1080 1080	FR408HR 1/2oz P/G	3.44 / 0.0098
Layer - 5	0.1270 0.0152	0.0050 (1-2116)	FR408HR 1/2oz Sig	3.77 / 0.0089
Layer - 6	0.1422 0.0152	1080 1080	FR408HR 1/2oz P/G	3.44 / 0.0098
Layer - 7	0.1270 0.0152	0.0050 (1-2116)	FR408HR 1/2oz Sig	3.77 / 0.0089
Layer - 8	0.1422 0.0152	1080 1080	FR408HR 1/2oz P/G	3.44 / 0.0098
Layer - 9	0.1270 0.0305	0.0050 (1-2116)	FR408HR 1oz Mix	3.77 / 0.0089
Layer - 10	0.1397 0.0152	1080 1080	FR408HR 1/2oz P/G	3.44 / 0.0098
Layer - 11	0.0762 0.0305	0.0030 (1-1080)	FR408HR 1oz Mix	3.48 / 0.0096
Layer - 12	0.0813 0.0305	106 106	FR408HR 1oz Mix	3.24 / 0.0106
Layer - 13	0.0762 0.0152	0.0030 (1-1080)	FR408HR 1/2oz P/G	3.48 / 0.0096
Layer - 14	0.1397 0.0305	1080 1080	FR408HR 1oz Mix	3.44 / 0.0098
Layer - 15	0.1270 0.0152	0.0050 (1-2116)	FR408HR 1/2oz P/G	3.77 / 0.0089
Layer - 16	0.1422 0.0152	1080 1080	FR408HR 1/2oz Sig	3.44 / 0.0098
Layer - 17	0.1270 0.0152	0.0050 (1-2116)	FR408HR 1/2oz P/G	3.77 / 0.0089
Layer - 18	0.1422 0.0152	1080 1080	FR408HR 1/2oz Sig	3.44 / 0.0098
Layer - 19	0.1270 0.0152	0.0050 (1-2116)	FR408HR 1/2oz P/G	3.77 / 0.0089
	0.1422	1080 1080	FR408HR	3.44 / 0.0098

Figure 16: Hub PCB stackup details.

1043
1044

1045

1046 The Hub PCB includes 10 ground planes that are needed to facilitate routing of the high-
 1047 speed differential signals. The 3 different ground plane patterns are needed to allow
 1048 relief of the ground plane layers that are immediately under the AC coupling capacitors
 1049 that are used in most of these high-speed differential signals. These 0201 size AC
 1050 coupling capacitors are needed on both sides of the PCB and relief of the ground planes
 1051 immediately under their pads minimizes the transmission line impedance bump caused by
 1052 these capacitors.

1053 In the layers with high speed differential traces the dielectric layers are kept thick enough
1054 so that the 100 Ohm traces do not become so narrow that their losses are too high. This
1055 results in card with an overall thickness of 3.0 mm. From the backside of the card, in a
1056 narrow strip along the top and bottom edges, the thickness of the card is milled down to
1057 2.4 mm so that it fits into standard ATCA card guides.

1058 The layout of the Hub PCB requires routing of 384 high-speed differential pairs. The
1059 main complication in this high speed routing is at the output of the 74 Channel FEX
1060 Readout Data MGT Fanout where all of the signals routing up to the ROD must cross
1061 over those routing to the Hub FPGA. This crossover is done without any layer changes
1062 by having all MGT differential pairs running to the ROD located in layers 14, 16, 18, 20
1063 and all MGT differential pairs routing to the Hub FPGA located in layers 3, 5, 7, 9.
1064 Layer transitions in the high speed signals are only used where these signals come to the
1065 surface to connect to a component such as the Hub FPGA or the AC coupling capacitors.

1066 These required high speed layer transitions are implemented with a 4 via component that
1067 provides 2 ground current return vias along with the differential via pair. The ground
1068 planes are relieved in an oval pattern around the differential via pair to maintain a
1069 constant transmission line impedance. All high speed trace pairs are length matched to
1070 0.5 mm using serpentes. All vias and Zone 2 backplane connector pin holes in the high
1071 speed traces have been back-drilled to remove the via stubs. 7 back-drill depths are used
1072 from the bottom side of the card and 4 back-drill depths are used from the top side.

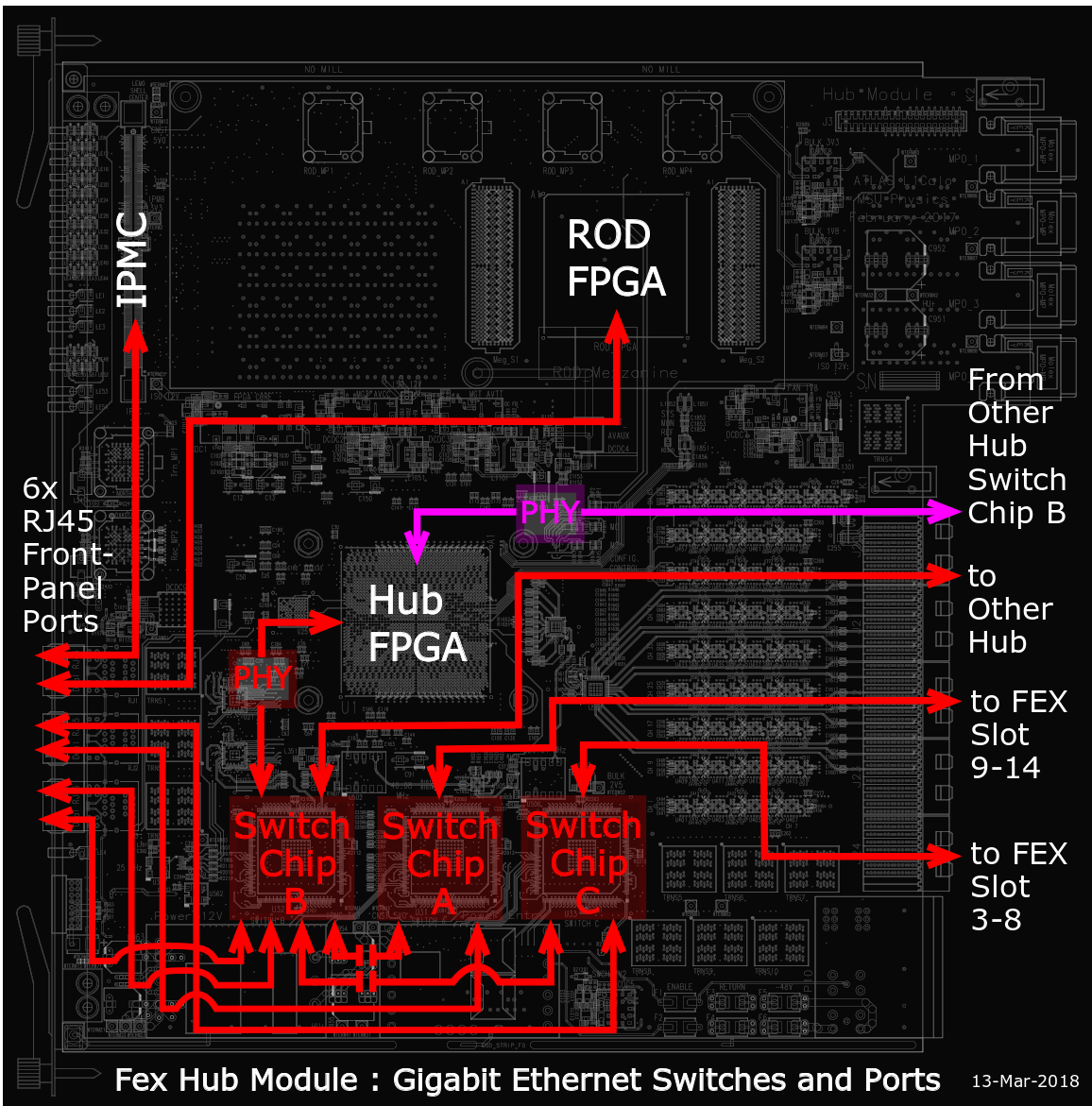
1073 The Hub PCB is built with Isola FR408HR laminate which is a low dielectric loss
1074 laminate that is appropriate for 10 Gb/sec digital routing. This is a high transition
1075 temperature laminate to facilitate assembly of the Hub Modules with a lead free process.

1076 The Hub design includes many components that use a center Exposed Pad that is soldered
1077 to a grounded thermal land for cooling. These thermal lands include an array of vias that
1078 connect them to the internal ground planes to help carry heat away from the associated
1079 component. To prevent wicking of solder into these vias (which would cause a poor
1080 solder connection to the associated component) hole plugs have been used in all thermal
1081 land via arrays on both the top and bottom sides of the Hub PCB.

1082 The Hub design uses 10 main power buses. There are not enough layers available to
1083 route each power bus on its own PCB layer. Instead 58 power area fills on 5 different
1084 layers are used to route the power buses on the Hub card.

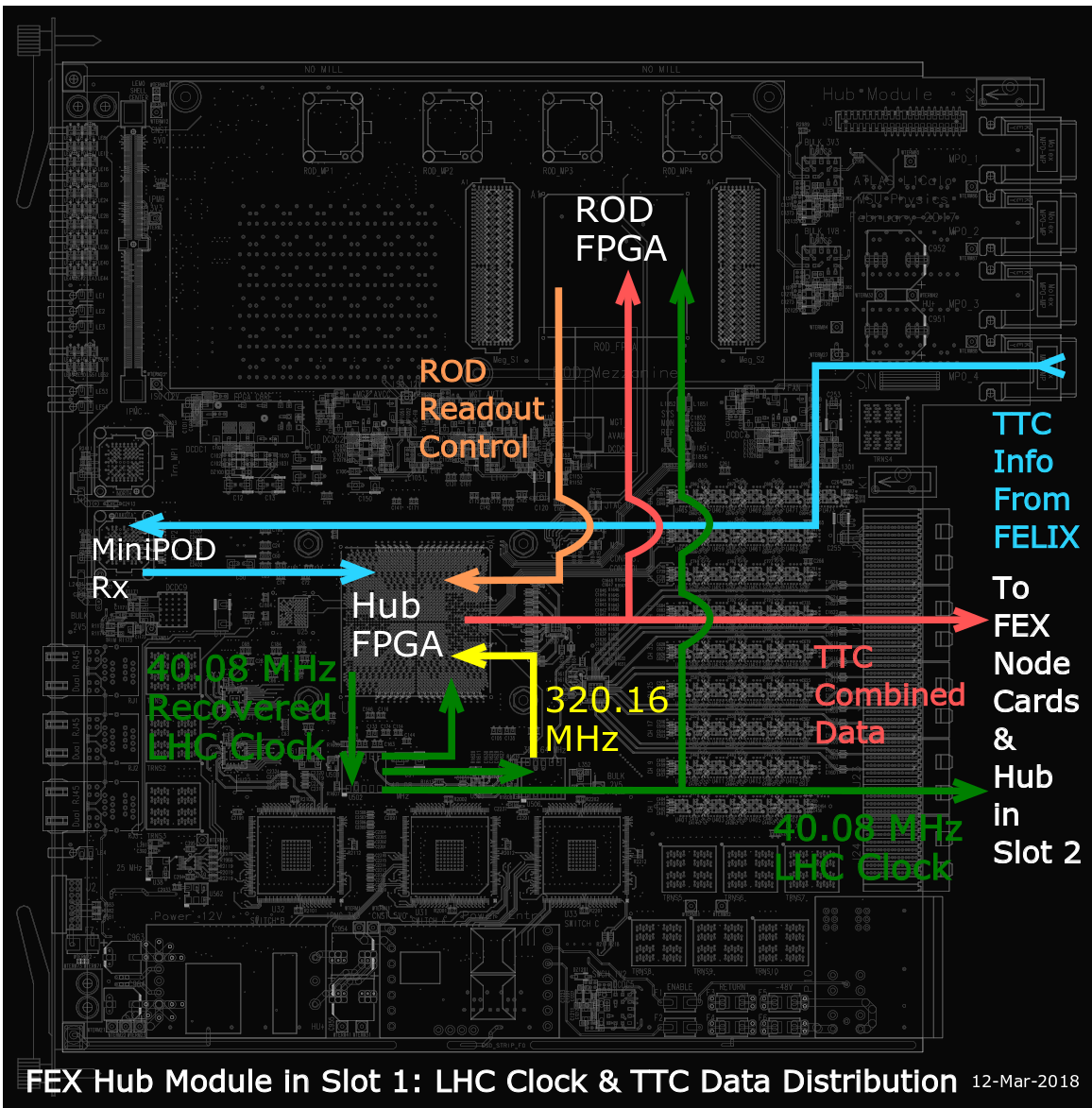
1085 The Hub PCB has 9162 drill through holes of 20 different hole types. All drills are
1086 through all layers. Blind vias are not used.

1087 The bare Hub PCB is manufactured with a gold surface finish to provide an optimum
1088 solder re-flow process during assembly.

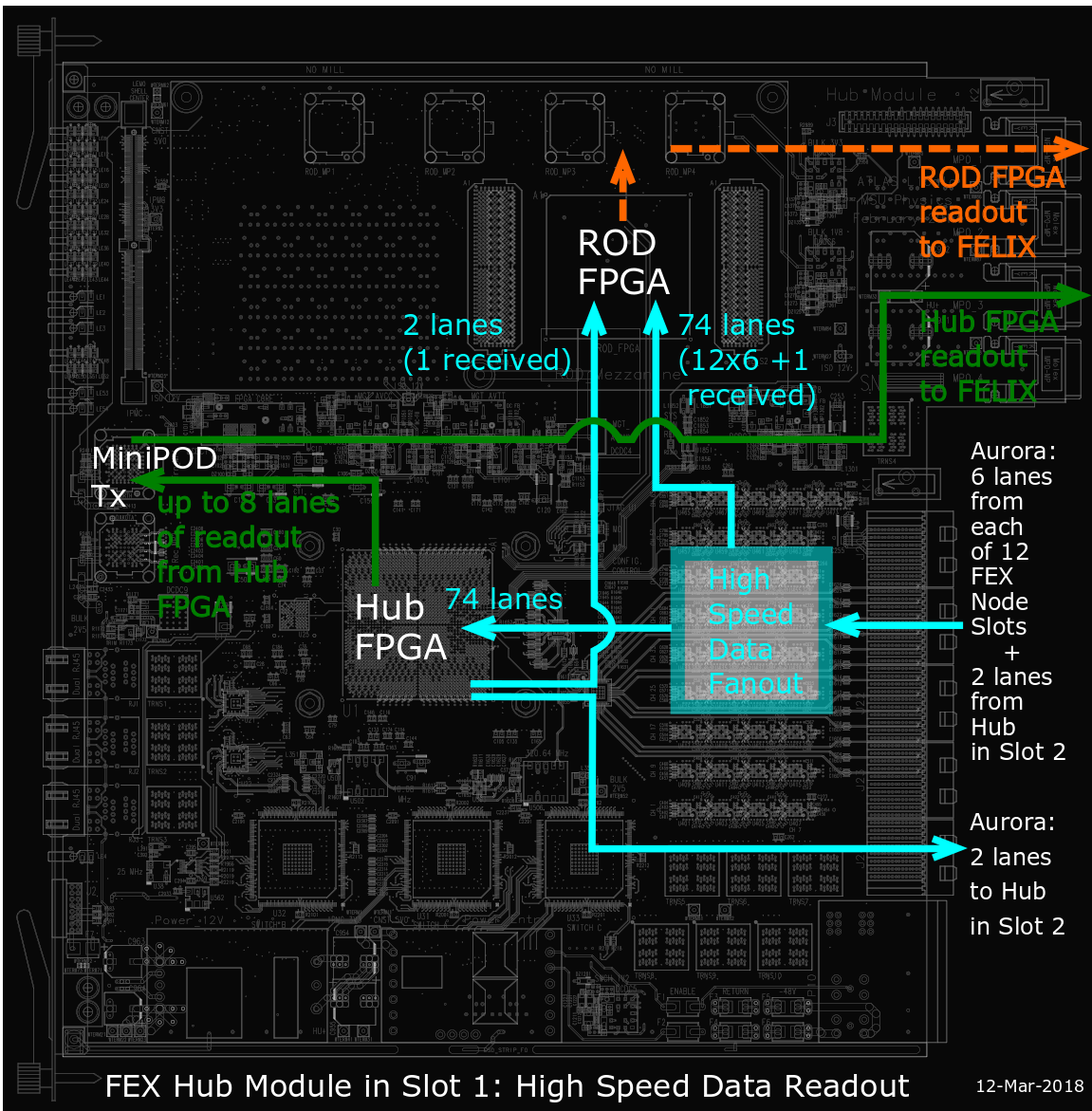


1089

1090 **Figure 17:** Board-level illustration of the Hub's Gigabit Ethernet switch connections.



1092 **Figure 18:** Board-level illustration of the Hub's LHC clock and TTC data distribution.



1093

1094

Figure 19: Board-level illustration of the high-speed data interfaces for the Hub.

1095

1096 **7 Programming Model**

1097 The Programming model is preliminary, and is expected to change significantly during
1098 detailed design.

1099 **7.1 Guidelines**

1100 The slow-control interface of the FEX-Hub obeys the following rules.

- 1101 • The system controller can read all registers; there are no ‘write only’ registers.
- 1102 • Three types of register are defined: Status Registers, Control Registers and Pulse
1103 Registers.
- 1104 • All Status Registers are read-only registers. Their contents can be modified only
1105 by the Hub hardware.
- 1106 • All Control Registers are read/write registers. Their contents can be modified only
1107 by system controller. Reading a Control Register returns the last value written to
1108 that register.
- 1109 • All Pulse Registers are read/write registers. Writing to them generates a pulse for
1110 those bits asserted. Reading them returns all bits as zero.
- 1111 • Attempts to write to read-only registers, or undefined portions of registers, result
1112 in the non-modifiable fields being left unchanged.
- 1113 • If the computer reads a register (e.g. a counter) which the Hub is modifying, a
1114 well-defined value is returned.
- 1115 • The power-up condition of all registers bits is zero, unless otherwise stated.

1116 **7.2 Register Map & Controllable Functions**

1117 The register map and the controllable functions are described in the Hub firmware
1118 specification [1.16] .

1119 **8 Testing and Commissioning**

1120 The testing and commissioning of the FEX-Hub module will be performed in two modes:
1121 (1) standalone as a single module in an ATCA shelf, (2) together with FEX (or test
1122 module) and ROD modules to test core FEX system functionality. Both of these testing
1123 phases can be performed with either one or two Hubs per shelf.

1124 There insufficient test modules capable of sourcing data in the ATCA backplane
1125 available in the L1Calo prototype phase to fully populate all 12 node slots, thus the
1126 current FEX-Hub design has not been tested with a full shelf of source nodes. Thus, a
1127 bandwidth test following the Final Design review will be performed prior to the
1128 Production Readiness Review.

1129 A detailed list of commissioning tests for the production FEX-Hub module is presented
1130 in **Appendix Section 32**. While this list may grow to cover more in-depth testing of Hub
1131 interfaces, it is already covering all Hub functionality.

1132 **8.1 Standalone and FEX System Tests**

1133 Standalone Hub tests will be performed to verify power distribution, FPGA configuration
1134 and basic functionality of the GbE network. To facilitate the requirement of Hub-to-Hub
1135 testing, the Hub module:

- 1136 • allows testing and validation of the DCS and control networks via direct
1137 connections to a second Hub module;
- 1138 • allows testing and validation of the DCS and control networks via front-panel
1139 connections to external computers, allowing thorough scanning of all IPbus
1140 targets;
- 1141 • allows the sending and receiving of high-speed signals from one Hub to another,
1142 providing a path to study Fabric Interface bandwidth limitations;
- 1143 • allows testing and validation of the fanout of clock and TTC control data
1144 information over the Fabric Interface.

1145 To facilitate the requirement of FEX-Hub-ROD testing, the Hub module:

- 1146 • provides Fabric Interface connections to the ROD with no Hub configuration
1147 required;
- 1148 • provides network switching functions with no Hub configuration required;
- 1149 • provides a clock to all node slots with no Hub configuration required;
- 1150 • functions as a single module without a second Hub module in the ATCA shelf;
- 1151 • sees a copy of the same data delivered to the ROD module.

1152 **8.2 Full Bandwidth Tests**

1153 To facilitate testing of the FEX-HUB and ROD with a full shelf of data sources,
1154 Michigan State University has designed a Hub Test Module (HTM) for this purpose. The
1155 HTM is an ATCA carrier card hosting a commercial mezzanine with a Kinex-7 FPGA.

1156 Thus, the HTM is capable of emulating FEX modules by

- 1157 • sourcing 6 lanes of multi-gigabit serial transmission lines to both Hub slots;
- 1158 • receiving the Hub-sourced clock;
- 1159 • receiving the combined TTC info signal from the Hub;
- 1160 • connecting to both GbE networks provided via Hub slots 1 and 2.

1161 Using a full shelf of HTM cards, the bandwidth conditions of a full FEX shelf will be
1162 tested. These tests will include a simultaneous test of:

- 1163 • 6 lanes of data traffic to both Hub slots from all 12 node slots, with a goal of
1164 testing up to the maximum anticipated L1Calo bandwidth of 9.6 Gbps;
- 1165 • distribution of the Hub clock to all 12 node slots;
- 1166 • distribution of the Hub TTC combined info to all 12 node slots;
- 1167 • full-bandwidth GbE traffic on both Hub Ethernet networks;
- 1168 • full-bandwidth ROD-Hub links, including the backplane links between Hub slots;

1169

1170 While all of these tests can be performed individually with a single test module, this test
1171 will emulate the expected rigors of L1Calo operations over Run 3 and Run 4.

1172 **9 FEX-Hub Prototype Tests**

1173 **9.1 Overview**

1174 Eight FEX-Hub prototype modules were manufactured in 2017. All of these modules
1175 have been tested, though some tests were only performed on a subset of Hub cards. Two
1176 of the prototype cards have been shipped to Cambridge, and are now part of the ROD test
1177 module bench. This section describes the test results for these prototype modules. While
1178 this section summarizes the salient details of the Hub tests, a full description of the Hub
1179 commissioning tests can be found in Section 32, which forms the production Hub
1180 commissioning plan as well.

1181 **9.2 Power and Cooling Tests**

1182 To perform power and cooling tests, all Hub MGTs were activated and running in the
1183 anticipated normal Hub configuration (Tx and Rx together). The FPGA fabric is
1184 primarily allocated to IBERT logic, but this is estimated to be a relatively small fraction
1185 of the FPGA fabric capacity.

1186 **9.2.1 Power Consumption**

1187 The two primary power draws on the Hub are the Hub FPGA, which consumes 33.4W in
1188 the configuration anticipated for L1Calo operations. The high-speed data fanout chips
1189 consume 21.8W in total. The MiniPODs, switch chips and IPMC all together consume
1190 less than 10W. The total power consumption for the Hub is found to be 67W in normal
1191 L1Calo operating conditions, which increases to 72W when operating all unconnected
1192 MGTs. The Hub supply capacity is 300W, of which 100W is reserved for the ROD.

1193 **9.2.2 MGT Rail Power Supply Capacity**

1194 The capacity of the Hub MGT rail power supplies were a significant concern for the
1195 prototype design, as a safety margin of 40% in DCDC supply capacity was desired for the
1196 all MGT rail supplies. This concern was driven by an apparent discrepancy between the
1197 predictions by the Xilinx Power Estimator (XPE) and measurements on Xilinx
1198 development boards, also observed by other ATLAS Xilinx users.

1199 The current draw measurements are given in the following table. The smallest margin
1200 observed is for MGT_AVTT at 36.5%, which is a satisfactory safety margin as the design
1201 is already using all MGTs supplied by that converter.

1202

1203

Converter	FPGA_ CORE	MGT_ AVCC	MGT_ AVTT	SWCH 1V2	BULK 1V8	FAN_ 1V8	BULK_ 3V3
Voltage	0.95 V	1.00 V	1.20 V	1.20 V	1.80 V	1.80 V	3.3 V
Draw	8.04 A	9.38 A	12.7 A	1.94 A	0.62 A	12.1 A	2.25 A
Capacity	40 A	20 A	20 A	12 A	12 A	20 A	12 A

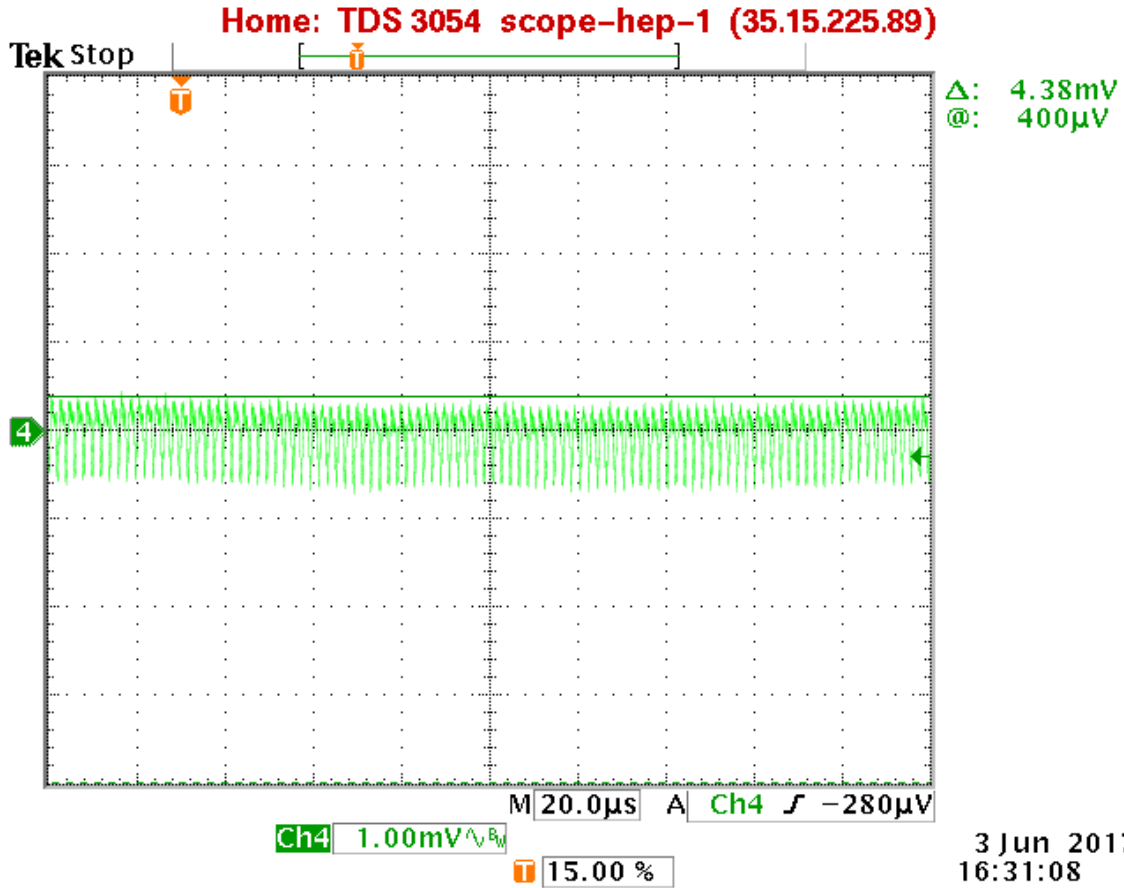
1204

1205 In this configuration the FPGA is consuming 33.4W. It should be noted that we do not
 1206 have direct access to the 1V8 MGT_AVAUX and 1V3 BULK_2V5 buses, but these are
 1207 included in the BULK_3V3 current.

1208 **9.2.3 MGT Rail Supply Noise**

1209 The Xilinx FPGAs and ON-Semi fanout chips specify a noise tolerance for the MGT rail
 1210 supplies, typically smaller than 10 mV pk-pk. Both GE (Lineage Power) D-Lynx series
 1211 and TI (Power Trends) PTH08Txyz series converters were evaluated for use on the Hub
 1212 Module, which both advertise noise characteristics compatible with the Hub
 1213 requirements. The D-Lynx converters were selected, primarily for the PMbus
 1214 connections offered on their control chips.

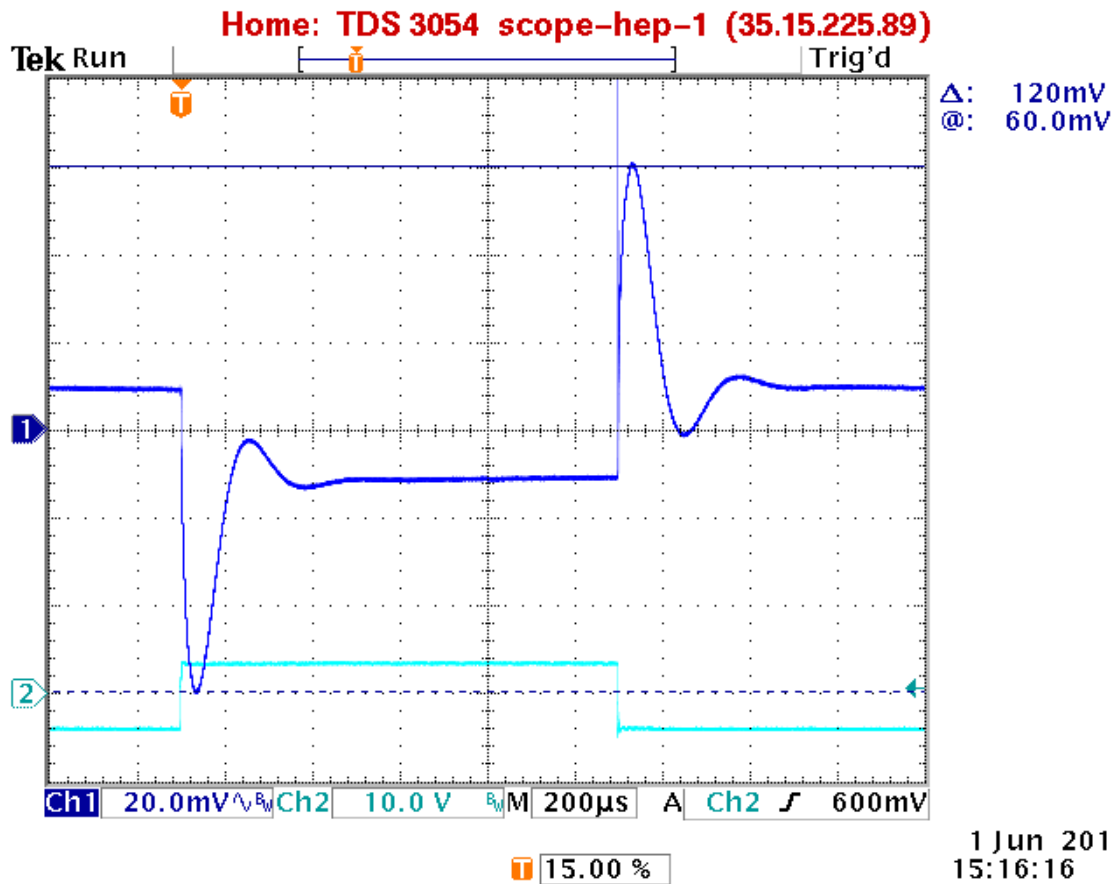
1215 All supplies on the Hub prototype have been tested and fall well within the noise
 1216 tolerance required. An example measurement is shown in **Figure 20** for the fanout 1.8V
 1217 supply, obtained with all DCDC supplies running.



1218

1219 **Figure 20:** Noise measurement for the 1.8V fanout DCDC power supply.

1220 Tests of the Hub DCDC supply stability have also been performed, and their performance
 1221 has been found to be satisfactory. An example is given in **Figure 21** wherein the
 1222 MGT_AVTT 1.2V supply load is pulsed from 7.2A to 12A at 500 Hz.



1223

1224 **Figure 21:** Stability test of the MGT_AVTT DCDC supply, obtained while pulsing the
 1225 supply load from 7.2A to 12A at a 500 Hz rate.

1226

1227 9.2.4 *FPGA Silicon Temp*

1228 The Hub FPGA silicon temperature has been measured using a full load, as described
 1229 above, and with normal shelf cooling fan speeds. Measurements of FPGA silicon
 1230 temperature across the Hub prototypes are typically 45C with small variance. It should
 1231 be noted that the usage of the FPGA fabric is minimal in this test, but it is not anticipated
 1232 that the Hub FPGA usage will be significant. In tests that activate all unused Hub FPGA
 1233 MGTs, the power draw increases by 5W to 38W and the silicon temperature increases by
 1234 1C to 46C.

1235 9.3 **Clock Tests**

1236 9.3.1 *Clock Generation and Distribution*

1237 The Hub module produces a 40.0787 MHz LHC reference clock with jitter characteristic
 1238 that is OC-192 compliant (optical carrier standard for 10 Gbps transmission).

1239 All clock distribution links have been verified at the recipient endpoint: this Hub's ROD,
1240 other Hub and all node slots using the FEX Test Module.

1241 **9.3.2 Hub PLL Relock**

1242 During testing of the Hub Modules these PLLs are checked to verify their "re-lock"
1243 frequency range, i.e. the reference frequency is initially set outside the PLL's operating
1244 range and then slowly brought within the operating range and the frequency where re-
1245 lock occurs is recorded. The re-lock test is done with the initial reference frequency set
1246 both below and above the operating range. The re-lock range of the 40.0787 MHz PLLs
1247 is typically a little over 2x the +/- 40 ppm minimum specified by their manufacturer. Note
1248 that this test also verifies that the Hub Modules will automatically re-lock to the LHC
1249 Reference Clock as soon as it becomes available again after an interruption. A signal
1250 indicating the state of the 40.0787 MHz PLL (i.e. locked or not locked) is sent to the
1251 Hub's FPGA where it can be made visible in an IPBus register.

1252

1253 When the LHC Reference Clock frequency is slewing the phase of the output of the
1254 Hub's 40.0787 MHz PLL will shift from its normal position with respect to its reference
1255 input. When the LHC is slewing up in frequency the output phase of the PLL will fall
1256 behind its normal position. At the maximum LHC slew rate of 220 Hz/sec there is a
1257 phase shift of about 3.2 degrees in the output of the PLL. Such a shift in phase is not
1258 something special to the PLLs used on the Hub Module rather it is an inherent
1259 characteristic of the PLL architecture. Increasing the "loop bandwidth" of the PLL will
1260 reduce this phase shift and reduce the ability of the PLL to reject the jitter in its input
1261 reference clock.

1262 **9.4 High-Speed Link Tests**

1263 Tests of the electrical connectivity and stability of the Hub high-speed links have been
1264 performed. This includes:

- 1265 • 4x MiniPOD receiver MGT links to the Hub FPGA (9.6 Gbps);
- 1266 • 8x MiniPOD transmitter MGT links from the Hub FPGA (9.6 Gbps);
- 1267 • 72x MGT links from the FEX data fanout to the Hub and ROD FPGAs (6.4 Gbps
1268 and 10.26 Gbps);
- 1269 • 2x (1x) MGT links from the other Hub slot to the Hub (ROD) FPGA (9.6 Gbps);
- 1270 • 2x (1x) MGT links from this Hub to the other Hub (ROD) FPGA (9.6 Gbps);
- 1271 • 14x MGT links from the Hub FPGA to the FEX slots (12x), the ROD on this Hub
1272 (1x) and the other Hub (1x) (6.4 Gbps);
- 1273 • 1x MGT link for ROD/Combined data from the other Hub (9.6 Gbps);
- 1274 • 1x MGT link from the ROD on this Hub (9.6 Gbps);

1275

1276 All high-speed links were tested using the Xilinx IBERT test firmware using SRBS7 test
1277 patterns. The data source was a FEX Test Module (FTM). All tests were performed at
1278 the line rates expected to be used for L1Calo operations. However due to limitations of
1279 the FTM, some tests were not able to be performed at 9.6 Gbps and in such instances a
1280 line rate of 10.26 Gbps was used. And due to the availability of only one FTM, only a
1281 subset of links corresponding to a single node slot could be tested simultaneously.

1282

1283 The duration of the tests was limited by the number of Hub modules required to be tested
1284 and the availability of the FTM. Thus, all links were tested to at least a bit error rate
1285 (BER) of less than $1E-12$ and a subset was tested to $1E-16$. In all tests of all Hub
1286 prototype cards, zero errors were observed.

1287

1288 As noted in the test plan, these tests are planned to be repeated using Hub Test Modules
1289 (HTMs) in a configuration that allows all links to be tested simultaneously.

1290 **9.5 Gigabit Ethernet Tests**

1291 This is a summary of the FEX-Hub Gigabit Ethernet tests, described in more detail in
1292 [1.15]. The FEX-Hub has three interconnected 8-port Broadcom GbE switch chips
1293 (denoted A, B, C here). Switch chip B has ports connected to both the other chips, A and
1294 C. The scope of the tests performed was to evaluate that all 22 GbE switch ports
1295 maintain reliable GbE links and that the bandwidth characteristics of the FEX-Hub GbE
1296 network are desirable.

1297 Regarding the first test aspect, verifying connectivity of the FEX-Hub GbE switch ports,
1298 all 8 of the Hub prototypes and one Hub prototype without a Ultrascale FPGA mounted
1299 were fully qualified in this test. No links were found to have connection or transmission
1300 issues.

1301 Regarding the second test aspect, it was found that using the FEX Hub Module
1302 connections between a single client and a single server maintain a bandwidth of 935
1303 Mbps, which is the same as that of the commercial switch. It is further found that when
1304 sending data from multiple clients to a single server, an overall bandwidth of 940 Mbps
1305 per switch is maintained. When using a single source of data into chip A and sinking via
1306 chips B or C, we further find bandwidth reliability. When multiple sources are sent into a
1307 multiple chips and sinked via a single chip, we observe that the bandwidth is split
1308 between sources, reflecting the maximum bandwidth for the single source chip. For
1309 example, when sourcing from chips A and C via a sink on chip B, we find a maximum
1310 bandwidth of 470 Mbps for chips A and B. This pattern continues as more sources are
1311 added. This behaviour is as expected for the design, and reflects what one would expect
1312 from a commercial GbE switch.

1313 **9.6 IPMC, Slow Control and Monitoring Tests**

1314 A LAPP IPMC has been used on the FEX-Hub prototypes. The basic functions such as
1315 power negotiation; Ethernet connection, LED management and hot swap have been tested
1316 successfully. For the final FEX-Hub, the LAPP IPMC may be replaced by the pin-
1317 compatible CERN IPMC.

1318 **9.7 Miscellaneous tests**

1319 All physical aspects of the Hub card have been verified: dimensions, insertion/extraction
1320 forces, ground points, control signals, I2C bus and feasibility of heat sinks. Furthermore,
1321 all front-panel features are verified: LEDs, JTAG, RJ45 jacks, and LEMO. The
1322 communication and control of all components on the card has been verified.

1323 **9.8 Conclusions**

1324 The FEX-Hub prototype modules have been systematically tested, yielding successful
1325 outcomes for all tests. Based on the results of these tests, there is no indication for
1326 changes to the Hub PCB or implementation of core functions. No tests thus far suggest
1327 that current Hub design will not satisfy the L1Calo operational requirements.

1328 **10 Planned Hub Module Production Yields**

1329 The construction of FEX-Hub modules will occur in two phases, prototype and
1330 production. The Hub modules were fabricated spring 2017. A total of eight prototype
1331 modules were produced, with delivery as follows:

- 1332 • Two prototype modules for function testing at MSU;
- 1333 • Two prototype modules for an integration test rig at CERN;
- 1334 • One prototype module each for Rutherford and Cambridge, for eFEX and ROD
1335 testing;
- 1336 • One prototype module for Argonne National Lab, for FELIX integration tests.
- 1337 • One spare prototype Hub module.

1338 A total of nineteen production Hub modules will be produced by April 2019, with
1339 delivery anticipated as:

- 1340 • Eight production modules to support the L1Calo system eFEX, jFEX and L1Topo
1341 shelves at CERN (note, there are two eFEX shelves and two Hubs per shelf);
- 1342 • Three spare production modules at CERN, dedicated for the L1Calo system;
- 1343 • Two production modules for function testing at MSU;
- 1344 • Two production modules the CERN test facility;
- 1345 • Two production modules for Rutherford and Cambridge (one per institute), for
1346 eFEX and ROD testing;
- 1347 • Two spare production module to be used as needed.

1348 **11 Special Notes**

- 1349 • The FEX-Hub module is not providing Fabric or Base Interface connections to the 2
1350 slots that do not exist in 14-slot shelves, i.e. shelves with 2 Hub slots and only 12
1351 Node slots.
- 1352 • As shown the FEX-Hub's Base Interface switch provides a connection to only one
1353 Shelf Manager.

12 Glossary

ATCA	Advanced Telecommunications Computing Architecture (industry standard).
BC	Bunch Crossing: the period of bunch crossings in the LHC and of the clock provided to ATLAS by the TTC, 24.95 ns.
BCMUX	Bunch-crossing multiplexing: used at the input to the CPM, JEM (from Phase I) and eFEX, this is a method of time-multiplexing calorimeter data, doubling the number of trigger towers per serial link.
CMX	Common Merger Extended Module.
CP	Cluster Processor: the L1Calo subsystem comprising the CPMs.
CPM	Cluster Processor Module.
CTP	Central Trigger Processor
DAQ	Data Acquisition
DCS	Detector Control System: the ATLAS system that monitors and controls physical parameters of the sub-systems of the experiment, such as gas pressure, flow-rate, high voltage settings, low-voltage power supplies, temperatures, leakage currents, etc.
ECAL	The electromagnetic calorimeters of ATLAS, considered as a single system.
ECR	Event Counter Reset signal from the TTC, used to initiate clearing of ROD memories
eFEX	Electron Feature Extractor.
FEX	Feature Extractor, referring to either an eFEX or jFEX module or subsystem.
FIFO	A first-in, first-out memory buffer.
FPGA	Field-Programmable Gate Array.
HTM	Hub Test Module
HCAL	The hadronic calorimeters of ATLAS, considered as a single system.
IPbus	An IP-based protocol implementing register-level access over Ethernet for module control and monitoring.
IPMB	Intelligent Platform Management Bus: a standard protocol used in ATCA shelves to implement the lowest-level hardware management bus.
IPM Controller	Intelligent Platform Management Controller: in ATCA systems, that portion of a module (or other intelligent component of the system) that interfaces to the IPMB.
IPMI	Intelligent Platform Management Interface: a specification and mechanism for providing inventory management, monitoring, logging,

and control for elements of a computer system. A component of, but not exclusive to, the ATCA standard.

JEM	Jet-Energy Module.
JEP	Jet-Energy Processor: the L1Calo subsystem comprising the JEMs.
jFEX	Jet Feature Extractor.
JTAG	A technique, defined by IEEE 1149.1, for transferring data to/from a device using a serial line that connects all relevant registers sequentially. JTAG stands for Joint Technology Assessment Group.
L0A	In Run 4, the Level-0 trigger accept signal.
L0Calo	In Run 4, the ATLAS Level-0 Calorimeter Trigger.
L1A	The Level-1 trigger accept signal.
L1Calo	The ATLAS Level-1 Calorimeter Trigger.
LHC	Large Hadron Collider.
MGT	As defined by Xilinx, this acronym stands for Multi-Gigabit Transceiver. However, it should be noted that it denotes a multi-gigabit transmitter–receiver pair.
MiniPOD	An embedded, 12-channel optical transmitter or receiver.
MPO	Multi-fibre Push-On/Pull-Off: a connector for mating two optical fibres.
PMA	Physical Media Attachment: a sub-layer of the physical layer of a network protocol.
ROD	Readout Driver.
RoI	Region of Interest: a geographical region of the experiment, limited in η and ϕ , identified by the Level-1 trigger (during Run 3) as containing candidates for Level-2 trigger objects requiring further information. In Run 4, RoIs are used in the same between the Level-0 and Level-1 triggers.
Shelf	A crate of ATCA modules.
SMA	Sub-Miniature version A: a small, coaxial RF connector.
Supercell	LAr calorimeter region formed by combining E_T from a number of cells adjacent in η and ϕ .
SLR	Super Logic Region. A single silicon die in a Xilinx Ultrascale FPGA,
TOB	connected by a silicon interposer. Trigger Object. A Compact data structure describing a trigger feature detected by a FEX module.
TTC	The LHC Timing, Trigger and Control system.
XTOB	Extended Trigger Object. A data packet passed to the readout path, contained more information about a TOB than can be accommodated on

the real-time path.

1355

1356 **13 Document Revision History**

Version	Date	Comments
0.01	16-09-14	Preliminary Draft
0.02	19-09-14	Language & grammar edits.
0.03	1-10-14	Final version for Preliminary Design Review
1.1	13-03-18	Updated version for Final Design Review

1357

1358

1359 **14 Appendix 1: Backplane Connector/Pin Tables**

1360 This Appendix enumerates the connector and pin connections intended for the Hub-FEX
 1361 and Hub-Hub backplane links in the Fabric Interface, Base Interface and Update
 1362 Interface.

1363 In the convention presented here, the FEX numbering below presumes that the module
 1364 called "FEX 01" is located in Logical Slot 3, FEX 02 in Slot 4,... and FEX 12 in Slot 14.

1365 **14.1 Connector and Signal Usage for a HUB Slot**

Rev: 23-Oct-2015 same as table from PDR after updating from FEX 01..12 to official numbering FEX 03..14
 Rev: 12-Mar-2018 use name "TTC Combined Data". For FEX slot: Keep only J23. Add LHC Clock & CombData from Hub 2

Connector Usage for a HUB Slot										
Connect Number	Row Num	Channel	a	b	c	Connector d	Pin Pairs e	f	g	h
J20/P20	01	Clocks	CLK1A+ Unused	CLK1A- signal pair	CLK1B+ Unused	CLK1B- signal pair	CLK2A+ Unused	CLK2A- signal pair	CLK2B+ Unused	CLK2B- signal pair
J20/P20	02	Upd Chan & Clocks	Tx4(UP)+ Unused	Tx4(UP)- signal pair	Rx4(UP)+ Unused	Rx4(UP)- signal pair	CLK3A+ Unused	CLK3A- signal pair	CLK3B+ Unused	CLK3B- signal pair
J20/P20	03	Update Channel	Tx2(UP)+ GE Pair C HUB FPGA	Tx2(UP)- HUB FPGA	Rx2(UP)+ GE Pair C HUB Switch	Rx2(UP)- HUB Switch	Tx3(UP)+ GE Pair D HUB FPGA	Tx3(UP)- HUB FPGA	Rx3(UP)+ GE Pair D HUB Switch	Rx3(UP)- HUB Switch
J20/P20	04	Update Channel	Tx0(UP)+ GE Pair A HUB FPGA	Tx0(UP)- HUB FPGA	Rx0(UP)+ GE Pair A HUB Switch	Rx0(UP)- HUB Switch	Tx1(UP)+ GE Pair B HUB FPGA	Tx1(UP)- HUB FPGA	Rx1(UP)+ GE Pair B HUB Switch	Rx1(UP)- HUB Switch
J20/P20	05	Fabric Channel 15	Tx2[15]+ Unused	Tx2[15]- signal pair	Rx2[15]+ Unused	Rx2[15]- signal pair	Tx3[15]+ Unused	Tx3[15]- signal pair	Rx3[15]+ Unused	Rx3[15]- signal pair
J20/P20	06		Tx0[15]+ Unused	Tx0[15]- signal pair	Rx0[15]+ Unused	Rx0[15]- signal pair	Tx1[15]+ Unused	Tx1[15]- signal pair	Rx1[15]+ Unused	Rx1[15]- signal pair
J20/P20	07	Fabric Channel 14	Tx2[14]+ Unused	Tx2[14]- signal pair	Rx2[14]+ Unused	Rx2[14]- signal pair	Tx3[14]+ Unused	Tx3[14]- signal pair	Rx3[14]+ Unused	Rx3[14]- signal pair
J20/P20	08		Tx0[14]+ Unused	Tx0[14]- signal pair	Rx0[14]+ Unused	Rx0[14]- signal pair	Tx1[14]+ Unused	Tx1[14]- signal pair	Rx1[14]+ Unused	Rx1[14]- signal pair
J20/P20	09	Fabric Channel 13	Tx2[13]+ RO Str 5 from FEX 14	Tx2[13]- FEX 14	Rx2[13]+ RO Str 3 from FEX 14	Rx2[13]- FEX 14	Tx3[13]+ RO Str 6 from FEX 14	Tx3[13]- FEX 14	Rx3[13]+ RO Str 4 from FEX 14	Rx3[13]- FEX 14
J20/P20	10		Tx0[13]+ LHC Clk to FEX 14	Tx0[13]- FEX 14	Rx0[13]+ RO Str 1 from FEX 14	Rx0[13]- FEX 14	Tx1[13]+ TTCCombData to FEX 14	Tx1[13]- FEX 14	Rx1[13]+ RO Str 2 from FEX 14	Rx1[13]- FEX 14
J21/P21	01	Fabric Channel 12	Tx2[12]+ RO Str 5 from FEX 13	Tx2[12]- FEX 13	Rx2[12]+ RO Str 3 from FEX 13	Rx2[12]- FEX 13	Tx3[12]+ RO Str 6 from FEX 13	Tx3[12]- FEX 13	Rx3[12]+ RO Str 4 from FEX 13	Rx3[12]- FEX 13
J21/P21	02		Tx0[12]+ LHC Clk to FEX 13	Tx0[12]- FEX 13	Rx0[12]+ RO Str 1 from FEX 13	Rx0[12]- FEX 13	Tx1[12]+ TTCCombData to FEX 13	Tx1[12]- FEX 13	Rx1[12]+ RO Str 2 from FEX 13	Rx1[12]- FEX 13
J21/P21	03	Fabric Channel 11	Tx2[11]+ RO Str 5 from FEX 12	Tx2[11]- FEX 12	Rx2[11]+ RO Str 3 from FEX 12	Rx2[11]- FEX 12	Tx3[11]+ RO Str 6 from FEX 12	Tx3[11]- FEX 12	Rx3[11]+ RO Str 4 from FEX 12	Rx3[11]- FEX 12
J21/P21	04		Tx0[11]+ LHC Clk to FEX 12	Tx0[11]- FEX 12	Rx0[11]+ RO Str 1 from FEX 12	Rx0[11]- FEX 12	Tx1[11]+ TTCCombData to FEX 12	Tx1[11]- FEX 12	Rx1[11]+ RO Str 2 from FEX 12	Rx1[11]- FEX 12

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J21/P21	05	Fabric Channel 10	Tx2[10]+ Tx2[10]- RO Str 5 from FEX 11	Rx2[10]+ Rx2[10]- RO Str 3 from FEX 11	Tx3[10]+ Tx3[10]- RO Str 6 from FEX 11	Rx3[10]+ Rx3[10]- RO Str 4 from FEX 11
	06		Tx0[10]+ Tx0[10]- LHC Clk to FEX 11	Rx0[10]+ Rx0[10]- RO Str 1 from FEX 11	Tx1[10]+ Tx1[10]- TTCCombData to FEX 11	Rx1[10]+ Rx1[10]- RO Str 2 from FEX 11
J21/P21	07	Fabric Channel 09	Tx2[09]+ Tx2[09]- RO Str 5 from FEX 10	Rx2[09]+ Rx2[09]- RO Str 3 from FEX 10	Tx3[09]+ Tx3[09]- RO Str 6 from FEX 10	Rx3[09]+ Rx3[09]- RO Str 4 from FEX 10
	08		Tx0[09]+ Tx0[09]- LHC Clk to FEX 10	Rx0[09]+ Rx0[09]- RO Str 1 from FEX 10	Tx1[09]+ Tx1[09]- TTCCombData to FEX 10	Rx1[09]+ Rx1[09]- RO Str 2 from FEX 10
J21/P21	09	Fabric Channel 08	Tx2[08]+ Tx2[08]- RO Str 5 from FEX 09	Rx2[08]+ Rx2[08]- RO Str 3 from FEX 09	Tx3[08]+ Tx3[08]- RO Str 6 from FEX 09	Rx3[08]+ Rx3[08]- RO Str 4 from FEX 09
	10		Tx0[08]+ Tx0[08]- LHC Clk to FEX 09	Rx0[08]+ Rx0[08]- RO Str 1 from FEX 09	Tx1[08]+ Tx1[08]- TTCCombData to FEX 09	Rx1[08]+ Rx1[08]- RO Str 2 from FEX 09
P22/J22	01	Fabric Channel 07	Tx2[07]+ Tx2[07]- RO Str 5 from FEX 08	Rx2[07]+ Rx2[07]- RO Str 3 from FEX 08	Tx3[07]+ Tx3[07]- RO Str 6 from FEX 08	Rx3[07]+ Rx3[07]- RO Str 4 from FEX 08
	02		Tx0[07]+ Tx0[07]- LHC Clk to FEX 08	Rx0[07]+ Rx0[07]- RO Str 1 from FEX 08	Tx1[07]+ Tx1[07]- TTCCombData to FEX 08	Rx1[07]+ Rx1[07]- RO Str 2 from FEX 08
P22/J22	03	Fabric Channel 06	Tx2[06]+ Tx2[06]- RO Str 5 from FEX 07	Rx2[06]+ Rx2[06]- RO Str 3 from FEX 07	Tx3[06]+ Tx3[06]- RO Str 6 from FEX 07	Rx3[06]+ Rx3[06]- RO Str 4 from FEX 07
	04		Tx0[06]+ Tx0[06]- LHC Clk to FEX 07	Rx0[06]+ Rx0[06]- RO Str 1 from FEX 07	Tx1[06]+ Tx1[06]- TTCCombData to FEX 07	Rx1[06]+ Rx1[06]- RO Str 2 from FEX 07
P22/J22	05	Fabric Channel 05	Tx2[05]+ Tx2[05]- RO Str 5 from FEX 06	Rx2[05]+ Rx2[05]- RO Str 3 from FEX 06	Tx3[05]+ Tx3[05]- RO Str 6 from FEX 06	Rx3[05]+ Rx3[05]- RO Str 4 from FEX 06
	06		Tx0[05]+ Tx0[05]- LHC Clk to FEX 06	Rx0[05]+ Rx0[05]- RO Str 1 from FEX 06	Tx1[05]+ Tx1[05]- TTCCombData to FEX 06	Rx1[05]+ Rx1[05]- RO Str 2 from FEX 06
P22/J22	07	Fabric Channel 04	Tx2[04]+ Tx2[04]- RO Str 5 from FEX 05	Rx2[04]+ Rx2[04]- RO Str 3 from FEX 05	Tx3[04]+ Tx3[04]- RO Str 6 from FEX 05	Rx3[04]+ Rx3[04]- RO Str 4 from FEX 05
	08		Tx0[04]+ Tx0[04]- LHC Clk to FEX 05	Rx0[04]+ Rx0[04]- RO Str 1 from FEX 05	Tx1[04]+ Tx1[04]- TTCCombData to FEX 05	Rx1[04]+ Rx1[04]- RO Str 2 from FEX 05
P22/J22	09	Fabric Channel 03	Tx2[03]+ Tx2[03]- RO Str 5 from FEX 04	Rx2[03]+ Rx2[03]- RO Str 3 from FEX 04	Tx3[03]+ Tx3[03]- RO Str 6 from FEX 04	Rx3[03]+ Rx3[03]- RO Str 4 from FEX 04
	10		Tx0[03]+ Tx0[03]- LHC Clk to FEX 04	Rx0[03]+ Rx0[03]- RO Str 1 from FEX 04	Tx1[03]+ Tx1[03]- TTCCombData to FEX 04	Rx1[03]+ Rx1[03]- RO Str 2 from FEX 04

P23/J23	01	Fabric Channel 02	Tx2[02]+ Tx2[02]- RO Str 5 from FEX 03	Rx2[02]+ Rx2[02]- RO Str 3 from FEX 03	Tx3[02]+ Tx3[02]- RO Str 6 from FEX 03	Rx3[02]+ Rx3[02]- RO Str 4 from FEX 03
	02		Tx0[02]+ Tx0[02]- LHC Clk to FEX 03	Rx0[02]+ Rx0[02]- RO Str 1 from FEX 03	Tx1[02]+ Tx1[02]- TTCCombData to FEX 03	Rx1[02]+ Rx1[02]- RO Str 2 from FEX 03
P23/J23	03	Fabric Channel 01	Tx2[01]+ Tx2[01]- RO Str 1 to othHUB	Rx2[01]+ Rx2[01]- RO Str 1 from othHUB	Tx3[01]+ Tx3[01]- RO Str 2 to othHUB	Rx3[01]+ Rx3[01]- RO Str2 from othHUB
	04		Tx0[01]+ Tx0[01]- LHC Clk to othHUB	Rx0[01]+ Rx0[01]- LHC Clk from othHUB	Tx1[01]+ Tx1[01]- TTC/ROD Ctl to othHUB	Rx1[01]+ Rx1[01]- TTC/ROD Ctl from othHUB
P23/J23	05	ShMC	BI_ShMCA+ BI_ShMCA- Unused signal pair	BI_ShMCA+ BI_ShMCA- Unused signal pair	BI_ShMCC+ BI_ShMCC- Unused signal pair	BI_ShMCD+ BI_ShMCD- Unused signal pair
P23/J23	06	Base Chan 02	BI_DA2+ BI_DA2- Unused signal pair	BI_DB2+ BI_DB2- Unused signal pair	BI_DC2+ BI_DC2- Unused signal pair	BI_DD2+ BI_DD2- Unused signal pair
P23/J23	07	Base Chan 03	BI_DA3+ BI_DA3- GE Pair A to FEX 03	BI_DB3+ BI_DB3- GE Pair B to FEX 03	BI_DC3+ BI_DC3- GE Pair C to FEX 03	BI_DD3+ BI_DD3- GE Pair D to FEX 03
P23/J23	08	Base Chan 04	BI_DA4+ BI_DA4- GE Pair A to FEX 04	BI_DB4+ BI_DB4- GE Pair B to FEX 04	BI_DC4+ BI_DC4- GE Pair C to FEX 04	BI_DD4+ BI_DD4- GE Pair D to FEX 04
P23/J23	09	Base Chan 05	BI_DA5+ BI_DA5- GE Pair A to FEX 05	BI_DB5+ BI_DB5- GE Pair B to FEX 05	BI_DC5+ BI_DC5- GE Pair C to FEX 05	BI_DD5+ BI_DD5- GE Pair D to FEX 05
P23/J23	10	Base Chan 06	BI_DA6+ BI_DA6- GE Pair A to FEX 06	BI_DB6+ BI_DB6- GE Pair B to FEX 06	BI_DC6+ BI_DC6- GE Pair C to FEX 06	BI_DD6+ BI_DD6- GE Pair D to FEX 06
J24/P24	01	Base Chan 07	BI_DA7+ BI_DA7- GE Pair A to FEX 07	BI_DB7+ BI_DB7- GE Pair B to FEX 07	BI_DC7+ BI_DC7- GE Pair C to FEX 07	BI_DD7+ BI_DD7- GE Pair D to FEX 07
J24/P24	02	Base Chan 08	BI_DA8+ BI_DA8- GE Pair A to FEX 08	BI_DB8+ BI_DB8- GE Pair B to FEX 08	BI_DC8+ BI_DC8- GE Pair C to FEX 08	BI_DD8+ BI_DD8- GE Pair D to FEX 08
J24/P24	03	Base Chan 09	BI_DA9+ BI_DA9- GE Pair A to FEX 09	BI_DB9+ BI_DB9- GE Pair B to FEX 09	BI_DC9+ BI_DC9- GE Pair C to FEX 09	BI_DD9+ BI_DD9- GE Pair D to FEX 09
J24/P24	04	Base Chan 10	BI_DA10+ BI_DA10- GE Pair A to FEX 10	BI_DB10+ BI_DB10- GE Pair B to FEX 10	BI_DC10+ BI_DC10- GE Pair C to FEX 10	BI_DD10+ BI_DD10- GE Pair D to FEX 10
J24/P24	05	Base Chan 11	BI_DA11+ BI_DA11- GE Pair A to FEX 11	BI_DB11+ BI_DB11- GE Pair B to FEX 11	BI_DC11+ BI_DC11- GE Pair C to FEX 11	BI_DD11+ BI_DD11- GE Pair D to FEX 11
J24/P24	06	Base Chan 12	BI_DA12+ BI_DA12- GE Pair A to FEX 12	BI_DB12+ BI_DB12- GE Pair B to FEX 12	BI_DC12+ BI_DC12- GE Pair C to FEX 12	BI_DD12+ BI_DD12- GE Pair D to FEX 12

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J24/P24	07	Base Chan 13	BI_DA13+ BI_DA13- GE Pair A to FEX 13	BI_DB13+ BI_DB13- GE Pair B to FEX 13	BI_DC13+ BI_DC13- GE Pair C to FEX 13	BI_DD13+ BI_DD13- GE Pair D to FEX 13
J24/P24	08	Base Chan 14	BI_DA14+ BI_DA14- GE Pair A to FEX 14	BI_DB14+ BI_DB14- GE Pair B to FEX 14	BI_DC14+ BI_DC14- GE Pair C to FEX 14	BI_DD14+ BI_DD14- GE Pair D to FEX 14
J24/P24	09	Base Chan 15	BI_DA15+ BI_DA15- Unused signal pair	BI_DB15+ BI_DB15- Unused signal pair	BI_DC15+ BI_DC15- Unused signal pair	BI_DD15+ BI_DD15- Unused signal pair
J24/P24	10	Base Chan 16	BI_DA16+ BI_DA16- Unused signal pair	BI_DB16+ BI_DB16- Unused signal pair	BI_DC16+ BI_DC16- Unused signal pair	BI_DD16+ BI_DD16- Unused signal pair

Note: the FEX numbering above follows the L1Calo convention to call
 "FEX 03" the module in ATCA Slot 3,
 "FEX 04" the module in ATCA Slot 4,
 "FEX 14" the module in ATCA Slot 14.

1371

Note: the name "othHUB" above stands for "the other HUB in the same ATCA crate"

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14.2 Connector and Signal Usage for a FEX Slot

Connector Usage for a FEX Slot

Connect Number	Row Num	Name	a	b	c	Connector d	Pin Pairs e	f	g	h
P23/J23	01	Fabric Channel 02	Tx2[02]+	Tx2[02]- RO Stream 3 to HUB 2	Rx2[02]+	Rx2[02]- RO Stream 5 to HUB 2	Tx3[02]+	Tx3[02]- RO Stream 4 to HUB 2	Rx3[02]+	Rx3[02]- RO Stream 6 to HUB 2
	02		Tx0[02]+	Tx0[02]- RO Stream 1 to HUB 2	Rx0[02]+	Rx0[02]- LHC Clock from Hub2	Tx1[02]+	Tx1[02]- RO Stream 2 to HUB 2	Rx1[02]+	Rx1[02]- TTCCombData from Hub2
P23/J23	03	Fabric Channel 01	Tx2[01]+	Tx2[01]- RO Stream 3 to HUB 1	Rx2[01]+	Rx2[01]- RO Stream 5 to HUB 1	Tx3[01]+	Tx3[01]- RO Stream 4 to HUB 1	Rx3[01]+	Rx3[01]- RO Stream 6 to HUB 1
	04		Tx0[01]+	Tx0[01]- RO Stream 1 to HUB 1	Rx0[01]+	Rx0[01]- LHC Clock from Hub1	Tx1[01]+	Tx1[01]- RO Stream 2 to HUB 1	Rx1[01]+	Rx1[01]- TTCCombData from Hub1
P23/J23	05	Base Chan 01	BI_DA1+ BI_DA1- GE Pair A IPbus Net	BI_DB1+ BI_DB1- GE Pair B IPbus Net	BI_DC1+ BI_DC1- GE Pair C IPbus Net	BI_DD1+ BI_DD1- GE Pair D IPbus Net				
P23/J23	06	Base Chan 02	BI_DA2+ BI_DA2- GE Pair A IPMC Net	BI_DB2+ BI_DB2- GE Pair B IPMC Net	BI_DC2+ BI_DC2- GE Pair C IPMC Net	BI_DD2+ BI_DD2- GE Pair D IPMC Net				
P23/J23	07	Base Chan 03	BI_DA3+ BI_DA3- Unused signal pair	BI_DB3+ BI_DB3- Unused signal pair	BI_DC3+ BI_DC3- Unused signal pair	BI_DD3+ BI_DD3- Unused signal pair				
P23/J23	08	Base Chan 04	BI_DA4+ BI_DA4- Unused signal pair	BI_DB4+ BI_DB4- Unused signal pair	BI_DC4+ BI_DC4- Unused signal pair	BI_DD4+ BI_DD4- Unused signal pair				
P23/J23	09	Base Chan 05	BI_DA5+ BI_DA5- Unused signal pair	BI_DB5+ BI_DB5- Unused signal pair	BI_DC5+ BI_DC5- Unused signal pair	BI_DD5+ BI_DD5- Unused signal pair				
P23/J23	10	Base Chan 06	BI_DA6+ BI_DA6- Unused signal pair	BI_DB6+ BI_DB6- Unused signal pair	BI_DC6+ BI_DC6- Unused signal pair	BI_DD6+ BI_DD6- Unused signal pair				

1373

1374 **15 Appendix 2: Hub Module FEX MGT Data Fanout**

1375 This section describes the 74 channel MGT Fanout on the Hub Module. This fanout
1376 receives FEX readout data from the Hub's ATCA Zone 2 connectors and sends this data
1377 to MGT transceiver inputs on both the ROD mezzanine card and to the Hub's own
1378 UltraScale Virtex FPGA. This fanout is based on the NB7VQ14M chip from On-Semi.
1379 Illustrations of the circuit diagrams can be found in **Figure 22** and **Figure 23**.

1380 **15.1 AC Coupling**

1381 The outputs from the NB7VQ14M fanout chips are AC coupled. 100 nFd 0201 size DC
1382 Blocking capacitors are used for this AC coupling. These capacitors are located very
1383 close the output pins on the NB7VQ14M fanout chips.

1384 **15.2 Input Common Mode Reference**

1385 The signals send to the Hub's MGT Fanout are all AC coupled at the sending end. Thus
1386 the input common mode voltage to NB7VQ14M fanout chips can and must be set with
1387 circuits on the Hub Module.

1388 The fanout chips internal VRef generator is used to set their common mode input voltage.
1389 When powered with a Vcc of 1.800 Volts this reference generator provides a 1.300 V +/-
1390 150 mV common mode input voltage to the fanout chips. This makes sense as the input
1391 circuit of these fanout chips is the bases of a long-tail NPN pair the emitters of which are
1392 feed by a current source.

1393 **15.3 Input Termination**

1394 The NB7VQ14M fanout chips contain their own input termination resistors. From a
1395 center tap there is a 50 Ohm resistor to each input. This center tap is tied to the common
1396 mode reference supply and bypassed to ground with a 47 nFd capacitor. In this way the
1397 common mode input voltage to the receiver is set, the 100 Ohm differential termination is
1398 realized, and a common mode termination is implemented.

1399 **15.4 Equalizer Enable**

1400 The NB7VQ14M fanout chips contain an equalizer that can reduce inter symbol
1401 interference on long copper PCB traces. This equalizer is enabled or removed from the
1402 fanout circuit by means of a logic level control pin.

1403 Because it is not yet clear if this equalizer will improve the MGT readout signals in the
1404 ATCA backplane application we will make the Equalizer Enable pin accessible on the
1405 Hub Module on a per slot basis. The assumption is that for the backplane losses from a

1406 given slot that either all 6 of the MGT readout signals from that slot will be improved by
1407 the equalizer or else none of them will.

1408 Thus from the point of view of the Equalizer Enables, the MGT fanout it is divided into
1409 13 section (12 FEXs and the Other Hub) with the equalizer enables individually
1410 programmable to each of these sections.

1411 The equalizer enable input pin has a 75k Ohm pull-down resistor. 6 of these in parallel is
1412 12.5k Ohm. When this logic input is at its default Low the equalizer is bypassed. The
1413 equalizer enable logic levels are:

- 1414 • Low is $< 0.35 V_{cc}$ High is $> 0.65 V_{cc}$.
- 1415 • With 1.8 Volt V_{cc} Low is < 0.630 and High is > 1.170 Volts
- 1416 • Current is under $\pm 150 \mu\text{Amp}$.

1417 The fanout equalizer enable pins are driven by a 1V8 HP Select I/O Bank on the Hub
1418 FPGA. In the Hi state, these control signals from the Hub FPGA are guaranteed to reach
1419 1.35 Volts (in LVCMOS_1V8 mode) or 1.400 Volts (in HSTL mode). So we are
1420 guaranteed to be able to remain in control of these equalizer enable inputs with the fanout
1421 chips operating from a V_{cc} as high as 2.154 Volts.

1422 **15.5 Reference Designators**

1423 The Hub Module uses an overall scheme to organize the reference designators of its
1424 many components. The fanout chips themselves run from U401 through U475 with an
1425 increment of 1 between channels. The various capacitors in these circuits (DC blocking,
1426 V_{cc} bypass, V_{Ref} bypass) run from C401 through C919 with an increment of 7 between
1427 channels.

1428 **15.6 Fanout V_{cc} Supply**

1429 The NB7VQ14M fanout chips can be powered with anything from 1.8 V to 3.3V. The
1430 lower supply voltages are attractive because of the reduced heat dissipation. From the
1431 data sheet I see no advantage in powering the fanout circuits from a 3.3 Volt supply. Ed
1432 Flaherty's ROD work indicates that 1V8 works as well or better than 2V5.

1433 There may be some advantage in using a fanout V_{cc} supply somewhat higher than the
1434 1V8 minimum listed in the NB7VQ14M data sheet. In any case this supply must be quiet
1435 as any noise that it puts onto these high speed MGT signals is likely to interfere with
1436 reception of these signals from across the ATCA backplane.

1437 Thus the Hub Module provides a private supply just for powering these fanout chips.
1438 This supply, FAN_1V8, is nominally set for 1.8 Volts. Because it does not power

1439 anything besides the fanout chips it could be adjusted up to at least 2.150 Volts if that is
1440 necessary.

1441 The expected current draw for the 74 fanout chips is 13 Amps. At maximum the fanout
1442 Vcc current draw should be less than 15 Amps. The heat from the 74 fanout chips is
1443 expected to be about 23 Watts.

1444 The Vcc pins on each fanout chip are bypassed with a 4.7 nFd and 100 nFd 0402 size
1445 ceramic capacitors as close as possible to the Vcc pins.

1446 **15.7 Routing Challenges**

1447 All of the differential pair traces associated with the FEX MGT data fanout circuits must
1448 be able to cleanly support 10 Gb/sec data rates. Interference and cross-talk must be kept
1449 to a minimum.

1450 This is especially true on the traces that run from the Zone 2 connectors to the inputs of
1451 the fanout chips. These MGT signals may be in poor condition after their travel across
1452 the backplane and through two ADFplus connectors.

1453 The 74 outputs running to the ROD must route out and separate from the 74 pairs that run
1454 to the Hub's FPGA. There is little space available on the Hub Module to hold the MGT
1455 fanout. Fanout chips are located on both sides of the card and the design of the side 2
1456 cover needs to take the height and heat dissipation from these parts into consideration.

1457 **15.8 Fanout Name**

1458 In a few places the documentation for the Hub Module may still call its FEX MGT data
1459 fanout by the name "GTH Fanout". This old name came from the original design of the
1460 Hub Module that used a Virtex-7 FPGA with only GTH type MGT transceivers. The old
1461 name has been replaced in most of the Hub's documentation but I know that it is still
1462 used in the net names.

1463 **15.9 Hub-Module FEX MGT Data Fanout Map**

1464 This FEX MGT Data Fanout Map is presented in two sections. The first section shows
1465 the map from the Zone 2 inputs through to the ROD MegArray connectors. The second
1466 section shows the map from the Zone 2 inputs through to the Hub's FPGA MGT inputs.
1467 Details of the design understandings:

- 1468 • The FEX cards are numbered 3:14 by their ATCA Logical Slot Number.
- 1469 • The 6 Aurora Lanes carrying FEX readout data are assigned to the ATCA Fabric
1470 Interface Channel Ports in the following way:

1471

Aurora Lane	0	1	2	3	4	5
FEX End ATCA	Tx0	Tx1	Tx2	Tx3	Rx2	Rx3
Hub End ATCA	Rx0	Rx1	Rx2	Rx3	Tx2	Tx3
Hub Zone 2 Pins	c,d	g,h	c,d	g,h	a,b	e,f
Hub Zone 2 Row	lower	lower	upper	upper	upper	upper

1472

1473

- 1474 • All FEX Aurora data on the ATCA backplane is “right side up”. That is, if for high
1475 speed routing considerations, a given FEX card criss-crosses some of its MGT
1476 Transmitter direct and complement output pins with the ATCA backplane direct and
1477 complement pins then it will also setup these MGT Transmitters to invert their output
1478 data.
- 1479 • The MegArray connector pinout is defined by the V1p4 document from 6-May-2015
1480 written by Ed.
- 1481 • With these understandings, all readout data delivered to the ROD will be “right side
1482 up” with the map that follows.
1483

1484 Description of the Columns in this Map Table:

- 1485 • MGT Fanout Channel Number, this table is listed in order of the MGT Fanout
1486 Channels on the Hub circuit board. The Hub Module netlist is in terms of MGT
1487 Fanout Channel Number.
- 1488 • FEX, this is the FEX card number 3:14, i.e. the ATCA Logical Slot Number of the
1489 FEX card.
- 1490 • Aurora Lane, this is the Aurora protocol Lane number of the readout data from this
1491 source, 0:5.
- 1492 • Zone 2 Input Pins, this column shows the ATCA Fabric Interface connector and pin
1493 numbers where this data source arrives on the Hub Module, e.g. J23-C/D2 means
1494 connector J23 pins C2 and D2. The pin carrying the direct signal (aka non-inverted
1495 signal) is always listed first, the pin carrying the complement signal (aka inverted
1496 signal) is listed second.
- 1497 • Layer, the signal layer (not physical layer) in the Hub PCB on which this differential
1498 pair is routed to the MGT Fanout Array.
- 1499 • Inverted, indicates whether or not the trace routing inverts this differential signal on
1500 its way from the Zone 2 connector to the MGT Fanout input.
- 1501 • MegAry Con, shows whether this signal is routed to the S1 or S2 MegArray
1502 connector.
- 1503 • MegAry Pins, lists the pins used in the MegArray connector for this readout signal,
1504 e.g. F/E39 means pins F39 and E39 are used for this differential signal. The pin
1505 carrying the direct signal is always listed first and the pin carrying the complement
1506 signal is listed second.
- 1507 • ROD FEX Input, this is the input to the ROD in Ed’s notation from his version V1p4
1508 MegArray Pinout from 6-May-2015.

- 1509 • Layer, the signal layer (not physical layer) in the Hub PCB on which this differential
 1510 pair is routed from the MGT Fanout output to the MegArray connector.
 1511 • Inverted, indicates whether or not the trace routing inverts this differential signal on
 1512 its way from the MGT Fanout to the MegArray connector.
 1513

1514 The map table for the connections between the backplane Zone 2 pins and the Hub's
 1515 FPGA is similar but instead of the MegArray connections it shows the connections to the
 1516 FPGA MTG Receivers in terms of Quad and channel within the Quad. Again the index
 1517 to this table is MGT Fanout Channel Number.

1518 Although the readout data from the FPGA on This Hub does not pass through the MGT
 1519 Fanout it is listed at the end of this table for completeness.

1520

1521 **Map from Zone 2 Fabric Interface Inputs to ROD MEG-Array Connectors**

MGT Fanout Channel	FEX	Aurora Lane	Zone 2 Input Pins	Layer	Inv	MEG-Array Con	MEG-Array Pins	ROD FEX Input	FEX Layer	Inv
1	3	0	J23-C/D2	7	N	S1	F/E39	0	7	N
2	3	1	J23-G/H2	8	Y	S1	J/H38	1	8	Y
3	3	2	J23-C/D1	9	N	S1	F/E37	2	9	N
4	3	3	J23-G/H1	6	Y	S1	J/H36	3	6	Y
5	3	4	J23-A/B1	7	N	S1	F/E35	4	7	N
6	3	5	J23-E/F1	8	Y	S1	J/H34	5	8	Y
7	4	0	J22-C/D10	9	N	S1	F/E33	6	9	N
8	4	1	J22-G/H10	6	Y	S1	J/H32	7	6	Y
9	4	2	J22-C/D9	7	N	S1	F/E31	8	7	N
10	4	3	J22-G/H9	8	Y	S1	J/H30	9	8	Y
11	4	4	J22-A/B9	9	N	S1	F/E29	10	9	N
12	4	5	J22-E/F9	6	Y	S1	J/H28	11	6	Y
13	5	0	J22-C/D8	7	N	S1	F/E27	12	7	N
14	5	1	J22-G/H8	8	Y	S1	J/H26	13	8	Y
15	5	2	J22-C/D7	9	N	S1	F/E25	14	9	N
16	5	3	J22-G/H7	6	Y	S1	J/H24	15	6	Y
17	5	4	J22-A/B7	7	N	S1	F/E23	16	7	N
18	5	5	J22-E/F7	8	Y	S1	J/H22	17	8	Y
19	6	0	J22-C/D6	9	N	S1	J/H20	18	9	N
20	6	1	J22-G/H6	6	Y	S1	F/E19	19	6	Y
21	6	2	J22-C/D5	7	N	S1	J/H18	20	7	N
22	6	3	J22-G/H5	8	Y	S1	F/E17	21	8	Y
23	6	4	J22-A/B5	9	N	S1	J/H16	22	9	N
24	6	5	J22-E/F5	6	Y	S1	F/E15	23	6	Y
25	7	0	J22-C/D4	7	N	S1	J/H14	24	7	N
26	7	1	J22-G/H4	8	Y	S1	F/E13	25	8	Y
27	7	2	J22-C/D3	9	N	S1	J/H12	26	9	N
28	7	3	J22-G/H3	6	Y	S1	F/E11	27	6	Y
29	7	4	J22-A/B3	7	N	S1	J/H10	28	7	N
30	7	5	J22-E/F3	8	Y	S1	F/E9	29	8	Y
31	8	0	J22-C/D2	9	N	S1	J/H8	30	9	N
32	8	1	J22-G/H2	6	Y	S1	F/E7	31	6	Y
33	8	2	J22-C/D1	7	N	S1	J/H6	32	7	N
34	8	3	J22-G/H1	8	Y	S1	F/E5	33	8	Y
35	8	4	J22-A/B1	9	N	S1	J/H4	34	9	N
36	8	5	J22-E/F1	6	Y	S1	F/E3	35	6	Y
MGT	FEX	Aurora	Zone 2			MEG-	MEG-	ROD	FEX	

Fanout Channel		Lane	Input Pins	Layer	Inv	Array Con	Array Pins	FEX Input	Layer	Inv
37	Other Hub	0	J23-C/D3	7	Y	S2	E/F3	HRD0	7	Y
38	Other Hub	1	J23-G/H3	8	N	S2	H/J8	HRD2	8	N
39	9	0	J21-C/D10	9	Y	S2	B/C4	71	9	Y
40	9	1	J21-G/H10	6	N	S2	E/F5	70	6	N
41	9	2	J21-C/D9	7	Y	S2	B/C6	69	7	Y
42	9	3	J21-G/H9	8	N	S2	E/F7	68	8	N
43	9	4	J21-A/B9	9	Y	S2	B/C8	67	9	Y
44	9	5	J21-E/F9	6	N	S2	E/F9	66	6	N
45	10	0	J21-C/D8	7	Y	S2	B/C10	65	7	Y
46	10	1	J21-G/H8	8	N	S2	E/F11	64	8	N
47	10	2	J21-C/D7	9	Y	S2	B/C12	63	9	Y
48	10	3	J21-G/H7	6	N	S2	E/F13	62	6	N
49	10	4	J21-A/B7	7	Y	S2	B/C14	61	7	Y
50	10	5	J21-E/F7	8	N	S2	E/F15	60	8	N
51	11	0	J21-C/D6	9	Y	S2	B/C16	59	9	Y
52	11	1	J21-G/H6	6	N	S2	E/F17	58	6	N
53	11	2	J21-C/D5	7	Y	S2	B/C18	57	7	Y
54	11	3	J21-G/H5	8	N	S2	E/F19	56	8	N
55	11	4	J21-A/B5	9	Y	S2	B/C20	55	9	Y
56	11	5	J21-E/F5	6	N	S2	E/F21	54	6	N
57	12	0	J21-C/D4	7	Y	S2	B/C22	53	7	Y
58	12	1	J21-G/H4	8	N	S2	E/F23	52	8	N
59	12	2	J21-C/D3	9	Y	S2	B/C24	51	9	Y
60	12	3	J21-G/H3	6	N	S2	E/F25	50	6	N
61	12	4	J21- A/B3	7	Y	S2	B/C26	49	7	Y
62	12	5	J21-E/F3	8	N	S2	E/F27	48	8	N
63	13	0	J21-C/D2	9	Y	S2	B/C28	47	9	Y
64	13	1	J21-G/H2	6	N	S2	E/F29	46	6	N
65	13	2	J21-C/D1	7	Y	S2	B/C30	45	7	Y
66	13	3	J21-G/H1	8	N	S2	E/F31	44	8	N
67	13	4	J21-A/B1	9	Y	S2	B/C32	43	9	Y
68	13	5	J21-E/F1	6	N	S2	E/F33	42	6	N
69	14	0	J20-C/D10	7	Y	S2	B/C34	41	7	Y
70	14	1	J20-G/H10	8	N	S2	E/F35	40	8	N
71	14	2	J20-C/D9	9	Y	S2	B/C36	39	9	Y
72	14	3	J20-G/H9	6	Y	S2	E/F37	38	6	Y
73	14	4	J20-A/B9	7	Y	S2	B/C38	37	7	Y
74	14	5	J20-E/F9	6	N	S2	E/F39	36	8	N
--	This Hub	0	--	-	-	S2	B/C2	HRD1	-	-
--	This Hub	1	--	-	-	S2	H/J6	HRD3	-	-

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Map from Zone 2 Fabric Interface Inputs to This Hub's FPGA MGT Inputs:

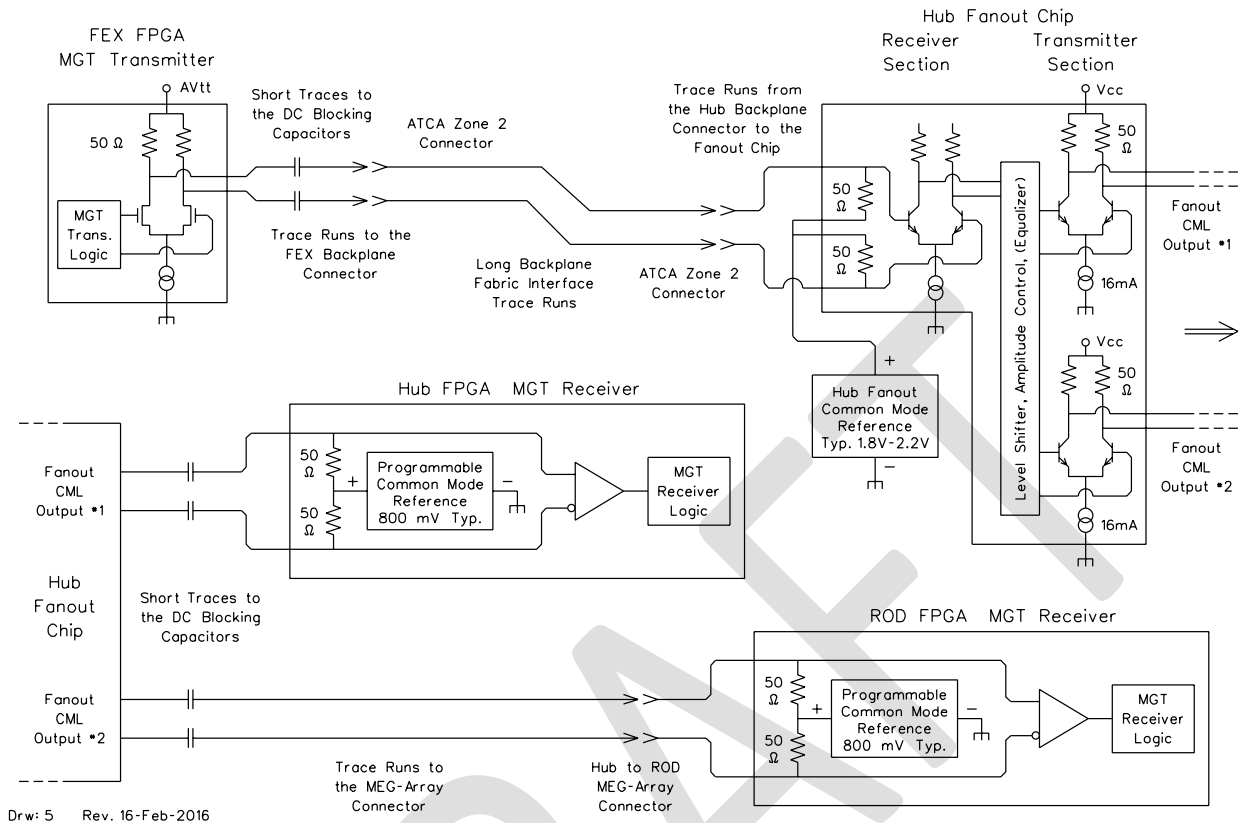
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MGT Fanout Channel	FEX	Aurora Lane	Zone 2 Input Pins	Layer	Inv	Hub FPGA Chan-Quad	MGT Type	Receiver Pins	Layer	Inv
1	3	0	J23-C/D2	7	N	Rx1-126	GTY	AF43/4	2	Y
2	3	1	J23-G/H2	8	Y	Rx0-126	GTY	AG45/6	3	N
3	3	2	J23-C/D1	9	N	Rx3-125	GTY	AH43/4	4	Y
4	3	3	J23-G/H1	6	Y	Rx2-125	GTY	AJ45/6	5	N
5	3	4	J23-A/B1	7	N	Rx1-125	GTY	AK43/4	2	Y
6	3	5	J23-E/F1	8	Y	Rx0-125	GTY	AL45/6	3	N
7	4	0	J22-C/D10	9	N	Rx3-124	GTY	AM43/4	4	Y
8	4	1	J22-G/H10	6	Y	Rx2-124	GTY	AN45/6	5	N
9	4	2	J22-C/D9	7	N	Rx1-128	GTY	V43/4	2	Y
10	4	3	J22-G/H9	8	Y	Rx0-128	GTY	W45/6	3	N
11	4	4	J22-A/B9	9	N	Rx3-127	GTY	Y43/4	4	Y
12	4	5	J22-E/F9	6	Y	Rx2-127	GTY	AA45/6	5	N
13	5	0	J22-C/D8	7	N	Rx1-127	GTY	AB43/4	2	Y
14	5	1	J22-G/H8	8	Y	Rx0-127	GTY	AC45/6	3	N
15	5	2	J22-C/D7	9	N	Rx3-126	GTY	AD43/4	4	Y
16	5	3	J22-G/H7	6	Y	Rx2-126	GTY	AE45/6	5	N
17	5	4	J22-A/B7	7	N	Rx1-130	GTY	K43/4	2	Y
18	5	5	J22-E/F7	8	Y	Rx0-130	GTY	L45/6	3	N
19	6	0	J22-C/D6	9	N	Rx3-129	GTY	M43/4	4	Y
20	6	1	J22-G/H6	6	Y	Rx2-129	GTY	N45/6	5	N
21	6	2	J22-C/D5	7	N	Rx1-129	GTY	P43/4	2	Y
22	6	3	J22-G/H5	8	Y	Rx0-129	GTY	R45/6	3	N
23	6	4	J22-A/B5	9	N	Rx3-128	GTY	T43/4	4	Y
24	6	5	J22-E/F5	6	Y	Rx2-128	GTY	U45/6	5	N
25	7	0	J22-C/D4	7	N	Rx3-132	GTY	B43/4	2	Y
26	7	1	J22-G/H4	8	Y	Rx2-132	GTY	C45/6	3	N
27	7	2	J22-C/D3	9	N	Rx1-132	GTY	D43/4	4	Y
28	7	3	J22-G/H3	6	Y	Rx0-132	GTY	E45/6	5	N
29	7	4	J22-A/B3	7	N	Rx1-131	GTY	F43/4	2	Y
30	7	5	J22-E/F3	8	Y	Rx0-131	GTY	G45/6	3	N
31	8	0	J22-C/D2	9	N	Rx3-130	GTY	H43/4	4	Y
32	8	1	J22-G/H2	6	Y	Rx2-130	GTY	J45/6	5	N
33	8	2	J22-C/D1	7	N	Rx2-231	GTH	G16/5	2	N
34	8	3	J22-G/H1	8	Y	Rx3-231	GTH	E16/5	3	Y
35	8	4	J22-A/B1	9	N	Rx3-131	GTY	E31/2	4	Y
36	8	5	J22-E/F1	6	Y	Rx2-131	GTY	G31/2	5	N
37	Other Hub	0	J23-C/D3	7	Y	Rx3-133	GTY	A31/2	2	N
38	Other Hub	1	J23-G/H3	8	N	Rx2-133	GTY	B33/4	3	N
39	9	0	J21-C/D10	9	Y	Rx1-133	GTY	C31/2	4	Y
40	9	1	J21-G/H10	6	N	Rx0-133	GTY	D33/4	5	N
41	9	2	J21-C/D9	7	Y	Rx0-232	GTH	E 2/1	2	N
42	9	3	J21-G/H9	8	N	Rx1-232	GTH	D 4/3	3	Y
43	9	4	J21-A/B9	9	Y	Rx2-232	GTH	C 2/1	4	N
44	9	5	J21-E/F9	6	N	Rx3-232	GTH	B 4/3	5	Y
45	10	0	J21-C/D8	7	Y	Rx0-233	GTH	D14/3	2	N
46	10	1	J21-G/H8	8	N	Rx1-233	GTH	C16/5	3	Y
47	10	2	J21-C/D7	9	Y	Rx2-233	GTH	B14/3	4	N
48	10	3	J21-G/H7	6	N	Rx3-233	GTH	A16/5	5	N
49	10	4	J21-A/B7	7	Y	Rx2-229	GTH	N 2/1	2	N
50	10	5	J21-E/F7	8	N	Rx3-229	GTH	M 4/3	3	Y
51	11	0	J21-C/D6	9	Y	Rx0-230	GTH	L 2/1	4	N
52	11	1	J21-G/H6	6	N	Rx1-230	GTH	K 4/3	5	Y
53	11	2	J21-C/D5	7	Y	Rx2-230	GTH	J 2/1	2	N
54	11	3	J21-G/H5	8	N	Rx3-230	GTH	H 4/3	3	Y

55	11	4	J21-A/B5	9	Y	Rx0-231	GTH	G 2/1	4	N
56	11	5	J21-E/F5	6	N	Rx1-231	GTH	F 4/3	5	Y
57	12	0	J21-C/D4	7	Y	Rx2-227	GTH	AA2/1	2	N
58	12	1	J21-G/H4	8	N	Rx3-227	GTH	Y 4/3	3	Y
59	12	2	J21-C/D3	9	Y	Rx0-228	GTH	W 2/1	4	N
60	12	3	J21-G/H3	6	N	Rx1-228	GTH	V 4/3	5	Y
61	12	4	J21-A/B3	7	Y	Rx2-228	GTH	U 2/1	2	N
62	12	5	J21-E/F3	8	N	Rx3-228	GTH	T 4/3	3	Y
63	13	0	J21-C/D2	9	Y	RX0-229	GTH	R 2/1	4	N
64	13	1	J21-G/H2	6	N	Rx1-229	GTH	P 4/3	5	Y
65	13	2	J21-C/D1	7	Y	Rx0-225	GTH	AL 2/1	2	N
66	13	3	J21-G/H1	8	N	Rx1-225	GTH	AK 4/3	3	Y
67	13	4	J21-A/B1	9	Y	Rx2-225	GTH	AJ 2/1	4	N
68	13	5	J21-E/F1	6	N	Rx3-225	GTH	AH 4/3	5	Y
69	14	0	J20-C/D10	7	Y	Rx0-226	GTH	AG 2/1	2	N
70	14	1	J20-G/H10	8	N	Rx1-226	GTH	AF 4/3	3	Y
71	14	2	J20-C/D9	9	Y	Rx2-226	GTH	AE 2/1	4	N
72	14	3	J20-G/H9	6	Y	Rx3-226	GTH	AD 4/3	5	Y
73	14	4	J20-A/B9	7	Y	Rx0-227	GTH	AC 2/1	2	N
74	14	5	J20-E/F9	6	N	Rx1-227	GTH	AB 4/3	3	Y

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Data Path - FEX to Hub and then to ROD



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Figure 22: Circuit diagram of FEX/Hub/ROD high-speed data paths.

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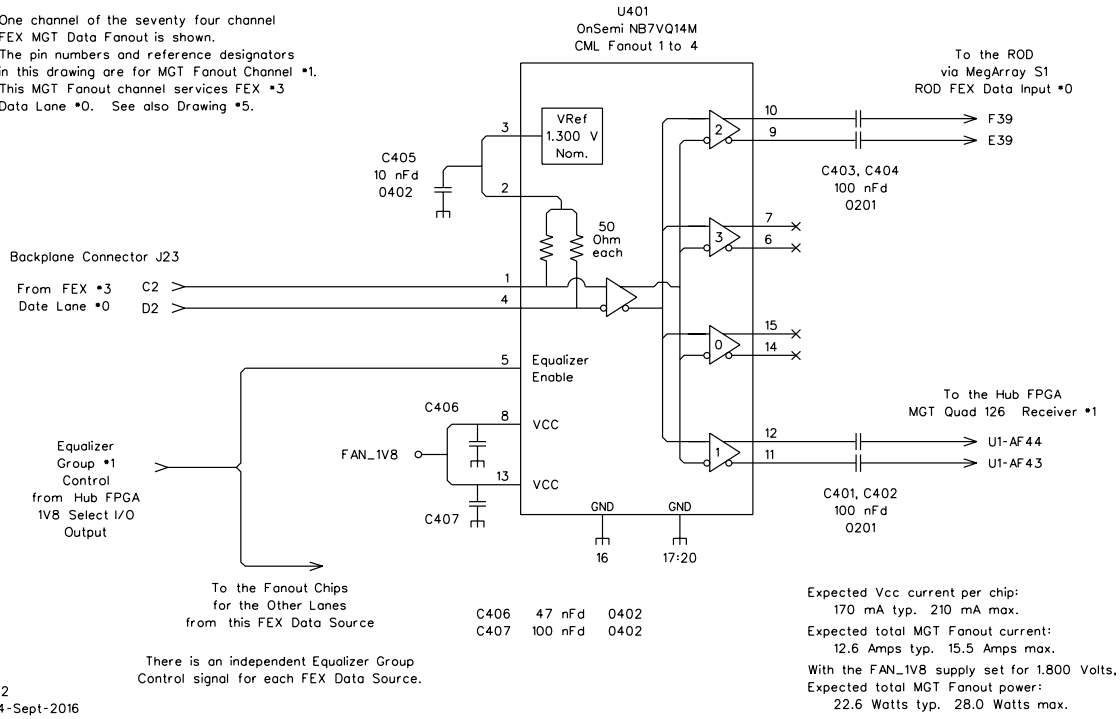
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FEX MGT Data FanOut

One channel of the seventy four channel FEX MGT Data Fanout is shown. The pin numbers and reference designators in this drawing are for MGT Fanout Channel #1. This MGT Fanout channel services FEX #3 Data Lane #0. See also Drawing #5.



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Figure 23: Hub MGT FanOut circuit diagram.

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1550 **16 Appendix 3: Hub-Module Clock Generation and Distribution**

1551 The Hub-Module uses 3 different clocks:

- 1552 • Ethernet 25.000 MHz Clock crystal controlled
- 1553 • 40.08 MHz LHC locked clock for FPGA logic
- 1554 • 320.64 MHz LHC locked clock for MGT Reference and FPGA logic

1555 **16.1 Ethernet 25.000 MHz Clock**

1556 The 25 MHz clock generation and distribution are shown in **Figure 24**. This clock is
1557 generated by a local crystal and thus is not LHC locked. All other clocks on the Hub Module
1558 are LHC locked. The main purpose of the 25.000 MHz clock is to run the Ethernet Switches
1559 and the Phys chips.

1560 The crystal that is used to generate this clock has better frequency tolerance and jitter
1561 specification than are required by either the Switch or Phys chips. The output of this crystal
1562 oscillator is fanned out 6 ways by a low jitter TI clock fanout chip. The 25 MHz clock
1563 signals from this fanout are all single ended back terminated 3V3 CMOS level. There are
1564 separate clock feeds to each of the 3 Switch chips and to both of the Phys chips. There is also
1565 a 25.000 MHz clock feed to a Global Clock input in Select I/O Bank 94 of the FPGA. This is
1566 in SLR #0 of the UltraScale FPGA.

1567 The clock input on the Switch chips requires a high level of 1.7 V min and 3.8 V max
1568 (XtalVdd + 0.5V max). The clock input on the Phys chips requires a high level of 2.5 V min
1569 and 3.3 V max. So a 3V3 clock is fine for both the Switch and Phys chips.

1570 Each of the Phys chips multiplies the 25.000 MHz clock that it receives up to 125 MHz.
1571 These Phys chips make their 125 MHz clocks available on output pins in case they are
1572 needed by the associated MACs. The 125 MHz clock outputs from the 2 Phys chips have
1573 been routed to Global Clock inputs in Select I/O Bank 68 of the FPGA. This is the same I/O
1574 Bank that handles all of the RGMII MAC interface connections between the FPGA and the
1575 Phys chips. This I/O Bank is in SLR #0 of the UltraScale FPGA.

1576 **16.2 40.08 MHz LHC Locked Clock**

1577 The Hub's 40.08 MHz clock generation is shown in **Figure 26**. This 40.08 MHz clock is
1578 designed to be locked to the LHC.

1579 To make this lock an LHC reference clock is received either as an FELIX Optical TTC signal
1580 using one of the Hub's MiniPOD Receivers or it is received from the Other Hub as a
1581 differential pair over the ATCA fabric interface backplane.

1582 Both the decoding of the optical LHC reference clock and the selection between using the
1583 optical reference or using the reference from the Other Hub are implemented in the Hub's
1584 FPGA. This is shown in the left-hand side of **Figure 26**.

1585 In either case, the selected LHC reference clock leaves Bank 68 of the FPGA as an LVDS
 1586 signal and is routed to an LVDS to single ended receiver U501 that is located right next to
 1587 the 40.08 MHz crystal controlled PLL U502. This crystal controlled PLL has a low loop
 1588 frequency so that it removes jitter from the selected LHC reference. When no LHC reference
 1589 is available the PLL will hold within 50 ppm of the nominal LHC frequency. A signal
 1590 indicating whether or not this PLL is locked to its reference is sent to a Select I/O input on
 1591 the Hub's FPGA where it can be monitored in an IPBus visible status register.

1592 The 40.08 MHz LVPECL output from this PLL is routed to a set of clock fanouts that are
 1593 shown in **Figure 26**. The First Fanout U503 drives 4 loads and then a Second Fanout U504
 1594 drives the 12 FEX cards plus the Other Hub over the Backplane. This two step fanout is
 1595 necessary because of the two Hub cards in a Shelf only the Hub that receives the FELIX
 1596 Optical TTC signal will drive its backplane clock lines. Thus the Second Fanout U504 can
 1597 be controlled from the Hub's FPGA so that it either operates normally or else it holds its
 1598 output pins static. Only on the Hub that receives the FELIX Optical TTC signal will this
 1599 Second Fanout be enabled and thus provide a backplane clock to the 12 FEX cards and to the
 1600 Other Hub.

1601 First Fanout U503 a TI CDCLVD1204 drives:

- 1602 • the ROD Mezzanine on This Hub
- 1603 • a Select I/O Global Clock input pair in Bank 71 of This Hub's FPGA for use as a logic
1604 clock
- 1605 • a reference to the 320.64 MHz Clock on This Hub
- 1606 • the Second 40.08 MHz Fanout on This Hub
- 1607

1608 Second 40.08 MHz Fanout U504 a TI CDCLVD1216 drives:

- 1609 • the 12 FEX cards over the backplane
- 1610 • the Other Hub over the backplane
- 1611

1612 The 2V5 and 3V3 power for the 40.08 MHz clock generation and distribution components is
 1613 LC filtered from the bulk supplies and distributed to these components on separate isolated
 1614 PCB area fills. The ground plane under these components has been partially separated from
 1615 the rest of the Hub's ground plane with a moat.

1616 **Figure 25** includes a note about FPGA differential pin pairs that receive this AC coupled
 1617 LVDS clock signals.

1618 **16.3 320.64 MHz LHC Locked Clock for MGT Reference and FPGA** 1619 **Logic**

1620 The Hub's 320.64 MHz clock is shown in **Figure 27**. This is also an LHC locked clock. It
 1621 uses a fanout copy of the Hub's 40.08 MHz clock as its reference.

1622 This 40.08 MHz LVDS reference signal is received by U505 and converted to a single ended
1623 CMOS reference signal for U506, the 320.64 MHz PLL. This crystal controlled PLL has a
1624 loop frequency that allows it to track changes in the output of the Hub's 40.08 MHz PLL. A
1625 signal indicating whether or not this PLL is locked to its reference is sent to a Select I/O input
1626 on the Hub's FPGA where it can be monitored in an IPBus visible status register.

1627 The LVPECL output from the 320.64 MHz PLL is delivered to U507 which is a
1628 MC100LVEP111 10 way LVPECL fanout.

1629 • 8 copies of the 320.64 MHz clock from this fanout are delivered to MGT Reference
1630 Clock inputs on This Hub's FPGA. These are delivered as AC coupled LVPECL signals.
1631 The MGT Reference Clock inputs that receive this clock are listed near the end of Section
1632 18.
1633

1634 • A copy of the 320.64 MHz clock from this fanout is delivered to a Select I/O Global
1635 Clock input pair in Bank 71 of This Hub's FPGA for use as a logic clock. Note that the
1636 correct options need to be set in this I/O Block to allow it to receive this AC coupled
1637 clock signal. See the note on **Figure 27**.
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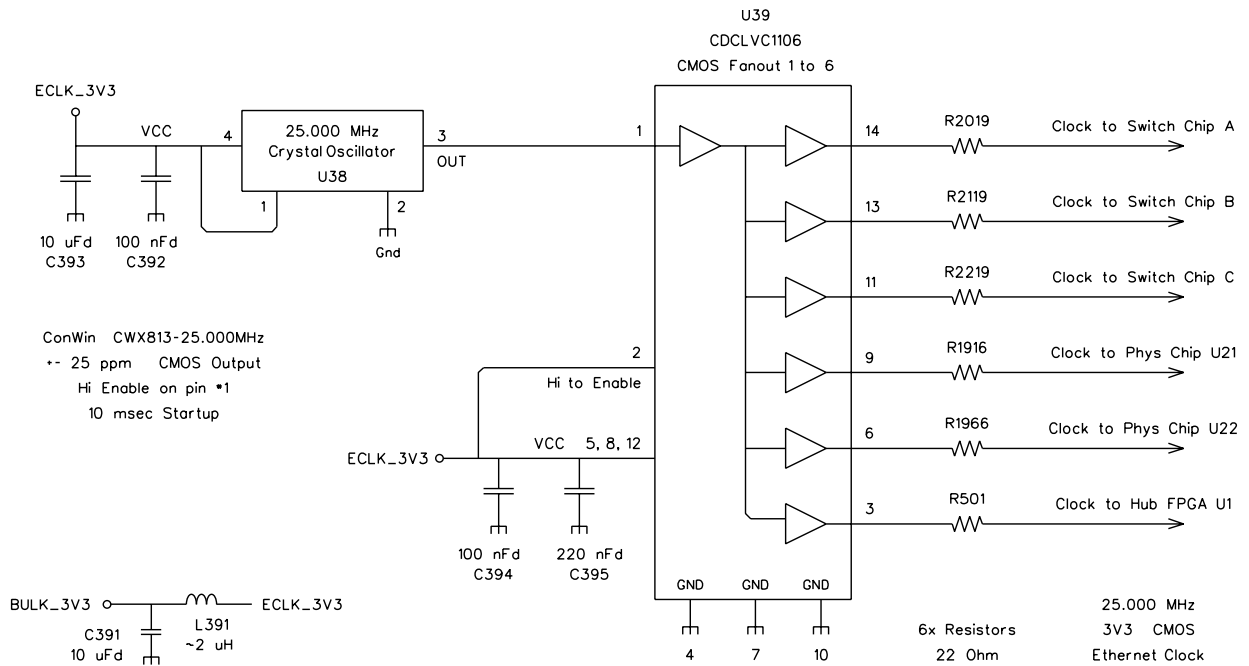
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Hub Module - 25 MHz Ethernet Clock

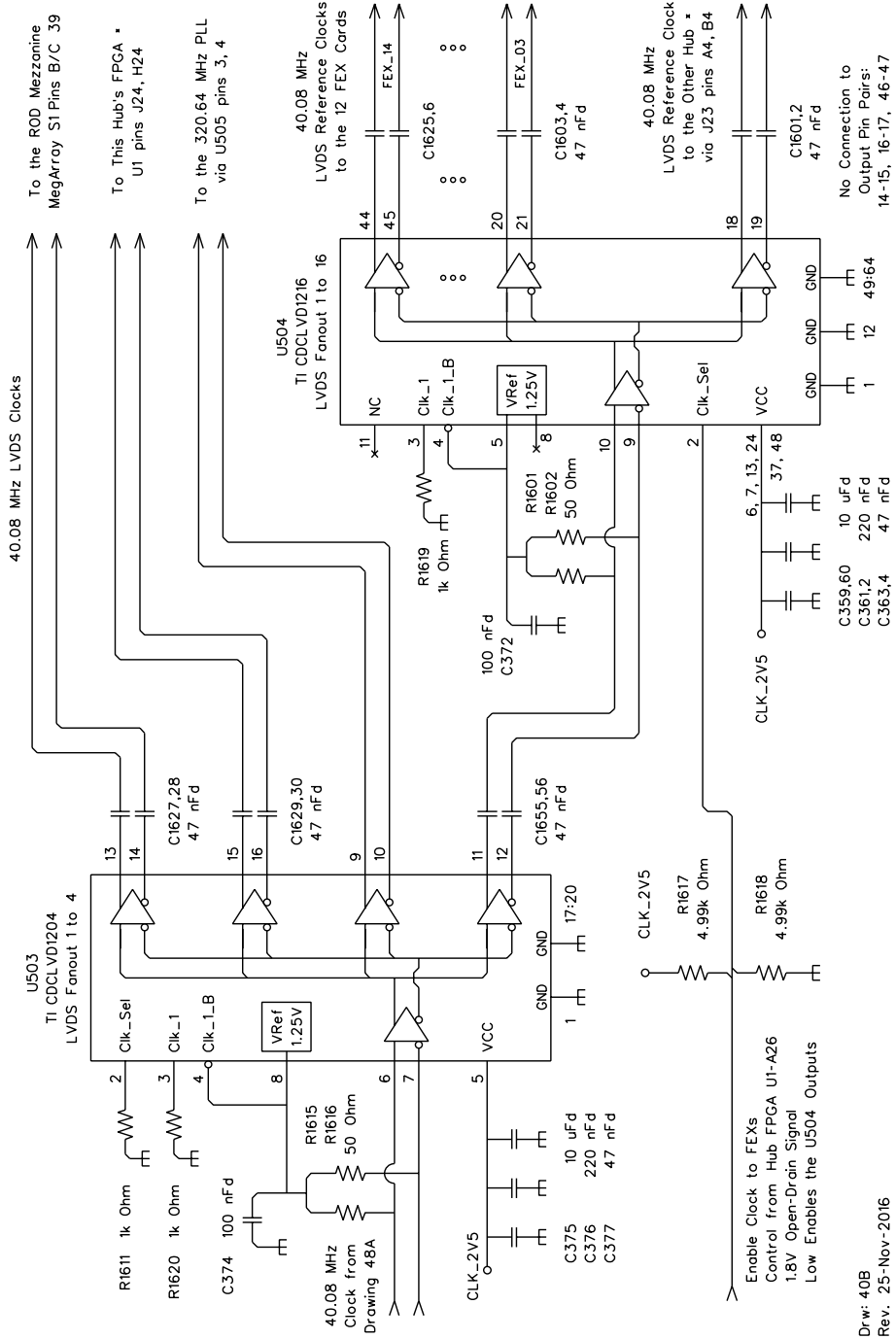


Drw: 39
Rev. 30-Dec-2015

Figure 24: Circuit diagram of Hub 25 MHz Ethernet clock.

1649

Hub 40.08 MHz LHC Clock Distribution



1650

1651

Figure 26: Circuit diagram for Hub 40.08 MHz clock distribution (2/2)

1652

1653

1659 **17 Appendix 4: Hub-Module Ethernet Line Circuits**

1660 This note describes the “line circuits” on the Hub Module that connect its various Ethernet
 1661 components to the twisted pair lines that run from the card. Here I used “twisted pair” to
 1662 mean both the ATCA Base Interface Ethernet links and the front panel RJ-45 unshielded
 1663 twisted pair cable (UTP cable) Ethernet links. The standard transformer coupled Ethernet
 1664 line circuits are often referred to in engineering slang as “Ethernet magnetics”. A circuit
 1665 diagram is shown in **Figure 28**.

1666 The very end of this note describes the capacitor coupled Ethernet line circuits that are used
 1667 for the Ethernet connections that have both ends on the same Hub Module.

1668 **17.1 Transformer Coupled Ethernet Line Circuits**

1669 At the Ethernet physical layer the Hub Module has three different types of devices that must
 1670 connect to standard transformer coupled Ethernet line circuits:

- 1671 • 17 line circuits to Broadcom BCM53128 Switch ports.
- 1672 • 13 of these run to the backplane Zone 2 Base Interface.
- 1673 • 4 of these run to the front panel RJ-45s.
- 1674 • 1 line circuit to the Micrel KSZ9031RNX Phys Chip for this Hub’s Virtex FPGA. This
 1675 circuit runs to the backplane Zone 2 Base Interface.
- 1676 • 1 line circuit to the Micrel KSZ9031RNX Phys Chip for the ROD Virtex FPGA on this
 1677 Hub card. This circuit runs to a front panel RJ-45 connector.
- 1678 • 1 line circuit to the TI DP83848C Phys Chip on the IPMC mezzanine module. This
 1679 circuit runs to a front panel RJ-45 connector.

1680

1681 Both modern voltage mode and older current mode connections to the Ethernet line circuits
 1682 are used on the Hub Module. The Broadcom BCM53128 and the Micrel KSZ9031RNX are
 1683 voltage mode devices. The TI DP83848C Phys Chip in the IPMC is a current mode device.

1684 The Ethernet line circuit for the IPMC has the added complication that currently it is a 10/100
 1685 Base-T only connection but in the future the IPMC may be supplied as a 10/100/1000 Base-T
 1686 device that will use 2 additional circuits and will presumably be a voltage mode device.

1687 The “magnetics” used on the Hub Module is a SMD device that holds 8 circuits per device,
 1688 i.e. 2 complete 10/100/1000 Base-T connections per device. It is a Pulse Engineering
 1689 HX5201NL part that can operate over the -40 to +85 deg. C temperature range. The
 1690 HX5201NL is of the recommended topology with its isolation transformer next to the Phys
 1691 port and its common mode choke next to its line port. This is a so called “8 core” per
 1692 Ethernet connection device and has a 3 wire common mode choke that can be used with
 1693 Power Over Ethernet.

1694 **17.2 Phys Side Connections**

1695 The connection to the Phys side of the magnetics is different for voltage mode and current
1696 mode devices.

- 1697 • The voltage mode Phys devices connect to the two outer primary side transformer
1698 terminals on each circuit and the primary center tap is tied to logic ground through a 100
1699 nFd capacitor.
- 1700 • The current mode Phys device connects to the two outer primary side transformer
1701 terminals as above. In addition each terminal on the Phys has a 50 Ohm resistor that runs
1702 to Vcc which is 3.3 Volts for the the DP83848C device on the IPMC. These 50 Ohm
1703 resistors are located on the IPMC mezzanine. The Vcc side of these resistors must be
1704 bypassed to ground. In addition the center tap of the transformer primary must be
1705 bypassed to ground with a 100 nFd cap and tied to Vcc, i.e. 3.3 Volts for the DP83848C
1706 device.
- 1707 • So the difference in these circuits on the Hub Module needs to be the inclusion of a
1708 jumper from the transformer primary center tap to the 3.3 Volt plane for any circuits that
1709 may need to operate in current mode, i.e. the IPMC A/Tx B/Rx circuits.

1710 **17.3 Line Side Connections**

1711 In the Hub application (which does not have Power Over Ethernet) the line side of the
1712 magnetics is tied to a front panel RJ-45 connector or to a Zone 2 Base Interface connection
1713 paying attention to the required strange pinout of the B and “C” circuits in the RJ-45
1714 connector. The center tap of the line side common mode choke is tied to ground through a
1715 Bob Smith termination (patented by Robert W. Smith).

1716 The intent of this termination of to absorb common mode energy in the line side circuit and
1717 thus to help reduce the radiation of this energy. This termination consists of a 75 Ohm series
1718 resistor from the common mode choke center tap in each of the 4 circuits in a given
1719 Ethernet connection. The far side of these 4 resistors are tied together and then tied to ground
1720 through a 1 nFd capacitor.

1721 For the Base Interface Ethernet connections the ground that this 1 nFd cap is tied to should
1722 clearly be the Logic Ground. For the front panel RJ-45 links one could argue that the 1 nFd
1723 cap should be tied to the Shelf ground or to the Logic Ground. Being an ATCA card the Hub
1724 Module has only a single pin Zone 1 connection to the Shelf Ground and thus this ground
1725 connection is likely to be noisy and not a very stiff ground point. Thus for the Hub’s front
1726 panel RJ-45 Ethernet connections the 1 nFd Bob Smith capacitor is tied to Logic Ground.

1727 **17.4 Ethernet Magnetics Connection Summary**

1728 In summary, each Ethernet connection (4 circuits) requires the following passive
1729 components:

- 1730 • 4x 100 nFd caps from the trans pri center tap to gnd
 - 1731 • 2x zero Ohm jumpers to 3V3 for current mode Tx,Rx only
 - 1732 • 4x 75 Ohm from common mode choke sec side center tap
-

- 1733 • 1x 1 nFd from the 75 Ohm resistors to ground

1734 **17.5 Front Panel RJ-45s**

1735 The front panel RJ-45 connectors used on the Hub Module are TE Connectivity 1888653-x
 1736 1x2 condo connectors. These are special condo connectors for ATCA because the standard
 1737 height RJ-45 condo connector is too tall to fit within the ATCA side 1 component height
 1738 limitation.

1739 The TE 1888653-x connector requires a notch in the front edge of the PCB or else it will stick
 1740 out to far. On the Hub Module this notch is a minimum of 16.00 mm wide (i.e the connector
 1741 itself requires a 16.00 mm wide notch and to this one needs to add some clearance and router
 1742 tool radius). The notch, in theory, needs to be 10.55mm deep. Using a 7.00 mm deep cutout
 1743 makes a better match to how far the other components (e.g. SFP+) stick out in front of the
 1744 Hub’s front panel.

1745 The Hub Module uses the 1888653-4 RJ-45 connector. This connector has the following
 1746 setup of its LEDs: LEDs 1,4 are in the lower, i.e. PCB level, RJ45; LEDs 2,3 are in the
 1747 upper RJ45.

1748 As installed on our Hub card and with the long axis of the front panel vertical:

1749 LEDs 1,2 are above their RJ45s
 1750 LEDs 3,4 are below their RJ45s.
 1751

1752	TE Part No.	LED_1	LED_2	LED_3	LED_4
1753	-----	-----	-----	-----	-----
1754	1888653-4	Green	Green	Yellow	Yellow

1755

1756 There are alternative versions of this connector available with different LED arrangements.
 1757 The 1888653-4 version has the common Green/Yellow LEDs and is available from stock.

1758 For the Hub’s Ethernet links that do not run through front panel RJ-45 connectors, green and
 1759 yellow LEDs are provided in a separate front panel LED array.

1760 The metal cover shell around the RJ-45 connectors, which makes no electrical connection to
 1761 the twisted pair cable, is tied to the Shelf Ground via its fingers that touch the front panel. In
 1762 addition the Shelf Ground net is run to the pins on this connector that attach to its metal cover
 1763 shell.

1764 **17.6 Capacitor Coupled Ethernet Line Circuits**

1765 There are two types of Ethernet connections on the Hub Module were both ends of the
 1766 connection are on the same module. These are:

- 1767 • The connections between the Broadcom BCM53128 Switch Chips: Chip A <--> Chip B
 1768 <--> Chip C.
 1769 • The connection from the Micrel KSZ9031RNX Phys Chip for this Hub's Virtex FPGA
 1770 to Switch Chip C on the same Hub Module.
 1771

1772 In these cases both ends of the Ethernet connection are on the same Hub Module and operate
 1773 with the same ground planes. Thus we do not have a large concern about common mode
 1774 signals on these links.

1775 To save circuit board space capacitor coupling can be used on these links. Both of these
 1776 devices have modern voltage mode physical layer transmitters which makes it much easier to
 1777 use capacitor coupling.

1778 Specific information about using capacitor coupling with the Broadcom BCM53128 Switch
 1779 Chip is given on page 29 of the BCM53128 "Layout and Design Guide" including an
 1780 example of capacitor coupling it to a different LDAC Phys device. Also see the Broadcom
 1781 note CAP-AN102 "Capacitive Coupling 10/100/1000 Base-T Ethernet Chip-to-Chip and
 1782 Backplane Applications".

1783 Information from Micrel about using capacitor coupling is given in their application note
 1784 AN-120.

1785 **17.7 Assignment of Ethernet "Magnetics"**

1786 The Pulse Engineering HX5201NL "magnetics" that are used on the Hub have 2 full Ethernet
 1787 port (i.e. 8 circuits) per module. They are assigned to the various Line Circuits in the
 1788 following way:

1789

Ref. Desig.	Mag Sect	Usage
TRNS1	Left Right	RJ1 Lower This Hub's ROD RJ1 Upper This Hub's IPMC
TRNS2	Left Right	RJ2 Lower Switch Chip "A" Port 6 RJ2 Upper Switch Chip "C" Port 6
TRNS3	Left Right	RJ3 Lower Switch Chip "B" Port 6 RJ3 Upper Switch Chip "B" Port 7
TRNS4	Left Right	This Hub's FPGA Phy U21 J20 Rw 3&4 to Other Hub Sw Chip B Port 5 BI Ch 2 J20 Rw 3&4 to Other Hub FPGA
TRNS5	Left Right	Chip C Port 5 BI Ch 3 J23 Rw 7 to Slot 3 FEX Chip C Port 4 BI Ch 4 J23 Rw 8 to Slot 4 FEX
TRNS6	Left Right	Chip C Port 3 BI Ch 5 J23 Rw 9 to Slot 5 FEX Chip C Port 2 BI Ch 6 J23 Rw 10 to Slot 6 FEX

TRNS7	Left Right	Chip C Port 1 BI Ch 7 J24 Rw 1 to Slot 7 FEX Chip C Port 0 BI Ch 8 J24 Rw 2 to Slot 8 FEX
TRNS8	Left Right	Chip A Port 5 BI Ch 9 J24 Rw 3 to Slot 9 FEX Chip A Port 4 BI Ch 10 J24 Rw 4 to Slot 10 FEX
TRNS9	Left Right	Chip A Port 3 BI Ch 11 J24 Rw 5 to Slot 11 FEX Chip A Port 2 BI Ch 12 J24 Rw 6 to Slot 12 FEX
TRNS10	Left Right	Chip A Port 1 BI Ch 13 J24 Rw 7 to Slot 13 FEX Chip A Port 0 BI Ch 14 J24 Rw 8 to Slot 14 FEX

1790

1791 **17.8 Assignment of Front Panel RJ-45 Connectors**

1792 The TE 1888653-x condo RJ-45 connector that are used on the front panel of the Hub
1793 Module are assigned in the following way:

Ref Desig	Connector	Usage
RJ1	Lower or Left Upper or Right	This Hub's ROD This Hub's IPMC
RJ2	Lower or Left Upper or Right	Switch Chip "A" Port 6 Switch Chip "C" Port 6
RJ3	Lower or Left Upper or Right	Switch Chip "B" Port 6 Switch Chip "B" Port 7

1794

1795 When viewed from the front with the card plugged into a crate and the long axis of its front
1796 panel vertical, then RJ1 is nearest the top of the Hub and RJ3 is nearest the bottom edge of the
1797 card.

1798 **17.9 Document / Verify the ROD's RJ45 Ethernet Connection**

1799 The ethernet connections on the ROD mezzanine card shown below come from pages 3 and
1800 20 of the 4-Sept-2015 ROD print set.

ROD's Ethernet			Hub Magnetics and RJ45 for the ROD			
ROD Net Name	U11 KSZ9031 Pin No.	MegArray S1 Pin No.	MegArray S1 Pin No.	TRNS1 Magnetics		Front Panel RJ45 Pin No.
				Primary Pin No.	Secondary Pin No.	
TxRxA_P	2	S1-B29	S1-B29	L3	L9	2
TxRxA_N	3	S1-C29	S1-C29	L1	L7	1
TxRxB_P	5	S1-B31	S1-B31	L6	L12	6
TxRxB_N	6	S1-C31	S1-C31	L4	L10	3
TxRxC_P	7	S1-B33	S1-B33	L22	L16	5

TxRxC_N	8	S1-C33	S1-C33	L24	L18	4
TxRxD_P	10	S1-B35	S1-B35	L19	L13	8
TxRxD_N	11	S1-C35	S1-C35	L21	L15	7

1801

1802 For the ROD application (which is a Voltage Mode Phys Chip) the magnetics primary center
 1803 tap has a 100 nFd capacitor to ground and the secondary center tap has a “Bob Jones” 50
 1804 Ohm 1 nFd in series to ground. Note as currently layed out it looks like all 4 pairs are
 1805 inverted.

1806 **17.10 Document / Verify the IPMC’s RJ45 Ethernet Connection**

1807 The current IPMC mezzanine supports 10/100 Mb/s Ethernet using a National/Texas
 1808 DP83848C 10/100 Base-T Phys chip. This Phys chip has an old type Current Mode
 1809 transmitter connection to the magnetics. The Hub must include jumpers so that it can support
 1810 either the current IPMC or a future version of the IPMC with a 1000 Base-T Phys chip that
 1811 would use a Voltage Mode connection the magnetics primary. The IPMC pinout includes
 1812 pins for all 4 pairs in the standard contemporary Base-T Ethernet.

IPMC Mezzanine		Hub Magnetics and RJ45 for the IPMC			
IPMC Net Name	IPMC Pin No.	Hub IPMC Socket Pin No.	TRNS1 Magnetics		Front Panel RJ45 Pin No.
			Primary Pin No.	Secondary Pin No.	
Gb_A+ / Eth_Tx+	171	171	R1	R7	1
Gb_A- / Eth_Tx-	172	172	R3	R9	2
Gb_B+ / Eth_Rx+	174	174	R4	R10	3
Gb_B- / Eth_Rx-	175	175	R6	R12	6
Gb_C+	177	177	R24	R18	4
Gb_C-	178	178	R22	R16	5
Gb_D+	180	180	R21	R15	7
Gb_D-	181	181	R19	R13	8

1813

1814 For the IPMC application (which is currently a Current Mode Phys Chip but could be a
 1815 Voltage Mode Phys Chip in the future) the magnetics primary center tap has a 100 nFd
 1816 capacitor to ground and the primary center tap for circuits A (Tx) and B (Rx) also have a
 1817 0603 jumpers to the BULK_3V3 supply. All of the secondary center taps have a “Bob
 1818 Jones” 50 Ohm 1 nFd in series to ground.

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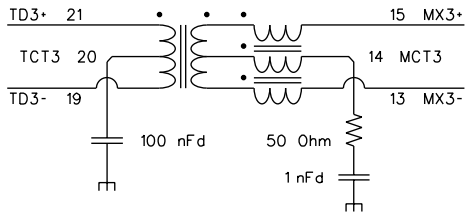
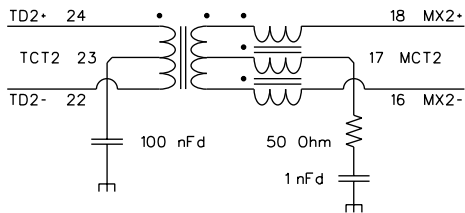
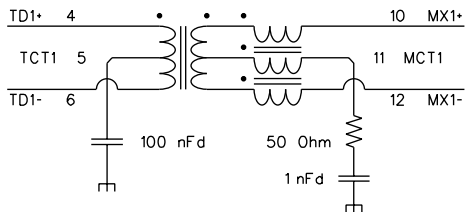
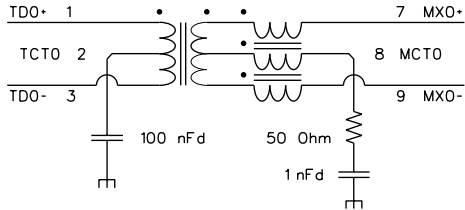
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1832

Ethernet Magnetics

Switch or Phys RJ-45 or Backplane



Magnetics
Pulse HX5201NL

Drw. 43

Front Panel RJ-45
AMP 1888653-4
Pin Assignments

Circuit	Pin
0+, DA+	1
0-, DA-	2
1+, DB+	3
1-, DB-	6
2+, DC+	4
2-, DC-	5
3+, DD+	7
3-, DD-	8

The Condo RJ-45 geometry has pin numbers that are correct for both sections (i.e. tabs up and down).

ATCA Backplane
Hub Slot Base Interface
Pin Assignments

Circuit	Pin
0+, DA+	A
0-, DA-	B
1+, DB+	C
1-, DB-	D
2+, DC+	E
2-, DC-	F
3+, DD+	G
3-, DD-	H

For a given Ethernet 4 pair connection routing may swap sections within one set of magnetics.

In a given section of magnetics routing may swap the Dir and Cmp pins just as long as this swap is made at both the input and output of that section.

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Figure 28: Circuit diagram for Hub Ethernet magnetics design.

1834 **18 Appendix 5: Hub Virtex FPGA MGT Transceiver Usage**

1835 A significant number of MGT Transceivers are used on the Hub Module’s Virtex FPGA.
 1836 The intent of this document is to describe in a single place all of the MGT Transceiver
 1837 connections to this FPGA. These connections are described in the text of this section, the
 1838 associated tables, and in **Figure 29**, **Figure 30**, and **Figure 31**. Notes:

- 1839 • The xcvu125_flvc2104 FPGA on the Hub Module contains 80 MGT Transceivers. 40
 1840 of these are GTY type transceivers and 40 of them are GTH type transceivers.
- 1841 • Both the GTY and GTH type transceivers are split across the two Super-Logic-Region
 1842 pieces of silicon in the xcvu125_flvc2104 FPGA. Half of each transceiver type is in each
 1843 of the two Super-Logic-Regions.
- 1844 • Note that MGT Reference Clocks can NOT be shared across Super-Logic-Regions.
- 1845 • All 80 of the MGT Receivers are used in the Hub Module design.
- 1846 • The specific MGT Receiver used for a given application has been selected on the
 1847 bases of providing the best PCB trace routing.
- 1848 • Only 30 of the MGT Transmitters are used in the Hub design.
- 1849 • Again PCB trace routing was the bases for selecting a given MGT Transmitter for a
 1850 specific application. In general this means that the MGT Transmitters with pins nearer
 1851 the perimeter were selected for use.
- 1852 •

1853 The following tables list only the MGT Transceiver inputs and outputs. The Reference
 1854 Clock inputs and the MGTAVTTRCAL_LC and MGTTRREF_LC pins are listed in a
 1855 separate table at the end of this section.

1856

Pin/Quad	Pin Name	I/O Type	Super Logic Reg.	Hub Module Net Connection
GTY Quad 133:				
A36	MGTYTXP3_133	GTY	1	'Comb_Data_to_Cap_to_FEX_08_Dir'
A37	MGTYTXN3_133	GTY	1	'Comb_Data_to_Cap_to_FEX_08_Cmp'
B38	MGTYTXP2_133	GTY	1	'Comb_Data_to_Cap_to_FEX_07_Dir'
B39	MGTYTXN2_133	GTY	1	'Comb_Data_to_Cap_to_FEX_07_Cmp'
C36	MGTYTXP1_133	GTY	1	
C37	MGTYTXN1_133	GTY	1	
D38	MGTYTXP0_133	GTY	1	
D39	MGTYTXN0_133	GTY	1	
A31	MGTYRXP3_133	GTY	1	'MGT_FO_CH_37_OUT_Hub_DIR'
A32	MGTYRXN3_133	GTY	1	'MGT_FO_CH_37_OUT_Hub_CMP'
B33	MGTYRXP2_133	GTY	1	'MGT_FO_CH_38_OUT_Hub_DIR'
B34	MGTYRXN2_133	GTY	1	'MGT_FO_CH_38_OUT_Hub_CMP'
C31	MGTYRXP1_133	GTY	1	'MGT_FO_CH_39_OUT_Hub_CMP'
C32	MGTYRXN1_133	GTY	1	'MGT_FO_CH_39_OUT_Hub_DIR'
D33	MGTYRXP0_133	GTY	1	'MGT_FO_CH_40_OUT_Hub_DIR'
D34	MGTYRXN0_133	GTY	1	'MGT_FO_CH_40_OUT_Hub_CMP'
GTY Quad 132:				

A40	MGTYTXP3_132	GTY	1	'Comb_Data_to_Cap_to_FEX_06_Dir'
A41	MGTYTXN3_132	GTY	1	'Comb_Data_to_Cap_to_FEX_06_Cmp'
C40	MGTYTXP2_132	GTY	1	
C41	MGTYTXN2_132	GTY	1	
E36	MGTYTXP1_132	GTY	1	
E37	MGTYTXN1_132	GTY	1	
E40	MGTYTXP0_132	GTY	1	
E41	MGTYTXN0_132	GTY	1	
B43	MGTYRXP3_132	GTY	1	'MGT_FO_CH_25_OUT_Hub_CMP'
B44	MGTYRXN3_132	GTY	1	'MGT_FO_CH_25_OUT_Hub_DIR'
C45	MGTYRXP2_132	GTY	1	'MGT_FO_CH_26_OUT_Hub_DIR'
C46	MGTYRXN2_132	GTY	1	'MGT_FO_CH_26_OUT_Hub_CMP'
D43	MGTYRXP1_132	GTY	1	'MGT_FO_CH_27_OUT_Hub_CMP'
D44	MGTYRXN1_132	GTY	1	'MGT_FO_CH_27_OUT_Hub_DIR'
E45	MGTYRXP0_132	GTY	1	'MGT_FO_CH_28_OUT_Hub_DIR'
E46	MGTYRXN0_132	GTY	1	'MGT_FO_CH_28_OUT_Hub_CMP'
GTY Quad 131:				
F34	MGTYTXP3_131	GTY	1	
F35	MGTYTXN3_131	GTY	1	
G36	MGTYTXP2_131	GTY	1	
G37	MGTYTXN2_131	GTY	1	
F38	MGTYTXP1_131	GTY	1	
F39	MGTYTXN1_131	GTY	1	
G40	MGTYTXP0_131	GTY	1	
G41	MGTYTXN0_131	GTY	1	
E31	MGTYRXP3_131	GTY	1	'MGT_FO_CH_35_OUT_Hub_CMP'
E32	MGTYRXN3_131	GTY	1	'MGT_FO_CH_35_OUT_Hub_DIR'
G31	MGTYRXP2_131	GTY	1	'MGT_FO_CH_36_OUT_Hub_DIR'
G32	MGTYRXN2_131	GTY	1	'MGT_FO_CH_36_OUT_Hub_CMP'
F43	MGTYRXP1_131	GTY	1	'MGT_FO_CH_29_OUT_Hub_CMP'
F44	MGTYRXN1_131	GTY	1	'MGT_FO_CH_29_OUT_Hub_DIR'
G45	MGTYRXP0_131	GTY	1	'MGT_FO_CH_30_OUT_Hub_DIR'
G46	MGTYRXN0_131	GTY	1	'MGT_FO_CH_30_OUT_Hub_CMP'
GTY Quad 130:				
H38	MGTYTXP3_130	GTY	1	
H39	MGTYTXN3_130	GTY	1	
J40	MGTYTXP2_130	GTY	1	'Comb_Data_to_Cap_to_FEX_05_Dir'
J41	MGTYTXN2_130	GTY	1	'Comb_Data_to_Cap_to_FEX_05_Cmp'
K38	MGTYTXP1_130	GTY	1	
K39	MGTYTXN1_130	GTY	1	
L40	MGTYTXP0_130	GTY	1	'Comb_Data_to_Cap_to_FEX_04_Dir'
L41	MGTYTXN0_130	GTY	1	'Comb_Data_to_Cap_to_FEX_04_Cmp'
H43	MGTYRXP3_130	GTY	1	'MGT_FO_CH_31_OUT_Hub_CMP'
H44	MGTYRXN3_130	GTY	1	'MGT_FO_CH_31_OUT_Hub_DIR'
J45	MGTYRXP2_130	GTY	1	'MGT_FO_CH_32_OUT_Hub_DIR'
J46	MGTYRXN2_130	GTY	1	'MGT_FO_CH_32_OUT_Hub_CMP'
K43	MGTYRXP1_130	GTY	1	'MGT_FO_CH_17_OUT_Hub_CMP'
K44	MGTYRXN1_130	GTY	1	'MGT_FO_CH_17_OUT_Hub_DIR'
L45	MGTYRXP0_130	GTY	1	'MGT_FO_CH_18_OUT_Hub_DIR'
L46	MGTYRXN0_130	GTY	1	'MGT_FO_CH_18_OUT_Hub_CMP'
GTY Quad 129:				

M38	MGTYTXP3_129	GTY	1	
M39	MGTYTXN3_129	GTY	1	
N40	MGTYTXP2_129	GTY	1	'Comb_Data_to_Cap_to_FEX_03_Dir'
N41	MGTYTXN2_129	GTY	1	'Comb_Data_to_Cap_to_FEX_03_Cmp'
P38	MGTYTXP1_129	GTY	1	
P39	MGTYTXN1_129	GTY	1	
R40	MGTYTXP0_129	GTY	1	'Comb_Data_to_Cap_to_Other_Hub_Dir'
R41	MGTYTXN0_129	GTY	1	'Comb_Data_to_Cap_to_Other_Hub_Cmp'
M43	MGTYRXP3_129	GTY	1	'MGT_FO_CH_19_OUT_Hub_CMP'
M44	MGTYRXN3_129	GTY	1	'MGT_FO_CH_19_OUT_Hub_DIR'
N45	MGTYRXP2_129	GTY	1	'MGT_FO_CH_20_OUT_Hub_DIR'
N46	MGTYRXN2_129	GTY	1	'MGT_FO_CH_20_OUT_Hub_CMP'
P43	MGTYRXP1_129	GTY	1	'MGT_FO_CH_21_OUT_Hub_CMP'
P44	MGTYRXN1_129	GTY	1	'MGT_FO_CH_21_OUT_Hub_DIR'
R45	MGTYRXP0_129	GTY	1	'MGT_FO_CH_22_OUT_Hub_DIR'
R46	MGTYRXN0_129	GTY	1	'MGT_FO_CH_22_OUT_Hub_CMP'
GTY Quad 128:				
T38	MGTYTXP3_128	GTY	0	
T39	MGTYTXN3_128	GTY	0	
U40	MGTYTXP2_128	GTY	0	
U41	MGTYTXN2_128	GTY	0	
V38	MGTYTXP1_128	GTY	0	
V39	MGTYTXN1_128	GTY	0	
W40	MGTYTXP0_128	GTY	0	
W41	MGTYTXN0_128	GTY	0	
T43	MGTYRXP3_128	GTY	0	'MGT_FO_CH_23_OUT_Hub_CMP'
T44	MGTYRXN3_128	GTY	0	'MGT_FO_CH_23_OUT_Hub_DIR'
U45	MGTYRXP2_128	GTY	0	'MGT_FO_CH_24_OUT_Hub_DIR'
U46	MGTYRXN2_128	GTY	0	'MGT_FO_CH_24_OUT_Hub_CMP'
V43	MGTYRXP1_128	GTY	0	'MGT_FO_CH_09_OUT_Hub_CMP'
V44	MGTYRXN1_128	GTY	0	'MGT_FO_CH_09_OUT_Hub_DIR'
W45	MGTYRXP0_128	GTY	0	'MGT_FO_CH_10_OUT_Hub_DIR'
W46	MGTYRXN0_128	GTY	0	'MGT_FO_CH_10_OUT_Hub_CMP'
GTY Quad 127:				
Y38	MGTYTXP3_127	GTY	0	
Y39	MGTYTXN3_127	GTY	0	
AA40	MGTYTXP2_127	GTY	0	'This_Hubs_RO_0_to_Cap_Other_ROD_Dir'
AA41	MGTYTXN2_127	GTY	0	'This_Hubs_RO_0_to_Cap_Other_ROD_Cmp'
AB38	MGTYTXP1_127	GTY	0	
AB39	MGTYTXN1_127	GTY	0	
AC40	MGTYTXP0_127	GTY	0	'This_Hubs_RO_1_to_Cap_Other_ROD_Cmp'
AC41	MGTYTXN0_127	GTY	0	'This_Hubs_RO_1_to_Cap_Other_ROD_Dir'
Y43	MGTYRXP3_127	GTY	0	'MGT_FO_CH_11_OUT_Hub_CMP'
Y44	MGTYRXN3_127	GTY	0	'MGT_FO_CH_11_OUT_Hub_DIR'
AA45	MGTYRXP2_127	GTY	0	'MGT_FO_CH_12_OUT_Hub_DIR'
AA46	MGTYRXN2_127	GTY	0	'MGT_FO_CH_12_OUT_Hub_CMP'
AB43	MGTYRXP1_127	GTY	0	'MGT_FO_CH_13_OUT_Hub_CMP'
AB44	MGTYRXN1_127	GTY	0	'MGT_FO_CH_13_OUT_Hub_DIR'
AC45	MGTYRXP0_127	GTY	0	'MGT_FO_CH_14_OUT_Hub_DIR'
AC46	MGTYRXN0_127	GTY	0	'MGT_FO_CH_14_OUT_Hub_CMP'
GTY Quad 126:				

AD38	MGTYTXP3_126	GTY	0	
AD39	MGTYTXN3_126	GTY	0	
AE40	MGTYTXP2_126	GTY	0	
AE41	MGTYTXN2_126	GTY	0	
AF38	MGTYTXP1_126	GTY	0	
AF39	MGTYTXN1_126	GTY	0	
AG40	MGTYTXP0_126	GTY	0	
AG41	MGTYTXN0_126	GTY	0	
AD43	MGTYRXP3_126	GTY	0	'MGT_FO_CH_15_OUT_Hub_CMP'
AD44	MGTYRXN3_126	GTY	0	'MGT_FO_CH_15_OUT_Hub_DIR'
AE45	MGTYRXP2_126	GTY	0	'MGT_FO_CH_16_OUT_Hub_DIR'
AE46	MGTYRXN2_126	GTY	0	'MGT_FO_CH_16_OUT_Hub_CMP'
AF43	MGTYRXP1_126	GTY	0	'MGT_FO_CH_01_OUT_Hub_CMP'
AF44	MGTYRXN1_126	GTY	0	'MGT_FO_CH_01_OUT_Hub_DIR'
AG45	MGTYRXP0_126	GTY	0	'MGT_FO_CH_02_OUT_Hub_DIR'
AG46	MGTYRXN0_126	GTY	0	'MGT_FO_CH_02_OUT_Hub_CMP'
GTY Quad 125:				
AH38	MGTYTXP3_125	GTY	0	
AH39	MGTYTXN3_125	GTY	0	
AJ40	MGTYTXP2_125	GTY	0	
AJ41	MGTYTXN2_125	GTY	0	
AK38	MGTYTXP1_125	GTY	0	
AK39	MGTYTXN1_125	GTY	0	
AL40	MGTYTXP0_125	GTY	0	
AL41	MGTYTXN0_125	GTY	0	
AH43	MGTYRXP3_125	GTY	0	'MGT_FO_CH_03_OUT_Hub_CMP'
AH44	MGTYRXN3_125	GTY	0	'MGT_FO_CH_03_OUT_Hub_DIR'
AJ45	MGTYRXP2_125	GTY	0	'MGT_FO_CH_04_OUT_Hub_DIR'
AJ46	MGTYRXN2_125	GTY	0	'MGT_FO_CH_04_OUT_Hub_CMP'
AK43	MGTYRXP1_125	GTY	0	'MGT_FO_CH_05_OUT_Hub_CMP'
AK44	MGTYRXN1_125	GTY	0	'MGT_FO_CH_05_OUT_Hub_DIR'
AL45	MGTYRXP0_125	GTY	0	'MGT_FO_CH_06_OUT_Hub_DIR'
AL46	MGTYRXN0_125	GTY	0	'MGT_FO_CH_06_OUT_Hub_CMP'
GTY Quad 124:				
AM38	MGTYTXP3_124	GTY	0	
AM39	MGTYTXN3_124	GTY	0	
AN40	MGTYTXP2_124	GTY	0	
AN41	MGTYTXN2_124	GTY	0	
AP38	MGTYTXP1_124	GTY	0	
AP39	MGTYTXN1_124	GTY	0	
AR40	MGTYTXP0_124	GTY	0	
AR41	MGTYTXN0_124	GTY	0	
AM43	MGTYRXP3_124	GTY	0	'MGT_FO_CH_07_OUT_Hub_CMP'
AM44	MGTYRXN3_124	GTY	0	'MGT_FO_CH_07_OUT_Hub_DIR'
AN45	MGTYRXP2_124	GTY	0	'MGT_FO_CH_08_OUT_Hub_DIR'
AN46	MGTYRXN2_124	GTY	0	'MGT_FO_CH_08_OUT_Hub_CMP'
AP43	MGTYRXP1_124	GTY	0	'Combined_Data_from_OTHER_Hub_Cmp'
AP44	MGTYRXN1_124	GTY	0	'Combined_Data_from_OTHER_Hub_Dir'
AR45	MGTYRXP0_124	GTY	0	'Rec_MP_Fiber_8_to_FPGA_Dir'
AR46	MGTYRXN0_124	GTY	0	'Rec_MP_Fiber_8_to_FPGA_Cmp'

1858

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Pin/Quad	Pin Name	I/O Type	Super Logic Reg.	Hub Module Net Connection
GTH Quad 233:				
A11	MGTHTXP3_233	GTH	1	'Comb_Data_to_Cap_to_FEX_09_Cmp'
A10	MGTHTXN3_233	GTH	1	'Comb_Data_to_Cap_to_FEX_09_Dir'
B9	MGTHTXP2_233	GTH	1	'Comb_Data_to_Cap_to_FEX_10_Cmp'
B8	MGTHTXN2_233	GTH	1	'Comb_Data_to_Cap_to_FEX_10_Dir'
C11	MGTHTXP1_233	GTH	1	
C10	MGTHTXN1_233	GTH	1	
D9	MGTHTXP0_233	GTH	1	
D8	MGTHTXN0_233	GTH	1	
A16	MGTHRXP3_233	GTH	1	'MGT_FO_CH_48_OUT_Hub_DIR'
A15	MGTHRXN3_233	GTH	1	'MGT_FO_CH_48_OUT_Hub_CMP'
B14	MGTHRXP2_233	GTH	1	'MGT_FO_CH_47_OUT_Hub_DIR'
B13	MGTHRXN2_233	GTH	1	'MGT_FO_CH_47_OUT_Hub_CMP'
C16	MGTHRXP1_233	GTH	1	'MGT_FO_CH_46_OUT_Hub_CMP'
C15	MGTHRXN1_233	GTH	1	'MGT_FO_CH_46_OUT_Hub_DIR'
D14	MGTHRXP0_233	GTH	1	'MGT_FO_CH_45_OUT_Hub_DIR'
D13	MGTHRXN0_233	GTH	1	'MGT_FO_CH_45_OUT_Hub_CMP'
GTH Quad 232:				
A7	MGTHTXP3_232	GTH	1	'Comb_Data_to_Cap_to_FEX_11_Cmp'
A6	MGTHTXN3_232	GTH	1	'Comb_Data_to_Cap_to_FEX_11_Dir'
C7	MGTHTXP2_232	GTH	1	
C6	MGTHTXN2_232	GTH	1	
E11	MGTHTXP1_232	GTH	1	
E10	MGTHTXN1_232	GTH	1	
E7	MGTHTXP0_232	GTH	1	
E6	MGTHTXN0_232	GTH	1	
B4	MGTHRXP3_232	GTH	1	'MGT_FO_CH_44_OUT_Hub_CMP'
B3	MGTHRXN3_232	GTH	1	'MGT_FO_CH_44_OUT_Hub_DIR'
C2	MGTHRXP2_232	GTH	1	'MGT_FO_CH_43_OUT_Hub_DIR'
C1	MGTHRXN2_232	GTH	1	'MGT_FO_CH_43_OUT_Hub_CMP'
D4	MGTHRXP1_232	GTH	1	'MGT_FO_CH_42_OUT_Hub_CMP'
D3	MGTHRXN1_232	GTH	1	'MGT_FO_CH_42_OUT_Hub_DIR'
E2	MGTHRXP0_232	GTH	1	'MGT_FO_CH_41_OUT_Hub_DIR'
E1	MGTHRXN0_232	GTH	1	'MGT_FO_CH_41_OUT_Hub_CMP'
GTH Quad 231:				
F13	MGTHTXP3_231	GTH	1	
F12	MGTHTXN3_231	GTH	1	
G11	MGTHTXP2_231	GTH	1	
G10	MGTHTXN2_231	GTH	1	
F9	MGTHTXP1_231	GTH	1	
F8	MGTHTXN1_231	GTH	1	
G7	MGTHTXP0_231	GTH	1	
G6	MGTHTXN0_231	GTH	1	
E16	MGTHRXP3_231	GTH	1	'MGT_FO_CH_34_OUT_Hub_CMP'

E15	MGTHRXN3_231	GTH	1	'MGT_FO_CH_34_OUT_Hub_DIR'
G16	MGTHRXP2_231	GTH	1	'MGT_FO_CH_33_OUT_Hub_DIR'
G15	MGTHRXN2_231	GTH	1	'MGT_FO_CH_33_OUT_Hub_CMP'
F4	MGTHRXP1_231	GTH	1	'MGT_FO_CH_56_OUT_Hub_CMP'
F3	MGTHRXN1_231	GTH	1	'MGT_FO_CH_56_OUT_Hub_DIR'
G2	MGTHRXP0_231	GTH	1	'MGT_FO_CH_55_OUT_Hub_DIR'
G1	MGTHRXN0_231	GTH	1	'MGT_FO_CH_55_OUT_Hub_CMP'
GTH Quad 230:				
H9	MGHTXP3_230	GTH	1	
H8	MGHTXN3_230	GTH	1	
J7	MGHTXP2_230	GTH	1	'Comb_Data_to_Cap_to_FEX_12_Cmp'
J6	MGHTXN2_230	GTH	1	'Comb_Data_to_Cap_to_FEX_12_Dir'
K9	MGHTXP1_230	GTH	1	
K8	MGHTXN1_230	GTH	1	
L7	MGHTXP0_230	GTH	1	'Comb_Data_to_Cap_to_FEX_13_Cmp'
L6	MGHTXN0_230	GTH	1	'Comb_Data_to_Cap_to_FEX_13_Dir'
H4	MGTHRXP3_230	GTH	1	'MGT_FO_CH_54_OUT_Hub_CMP'
H3	MGTHRXN3_230	GTH	1	'MGT_FO_CH_54_OUT_Hub_DIR'
J2	MGTHRXP2_230	GTH	1	'MGT_FO_CH_53_OUT_Hub_DIR'
J1	MGTHRXN2_230	GTH	1	'MGT_FO_CH_53_OUT_Hub_CMP'
K4	MGTHRXP1_230	GTH	1	'MGT_FO_CH_52_OUT_Hub_CMP'
K3	MGTHRXN1_230	GTH	1	'MGT_FO_CH_52_OUT_Hub_DIR'
L2	MGTHRXP0_230	GTH	1	'MGT_FO_CH_51_OUT_Hub_DIR'
L1	MGTHRXN0_230	GTH	1	'MGT_FO_CH_51_OUT_Hub_CMP'
GTH Quad 229:				
M9	MGHTXP3_229	GTH	1	
M8	MGHTXN3_229	GTH	1	
N7	MGHTXP2_229	GTH	1	'Comb_Data_to_Cap_to_FEX_14_Cmp'
N6	MGHTXN2_229	GTH	1	'Comb_Data_to_Cap_to_FEX_14_Dir'
P9	MGHTXP1_229	GTH	1	
P8	MGHTXN1_229	GTH	1	
R7	MGHTXP0_229	GTH	1	'This_Hubs_RO_0_to_Cap_Its_ROD_Dir'
R6	MGHTXN0_229	GTH	1	'This_Hubs_RO_0_to_Cap_Its_ROD_Cmp'
M4	MGTHRXP3_229	GTH	1	'MGT_FO_CH_50_OUT_Hub_CMP'
M3	MGTHRXN3_229	GTH	1	'MGT_FO_CH_50_OUT_Hub_DIR'
N2	MGTHRXP2_229	GTH	1	'MGT_FO_CH_49_OUT_Hub_DIR'
N1	MGTHRXN2_229	GTH	1	'MGT_FO_CH_49_OUT_Hub_CMP'
P4	MGTHRXP1_229	GTH	1	'MGT_FO_CH_64_OUT_Hub_CMP'
P3	MGTHRXN1_229	GTH	1	'MGT_FO_CH_64_OUT_Hub_DIR'
R2	MGTHRXP0_229	GTH	1	'MGT_FO_CH_63_OUT_Hub_DIR'
R1	MGTHRXN0_229	GTH	1	'MGT_FO_CH_63_OUT_Hub_CMP'
GTH Quad 228:				
T9	MGHTXP3_228	GTH	0	
T8	MGHTXN3_228	GTH	0	
U7	MGHTXP2_228	GTH	0	'This_Hubs_RO_1_to_Cap_Its_ROD_Dir'
U6	MGHTXN2_228	GTH	0	'This_Hubs_RO_1_to_Cap_Its_ROD_Cmp'
V9	MGHTXP1_228	GTH	0	
V8	MGHTXN1_228	GTH	0	
W7	MGHTXP0_228	GTH	0	'Comb_Data_to_Cap_to_ROD_Dir'
W6	MGHTXN0_228	GTH	0	'Comb_Data_to_Cap_to_ROD_Cmp'
T4	MGTHRXP3_228	GTH	0	'MGT_FO_CH_62_OUT_Hub_CMP'

T3	MGTHRXN3_228	GTH	0	'MGT_FO_CH_62_OUT_Hub_DIR'
U2	MGTHRXP2_228	GTH	0	'MGT_FO_CH_61_OUT_Hub_DIR'
U1	MGTHRXN2_228	GTH	0	'MGT_FO_CH_61_OUT_Hub_CMP'
V4	MGTHRXP1_228	GTH	0	'MGT_FO_CH_60_OUT_Hub_CMP'
V3	MGTHRXN1_228	GTH	0	'MGT_FO_CH_60_OUT_Hub_DIR'
W2	MGTHRXP0_228	GTH	0	'MGT_FO_CH_59_OUT_Hub_DIR'
W1	MGTHRXN0_228	GTH	0	'MGT_FO_CH_59_OUT_Hub_CMP'
GTH Quad 227:				
Y9	MGTHTXP3_227	GTH	0	
Y8	MGTHTXN3_227	GTH	0	
AA7	MGTHTXP2_227	GTH	0	'MiniPOD_Trans_Fiber_0_Data_Cmp'
AA6	MGTHTXN2_227	GTH	0	'MiniPOD_Trans_Fiber_0_Data_Dir'
AB9	MGTHTXP1_227	GTH	0	
AB8	MGTHTXN1_227	GTH	0	
AC7	MGTHTXP0_227	GTH	0	'MiniPOD_Trans_Fiber_1_Data_Cmp'
AC6	MGTHTXN0_227	GTH	0	'MiniPOD_Trans_Fiber_1_Data_Dir'
Y4	MGTHRXP3_227	GTH	0	'MGT_FO_CH_58_OUT_Hub_CMP'
Y3	MGTHRXN3_227	GTH	0	'MGT_FO_CH_58_OUT_Hub_DIR'
AA2	MGTHRXP2_227	GTH	0	'MGT_FO_CH_57_OUT_Hub_DIR'
AA1	MGTHRXN2_227	GTH	0	'MGT_FO_CH_57_OUT_Hub_CMP'
AB4	MGTHRXP1_227	GTH	0	'MGT_FO_CH_74_OUT_Hub_CMP'
AB3	MGTHRXN1_227	GTH	0	'MGT_FO_CH_74_OUT_Hub_DIR'
AC2	MGTHRXP0_227	GTH	0	'MGT_FO_CH_73_OUT_Hub_DIR'
AC1	MGTHRXN0_227	GTH	0	'MGT_FO_CH_73_OUT_Hub_CMP'
GTH Quad 226:				
AD9	MGTHTXP3_226	GTH	0	
AD8	MGTHTXN3_226	GTH	0	
AE7	MGTHTXP2_226	GTH	0	'MiniPOD_Trans_Fiber_2_Data_Cmp'
AE6	MGTHTXN2_226	GTH	0	'MiniPOD_Trans_Fiber_2_Data_Dir'
AF9	MGTHTXP1_226	GTH	0	
AF8	MGTHTXN1_226	GTH	0	
AG7	MGTHTXP0_226	GTH	0	'MiniPOD_Trans_Fiber_4_Data_Cmp'
AG6	MGTHTXN0_226	GTH	0	'MiniPOD_Trans_Fiber_4_Data_Dir'
AD4	MGTHRXP3_226	GTH	0	'MGT_FO_CH_72_OUT_Hub_CMP'
AD3	MGTHRXN3_226	GTH	0	'MGT_FO_CH_72_OUT_Hub_DIR'
AE2	MGTHRXP2_226	GTH	0	'MGT_FO_CH_71_OUT_Hub_DIR'
AE1	MGTHRXN2_226	GTH	0	'MGT_FO_CH_71_OUT_Hub_CMP'
AF4	MGTHRXP1_226	GTH	0	'MGT_FO_CH_70_OUT_Hub_CMP'
AF3	MGTHRXN1_226	GTH	0	'MGT_FO_CH_70_OUT_Hub_DIR'
AG2	MGTHRXP0_226	GTH	0	'MGT_FO_CH_69_OUT_Hub_DIR'
AG1	MGTHRXN0_226	GTH	0	'MGT_FO_CH_69_OUT_Hub_CMP'
GTH Quad 225:				
AH9	MGTHTXP3_225	GTH	0	
AH8	MGTHTXN3_225	GTH	0	
AJ7	MGTHTXP2_225	GTH	0	'MiniPOD_Trans_Fiber_6_Data_Cmp'
AJ6	MGTHTXN2_225	GTH	0	'MiniPOD_Trans_Fiber_6_Data_Dir'
AK9	MGTHTXP1_225	GTH	0	
AK8	MGTHTXN1_225	GTH	0	
AL7	MGTHTXP0_225	GTH	0	'MiniPOD_Trans_Fiber_8_Data_Cmp'
AL6	MGTHTXN0_225	GTH	0	'MiniPOD_Trans_Fiber_8_Data_Dir'
AH4	MGTHRXP3_225	GTH	0	'MGT_FO_CH_68_OUT_Hub_CMP'

AH3	MGTHRXN3_225	GTH	0	'MGT_FO_CH_68_OUT_Hub_DIR'
AJ2	MGTHRXP2_225	GTH	0	'MGT_FO_CH_67_OUT_Hub_DIR'
AJ1	MGTHRXN2_225	GTH	0	'MGT_FO_CH_67_OUT_Hub_CMP'
AK4	MGTHRXP1_225	GTH	0	'MGT_FO_CH_66_OUT_Hub_CMP'
AK3	MGTHRXN1_225	GTH	0	'MGT_FO_CH_66_OUT_Hub_DIR'
AL2	MGTHRXP0_225	GTH	0	'MGT_FO_CH_65_OUT_Hub_DIR'
AL1	MGTHRXN0_225	GTH	0	'MGT_FO_CH_65_OUT_Hub_CMP'
GTH Quad 224:				
AM9	MGHTXP3_224	GTH	0	'MiniPOD_Trans_Fiber_10_Data_Cmp' 'MiniPOD_Trans_Fiber_10_Data_Dir' 'MiniPOD_Trans_Fiber_11_Data_Cmp' 'MiniPOD_Trans_Fiber_11_Data_Dir' 'This_RODs_Readout_Ctrl_to_GTH_Input_Cmp' 'This_RODs_Readout_Ctrl_to_GTH_Input_Dir' 'Rec_MP_Fiber_2_to_FPGA_Dir' 'Rec_MP_Fiber_2_to_FPGA_Cmp' 'Rec_MP_Fiber_4_to_FPGA_Dir' 'Rec_MP_Fiber_4_to_FPGA_Cmp' 'Rec_MP_Fiber_6_to_FPGA_Dir' 'Rec_MP_Fiber_6_to_FPGA_Cmp'
AM8	MGHTXN3_224	GTH	0	
AN7	MGHTXP2_224	GTH	0	
AN6	MGHTXN2_224	GTH	0	
AP9	MGHTXP1_224	GTH	0	
AP8	MGHTXN1_224	GTH	0	
AR7	MGHTXP0_224	GTH	0	
AR6	MGHTXN0_224	GTH	0	
AM4	MGTHRXP3_224	GTH	0	
AM3	MGTHRXN3_224	GTH	0	
AN2	MGTHRXP2_224	GTH	0	
AN1	MGTHRXN2_224	GTH	0	
AP4	MGTHRXP1_224	GTH	0	
AP3	MGTHRXN1_224	GTH	0	
AR2	MGTHRXP0_224	GTH	0	
AR1	MGTHRXN0_224	GTH	0	

1860

1861 Now we list the Reference Clock inputs and the MGTAVTTRCAL_LC and
 1862 MGTRREF_LC pin connections. All Quads that have MGTAVTTRCAL_LC and
 1863 MGTRREF_LC pins have the appropriate resistors and supplies connected to them. In this
 1864 file I'm just listing the reference designators of the MGT Termination Calibration Resistors.

1865

Pin/Quad	Pin Name	I/O Type	Super Logic Reg.	Hub Module Net Connection
GTY Quad 133:				
H34	MGTREFCLK1P_133	GTY	1	
H35	MGTREFCLK1N_133	GTY	1	
J36	MGTREFCLK0P_133	GTY	1	
J37	MGTREFCLK0N_133	GTY	1	
GTY Quad 132:				
K34	MGTREFCLK1P_132	GTY	1	'MHZ_320.64_COPY_2_DIR' 'MHZ_320.64_COPY_2_CMP'
K35	MGTREFCLK1N_132	GTY	1	
L36	MGTREFCLK0P_132	GTY	1	
L37	MGTREFCLK0N_132	GTY	1	
GTY Quad 131:				
M34	MGTREFCLK1P_131	GTY	1	
M35	MGTREFCLK1N_131	GTY	1	
N36	MGTREFCLK0P_131	GTY	1	

N37	MGTREFCLK0N_131	GTY	1		
GTY Quad 130:					
P34	MGTREFCLK1P_130	GTY	1	'MHZ_320.64_COPY_1_DIR' 'MHZ_320.64_COPY_1_CMP' R114 R114	
P35	MGTREFCLK1N_130	GTY	1		
R36	MGTREFCLK0P_130	GTY	1		
R37	MGTREFCLK0N_130	GTY	1		
D40	MGTAVTTRCAL_LN	NA	NA		
D41	MGTRREF_LN	NA	NA		
GTY Quad 129:					
T34	MGTREFCLK1P_129	GTY	1		
T35	MGTREFCLK1N_129	GTY	1		
U36	MGTREFCLK0P_129	GTY	1		
U37	MGTREFCLK0N_129	GTY	1		
GTY Quad 128:					
V34	MGTREFCLK1P_128	GTY	0		
V35	MGTREFCLK1N_128	GTY	0		
W36	MGTREFCLK0P_128	GTY	0		
W37	MGTREFCLK0N_128	GTY	0		
GTY Quad 127:					
Y34	MGTREFCLK1P_127	GTY	0	'MHZ_320.64_COPY_3_DIR' 'MHZ_320.64_COPY_3_CMP'	
Y35	MGTREFCLK1N_127	GTY	0		
AA36	MGTREFCLK0P_127	GTY	0		
AA37	MGTREFCLK0N_127	GTY	0		
GTY Quad 126:					
AB34	MGTREFCLK1P_126	GTY	0		
AB35	MGTREFCLK1N_126	GTY	0		
AC36	MGTREFCLK0P_126	GTY	0		
AC37	MGTREFCLK0N_126	GTY	0		
GTY Quad 125:					
AE36	MGTREFCLK0P_125	GTY	0	'MHZ_320.64_COPY_0_DIR' 'MHZ_320.64_COPY_0_CMP' R113 R113	
AE37	MGTREFCLK0N_125	GTY	0		
AD34	MGTREFCLK1P_125	GTY	0		
AD35	MGTREFCLK1N_125	GTY	0		
AH40	MGTAVTTRCAL_LC	NA	NA		
AH41	MGTRREF_LC	NA	NA		
GTY Quad 124:					
AF34	MGTREFCLK1P_124	GTY	0		
AF35	MGTREFCLK1N_124	GTY	0		
AG36	MGTREFCLK0P_124	GTY	0		
AG37	MGTREFCLK0N_124	GTY	0		

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Pin/Quad	Pin Name	I/O Type	Super Logic Reg.	Hub Module Net Connection
GTH Quad 233:				
H13	MGTREFCLK1P_233	GTH	1	
H12	MGTREFCLK1N_233	GTH	1	
J11	MGTREFCLK0P_233	GTH	1	
J10	MGTREFCLK0N_233	GTH	1	
GTH Quad 232:				
K13	MGTREFCLK1P_232	GTH	1	'MHZ_320.64_COPY_7_DIR'
K12	MGTREFCLK1N_232	GTH	1	'MHZ_320.64_COPY_7_CMP'
L11	MGTREFCLK0P_232	GTH	1	
L10	MGTREFCLK0N_232	GTH	1	
GTH Quad 231:				
M13	MGTREFCLK1P_231	GTH	1	
M12	MGTREFCLK1N_231	GTH	1	
N11	MGTREFCLK0P_231	GTH	1	
N10	MGTREFCLK0N_231	GTH	1	
D6	MGTREF_RN	NA	NA	R116
D7	MGTAVTTRCAL_RN	NA	NA	R116
GTH Quad 230:				
P13	MGTREFCLK1P_230	GTH	1	
P12	MGTREFCLK1N_230	GTH	1	
R11	MGTREFCLK0P_230	GTH	1	'MHZ_320.64_COPY_8_DIR'
R10	MGTREFCLK0N_230	GTH	1	'MHZ_320.64_COPY_8_CMP'
GTH Quad 229:				
T13	MGTREFCLK1P_229	GTH	1	
T12	MGTREFCLK1N_229	GTH	1	
U11	MGTREFCLK0P_229	GTH	1	
U10	MGTREFCLK0N_229	GTH	1	
GTH Quad 228:				
V13	MGTREFCLK1P_228	GTH	0	
V12	MGTREFCLK1N_228	GTH	0	
W11	MGTREFCLK0P_228	GTH	0	
W10	MGTREFCLK0N_228	GTH	0	
GTH Quad 227:				
Y13	MGTREFCLK1P_227	GTH	0	'MHZ_320.64_COPY_6_DIR'
Y12	MGTREFCLK1N_227	GTH	0	'MHZ_320.64_COPY_6_CMP'
AA11	MGTREFCLK0P_227	GTH	0	
AA10	MGTREFCLK0N_227	GTH	0	
GTH Quad 226:				
AB13	MGTREFCLK1P_226	GTH	0	
AB12	MGTREFCLK1N_226	GTH	0	
AC11	MGTREFCLK0P_226	GTH	0	
AC10	MGTREFCLK0N_226	GTH	0	
AH6	MGTREF_RC	NA	NA	R115

AH7	MGTAVTTRCAL_RC	NA	NA	R115
GTH Quad 225:				
AD13	MGTREFCLK1P_225	GTH	0	
AD12	MGTREFCLK1N_225	GTH	0	
AE11	MGTREFCLK0P_225	GTH	0	'MHZ_320.64_COPY_9_DIR'
AE10	MGTREFCLK0N_225	GTH	0	'MHZ_320.64_COPY_9_CMP'
GTH Quad 224:				
AF13	MGTREFCLK1P_224	GTH	0	
AF12	MGTREFCLK1N_224	GTH	0	
AG11	MGTREFCLK0P_224	GTH	0	
AG10	MGTREFCLK0N_224	GTH	0	

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Hub - GTY Transceivers - QUADs 124:133

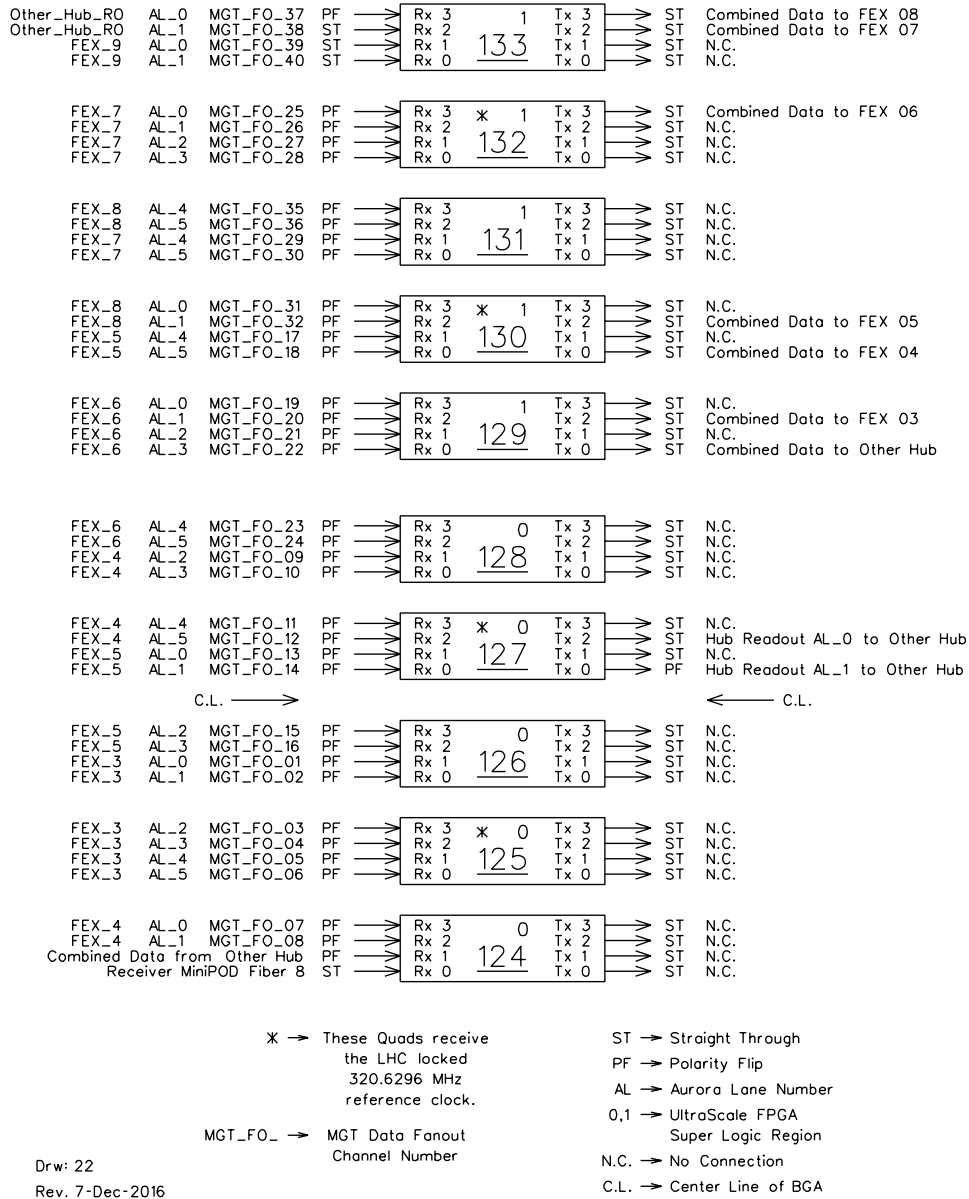
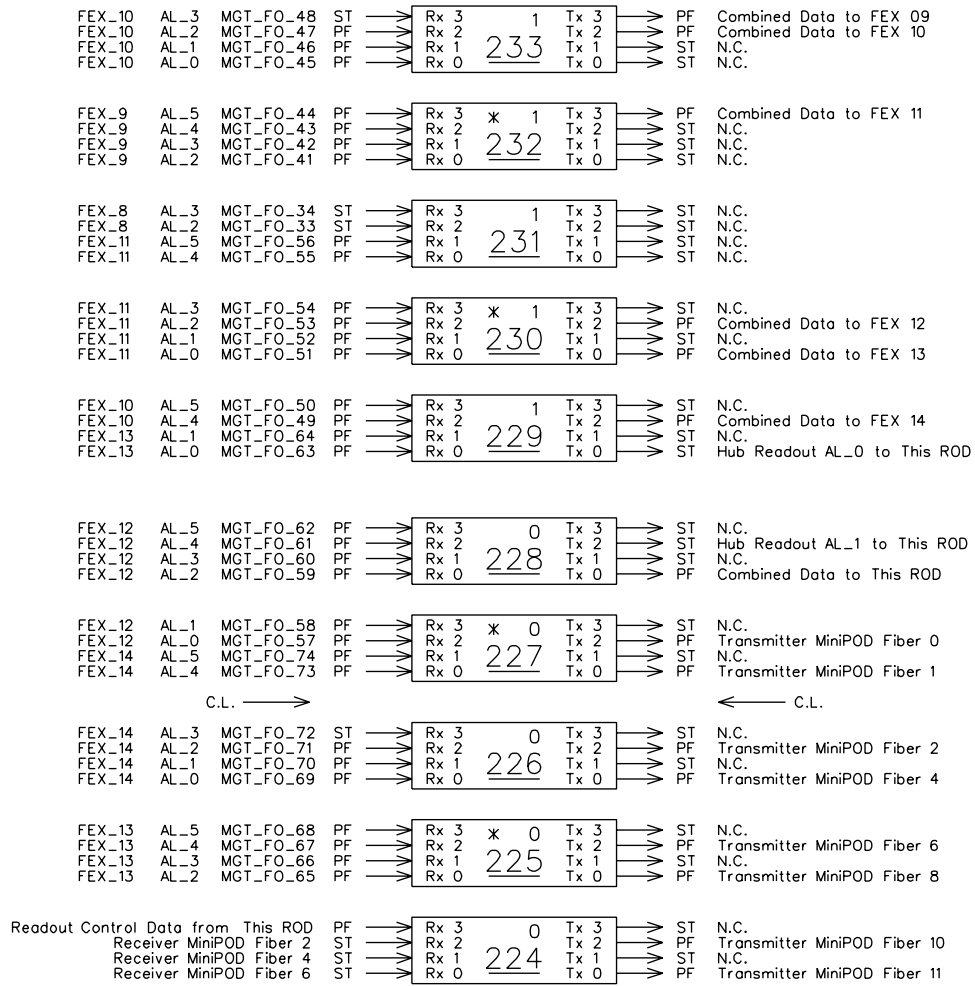


Figure 29: Hub GTY Transceiver Quad Assignments

Hub - GTH Transceivers - QUADs 224:233



* → These Quads receive the LHC locked 320.6296 MHz reference clock.

MGT_FO_ → MGT Data Fanout Channel Number

ST → Straight Through
 PF → Polarity Flip
 AL → Aurora Lane Number
 0,1 → UltraScale FPGA Super Logic Region
 N.C. → No Connection
 C.L. → Center Line of BGA

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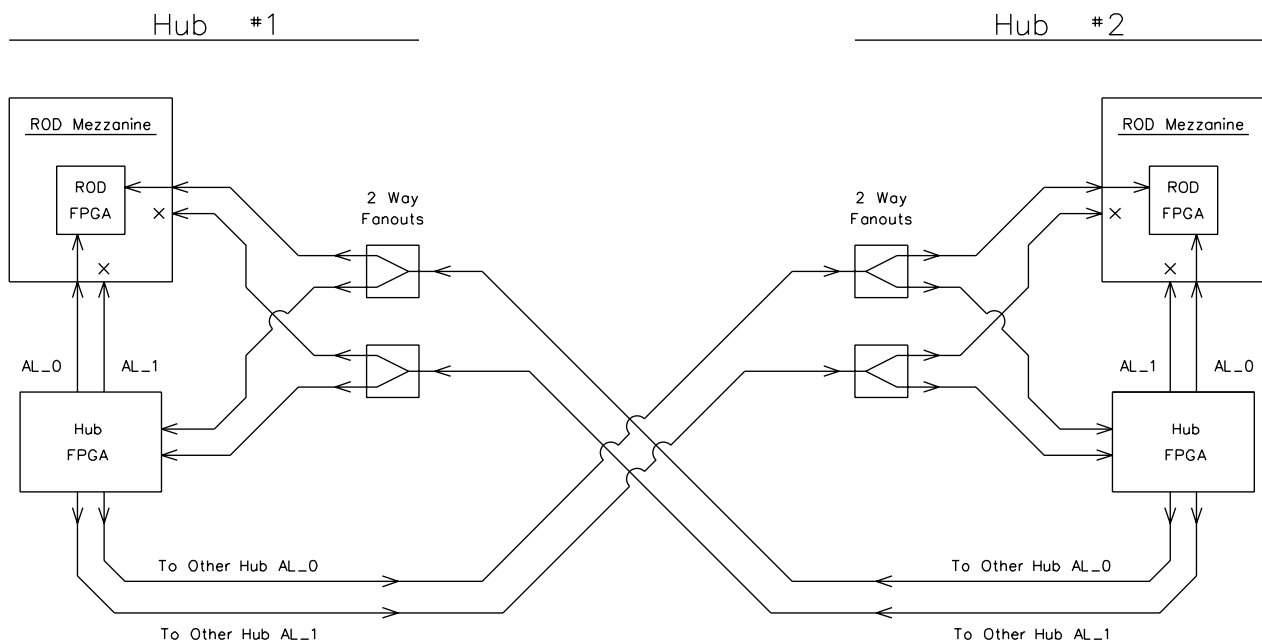
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Figure 30: Hub GTH Transceiver Quad assignments.

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Hub Readout Data Connections



The lines in this drawing show the flow of Hub Readout Data both within a Hub card and between the two Hub cards.

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Figure 31: Hub Readout Data Connections.

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1891 **19 Appendix 6: Hub Virtex FPGA Select I/O Usage**

1892 A significant number of Select I/O signals are used on the Hub Module’s UltraScale Virtex
 1893 FPGA. The intent of this document is to list in a single place all of the Select I/O lines that
 1894 are used on the Hub FPGA. About 183 Select I/O pins are connected in the Hub design.

1895 Notes:

- 1896 • Currently all Select I/O connections to the Hub FPGA are made to Banks: 65, 67, 68, 70,
 1897 71, 72, 84, and 94.
- 1898 • Bank 65 is used for Configuration of the FPGA from FLASH memory - Master BPI mode
 1899 Configuration. Currently none of the Bank 65 Select I/O pins are used after
 1900 Configuration except for the two pins that allow I2C slave access to the FPGA’s System
 1901 Monitor.
- 1902 • Banks 84 and 94 are operated with a Vcco of 3V3. The Select I/O lines from Banks 84
 1903 and 94 are used for all of the 3V3 logic connections to the Hub Virtex FPGA.
- 1904 • The only signals that are routed to Select I/O Banks 70, 71, 72 are:
 1905 • the 13 Equalizer Enable signals that control the MGT Fanout equalizers (these are
 1906 static low current output lines with non-critical routing),
 1907 • the 2 PLL Lock-Detect inputs to the FPGA which should be static during normal
 1908 operation,
 1909 • the 1 “clock select” signal that controls whether or not the 40.08 MHz reference clock
 1910 outputs in Zone 2 are active or not. This is a static low current output,
 1911 • and 3 differential clock signals inputs that use Bank 71 because it is adjacent to the
 1912 clock generation chips. Bank 71 is of the HP type and is on SLR #1. These clock
 1913 signals are the 40.08 MHz Logic Clock, the 320.64 MHz Logic Clock, and the 40.08
 1914 MHz Reference Clock from the Other Hub Module.
- 1915 • Currently there are no connections to Bank 66. The reason for this is to facilitate routing
 1916 access for required configuration signals to the very deep rings on Bank 65. These
 1917 configuration signals need to go 14 or 15 rings in. Except for this - Bank 66 is perfectly
 1918 usable HP type Select I/O signals. Bank 66 does have Vcco power.
- 1919 • All banks that must handle high speed Select I/O signals have their VRP and VREF
 1920 pins connected to the appropriate resistors. I have listed the reference designators of the
 1921 resistors associated with these pins (instead of listing a not interesting net name).
- 1922 • All of the Select I/O Banks that we are using in the Hub design come from Super Logic
 1923 Region #0 in the XCVU125 stacked silicon FPGA, except for Banks 70, 71, and 72 which
 1924 are part of Super Logic Region #1.

1925

Bank 65:	1V8 I/O HP SLR #0	44 Hub Connections
BE20	IO L24P T3U N10 EMCCLK 65	'NO_CONN_FPGA_BANK_65_BE20'
BF20	IO L24N T3U N11 DOUT CSO B 65	'NO_CONN_FPGA_BANK_65_BF20'
BD20	IO T3U N12 PERSTN0 65	'NO_CONN_FPGA_BANK_65_BD20'
BE16	IO L23P T3U N8 I2C_SCLK 65	'HUB_I2C_TO_FPGA_SCL'
BF16	IO L23N T3U N9 I2C_SDA 65	'HUB_I2C_TO_FPGA_SDA'
BE19	IO L22P T3U N6 DBC_AD0P_D04 65	'FLASH_D04'
BF19	IO L22N T3U N7 DBC_AD0N_D05 65	'FLASH_D05'
BD18	IO L21P T3L N4 AD8P_D06 65	'FLASH_D06'
BE18	IO L21N T3L N5 AD8N_D07 65	'FLASH_D07'
BE17	IO L20P T3L N2 AD1P_D08 65	'FLASH_D08'
BF17	IO L20N T3L N3 AD1N_D09 65	'FLASH_D09'

BD17	IO L19P T3L N0 DBC AD9P D10 65	'FLASH D10'
BD16	IO L19N T3L N1 DBC AD9N D11 65	'FLASH D11'
BC20	IO L18P T2U N10 AD2P D12 65	'FLASH D12'
BC19	IO L18N T2U N11 AD2N D13 65	'FLASH D13'
BA19	IO L17P T2U N8 AD10P D14 65	'FLASH D14'
BB19	IO L17N T2U N9 AD10N D15 65	'FLASH D15'
BA21	IO L16P T2U N6 QBC AD3P A00 D16 65	'FLASH A00'
BB21	IO L16N T2U N7 QBC AD3N A01 D17 65	'FLASH A01'
BB18	IO L15P T2L N4 AD11P A02 D18 65	'FLASH A02'
BC18	IO L15N T2L N5 AD11N A03 D19 65	'FLASH A03'
AY20	IO L14P T2L N2 GC A04 D20 65	'FLASH A04'
BA20	IO L14N T2L N3 GC A05 D21 65	'FLASH A05'
BC21	IO T2U N12 CSI ADV B 65	'NO_CONN_FPGA_BANK_65_BC21'
AY19	IO L13P T2L N0 GC QBC A06 D22 65	'FLASH A06'
AY18	IO L13N T2L N1 GC QBC A07 D23 65	'FLASH A07'
AV20	IO L12P T1U N10 GC A08 D24 65	'FLASH A08'
AW20	IO L12N T1U N11 GC A09 D25 65	'FLASH A09'
AV19	IO T1U N12 PERSTN1 65	'NO_CONN_FPGA_BANK_65_AV19'
AW18	IO L11P T1U N8 GC A10 D26 65	'FLASH A10'
AW17	IO L11N T1U N9 GC A11 D27 65	'FLASH A11'
AV21	IO L10P T1U N6 QBC AD4P A12 D28 65	'FLASH A12'
AW21	IO L10N T1U N7 QBC AD4N A13 D29 65	'FLASH A13'
AU18	IO L9P T1L N4 AD12P A14 D30 65	'FLASH A14'
AV18	IO L9N T1L N5 AD12N A15 D31 65	'FLASH A15'
AT21	IO L8P T1L N2 AD5P A16 65	'FLASH A16'
AU21	IO L8N T1L N3 AD5N A17 65	'FLASH A17'
AT19	IO L7P T1L N0 QBC AD13P A18 65	'FLASH A18'
AU19	IO L7N T1L N1 QBC AD13N A19 65	'FLASH A19'
AR20	IO L6P T0U N10 AD6P A20 65	'FLASH A20'
AT20	IO L6N T0U N11 AD6N A21 65	'FLASH A21'
AR19	IO L5P T0U N8 AD14P A22 65	'FLASH A22'
AR18	IO L5N T0U N9 AD14N A23 65	'FLASH A23'
AM21	IO L4P T0U N6 DBC AD7P A24 65	'FLASH A24'
AN21	IO L4N T0U N7 DBC AD7N A25 65	'FLASH A25'
AM19	IO L3P T0L N4 AD15P A26 65	'NO_CONN_FPGA_BANK_65_AM19'
AN19	IO L3N T0L N5 AD15N A27 65	'NO_CONN_FPGA_BANK_65_AN19'
AN20	IO L2P T0L N2 FOE B 65	'FLASH_OUTPUT_ENB_B'
AP20	IO L2N T0L N3 FWE FCS2 B 65	'FLASH_WRITE_ENB_B'
AP21	IO T0U N12 VRP A28 65	R101
AN18	IO L1P T0L N0 DBC RS0 65	'NO_CONN_FPGA_BANK_65_AN18'
AP18	IO L1N T0L N1 DBC RS1 65	'NO_CONN_FPGA_BANK_65_AP18'
AM18	VREF 65	R106

This is a complete list of all pins in Bank 65 including 9 No_Conn_spare unused pins.

Bank 66: 1V8 I/O HP SLR #0

2 Hub Connections

Except for the resistor pins no pins in Bank 66 are currently in use - all are "No_Conn_" spare not connected pins.

AM27 IO T0U N12 VRP 66

R102

AM22 VREF_66

R107

Bank 67: 1V8 I/O HP SLR #0

27 Hub Connections

BE25	IO L23P T3U N8 67	'OVERALL ADRS 1 TO RES NET'
BF25	IO L23N T3U N9 67	'OVERALL ADRS 0 TO RES NET'
BE27	IO L22P T3U N6 DBC AD0P 67	'OVERALL ADRS 3 TO RES NET'
BE28	IO L22N T3U N7 DBC AD0N 67	'OVERALL ADRS 5 TO RES NET'
BF26	IO L20P T3L N2 AD1P 67	'OVERALL ADRS 2 TO RES NET'
BF27	IO L20N T3L N3 AD1N 67	'OVERALL ADRS 4 TO RES NET'
BA29	IO L18P T2U N10 AD2P 67	'Hub I2C to FPGA_SCL'
BB29	IO L18N T2U N11 AD2N 67	'Hub I2C to FPGA_SDA'
AW27	IO L14P T2L N2 GC 67	'ROD_PRESENT_B_TO_FPGA'
AW28	IO L14N T2L N3 GC 67	'ROD_Power_Control_2_FPGA'
BB28	IO T2U N12 67	'FPGA RODs SMBALERT B'
AY27	IO L13P T2L N0 GC QBC 67	'TBD_SPARE_LINK_2_DIR'
AY28	IO L13N T2L N1 GC QBC 67	'TBD_SPARE_LINK_2_CMP'
AV29	IO L12P T1U N10 GC 67	'ROD_Power_Control_4_FPGA'
AV30	IO L12N T1U N11 GC 67	'ROD_Power_Control_3_FPGA'
AU28	IO L11P T1U N8 GC 67	'SPARE_OSC_TO_FPGA_DIR'
AV28	IO L11N T1U N9 GC 67	'SPARE_OSC_TO_FPGA_CMP'
AT30	IO L10P T1U N6 QBC AD4P 67	'ACCESS SIGNAL 1 FROM FPGA'
AT31	IO L10N T1U N7 QBC AD4N 67	'ACCESS SIGNAL 2 FROM FPGA'
AT29	IO L9P T1L N4 AD12P 67	'TBD_SPARE_LINK_3_DIR'
AU29	IO L9N T1L N5 AD12N 67	'TBD_SPARE_LINK_3_CMP'
AT27	IO L8P T1L N2 AD5P 67	'TBD_SPARE_LINK_1_DIR'
AU27	IO L8N T1L N3 AD5N 67	'TBD_SPARE_LINK_1_CMP'
AV26	IO L7P T1L N0 QBC AD13P 67	'TBD_SPARE_LINK_0_DIR'
AW26	IO L7N T1L N1 QBC AD13N 67	'TBD_SPARE_LINK_0_CMP'
AP31	IO T0U N12 VRP 67	R103
AM28	VREF 67	R108

The remaining Bank 67 pins are not connected and are not listed here.

Bank 68:	1V8 I/O HP SLR #0	41 Hub Connections
BF30	IO L24P T3U N10 68	'HUB_FPGA_LED51_DRV'
BF31	IO L24N T3U N11 68	'HUB_FPGA_LED52_DRV'
BA30	IO T3U N12 68	'Phys U21 MDIO'
BC31	IO L23P T3U N8 68	'Phys U21_RXD0_MODE0'
BD31	IO L23N T3U N9 68	'No Conn FPGA BD31'
BE29	IO L22P T3U N6 DBC AD0P 68	'OVERALL ADRS 6 TO RES NET'
BF29	IO L22N T3U N7 DBC AD0N 68	'HUB_FPGA_LED50_DRV'
BA31	IO L21P T3L N4 AD8P 68	'Phys U22 INT B'
BB31	IO L21N T3L N5 AD8N 68	'Phys U21_RX_DV_CLK125_EN'
BD30	IO L20P T3L N2 AD1P 68	'No Conn FPGA BD30'
BE30	IO L20N T3L N3 AD1N 68	'OVERALL ADRS 7 TO RES NET'
BC29	IO L19P T3L N0 DBC AD9P 68	'No Conn FPGA BC29'
BC30	IO L19N T3L N1 DBC AD9N 68	'Phys U21 INT B'
BA36	IO L18P T2U N10 AD2P 68	'Phys U21_TXD0'
BB36	IO L18N T2U N11 AD2N 68	'Phys U21_TXD2'
BB32	IO L17P T2U N8 AD10P 68	'Phys U21 MDC'
BB33	IO L17N T2U N9 AD10N 68	'Phys U21_RXD2_MODE2'
BA34	IO L16P T2U N6 QBC AD3P 68	'Phys U21 GTX_CLK'
BB34	IO L16N T2U N7 QBC AD3N 68	'Phys U21_TX_EN'
AY32	IO L15P T2L N4 AD11P 68	'Phys U21_RXD1_MODE1'
BA32	IO L15N T2L N5 AD11N 68	'No Conn FPGA BA32'

AW33	IO L14P T2L N2 GC 68	'Phys U22 RX CLK PHYAD2'
AY33	IO L14N T2L N3 GC 68	'Phys U21 RXD3 MODE3'
BA35	IO T2U N12 68	'Phys U21 TXD3'
AY34	IO L13P T2L N0 GC QBC 68	'Phys U22 CLK125 LED MODE'
AY35	IO L13N T2L N1 GC QBC 68	'Phys U21 TXD1'
AU33	IO L12P T1U N10 GC 68	'Phys U21 CLK125 LED MODE'
AU34	IO L12N T1U N11 GC 68	'Phys U22 TX EN'
AW32	IO T1U N12 68	'Phys U22 RX DV CLK125 EN'
AV33	IO L11P T1U N8 GC 68	'Phys U21 RX CLK PHYAD2'
AV34	IO L11N T1U N9 GC 68	'Phys U22 RXD2 MODE2'
AV36	IO L10P T1U N6 QBC AD4P 68	'Phys U22 RXD1 MODE1'
AW36	IO L10N T1U N7 QBC AD4N 68	'Phys U22 MDC'
AV35	IO L9P T1L N4 AD12P 68	'Phys U22 RXD0 MODE0'
AW35	IO L9N T1L N5 AD12N 68	'Phys U22 MDIO'
AU31	IO L8P T1L N2 AD5P 68	'No Conn FPGA AU31'
AU32	IO L8N T1L N3 AD5N 68	'Phys U22 RXD3 MODE3'
AV31	IO L7P T1L N0 QBC AD13P 68	'Ref 40.08 MHz from FPGA to Rec Dir'
AW31	IO L7N T1L N1 QBC AD13N 68	'Ref 40.08 MHz from FPGA to Rec Cmp'
AR36	IO L6P T0U N10 AD6P 68	'Phys U22 TXD0'
AT36	IO L6N T0U N11 AD6N 68	'Phys U22 TXD1'
AP33	IO L5P T0U N8 AD14P 68	'No Conn FPGA AP33'
AR33	IO L5N T0U N9 AD14N 68	'No Conn FPGA AR33'
AR35	IO L4P T0U N6 DBC AD7P 68	'Phys U22 TXD2'
AT35	IO L4N T0U N7 DBC AD7N 68	'Phys U22 TXD3'
AR32	IO L3P T0L N4 AD15P 68	'No Conn FPGA AR32'
AT32	IO L3N T0L N5 AD15N 68	'No Conn FPGA AT32'
AR34	IO L2P T0L N2 68	'No Conn FPGA AR34'
AT34	IO L2N T0L N3 68	'Phys U22 GTX CLK'
AU36	IO T0U N12 VRP 68	R104
AN32	IO L1P T0L N0 DBC 68	'No Conn FPGA AN32'
AP32	IO L1N T0L N1 DBC 68	'No Conn FPGA AP32'
AM32	VREF 68	R109

This is a complete list of all pins in Bank 68 including 12 No_Conn_spare unused pins.

Bank 84:	3V3 I/O HR SLR #0	24 Hub Connections
AP17	IO L24P T3U N10 84	'ROD Power Enable B'
AR17	IO L24N T3U N11 84	'ROD Power Enable'
AM16	IO T3U N12 84	'ALL_HUB_POWER_GOOD_TO_FPGA'
AN15	IO L23P T3U N8 84	'Trans MiniPOD SCL'
AP15	IO L23N T3U N9 84	'Trans MiniPOD SDA'
AV16	IO L22P T3U N6 DBC AD0P 84	'FPGA_SW_C_LOOP_DETECTED'
AV15	IO L22N T3U N7 DBC AD0N 84	'FPGA_SW_C_ATC_LOOP_DET'
AN16	IO L21P T3L N4 AD8P 84	'Trans MiniPOD INTR B'
AP16	IO L21N T3L N5 AD8N 84	'Hubs SMB Alert B'
AT17	IO L20P T3L N2 AD1P 84	'No Conn FPGA AT17'
AU17	IO L20N T3L N3 AD1N 84	'No Conn FPGA AU17'
AT16	IO L19P T3L N0 DBC AD9P 84	'FPGA_SW_B_MDC'
AU16	IO L19N T3L N1 DBC AD9N 84	'FPGA_SW_B_MDIO'
AP13	IO L18P T2U N10 AD2P 84	'Trans MiniPOD RESET B'
AR13	IO L18N T2U N11 AD2N 84	'Recvr MiniPOD SDA'
AU12	IO L17P T2U N8 AD10P 84	'ISO_SLOT_HW_ADRS_2'
AU11	IO L17N T2U N9 AD10N 84	'ISO_SLOT_HW_ADRS_3'

AR15	IO L16P T2U N6 QBC AD3P 84	'Recvr MiniPOD INTR B'
AR14	IO L16N T2U N7 QBC AD3N 84	'Recvr MiniPOD RESET B'
AR12	IO L15P T2L N4 AD11P 84	'Recvr MiniPOD SCL'
AT12	IO L15N T2L N5 AD11N 84	'ISO SLOT HW ADRS 0'
AT15	IO L14P T2L N2 GC 84	'CLOCK 25 MHz FPGA'
AT14	IO L14N T2L N3 GC 84	'FPGA SW B ATC LOOP DET'
AT11	IO T2U N12 84	'ISO SLOT HW ADRS 1'
AU14	IO L13P T2L N0 GC QBC 84	'No Conn FPGA AU14'
AU13	IO L13N T2L N1 GC QBC 84	'FPGA SW B LOOP DETECTED'
AM17	VREF 84	R111

This is a complete list of all pins in Bank 84 including 3 No_Conn_spare unused pins.

Bank 94:	3V3 I/O HR SLR #0	22 Hub Connections
AW13	IO L12P T1U N10 GC 94	'FPGA SW A MDC'
AW12	IO L12N T1U N11 GC 94	'ISO SLOT HW ADRS 5'
AY13	IO T1U N12 94	'FPGA SW C MDC'
AV14	IO L11P T1U N8 GC 94	'No Conn FPGA AV14'
AV13	IO L11N T1U N9 GC 94	'FPGA SW A ATC LOOP DET'
BA11	IO L10P T1U N6 QBC AD4P 94	'SHELF ADRS 7 TO FPGA'
BB11	IO L10N T1U N7 QBC AD4N 94	'SHELF ADRS 5 TO FPGA'
AY12	IO L9P T1L N4 AD12P 94	'ISO SLOT HW ADRS 7'
BA12	IO L9N T1L N5 AD12N 94	'SHELF ADRS 6 TO FPGA'
BB13	IO L8P T1L N2 AD5P 94	'SHELF ADRS 3 TO FPGA'
BB12	IO L8N T1L N3 AD5N 94	'SHELF ADRS 4 TO FPGA'
AV11	IO L7P T1L N0 QBC AD13P 94	'ISO SLOT HW ADRS 4'
AW11	IO L7N T1L N1 QBC AD13N 94	'ISO SLOT HW ADRS 6'
AY17	IO L6P T0U N10 AD6P 94	'No Conn FPGA AY17'
BA17	IO L6N T0U N11 AD6N 94	'No Conn FPGA BA17'
BA14	IO L5P T0U N8 AD14P 94	'SHELF ADRS 2 TO FPGA'
BB14	IO L5N T0U N9 AD14N 94	'SHELF ADRS 1 TO FPGA'
BB17	IO L4P T0U N6 DBC AD7P 94	'No Conn FPGA BB17'
BB16	IO L4N T0U N7 DBC AD7N 94	'I2C Buf 1503 ENABLE'
BA16	IO L3P T0L N4 AD15P 94	'I2C Buf 1501 ENABLE'
BB15	IO L3N T0L N5 AD15N 94	'SHELF ADRS 0 TO FPGA'
AW15	IO L2P T0L N2 94	'FPGA SW A MDIO'
AY14	IO L2N T0L N3 94	'FPGA SW C MDIO'
BC16	IO T0U N12 94	'No Conn FPGA BC16'
AY15	IO L1P T0L N0 DBC 94	'FPGA SW A LOOP DETECTED'
BA15	IO L1N T0L N1 DBC 94	'I2C Buf 1502 ENABLE'
AW16	VREF 94	R112

This is a complete list of all pins in Bank 94 including 5 No_Conn_spare unused pins.

Bank 70:	1V8 I/O HP SLR #1	3 Connections PLL-Det FEX Ref Clk Enb
B26	IO L24P T3U N10 70	'PLL 320.64 MHz Lock Detect to FPGA'
B27	IO L22P T3U N6 DBC AD0P 70	'PLL 40.08 MHz Lock Detect to FPGA'
A26	IO L24N T3U N11 70	'Select Input Second 40 Fanout'

Only the Bank 70 signals used in the Hub design are listed.

Bank 71:	1V8 I/O HP SLR #1	15 Connections Clocks and Equalizer Enb
B22	IO L24N T3U N11 71	'MGT FO EQU ENB_GRP 6'

B25	IO L23P T3U N8 71	'MGT FO EQU ENB GRP 3'
A25	IO L23N T3U N9 71	'MGT FO EQU ENB GRP 2'
C25	IO L21N T3L N5 AD8N 71	'MGT FO EQU ENB GRP 1'
A24	IO L20P T3L N2 AD1P 71	'MGT FO EQU ENB GRP 4'
A23	IO L20N T3L N3 AD1N 71	'MGT FO EQU ENB GRP 9'
C24	IO L19N T3L N1 DBC AD9N 71	'MGT FO EQU ENB GRP 5'
H23	IO L14P T2L N2 GC 71	'Ref 40.08 MHz from Other Hub Dir'
G23	IO L14N T2L N3 GC 71	'Ref 40.08 MHz from Other Hub Cmp'
J24	IO L12P T1U N10 GC 71	'Logic Clk 40.08 MHz to FPGA Dir'
H24	IO L12N T1U N11 GC 71	'Logic Clk 40.08 MHz to FPGA Cmp'
K22	IO L11P T1U N8 GC 71	'Logic Clk 320.64 MHz to FPGA Dir'
J22	IO L11N T1U N9 GC 71	'Logic Clk 320.64 MHz to FPGA Cmp'
P22	IO T0U N12 VRP 71	R105
P21	VREF 71	R110

The remaining 39 pins in Bank 71 are not used in the Hub design and are not listed here.

Bank 72:	1V8 I/O HP SLR #1	6 Connections Equalizer Enables
A18	IO L24N T3U N11 72	'MGT FO EQU ENB GRP 13'
A20	IO L23P T3U N8 72	'MGT FO EQU ENB GRP 11'
A19	IO L23N T3U N9 72	'MGT FO EQU ENB GRP 12'
A21	IO L21N T3L N5 AD8N 72	'MGT FO EQU ENB GRP 10'
D20	IO L20P T3L N2 AD1P 72	'MGT FO EQU ENB GRP 7'
C20	IO L19P T3L N0 DBC AD9P 72	'MGT FO EQU ENB GRP 8'

Only the Bank 72 signals used in the Hub design are listed.

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1941 **20 Appendix 7: Hub FPGA Signal Types**

1942 For each signal “type” that connects to the Hub’s FPGA this file provides:

- 1943 • A short description of the function of that signal type.
- 1944 • A description of how the I/O Block that handles that signal type should be setup.
- 1945 • A description of the FPGA logic that is necessary to properly handle that signal type in a
- 1946 minimal safe Hub firmware implementation.
- 1947 • Where applicable a reference is given to the Hub Circuit Diagram(s) where that signal
- 1948 type is shown so that you can see how it is used on the Hub circuit board.

1949 **20.1 Select I/O Signals:**

1950 **20.1.1 Clock and Clock Management Signals**

1951 This sections lists the various Select I/O clock signals and clock management signals in the
1952 Hub design. See **Figure 24**, **Figure 25**, **Figure 26** and **Figure 27**.

1953 *CLOCK_25_MHz_FPGA*

1954 This is a single ended clock input to the FPGA. This clock is used in the Ethernet
1955 circuits. This is not an LHC locked clock. This is a 3.3V CMOS clock signal that is
1956 always running. The FPGA needs to always provide a 3.3V CMOS receiver for it. No
1957 special internal FPGA termination should be necessary to correctly receive this clock
1958 signal.

1959 *Logic_Clk_320.64_MHz_to_FPGA_Dir/Cmp, Logic_Clk_40.08_MHz_to_FPGA_Dir/Cmp*

1960 These are the main Logic Clock signals for the Hub FPGA. These are AC coupled LHC
1961 locked clocks. The FPGA must receive them as differential signals, 100 Ohm terminate
1962 them, and DC Bias these FPGA inputs by including the proper combination of
1963 DQS_Bias and EQ_Level0 attributes in the setup of these I/O Blocks. Even if these
1964 clocks are not used in a minimal safe FPGA design they must still be properly received.

1965 *Ref_40.08_MHz_from_Other_Hub_Dir/Cmp*

1966 This is an AC coupled LVDS input to the Hub FPGA. In a shelf with two Hub Modules
1967 this clock path is used on the Hub that does not receive an Optical Felix TTC signal.
1968 Because this is AC coupled the I/O Block that receives this signal must be setup with the
1969 correct combination of the DQS_Bias and EQ_Level0 attributes. This FPGA input
1970 should include a 100 Ohm differential terminator. This input needs to be setup and
1971 instantiated in all versions of the Hub FPGA firmware.

1972 *Ref_40.08_MHz_from_FPGA_to_Rec_Dir/Cmp*

1973 This is an LVDS output from the Hub FPGA that runs to an LVDS receiver and then
1974 connects to the reference input on the 40.08 MHz PLL. I believe that we should include
1975 this output even in a minimal safe FPGA design even if we only tie the input to the LVDS
1976 driver Low.

1977 *PLL_40.08_MHz_Lock_Detect_to_FPGA, PLL_320.64_MHz_Lock_Detect_to_FPGA*

1978 These are two Lock Detect signals from the PLL Clock circuits on the Hub Module.
1979 When Hi they indicate that the associated PLL has locked onto its reference input. The
1980 FPGA needs to always provide 1.8V CMOS receivers for these two signals.

1981 *Select_Input_Second_40_Fanout*

1982 This signal is an output from the Hub FPGA. It is used to enable or disable the Hub
 1983 circuit board from sending out 40.08 MHz Reference Clocks on Zone-2 of the Backplane.
 1984 Recall that in a shelf with 2 Hub Modules, that only the primary Hub that receives the
 1985 Optical Felix TTC signal will send out its 40.08 MHz Reference Clocks to the FEX
 1986 modules. The secondary Hub (the Hub that does not receive an Optical Felix TTC
 1987 signal) must not send out its Zone-2 Reference Clocks. This is a 1.8V CMOS open-drain
 1988 output from the Hub Module. When Low it enables the Hub Module to send out its Zone-
 1989 2 Reference Clocks. When the open-drain output transistor in the FPGA I/O Block is Off
 1990 then its backplane Reference Clock output drives will be shutdown. In a minimal safe
 1991 design I think that we want this open-drain output to pull this signal Low so that we can
 1992 see these Reference Clock outputs.

1993 *SPARE_OSC_TO_FPGA_Dir/Cmp*

1994 This is a spare differential clock input to the Hub FPGA. As long as we are not installing
 1995 this part (U562) then nothing special needs to be done with these input pins to the FPGA
 1996 even in a minimal safe FW design.

1997 **20.1.2 Ethernet Switch Chip Management Signals**

1998 Each of the 3 Broadcom Ethernet Switch chips has its own set of 4 management signals with
 1999 the Hub FPGA. See Hub Circuit Diagram 17.

2000 *FPGA_SW_?_ATC_LOOP_DET*

2001 This is a control signal from the Hub FPGA to the Ethernet Switch chips. I assume that
 2002 this signal will eventually be controlled from a bit in an IPBus visible register. A
 2003 minimal Hub FPGA design could just tie this signal Low. A Slow Slew and 4 mA Drive
 2004 level is fine for this 3.3V CMOS static level output signal.

2005 *FPGA_SW_?_LOOP_DETECTED*

2006 This is a status signal from the Broadcom Switch chips to the Hub FPGA. I assume that
 2007 this status bit will eventually be visible in an IPBus register. The FPGA needs to at least
 2008 always provide a receiver for this 3.3V CMOS input signal.

2009 *FPGA_SW_?_MDC*

2010 Because the MDC/MDIO interface on the Broadcom Switch chips is in Slave mode, this
 2011 clock signal runs from the Hub FPGA to the Switch chip. Eventually I assume that these
 2012 pins on the Hub FPGA will be controlled by firmware that implements the MDC/MDIO
 2013 part of a MAC. For minimal safe firmware this line could just be driven Low by a Slow
 2014 Slew 4 mA 3.3V CMOS output driver.

2015 *FPGA_SW_?_MDIO*

2016 This is a bi-directional data line between the Hub FPGA and the MDC/MDIO interface in
 2017 the Broadcom Switch chips. Eventually I assume that these pins on the Hub FPGA will
 2018 be handled by firmware that implements the MDC/MDIO part of a MAC. In a minimal
 2019 safe Hub FPGA design I would provide a 3.3V CMOS receiver for this signal with a
 2020 weak pull-up resistor at its input.

2021 **20.1.3 Hardware Address Signals**2022 *ISO_SLOT_HW_ADRS_?*

2023 These 8 signals bring the backplane Hardware Slot Address to the Hub FPGA. The
 2024 IPMC module also receives these signals. Even if the Hub FPGA is not going to use this
 2025 Hardware Slot number information it must still receive these 8 lines with 3.3V CMOS
 2026 receivers. See Hub Circuit Diagram 13.

2027 *SHELF_ADRS_?_TO_FPGA*

2028 These are 8 signals that bring the Shelf Address information from the IPMC to the Hub's
 2029 FPGA. These lines connect to "User I/O" pins on one of the ARM CPUs in the IPMC
 2030 module. The Hub Firmware needs to at least always provide 3.3V CMOS receivers for
 2031 these signals.

2032 *OVERALL_ADRS_?_TO_RES_NET*

2033 These are 8 outputs from the Hub FPGA that provide an Overall Hardware Address to the
 2034 ROD mezzanine. This Overall Hardware Address is made up of the Slot Hardware
 2035 Address that comes from the Backplane and the Shelf Hardware Address that comes
 2036 from the IPMC. In a minimal safe FPGA implementation I would just tie all 8 of these
 2037 Overall Hardware Address lines Low. These can be 1.8V CMOS Slow Slew 4 mA Drive
 2038 outputs.

2039 **20.1.4 I2C Bus Signals**2040 *Hub_I2C_to_FPGA_SCL, Hub_I2C_to_FPGA_SDA*

2041 Note that this I2C bus makes TWO connections to the Hub FPGA. See Hub Circuit
 2042 Diagram 37.

2043 It connects to pins:

2044 BE16 IO_L23P_T3U_N8_I2C_SCLK_65

2045 BF16 IO_L23N_T3U_N9_I2C_SDA_65

2046 that provide for a Slave I2C interface to the FPGA System Monitor, and it connects to pins:

2047 BA29 IO_L18P_T2U_N10_AD2P_67

2048 BB29 IO_L18N_T2U_N11_AD2N_67

2049 so that one can implement a Master I2C interface so that for example the Hub FPGA can talk to the
 2050 Hub's DCDC Converter power supplies.

2051 In a minimal safe design both of these I2C signals at both pin pairs should connect to
 2052 1.8V CMOS Receivers.

2053 *I2C_Buf_150?_ENABLE*

2054 These are control signals from the Hub FPGA to the Sensor I2C Bus translator/buffer
 2055 chips. These translator/buffer chips allow the overall Sensor I2C Bus on the ROD-Hub
 2056 cards to be divided up into sections. Eventually we may need to control dividing up the
 2057 Sensor I2C bus either from bits in an IPBus visible register or from a control signal from
 2058 the ROD to the Hub. For a minimal safe Hub FPGA design these 3 I2C buffer control
 2059 signals can just be tied Hi which will enable these I2C translator/buffers. These control
 2060 signals are 3.3V Slow Slew 4 mA Drive outputs from the Hub FPGA.

2061 **20.1.5 MiniPOD Management Signals**

2062 Each of the MiniPODs has 4 management signals associated with it. The Hub's Receiver and
 2063 Transmitter MiniPODs each have their own private set of these 4 management signals. Hub
 2064 Circuit Diagram 21 shows the layout of these signals. The setup of the MiniPOD
 2065 management signals on the Hub is very similar to that used on the CMX card.

2066 *Recvr_MiniPOD_INTR_B, Trans_MiniPOD_INTR_B*

2067 *Interrupt signals from the MiniPODs to the FPGA. Low indicates interrupt. The FPGA*
 2068 *should always provide 3.3V CMOS receivers for these two signals.*

2069 *Recvr_MiniPOD_RESET_B, Trans_MiniPOD_RESET_B*

2070 *These are Reset signals from the FPGA to the MiniPODs. Low indicates Reset. A minimal*
 2071 *safe design should at least drive these lines Hi with a Slow Slew 4 mA Drive 3.3V CMOS*
 2072 *output. In a full firmware design I assume that these Reset signals will be controlled from*
 2073 *bits in an IPBus visible register.*

2074 *Recvr_MiniPOD_SCL, Trans_MiniPOD_SCL*

2075 These are the clock signals for the bi-directional serial data path between the FPGA and
 2076 the MiniPODs. In a minimal safe design I would drive this signals Low with a Slow
 2077 Slew 4 mA Drive 3.3V CMOS output.

2078 *Recvr_MiniPOD_SDA, Trans_MiniPOD_SDA*

2079 These are the bi-directional data lines for the serial data path between the FPGA and the
 2080 MiniPODs. In a minimal design I would provide a 3.3V CMOS receiver for these
 2081 signals.

2082 **20.1.6 Miscellaneous Select I/O Signals**

2083 *ACCESS_SIGNAL_?_FROM_FPGA*

2084 These two output signals from the FPGA run to a translator/buffer chip and then to pins in
 2085 the front panel J2 connector. See Hub Circuit Diagram 53. The purpose of these signals
 2086 is to allow one to see with an oscilloscope some aspect of the FPGA's operation. Unless
 2087 needed for something special these 1.8V CMOS output signals can be configured for a
 2088 Slow Slew rate and modest 4 mA Drive. A minimal safe Hub FPGA design could just tie
 2089 these 2 signals Low.

2090 *HUB_FPGA_LED5?_DRV*

2091 These three signals are outputs from the Hub FPGA that control front panel LEDs. These
 2092 are 1.8V CMOS signals and using a Slow Slew and 4 mA of Drive would be fine. A
 2093 minimal safe Hub FPGA design could just tie these 3 output signals Low.

2094 *Hubs_SMB_Alert_B*

2095 This is an input signal to the Hub's FPGA from the 7 DCDC Converter power supplies on
 2096 the Hub Module. When Low it indicates that one or more of these Hub power supplies is
 2097 in trouble (or at least wants attention). Normally this signal should be Hi. This is a 3.3V
 2098 CMOS signal and the FPGA must always have a receiver for it even if it does not make
 2099 use of this signal.

2100 *ALL_HUB_POWER_GOOD_TO_FPGA*

2101 This is an input signal to the Hub's FPGA from the Power Control circuits on the Hub
 2102 Module. This is a 3.3V Select I/O signal in Bank 84. When Low this signal indicates
 2103 that there is some kind of power supply problem on the Hub Module. When Hi this
 2104 signal indicates: that all 7 DCDC Converters report that they are operating correctly, and
 2105 that the Isolated +12V supply is Enabled, and that the output from the Linear
 2106 MGT_AVAUX and BULK_2V5 supplies is good. The Hub FPGA must always
 2107 instance a 3.3V CMOS receiver for this signal even if it does not make use of this signal.
 2108 This signal comes through a 2.7k Ohm isolation resistor from a 5V source.

2109 *MGT_FO_EQU_ENB_GRP_?*

2110 These 13 control signals are outputs from the Hub FPGA that enable or disable the
 2111 equalization in the MGT Fanout chips. All fanout chips that service a given data source
 2112 either have their equalization enabled or disabled. I assume that eventually these 13
 2113 equalization enable signals will be separately controllable from bits in an IPBus visible
 2114 register. In a minimal safe Hub FPGA design all of the Equalization Enable signals can
 2115 just be tied HI. I would drive them as 1.8V CMOS outputs with Slow Slew and 8 mA of
 2116 Drive. The loading on these signals will only be about 150 uA but the high Drive level
 2117 may help if we need to ramp up the FAN_1V8 rail voltage.

2118 *TBD_SPARE_LINK_?_ Dir/Cmp*

2119 These are 8 To Be Determined spare lines between the Hub and ROD FPGAs.
 2120 Currently none of them have an assigned function. If needed they can be operated as
 2121 either 8 separate 1.8V CMOS signals or as 4 separate LVDS signals. As with all CMOS
 2122 signals we can not just leave them floating. As unassigned spare signals the agreement
 2123 with ROD is that we will run them as 8 separate CMOS signals and that the Hub will
 2124 drive them and the ROD will receive them. Further the agreement with ROD is that the
 2125 Hub will keep these signals tri-stated until the ROD asserts it Power Control #2 signal HI
 2126 to the Hub. See Hub Circuit Diagram 42. Even in a minimal safe firmware design the
 2127 Hub needs to implement this functionality. These 8 lines should be driven with Slow
 2128 Slew 4 mA Drive 1.8V CMOS output blocks. See also Section 26.

2129 **20.1.7 Phys_U21 and Phys_U22 signals**

2130 Each Phys Chip makes 16 connections with the Hub's FPGA. These Phys Chip <--> FPGA
 2131 connections are shown in **Figure 43** and make up a RGMII interface bus.

2132 In the real Hub operation these 16 signals will be managed by MAC IP firmware. This
 2133 RGMII connection between the FPGA and the Phys Chips includes signals that may require
 2134 fast slew rates, higher drive current, and DCI back (series) termination. These RGMII signals
 2135 have been laid out carefully on the Hub circuit to minimize cross-talk, reflections, and signal
 2136 loss. Careful consideration must be given to how the RGMII signals are handled in the
 2137 FPGA I/O Blocks to provide both a good RGMII interface and to minimize interference with
 2138 other parts of the Hub Module.

2139 For a minimal safe Hub FPGA design we still should handle these CMOS signals in a defined
 2140 rational way.

2141 I would provide Low current Drive Slow Slew 1.8V CMOS outputs tied Low for the
 2142 following signals:

2143 Phys_U2?_TXD0

2144 Phys_U2?_TXD1
 2145 Phys_U2?_TXD2
 2146 Phys_U2?_TXD3
 2147 Phys_U2?_TX_EN
 2148 Phys_U2?_GTX_CLK
 2149 Phys_U2?_MDC
 2150

2151 I would provide 1.8V CMOS receivers for the following signals:

2152 Phys_U2?_RXD0__MODE0
 2153 Phys_U2?_RXD1__MODE1
 2154 Phys_U2?_RXD2__MODE2
 2155 Phys_U2?_RXD3__MODE3
 2156 Phys_U2?_RX_CLK__PHYAD2
 2157 Phys_U2?_RX_DV__CLK125_EN
 2158 Phys_U2?_CLK125__LED_MODE
 2159 Phys_U2?_MDIO
 2160 Phys_U2?_INT_B

2161 **20.1.8 ROD Present and ROD Power Control Signals**

2162 These 7 signals have to do with letting the Hub know whether or not a ROD is installed on it,
 2163 Controlling (i.e. enabling) the power on the ROD, and letting the Hub know whether or not
 2164 all ROD power is good and that the ROD is ready for normal trigger system operation. See
 2165 also Section 26 for further discussion.

2166 *ROD_PRESENT_B_TO_FPGA*

2167 This signal is a pull-down resistor on the ROD. When the ROD is NOT present this
 2168 signal goes HI on the Hub. The Hub must always provide a 1.8V CMOS receiver for this
 2169 signal even if it does not use it.

2170 *ROD_Power_Control_2_FPGA*

2171 This is an input to the Hub's FPGA. When HI this signal indicates that all power supplies
 2172 on the ROD are operating correctly. The Hub must always provide a 1.8V CMOS
 2173 receiver for this signal even if it does not use it.

2174 *ROD_Power_Control_3_FPGA*

2175 This is an input to the Hub's FPGA. When HI this signal indicates that the ROD is
 2176 Configured and fully ready for normal L1Calo operation. The Hub must always provide
 2177 a 1.8V CMOS receiver for this signal even if it does not use it.

2178 *ROD_Power_Control_4_FPGA*

2179 This is a spare power control signal. In a minimal safe firmware design the Hub should
 2180 provide a 1.8V CMOS receiver for this signal with a weak pull-up resistor at its input.

2181 *ROD_Power_Enable, ROD_Power_Enable_B*

2182 These two signal are outputs from the Hub FPGA that through some hardwired logic on
 2183 the Hub tell the ROD when it may turn ON its power supplies. The hardwired logic
 2184 associated with these signals is shown in Hub Circuit Diagram 32. These are 3.3V Slow
 2185 Slew 4 mA Drive CMOS outputs. A minimal safe design (that just locks OFF the ROD
 2186 power) should set ROD_Power_Enable Low and set ROD_Power_Enable_B Hi.

2187 *FPGA_RODs_SMBALERT_B*

2188 This is an input to the Hub's FPGA that when LOW indicates a power supply problem on
 2189 the ROD. During normal operation this signal should always be HI. Pull up current to
 2190 1V8 is provided by a 1k Ohm resistor on page 25 of the ROD schematics. A normal 1.8V
 2191 CMOS receiver should be used. The FPGA needs to always provide a receiver for this
 2192 signal.

2193 **20.2 MGT Transceiver Signals**

2194 *Comb_Data_to_Cap_to_FEX_*_Dir/Cmp, Comb_Data_to_Cap_to_Other_Hub_Dir/Cmp,*
 2195 *Comb_Data_to_Cap_to_ROD_Dir/Cmp*

2196 These 14 Combined Data signals are MGT Outputs from the FPGA. Hub Circuit Diagrams
 2197 22 and 23 indicate which of the Combined Data signals needed to be inverted in their MGT
 2198 Transmitter in order to provide standard right-side-up polarity over the Backplane and at the
 2199 Receiver.

2200 *This_Hubs_RO_?_to_Cap_Its_ROD_Dir/Cmp, This_Hubs_RO_?_to_Cap_Other_ROD_Dir/Cmp*

2201 These 4 MGT outputs are the readout data from the Hub FPGA. One of these links goes to
 2202 the ROD on This Hub (where it can only receive the Lane 0 signal) and the second pair goes
 2203 to the MGT Fanout on the Other Hub from which it is routed to both the Other Hub's FPGA
 2204 and to the Other Hub's ROD. Hub Circuit Diagrams 22 and 23 indicate the MGT
 2205 Transmitter logic inversions that should be included in the firmware setup.

2206 *MiniPOD_Trans_Fiber_??_Data_Dir/Cmp*

2207 These are 8 MGT Transmitter outputs that run to the Transmitter MiniPOD. Hub Circuit
 2208 Diagram 23 indicates which of these MGT Transmitters needs to include a logic inversion so
 2209 that all 8 of these Transmitter MiniPOD fibers provide a right-side-up light signal.

2210 *Rec_MP_Fiber_?_to_FPGA_Dir/Cmp*

2211 These 4 MGT inputs come from the Receiver MiniPOD. Hub Circuit Diagrams 22 and 23
 2212 indicate which of these links need to be inverted in the MGT receiver in order to compensate
 2213 in a polarity flip in the trace routing.

2214 *MGT_FO_CH_??_OUT_Hub_Dir/Cmp*

2215 These are the 74 MGT inputs to the Hub FPGA that carry the FEX readout data and the
 2216 readout data from the Other Hub. Hub Circuit Diagrams 22 and 23 indicate which of these
 2217 MGT Receivers need to invert their input signal. These 74 signals are specified by their
 2218 MGT_Fanout_Channel number.

2219 *Combined_Data_from_OTHER_Hub_Dir/Cmp*

2220 This signal is an MGT Input to the Hub FPGA. As indicated in Hub Circuit Diagram 22 the
 2221 MGT receiver for this signal needs to invert it to compensate for the polarity flip in the Hub
 2222 circuit board traces.

2223 *This RODs Readout Ctrl to GTH Input Dir/Cmp*

2224 This is the MGT input for the Readout Control data from the ROD on This Hub. Hub Circuit
2225 Diagram 23 indicates that this MGT Receiver should be setup to provide a logic inversion to
2226 properly receive this data.

2227 Note that this high bandwidth link from the ROD to the Hub FPGA was provided so that if
2228 the ROD ever needs to send a lot Readout Control information to the FEX data sources that
2229 we can provide such a data path (i.e. to match the bandwidth of the Combined Data links to
2230 the FEX cards).

2231 On the other hand if the ROD only needs to send one bit On/Off Readout Control to the Hub
2232 FPGA then one of the ROD-Hub TBD spare links could be used to transport that simple type
2233 of Readout Control.

2234 *MHz_320.64_COPY_?_ Dir/Cmp*

2235 These 8 clocks are the MGT Reference clock inputs to the Hub FPGA. They have been
2236 spread through out the 20 MGT Quads so that no MGT Transceiver needs to go further than
2237 the adjacent Quad to get its reference clock signal. These are AC coupled LHC locked clock
2238 signals. All clock polarities have been kept right-side-up to keep clock duty factor
2239 uncertainty from turning into clock jitter. See Hub Circuit Diagram 41.

2240

2241 **21 Appendix 8: Hub-Module IPMC Connections**

2242 The Hub Module design includes a large number of connections to the IPMC mezzanine
 2243 card. These connections are described in following sections of this document and are shown
 2244 in **Figure 33**, **Figure 34** and **Figure 35** as well as **Figure 36**.

2245 **21.1 Connections Shown in Figure 33**

2246 *Backplane IPMB A and B:*

2247 The IPMC is connected to the Shelf Manager by the two IPMB buses. The A and B IPMB
 2248 Buses enter the Hub Module on the Zone 1 connector and have a rather long path up to near
 2249 the top of the IPMC socket. These two I2C buses are routed to keep them away from noise
 2250 sources as much as possible.

2251 *Slot Hardware Address:*

2252 The 8 Slot Hardware Address signals allow the Hub Module to know what slot it is in but not
 2253 what Shelf it is in in the overall L1Calo system it is in. The Slot Hardware Address enters the
 2254 Hub Module on its Zone 1 connector and is routed up to near the top of the IPMC socket.
 2255 Near next to the IPMC socket are located the 4.99k Ohm pull-up resistors to IPMC_3V3 and
 2256 the 100 nFd noise bypass capacitors.

2257 A point to note is that both the IPMC and the Hub's FPGA need to know the Slot Hardware
 2258 Address. This is accomplished by also running these 8 signals to a 3V3 Select I/O Bank in
 2259 the Hub's FPGA. These 8 connections to the Hub's FPGA include 470 Ohm isolation
 2260 resistors.

2261 A potential issue involves IPMC trying to read the Slot Hardware Address lines before the
 2262 FPGA has powered up. In that situation these lines may be held low by the input protection
 2263 diodes on the FPGA. If that is the case then stronger pull-ups will be used along with higher
 2264 value isolation resistors. These are static signals so rather high value isolation resistors
 2265 should be OK. In any case I don't think that this should require a full buffer for these signals.

2266 *Front Panel Switch:*

2267 The Hub Module uses a front panel switch that is permanently mounted to the back side of
 2268 the PCB. The required sense of this switch is not well explained in the IPMC documentation.
 2269 I believe that it should be "open" when the front panel handle is fully closed and latched.
 2270 The switch wiring is up-side-down from common rational practice, i.e. the switch connects
 2271 to 3V3 and uses a pull-down resistor) but it is connected as the IPMC document
 2272 recommends.

2273 **21.2 Connections Shown in Figure 34**

2274 *Front Panel LEDs:*

2275 The IPMC directly drives the 4 ATCA front panel LEDs. The required setup of these LEDs
 2276 is not explained in the IPMC documentation. I believe that they use normal GPIO pins their
 2277 ARM uProcessor to drive these LEDs. I believe that the user needs to supply the LED series
 2278 resistor but this is never explained. I believe that they are trying to drive the anode of the
 2279 LED (backwards from rational practice) but this is not explained in their document. On the
 2280 Hub I have connected the LED cathode pin to Ground and put the series resistor between the
 2281 LED anode and the LED pin on the IPMC.

2282 *Pay Load Enable Signal:*

2283 I believe that the Pay Load Enable signal goes Hi when it wants to turn ON the card. Opto-
 2284 Coupler isolation is used between the IPMC and the Control pin on the Isolated +12V power
 2285 supply. The cathode of this LED is Grounded and its anode is tied to the IPMC's
 2286 12V_Enable pin through a 330 Ohm LED series resistor.

2287 The Opto-Coupler's LED will illuminate when the IPMC's 12V_Enable pin goes HI, and will
 2288 turn ON the Opto-Coupler's transistor and will turn ON the Isolated +12V supply.

2289 To allow power up the Hub Module in the absence of an IPMC or on the bench in the
 2290 absence of a Shelf Manager for the IPMC to talk to, I have included two jumper locations
 2291 JMP5 and JMP6. Install JMP5 and remove JMP6 for normal operation controlled by the
 2292 IPMC. Install JMP6 and remove JMP5 to turn on the Hub's Isolated +12V supply all of the
 2293 time.

2294 Note that the 12V_Enable signal is also routed to the Hub's power supply supervisor circuits.
 2295 This signal is used both as part of the startup sequence for the Hub Module's DCDC
 2296 converters and also during the shutdown sequence. This 12V_Enable signal falling is the
 2297 first indication that the Hub is going to power down. Using this signal to shutdown the Hub's
 2298 DCDC converters allows then time to ramp down before the Isolated +12V power bus falls
 2299 below threshold.

2300 *Power Entry Module Alarm:*

2301 The single Alarm pin signal from the ATCA Power Entry Module is connected to the
 2302 ALARM_A pin on the IPMC. This connections includes a 4.99k Ohm pull-up to
 2303 IPMC_3V3. The Hub Module makes no connection to the IPMC's ALARM_B pin.

2304 *Management I2C Bus:*

2305 The IPMC's Management I2C bus is connected to both the ATCA Power Entry Module and
 2306 to the FRU-SDR EEPROM. The I2C bus address of the Power Entry Module is set by
 2307 resistor R955 connected between its pin #10 and Ground. The IPMC documentation does not
 2308 say what I2C address it expects the Power Entry Module to appear at. The FRU-SDR
 2309 EEPROM is a ST Micro M24256 that is configured by its Ex pins to appear as 32k words of

2310 8 bits at I2C address 1010000. The EEPROM's WC pin is tied Low to allow write
2311 operations.

2312 **21.3 Connections Shown in Figure 35**

2313 *Power for the IPMC:*

2314 3.3 Volt power for the IPMC is supplied by the ATCA Power Entry Module. This power bus
2315 is called IPMC_3V3 and is used only by the IPMC and the components immediately
2316 associated with it. The IPMC_3V3 bus is energized any time that the Power Entry Module
2317 receives backplane 48 Volt power.

2318 *IPMC Ethernet Port:*

2319 The Hub Module provide the Ethernet Magnetics and RJ45 connector for the IPMC. The
2320 current IPMC is a 10/100 speed only device that uses only 2 of the 4 pairs in the standard
2321 Ethernet connection. This device requires an old "current" mode type of connection to its
2322 magnetics. The Hub Module provides the required environment the existing IPMC and can
2323 also be setup via jumpers for a 10/100/1000 speed voltage mode operation that a future IPMC
2324 would most likely require.

2325 The Ethernet connection to the IPMC is via a front panel RJ45 connector on the Hub Module.
2326 In this way the IPMC can be connected to the DCS Ethernet in a 2 Hub Shelf or operated
2327 with a single Ethernet up-link in a one Hub test setup.

2328 *Shelf Address:*

2329 The IPMC needs to obtain the Shelf Address of the shelf that it finds itself in from the Shelf
2330 Manager. Then the IPMC needs to make the Shelf Address available on 8 of its User I/O
2331 output pins. These IPMC User I/O pins are connected to pins on the Hub's FPGA through
2332 isolation resistors. The point of this is to send the Shelf Address to the Hub FPGA. The Hub
2333 FPGA will use a combination of this Self Address and the Slot Hardware Address to generate
2334 the Ethernet Address that it will use for IPBus communication.

2335 A combination of the Shelf Address and the Slot Hardware Address is also sent to the ROD
2336 so that it can also generate the Ethernet Address that its FPGA will use for IPBus
2337 communication.

2338 *Sensor I2C Bus*

2339 The IPMC Sensor I2C Bus is used to collect monitoring data about power supply voltages and
2340 currents and device temperatures on the ROD and Hub. The IPMC will forward this
2341 hardware monitoring information over Ethernet to the Atlas DCS system. The layout of the
2342 Sensor I2C Bus is shown in **Figure 36**.

2343 As shown in this drawing, three I2C bus buffer/translators are used both to drive the large
2344 number of devices on this bus, a combination of ROD and Hub devices, and also to translate
2345 between the sections of the Sensor I2C Bus that are 3V3 and the sections that are 1V8 level

2346 I2C bus. The buffer/translator part that is used on the Hub is the Linear Technology
 2347 LTC4315. If necessary these buffer/ translators can also be used to separate the various
 2348 sections of overall Sensor I2C bus under control of the Hub FPGA.

2349 At times other devices will need to initiate and master cycles on the Sensor I2C Bus, e.g. to
 2350 setup parameters in the GE DCDC power converters on both the ROD and Hub modules. A
 2351 User I/O input pin on the IPMC to disable its collection sweeps of monitoring data might be
 2352 useful during the short and infrequent periods when other devices need to initiate and master
 2353 cycles on this bus.

2354 **I2C Addresses on the Sensor I2C Bus**

ROD	Binary	Decimal	TI-GE Octal
FPGA Master	0100 000	32	--
LM82 Temp Monitor	0011 001	25	--
MDT040 1V0	0011 010	26	32
MDT040 1V05	0011 011	26	33
PDT012 1V2	0011 100	28	34
PDT006 1V8	0011 101	29	35
PDT006 2V5	0011 110	30	36
PDT006 3V3	0011 111	31	37
SI5338 Clk Gen	1110 000	112	--
Hub			
Hub	Binary	Decimal	TI-GE Octal
FPGA Master	0101 001	41	--
FPGA Sys Mon Slv	0101 010	42	--
MDT040 FPGA_CORE	0110 000	48	50
UDT020 MGT_AVCC	0110 001	49	51
UDT020 MGT_AVTT	0110 010	50	52
PDT012 SWCH_1V2	0110 011	51	53
PDT012 BULK_1V8	0110 100	52	54
UDT020 FAN_1V8	0110 101	53	55
PDT020 BULK_3V3	0110 110	54	56

2355

2356 Note that a number of addresses are reserved:

2357 0:12, 40, 44, 45, 55, 64:68, 72:75, 99, 120:127 all in decimal.

2358 The MSB of the address of the GE/TI converters must be zero.

2359 Decimal means take the whole 7 bit I2C address and represent it as a decimal number.

2360 TI-GE Octal means take the 6 least significant address binary bits and represent them as 2
 2361 octal digits, i.e. the setup of the address programming resistors on the TPS40400.

IPMC: HW-Adrs, Handle Switch, IPMBus

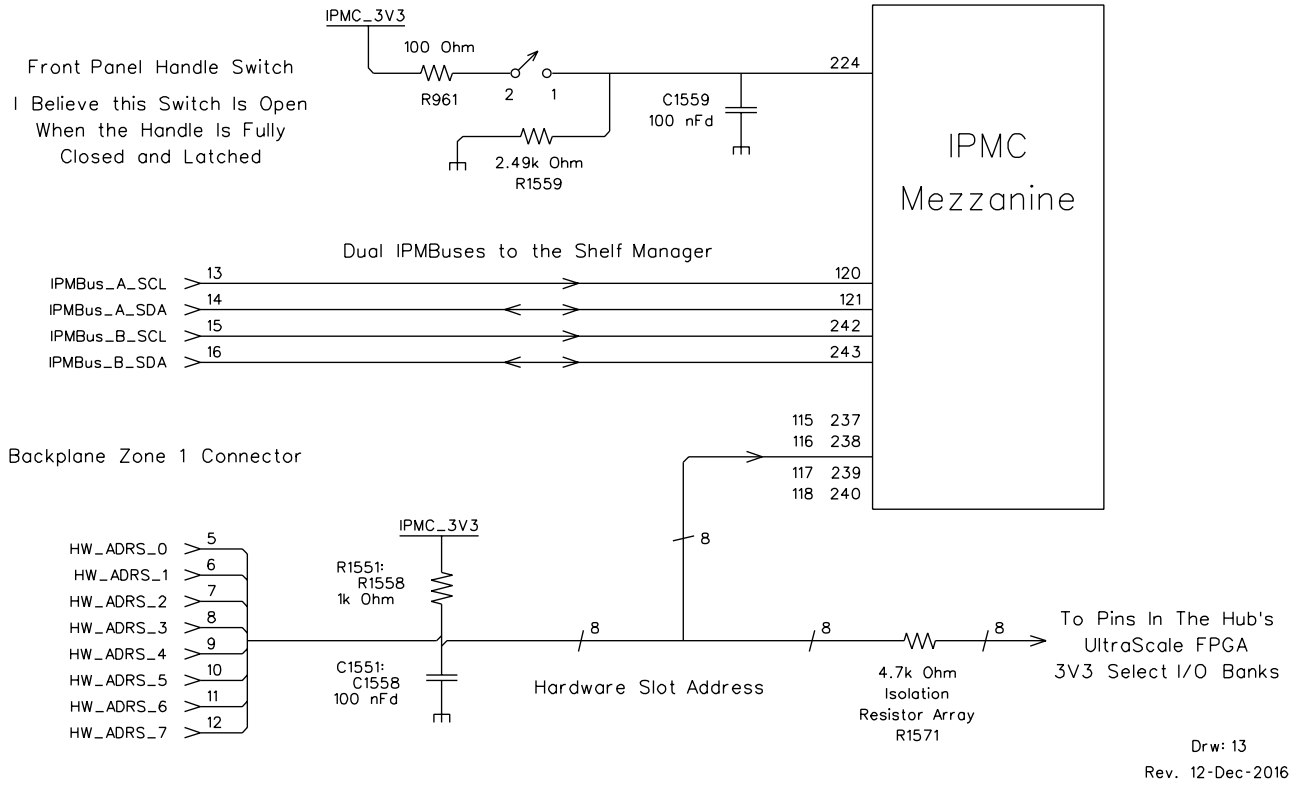
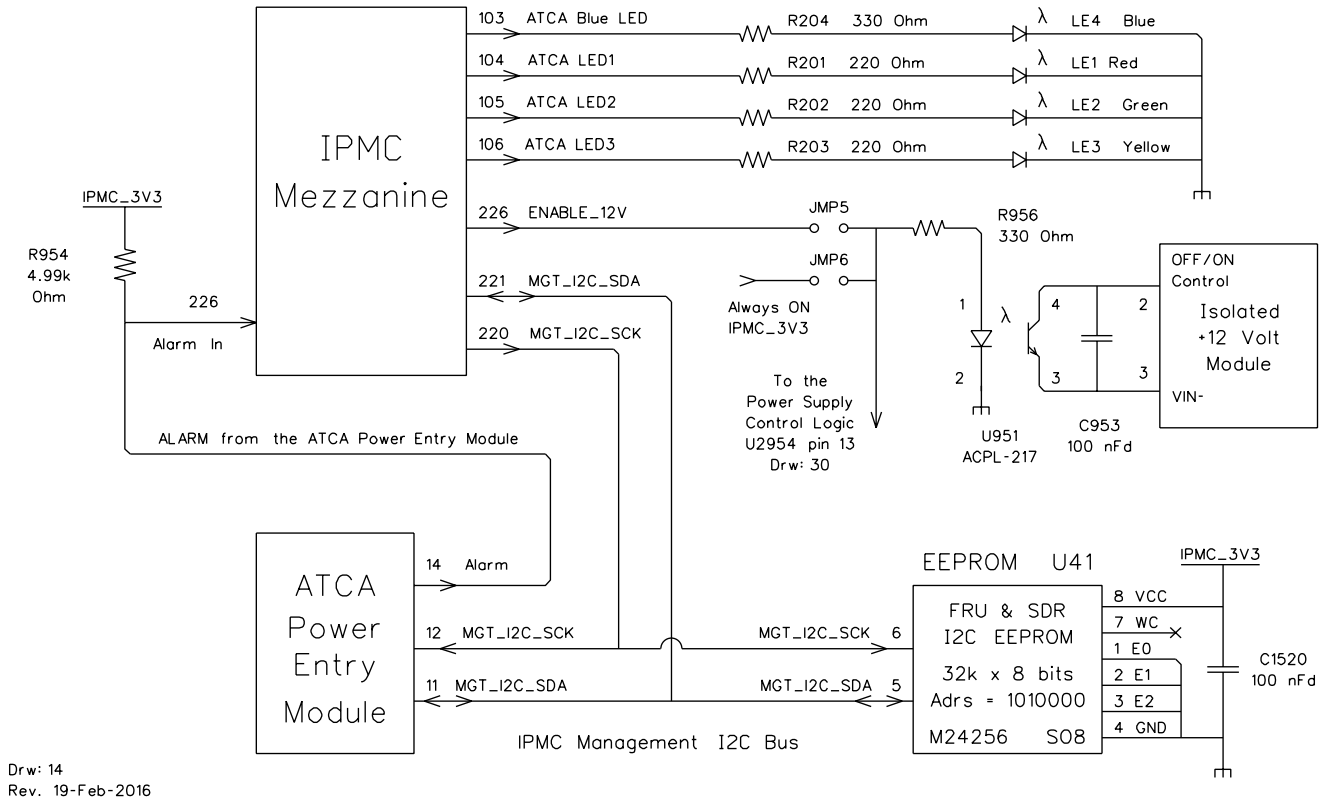


Figure 33: Hub IPMC circuit diagram (1/3)

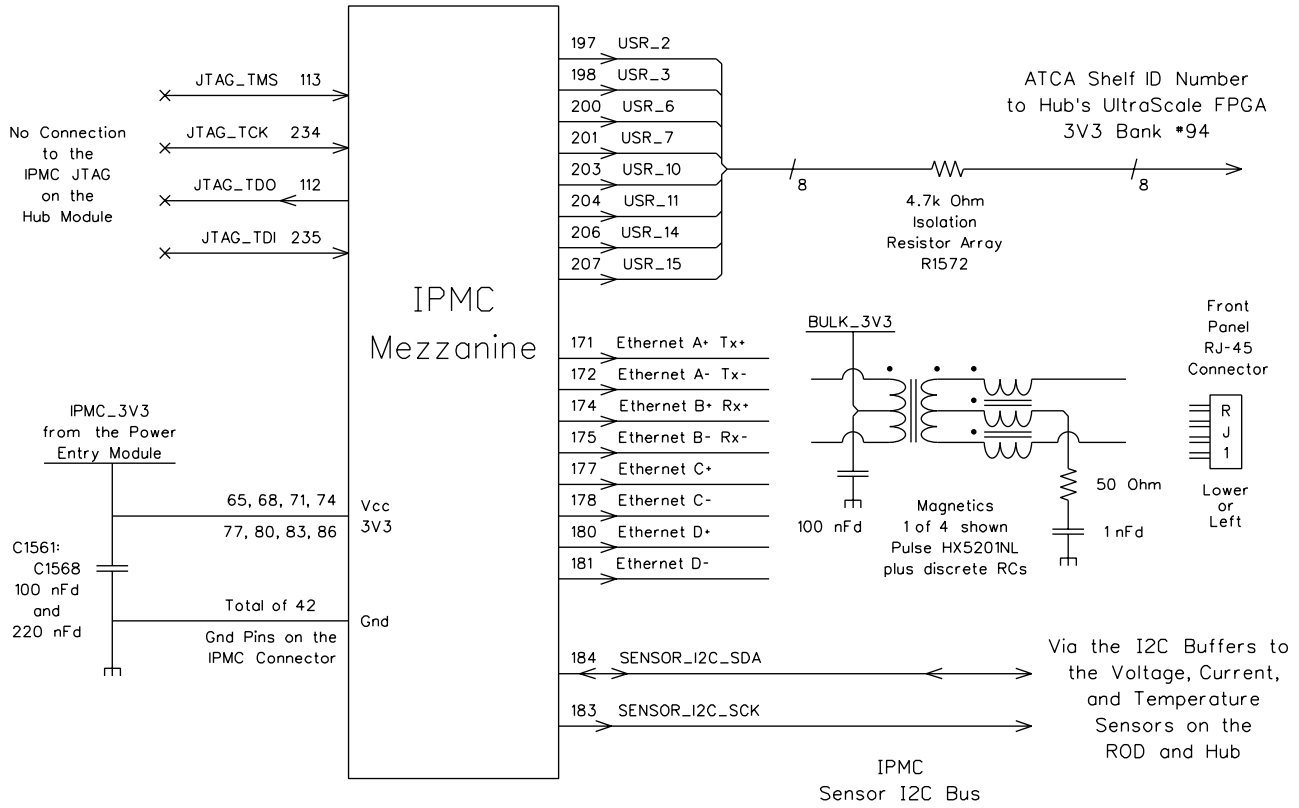
IPMC: Power Entry Alarm, Mgt. I2C, Payload Enable, LEDs



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Figure 34: Hub IPMC circuit diagram (2/3)

IPMC: Vcc-Gnd, Ethernet, User I/O, JTAG, Sensor I2C



Rev. 12-Dec-2016

Drw: 16

Figure 35: Hub IPMC circuit diagram (3/3)

Hub-Module IPMC Sensor I2C Bus

3x DISCEN pulled to 3V3 with 10k R1503, R1513, R1523. Hi enables the Auto-Disconnect.

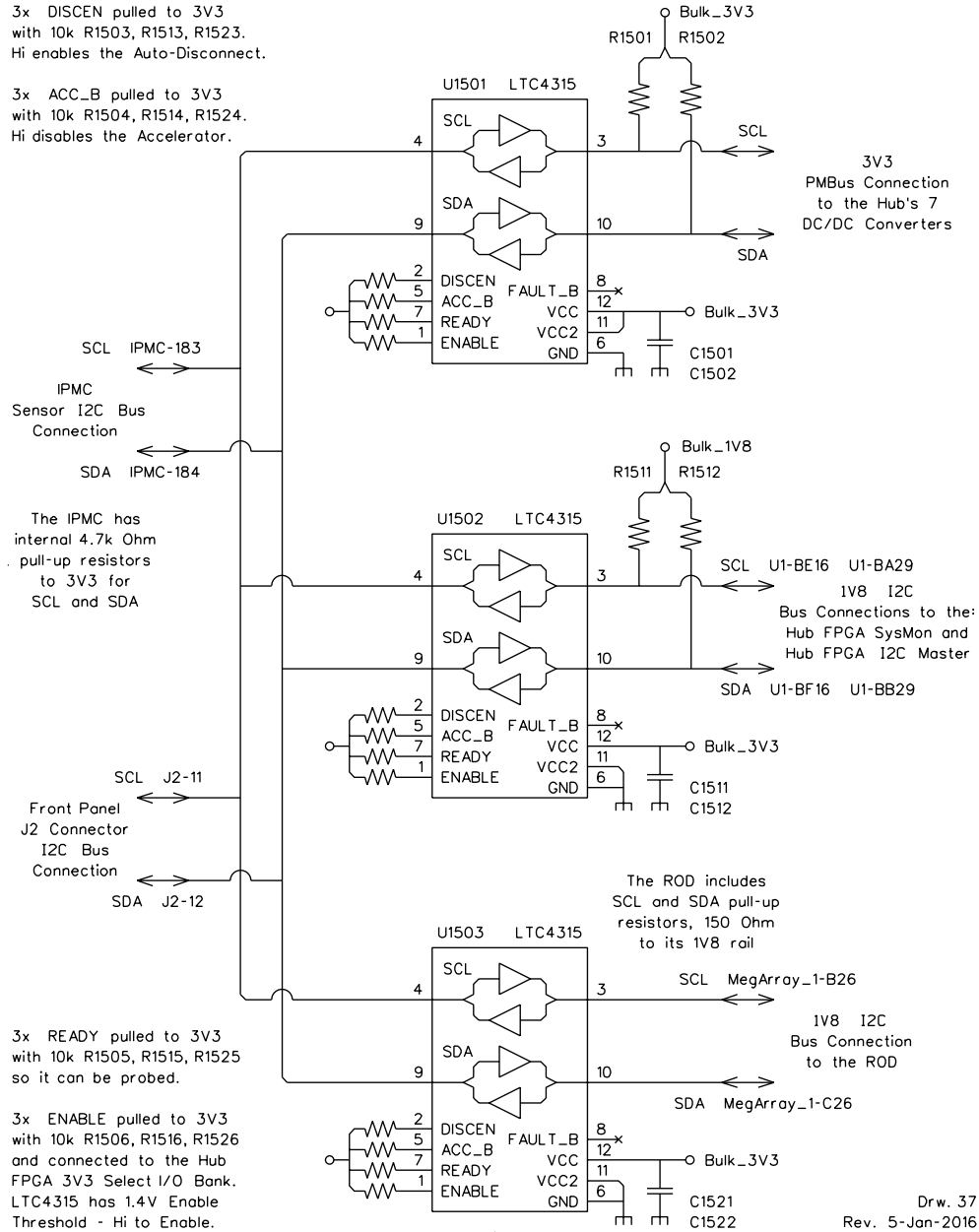
3x ACC_B pulled to 3V3 with 10k R1504, R1514, R1524. Hi disables the Accelerator.

The IPMC has internal 4.7k Ohm pull-up resistors to 3V3 for SCL and SDA

The ROD includes SCL and SDA pull-up resistors, 150 Ohm to its 1V8 rail

3x READY pulled to 3V3 with 10k R1505, R1515, R1525 so it can be probed.

3x ENABLE pulled to 3V3 with 10k R1506, R1516, R1526 and connected to the Hub FPGA 3V3 Select I/O Bank. LTC4315 has 1.4V Enable Threshold - Hi to Enable.



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2371

2372

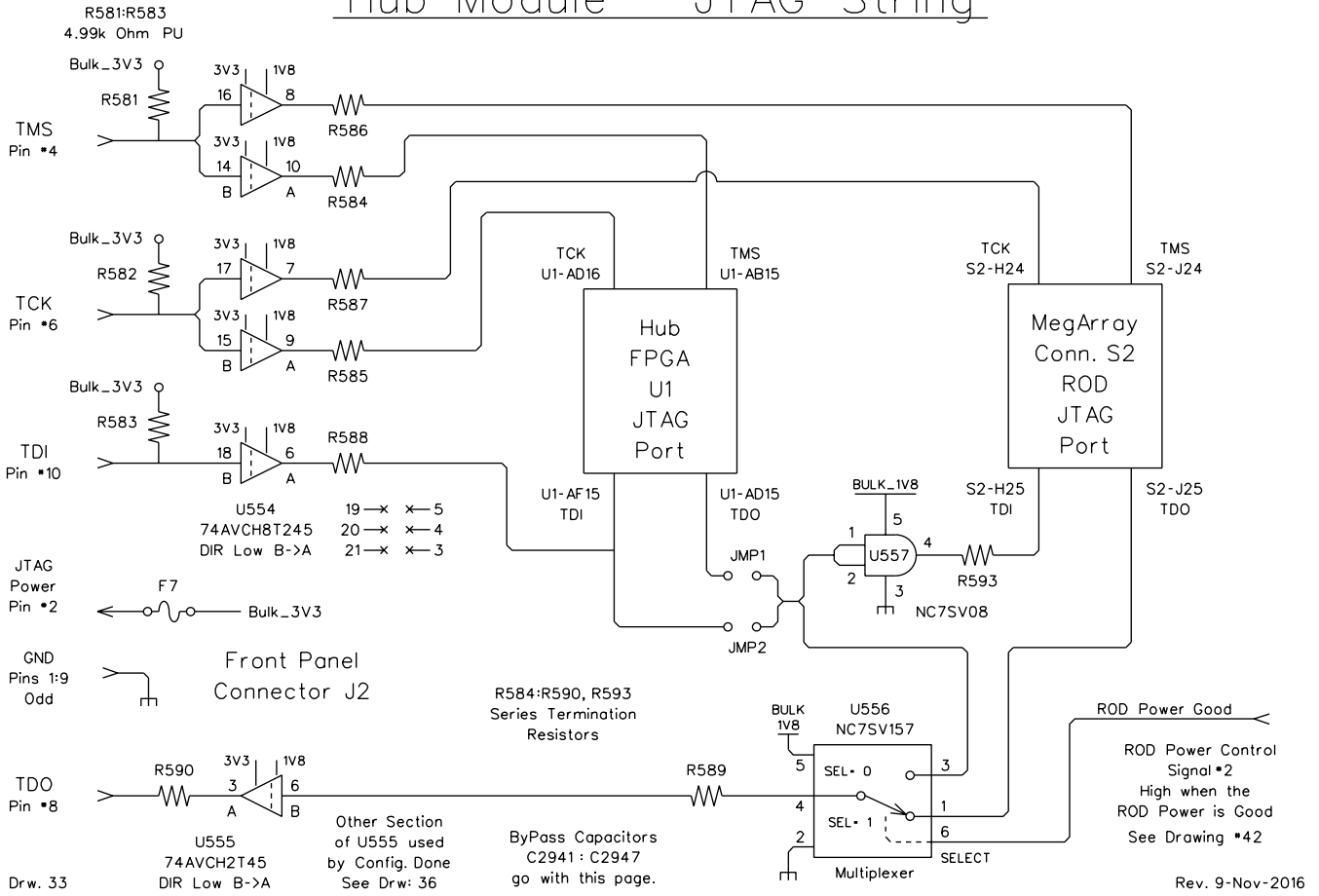
2373

2374

Figure 36: Hub I2C sensor bus circuit diagram.

2375

Hub-Module JTAG String



2408

~ ~ ~

Figure 37: Hub circuit diagram for JTAG string.

2410

2411 **23 Appendix 10: Hub-Module Jumpers**

2412 This note collects in one place a description of all of the jumpers on the Hub Module except
2413 for the jumpers associated with the 3 Switch Chips. The Switch Chip jumper are described
2414 in Section 30.

2415 All of these jumpers are typically used to control various functions on the Hub Module that
2416 need to be defined during the power up process or that can not be controlled through IPBus
2417 registers.

2418 **23.1 IPMC Ethernet A/Tx, B/Rx, Mag CT to 3V3, R1405 & R1410**

2419 IPMC Ethernet A/Tx B/Rx circuits magnetics primary side center tap connection to the
2420 3.3V bus. The issue is that all of the connections to the Hub's Ethernet Magnetics use
2421 modern "voltage mode" connections except for the IPMC. The IPMC uses an old "current
2422 mode" National/TI DP83848 Phys chip. This current mode connection to the Magnetics
2423 requires that the center taps on the primary side be connected to the 3V3 bus. The normal
2424 100 nFd capacitor from the primary center taps to ground is used for either voltage mode or
2425 current mode connections to the Magnetics.

2426 The two jumpers that make these connections are R1405 and R1410.

2427 Default setup:

2428 For the current version of the IPMC with a current mode Phys chip we need to install
2429 both of these jumpers to tie the center taps to 3V3. These are Zero_Ohm jumpers. If a
2430 newer version of the IPMC is ever made then we may need to remove these jumpers.

- 2431 • R1405 R1410 Installed

2432 **23.2 Virtex FPGA Configuration Mode R1811 through R1816**

2433 These 6 jumpers control the M2, M1, and M0 Configuration Mode pins on the Virtex FPGA.
2434 Normally this FPGA is Configured via Master BPI mode from its dedicated Parallel NOR
2435 Flash Memory device U25. The Master BPI mode requires the three M lines to be set: 0,1,0.

2436 Never install both the HI and LOW jumpers for a given signal. Installed jumpers are to be
2437 100 Ohm resistors.

2438 Install R1816 to pull M2 LOW R1815 to pull M2 HI

2439 Install R1814 to pull M1 LOW R1813 to pull M1 HI

2440 Install R1812 to pull M0 LOW R1811 to pull M0 HI

2441 Default setup:

2442 Select Master BPI Configuration Mode.

2443 Set M2, M1, M0 to: 0, 1, 0.

- 2444 • R1812, R1813, R1816 Installed
-

- 2445 • R1811, R1814, R1815 NOT installed

2446 **23.3 Power On Reset Delay Override R1821 and R1822**

2447 These two jumpers control how long the FPGA waits after it has powered up until it begins
2448 its Configuration process. This delay allows time for the Parallel NOR Flash Configuration
2449 Memory to wake up and get itself organized. The options are Standard Delay or Shorter
2450 Delay. These two jumpers control the state of the FPGA's POR_OVERRIDE pin.

2451 Never install both the Standard and Short Delay jumpers at the same time. These are Zero
2452 Ohm jumpers.

- 2453 Install R1821 for a Shorter Delay
- 2454 Install R1822 for a Standard Delay
- 2455

2456 Default Setup:

2457 We want the Standard Delay.

- 2458 • R1822 Installed
- 2459 • R1821 NOT Installed

2460 **23.4 Configuration Bank Voltage Select R1823 and R1824**

2461 These two jumpers are used to VCCO voltage range of BANK 0 and of the Configuration
2462 part of Bank 65 during Configuration. The two ranges are: 3V3/2V5 and 1V8 and under.
2463 These jumpers control the state of the FPGA's CFGBVS_0 pin.

2464 Never install both jumpers at the same time.

2465 These are Zero Ohm jumpers.

- 2466 Install R1823 for 3V3/2V5 voltage range Configuration
- 2467 Install R1824 for 1V8 and under voltage range Config

2468 Default Setup:

2469 We need the 1V8 and under voltage range Configuration.

- 2470 • R1824 Installed
- 2471 • R1823 NOT Installed

2472 **23.5 Pull-Ups During Configuration R1825 and R1826**

2473 These two jumpers are used to control whether or not the FPGA turns on weak pull-ups
2474 during its Configuration process. The weak pull-ups are on all of its Select I/O pins and can
2475 be used to define a fixed state of these CMOS signals during the Configuration process, i.e.
2476 no floating receiver inputs. These two jumpers control the state of the FPGA's PUDC_B_0
2477 pin.

2478 Never install both jumpers at the same time.

2479 These are 100 Ohm jumpers.

2480 1. Install R1825 to turn OFF the weak pull-ups

2481 2. Install R1826 to turn ON the weak pull-ups

2482 during Configuration

2483 Default Setup:

2484 We select to turn on weak pull-ups during Configuration.

2485 • R1826 Installed

2486 • R1825 NOT Installed

2487 **23.6 VBATT R1827**

2488 Jumper R1827 connects the FPGA's VBATT pin to ground.

2489 Default Setup:

2490 We are not using VBATT so we want to connect this FPGA pin to Ground. This is a
2491 Zero Ohm jumper.

2492 • R1827 Installed

2493 **23.7 JTAG Skip the Hub FPGA JMP1 and JMP2**

2494 Jumpers JMP1 and JMP2 control whether or not the JTAG string on the Hub Module
2495 includes the Hub's Virtex FPGA. Normally we want to include the Hub's FPGA in the
2496 JTAG string. Install either JMP1 or JMP2 - never install both at once.

2497 Install JMP1 (and remove JMP2) to include the

2498 Hub's FPGA in the JTAG string

2499 Install JMP2 (and remove JMP1) to skip over the

2500 Hub's FPGA in the JTAG string

2501 Default Setup:

2502 We want to include the Hub's FPGA in the JTAG string.

2503 • JMP1 Installed

2504 • JMP2 NOT Installed

2505 **23.8 DONE Included in ROD Power Control JMP3 and JMP4**

2506 Jumpers JMP3 and JMP4 control whether or not the Hub FPGA Configuration DONE signal
2507 is included in the "AND" gate that generates the power enable signal to the ROD mezzanine
2508 card.

Option	Pull-Up	Pull-Down
PHYAD0	R1901	R1902
PHYAD1	R1903	R1904
PHYAD2	R1905	R1906
Mode_0	R1911	R1912
Mode_1	R1909	R1910
Mode_2	R1908	---
Mode_3	R1907	---
CLK125_EN	R1913	---
LED_Mode	R1914	---

2546

2547

2548 This table shows the Reference Designators for Phys chip U21. Phys chips U22 has the same
2549 setup but its Reference Designators are higher by 50.

2550 In all cases, if installed, the pull-up resistor should be 10k Ohms and the pull-down resistor
2551 should be 1k Ohm.

2552 The PHYADx jumpers set the address of the Management Interface Port on the
2553 KSZ9031RNX. The Management Port PHYAD bits 3 and 4 are internally always set to 0,0.
2554 To set one of these three PHYAD bits HI install the associated pull-up resistor. To set one
2555 low install the pull-down resistor.

2556 The Hub Module provides easy control of only the Mode_0 and Mode_1 lines. This provides
2557 the following 4 options for the Phys chip (Mode bits listed Mode_3, ..., Mode_0).

2558 1100 RGMII 1000 Base-T fullduplex only
2559 1101 RGMII 1000 Base-T full or half duplex
2560 1110 RGMII 10/100/100 all but 1000 half duplex
2561 1111 RGMII 10/100/1000 full or half duplex
2562

2563 CLK125_EN is pulled up by R1913 thus enabling the Phys chip to send its 125 MHz clock
2564 back to the MAC in the Hub's FPGA.

2565 LED_Mode is pulled up by R1914 thus setting up the Phys chip for Single LED mode.

2566 Default Setup:

2567 Note that Phys chips U21 and U22 are setup with the same Management Port PHYAD
2568 which is OK because they each have their own private Management Power connection in
2569 the Hub's FPGA.

- 2570 • PHYADx:
 - 2571 ○ Set the 3 controllable PHYAD lines Low.
 - 2572 ○ Install 1k Ohm in R1902, R1904, R1906.
 - 2573 ○ Leave R1901, R1903, R1905 open.
- 2574 • Mode:
 - 2575 ○ Set all Mode lines Hi.
 - 2576 ○ Install 10k Ohm in R1907 R1908 R1909 and R1911.
 - 2577 ○ Leave R1910 and R1912 open.

- 2578 • *CLK125_EN:*
- 2579 ○ *Enable the 125 MHz Clock.*
- 2580 ○ *Install a 10k Ohm resistor in R1913.*
- 2581 • *LED_Mode:*
- 2582 ○ *Enable Single LED Mode.*
- 2583 ○ *Install a 10k Ohm resistor in R1914.*

2584 **23.11 DCDC Converter with LC Output Filter Feedback Jumpers**

2585 3 of the DCDC Converters on the Hub Module include an LC Output Filter to reduce the
 2586 switching noise that is present in their output voltage. These 3 converters include jumpers to
 2587 provide some options in how their control loop feedback is setup. These 3 converters and
 2588 their jumpers are:

2589

DCDC-2 MGT_AVCC	JMP1051	JMP1052	JMP1053	JMP1054
DCDC-3 MGT_AVTT	JMP1101	JMP1102	JMP1103	JMP1104
DCDC-7 FAN_1V8	JMP1301	JMP1302	JMP1303	JMP1304

2590

2591 Jumpers JMP1051, JMP1052 (and JMP1101, JMP1102 and JMP1301, JMP1302) control
 2592 whether the the V_SENSE_+ feedback is taken before or after the output filter inductor.
 2593 JMP1051 selects before the output inductor and JMP1052 selects after the inductor.

2594 Jumpers JMP1053, JMP1054 (and JMP1103, JMP1104 and JMP1303, JMP1304) control
 2595 whether the the RC coupled feedback is taken before or after the output filter inductor.
 2596 JMP1053 selects before the output inductor and JMP1054 selects after the inductor.

2597 During initial pro-type manufacturing none of these 4 jumpers will be installed by the
 2598 assembly company.

2599 **23.12 ATCA “Shelf Ground” to “Logic Ground” Connection R959**

2600 ATCA Specification 4.96 requires a jumper that can optionally macke a connection between
 2601 the ATCA Shelf Ground and the ATCA Logic Ground. On the Hub Module this optional
 2602 link between these ground systems is made by R959.

2603 Install a zero Ohm jumper at R959 to connect the Shelf and Logic Grounds.

2604 Note that one could also use a high value resistor so that there are not significant currents
 2605 or loops between these two ground systems will still providing a path to remove static
 2606 charge from the card.

2607 Default Setup:

2608 A 1 Meg Ohm resistor will be installed in location R959.

2609 **23.13 Jumper on the Sensor I2C Bus EEPROM**

2610 U1541 is a soic_8 location that can hold a M24256 EEPROM that appears on the Hub's
2611 Sensor I2C bus. There are 4 jumpers associated with the operation of the EEPROM.

- 2612 3. JMP1541 controls the chip's E0 Enable pin (aka Address Select)
- 2613 4. JMP1542 controls the chip's E1 Enable pin (aka Address Select)
- 2614 5. JMP1543 controls the chip's E2 Enable pin (aka Address Select)
- 2615 Zero Ohm jumper install --> Enable pin is Hi

2616 Open --> Enable pin is Low

2617 JMP1544 controls the chip's WC_B pin

2618 Zero Ohm jumper install --> WC_B pin is Hi

2619 --> Write operations are Disabled

2620 Open --> WC_B pin is Low

2621 --> Write operations are Enabled

2622

2623 Default Setup: Neither U1541 or any of the jumpers JMP1541:JMP1544 are installed.

2624

2625 **24 Appendix 11: Hub-Module Front Panel LEDs**

2626 This note collects the information about the LED displays that are used on the front panel of
2627 the Hub Module. The Hub Module includes front panel LEDs to indicate the following:

- 2628 • Four that are required by the ATCA format and are managed by the IPMC mezzanine
 - 2629 ○ Mandatory LED_1
 - 2630 ○ Optional LED_2
 - 2631 ○ Optional LED_3
 - 2632 ○ Mandatory Blue
- 2633 • Two general health/rationality LEDs
 - 2634 ○ Has the IPMC Enabled the Pay Load Power ?
 - 2635 ○ Are all of the Hub's DCDC Converters running OK ?
- 2636 • Five LEDs for the ROD Mezzanine
- 2637 • Three LEDs for the Hub Module that are managed by the Hub's Virtex FPGA.
- 2638 • Six RJ-45 Ethernet connectors with 2 LEDs each
 - 2639 ○ RJ1 Upper/Right for This Hub's IPMC
 - 2640 ○ *RJ1 Lower/Left for This Hub's ROD Mezzanine FPGA*
 - 2641 ○ *RJ2 Upper/Right for This Hub's Switch Chip "C"*
 - 2642 ○ *RJ2 Lower/Left for This Hub's Switch Chip "A"*
 - 2643 ○ *RJ3 Upper/Right for This Hub's Switch Chip "B"*
 - 2644 ○ *RJ3 Lower/Left for This Hub's Switch Chip "B"*
- 2645 • Two LEDs each for 20 other Ethernet connections
 - 2646 ○ Switch Ports to the FEXs
 - 2647 ○ *1 This Hub's Switch Port to the Other Hub's FPGA*
 - 2648 ○ *1 This Hub's Switch Port to This Hub's FPGA*
 - 2649 ○ 1 This Hub's FPGA Phys to the Other Hub's Switch
 - 2650 ○ 1 This Hub's FPGA Phys to This Hub's Switch
 - 2651 ○ *1 Switch Chip "A" side of A <--> B connection*
 - 2652 ○ *1 Switch Chip "B" side of A <--> B connection*
 - 2653 ○ *1 Switch Chip "B" side of B <--> C connection*
 - 2654 ○ *1 Switch Chip "C" side of B <--> C connection*
 - 2655

2656 This is a total of 66 front panel LEDs. An illustration of the layout of these LEDs on the
2657 front panel is shown in **Figure 38**, **Figure 39** and **Figure 40**.

2658 The 4 ATCA LEDs use the 3mm Mentor 1271.100x "single column" light pipes to reach the
2659 front panel.

2660 The 2 General Health LEDs also use the same 3mm Mentor 1271.100x light pipes.

2661 The 5 ROD LEDs, and the 3 Hub LEDs, and the 40 "Other Ethernet Connections" LEDs use
2662 the 2mm Mentor 1296.10x4 light pipe array. This is a 4 column light pipe array. They are
2663 layed out in a 4x2 array and a 4x10 array.

2664 The Hub Module uses SMD LEDs on side 1 of the PCB and light pipe assemblies to route
2665 them to the front panel. This design is driven by the need to place the required ATCA LEDs
2666 in specific locations and to use very little space along the West edge of the card for these
2667 LEDs.

2668 The LEDs are in two categories: single column and 4 column. Note that in this document
2669 the words row and column refer to viewing the Hub Module from the front as it normally
2670 looks when plugged into a crate, i.e. columns are vertical along the long axis of the front
2671 panel.

2672 The single column setup has a 3.0 mm diameter light pipe that is centered 5.08 mm to the
2673 right of the side 1 surface of the PCB. This uses a Mentor 1271.100x light pipe and an
2674 Osram LED:

2675 LxT673 P-LLC-2 3.0x3.4 package Vf Blue typ 2.9/3.1 at 5/10 mA

2676 Hyper TOPLED Blue, Green Vf Grn typ 2.8/3.0 at 5/10 mA

2677 2006

2678 LxT676 P-LLC-2 3.0x3.4 package Vf Red typ 1.9/1.95 at 5/10 mA

2679 Hyper TOPLED Red, Yellow Vf Yel typ 1.9/1.95 at 5/10 mA

2680 2007

2681

2682 Many other Osram parts in the 2-PLCC Advanced Power TOPLEDs are available.

2683

2684 The 4 column setup has 1.95 mm Mentor 1296.10x4 light pipes. The first light pipe is
2685 centered 2.54 mm to the right of the side 1 surface of the PCB. The next light pipe is
2686 centered 2.54 mm to the right of the first one and so on. Center to Center the rows are spaced
2687 by 5.08 mm. This provides some limited space for labels. This 4 column setup with the
2688 Mentor 1296.10x4 light pipe array uses an Osram LED in the 0805 case size package:

2689 LG R971 green Vf about 2.0 to 2.1 at 5 to 10 mA

2690 LS R976 super red Vf about 1.9 at 5 to 10 mA

2691 LY R976 yellow Vf about 1.9 at 5 to 10 mA

2692

2693 Many other 0805 case size types are available from Osram for example: LH R974 hyper red.

2694 Ed needs a blue LEDs in this 4 column setup for the ROD display. Osram does not seem to
2695 make one in the correct package to work with the Mentor 1296.10x4 light pipes. The
2696 problem is to find a quality blue LED in the 0805 package size with the right optics to put
2697 light into the light pipe and the same suggested PCB layout pattern. So far the Avago
2698 HSMR-C170 looks OK except for the PCB layout pattern.

2699 **24.1 LEDs Driven by the IPMC Mezzanine**

2700 These are the 4 ATCA Status LEDs that are driven by the IPMC mezzanine card. I believe
 2701 that the IPMC mezzanine directly drives the anodes of these LEDs through series resistors
 2702 and that the cathodes of these LEDs are just tied to ground. See also the 2 IPMC Ethernet
 2703 LEDs that are listed below under “not driven”.

LED Ref Desgntnr	Display	Source -Pin
LE1	ATCA Mandatory Red LED_1	IPMC Mezz Socket 104
LE2	ATCA Optional Green LED_2	IPMC Mezz Socket 105
LE3	ATCA Optional Red LED_3	IPMC Mezz Socket 106
LE4	ATCA Mandatory Blue	IPMC Mezz Socket 103

2704

2705 **24.2 LEDs Driven by the Switch Chips**

2706 The switch chips used in the Hub module can drive up to 4 LEDs per ethernet port. Control
 2707 registers in these chips allow you to select what types of information about a given ethernet
 2708 port are displayed on its LEDs.

2709 The Hub module provides 2 LEDs per switch chip ethernet port. By default one of these
 2710 LEDs shows if the port is operating at 10/100 vs 1000 speed and the other LED shows if a
 2711 connection exists on that port and when a connection exists whether or not it is currently
 2712 moving data.

2713 In the following table for LE5:LE40, the Speed LED is Green and the Link Activity LED is
 2714 Yellow.

2715 In the section of the table that describes the front panel RJ-45 connectors recall that these are
 2716 TE Connectivity part number 1888653-4 “condo” connectors. The -4 indicates the LED
 2717 colors for each socket:

TE Part No.	LED_1	LED_2	LED_3	LED_4
-----	-----	-----	-----	-----
1888653-4	Green	Green	Yellow	Yellow

2721

2722 Note, if we change which switch port is connected to which Base Interface target then we
 2723 should also change the connections to these LEDs to keep them in rational BI Channel order.

2724 Recall which 53128 Switch Chip LED Pin is used to indicate what information about a given
 2725 53128 Switch Chip Port:

2726

Link Speed			Link Active		
Port	Pin Num	Pin Name	Port	Pin Num	Pin Name

7	168	LEDP0	7	170	LEDP1
6	174	LEDP4	6	175	LEDP5
5	178	LEDP8	5	179	LEDP9
4	184	LEDP12	4	185	LEDP13
3	189	LEDP16	3	190	LEDP17
2	194	LEDP20	2	195	LEDP21
1	198	LEDP24	1	199	LEDP25
0	256	LEDP28	0	1	LEDP29

2727

2728 These are the switch chip port numbers as defined in the 53128 documentation.

2729 The switch chip LEDs are arranged on the Hub module front panel in the following way:

LED Ref Desgnt	Display	Source	Pin
LE5	BI "Channel 2" Speed Grn	Sw Chip B Port 5	LED8-178
LE6	BI "Channel 2" Lnk-Act Yel	Sw Chip B Port 5	LED9-179
LE7	BI Channel 3 Speed Grn	Sw Chip C Port 5	LED8-178
LE8	BI Channel 3 Lnk-Act Yel	Sw Chip C Port 5	LED9-179
LE9	BI Channel 4 Speed Grn	Sw Chip C Port 4	LED12-184
LE10	BI Channel 4 Lnk-Act Yel	Sw Chip C Port 4	LED13-185
LE11	BI Channel 5 Speed Grn	Sw Chip C Port 3	LED16-189
LE12	BI Channel 5 Lnk-Act Yel	Sw Chip C Port 3	LED17-190
LE13	BI Channel 6 Speed Grn	Sw Chip C Port 2	LED20-194
LE14	BI Channel 6 Lnk-Act Yel	Sw Chip C Port 2	LED21-195
LE15	BI Channel 7 Speed Grn	Sw Chip C Port 1	LED24-198
LE16	BI Channel 7 Lnk-Act Yel	Sw Chip C Port 1	LED25-199
LE17	BI Channel 8 Speed Grn	Sw Chip C Port 0	LED28-256
LE18	BI Channel 8 Lnk-Act Yel	Sw Chip C Port 0	LED29-1
LE19	BI Channel 9 Speed Grn	Sw Chip A Port 5	LED8-178
LE20	BI Channel 9 Lnk-Act Yel	Sw Chip A Port 5	LED9-179
LE21	BI Channel 10 Speed Grn	Sw Chip A Port 4	LED12-184
LE22	BI Channel 10 Lnk-Act Yel	Sw Chip A Port 4	LED13-185
LE23	BI Channel 11 Speed Grn	Sw Chip A Port 3	LED16-189
LE24	BI Channel 11 Lnk-Act Yel	Sw Chip A Port 3	LED17-190
LE25	BI Channel 12 Speed Grn	Sw Chip A Port 2	LED20-194
LE26	BI Channel 12 Lnk-Act Yel	Sw Chip A Port 2	LED21-195
LE27	BI Channel 13 Speed Grn	Sw Chip A Port 1	LED24-198
LE28	BI Channel 13 Lnk-Act Yel	Sw Chip A Port 1	LED25-199
LE29	BI Channel 14 Speed Grn	Sw Chip A Port 0	LED28-256
LE30	BI Channel 14 Lnk-Act Yel	Sw Chip A Port 0	LED29-1
LE31	SW to Hub FPGA Speed Grn	Sw Chip B Port 4	LED12-184
LE32	Sw to Hub FPGA Lnk-Act Yel	Sw Chip B Port 4	LED13-185
LE33	Sw B to Sw A Speed Grn	Sw Chip B Port 2	LED20-194
LE34	Sw B to Sw A Lnk-Act Yel	Sw Chip B Port 2	LED21-195
LE35	Sw B to Sw C Speed Grn	Sw Chip B Port 3	LED16-189
LE36	Sw B to Sw C Lnk-Act Yel	Sw Chip B Port 3	LED17-190
LE37	Sw A to Sw B Speed Grn	Sw Chip A Port 7	LED0-168
LE38	Sw A to Sw B Lnk-Act Yel	Sw Chip A Port 7	LED1-170
LE39	Sw C to Sw B Speed Grn	Sw Chip C Port 7	LED0-168
LE40	Sw C to Sw B Lnk-Act Yel	Sw Chip C Port 7	LED1-170

And now the RJ-45 LEDs driven by the Switch Chips

LED Ref Desgnt	Display	Source	Pin
LED_59	RJ2-LED2 Grn	RJ2 Upper or Right Sw Chip C Port 6	LED4-174
LED_60	RJ2-LED3 Yel	Sw Chip C Port 6	LED5-175
LED_61	RJ2-LED1 Grn	RJ2 Lower or Left Sw Chip A Port 6	LED4-174
LED_62	RJ2-LED4 Yel	Sw Chip A Port 6	LED5-175
LED_63	RJ3-LED2 Grn	RJ3 Upper or Right Sw Chip B Port 7	LED0-168
LED_64	RJ3-LED3 Yel	Sw Chip B Port 7	LED1-170
LED_65	RJ3-LED1 Grn	RJ3 Lower or Left Sw Chip B Port 6	LED4-174
LED_66	RJ3-LED4 Yel	Sw Chip B Port 6	LED5-175

2730

2731 **24.3 LEDs Driven by the Phys Chips on the Hub Module**

2732 The two KSZ9031RNX Phys chips on the Hub Module each drive two LEDs. These LEDs
 2733 are not directly driven by the Phys chips but rather they are driven through a buffer. The
 2734 Hub’s Phys chip LEDs are arranged on the front panel in the following way:

LED Ref Desgnt	Display	Source	Pin
LE41	Hub FPGA to Sw Link Grn	Phys U22	LED2-15
LE42	Hub FPGA to Sw Active Yel	Phys U22	LED1-17
LE43	Hub FPGA to BI Ch 2 Link Grn	Phys U21	LED2-15
LE44	Hub FPGA to BI Ch 2 Active Yel	Phys U21	LED1-17

2735

2736 **24.4 LEDs Driven by the ROD Mezzanine Card**

2737 The ROD mezzanine controls two types of LEDs on the Hub Module. It controls 5 LEDs
 2738 that indicate the “Status” of the ROD and it controls two LEDs that indicate the operation of
 2739 the ROD’s Ethernet Phys chip which is also a KSZ9031RNX.

2740 In all 7 cases the Hub module provides buffering for the 1V8 logic control signals that come
 2741 from the ROD for these LEDs. In all 7 cases the LED is illuminated when the control signal
 2742 from the ROD is Low.

2743 Note that an 8th control signal from the ROD is used to set the state of the front panel Lemo
 2744 connector on the Hub. The Hub provides an open collector driver for this Lemo. When this
 2745 control signal from the ROD is Hi then this open collector Lemo driver pulls down.

LED Ref Desgnt	Display	Source	Pin
LED_57	RJ1-LED1 RJ1 Lower or Left Lnk Grn	MegArray S1	B1
LED_58	RJ1-LED4 RJ1 Lower or Left Act Yel	MegArray S1	B2
LED_45	Prog_Done_LED_B Green	MegArray S1	B3

J1	LEMO not an LED	MegArray S1	B4
LED_46	Pwr_Good_LED_B Green	MegArray S1	C1
LED_47	SMB_Alert_LED_B RED	MegArray S1	C2
LED_48	GP_LED_B Blue	MegArray S1	C3
LED_49	Run_LED_B Blue	MegArray S1	C4

2746

2747

ROD MegArray Conn Specification			
MegArray S1 Pin#	Old Name	New Current Name	LED Color
B1	LED-0	Phy_LED2_B	Green
B2	LED-Y	Phy_LED1_B	Yellow
B3	LED-B	Prog_Done_LED_B	Green
B4	LEMO-0	LEMO not an LED	--
C1	LED-1	Pwr_Good_LED_B	Green
C2	LED-R	SMB_Alert_LED_B	RED
C3	LED-G	GP_LED_B	Blue
C4	LEMO-1	Run_LED_B	Blue

2748

2749 **24.5 LEDs Driven by the Hub Module’s FPGA**

2750 The Hub Module’s FPGA directly controls 3 Front Panel LEDs using 3 of its Select I/O signals. The
 2751 Hub provides buffers between its FPGA pins and these LEDs. The Select I/O signals that are used to
 2752 control these 3 LEDs are listed in Section 19.

2753

LED Ref Desgnt	Display	Source	Pin
LE50	Hub FPGA LED Grn	Hub FPGA Select I/O	--
LE51	Hub FPGA LED Yel	Hub FPGA Select I/O	--
LE52	Hub FPGA LED Red	Hub FPGA Select I/O	--

2754

2755 **24.6 LEDs NOT Driven by the IPMC Card’s Ethernet Connection**

2756 Besides the 4 “ATCA Status” LEDs listed above, the IPMC also could have driven LEDs
 2757 to indicate the operation of its Ethernet circuit. The IPMC uses a National/TI DP83848 Phys
 2758 chip which does directly drive LED but these pins were not routed out on the IPMC to its
 2759 edge connector. So as far as I know we cannot directly see the status of the ethernet
 2760 connection to the IPMC mezzanine card. There is still the issue of what to do with these
 2761 LEDs in the Hub’s RJ-45 Ethernet connector for the IPMC.

2762

LED Ref Desgnt	Display	Source	Pin
LED_55	RJ1-LED2 RJ1 Upper or Right Green	---	
LED_56	RJ1-LED3 RJ1 Upper or Right Yellow	---	

2763 **24.7 Two Rationality LEDs**

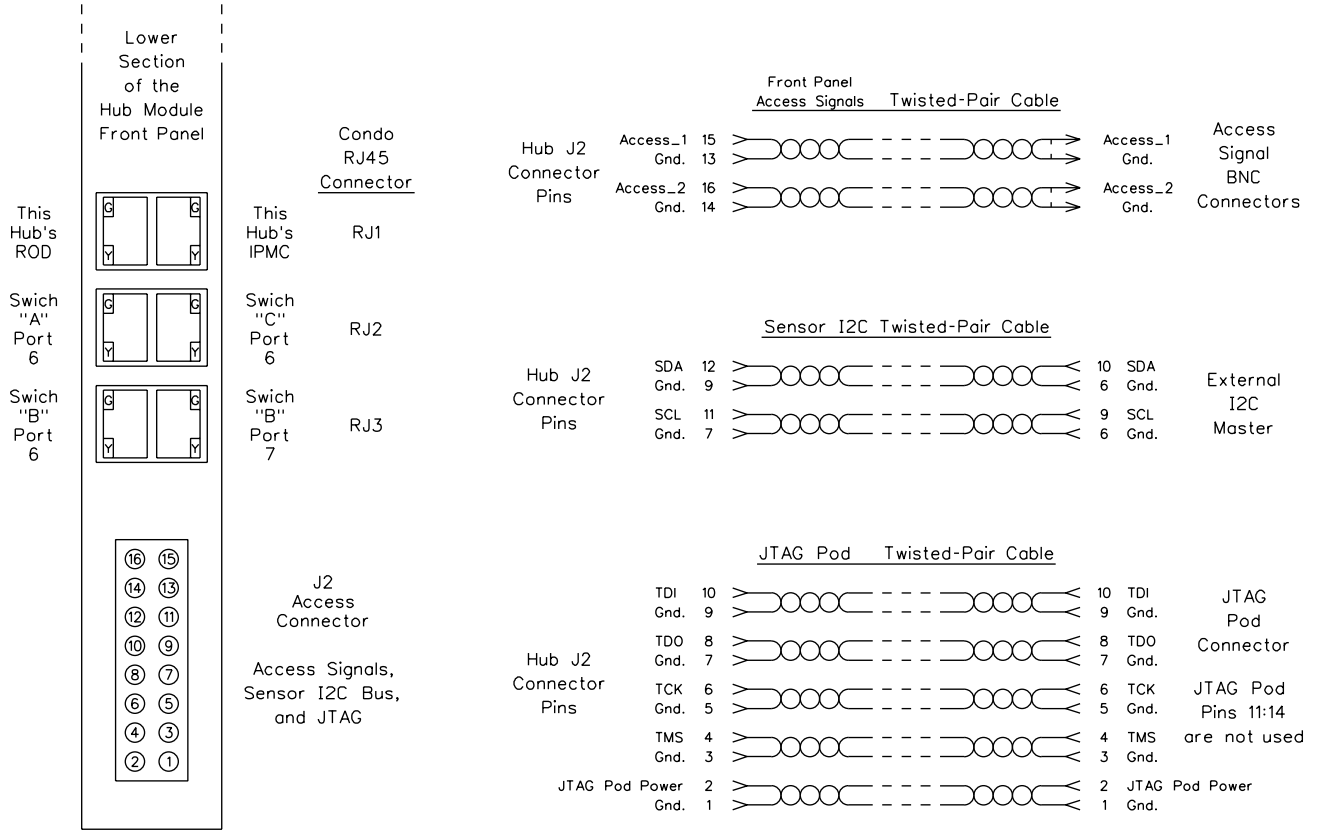
2764 There are two front panel LEDs that show the general health of the Hub Module. These two
2765 LEDs indicate to the user whether or not it is “rational” to consult the other LEDs on the
2766 card.

- 2767 • One of these LEDs (LED 53) shows whether or not the Isolated +12V supply is running.
2768 • The other LED (LED 54) shows whether or not all of the power buses on the Hub
2769 Module are operating within tolerance.
2770

2771 The cathode of the Iso +12V LED is connected to ground. The anode of this LED is
2772 connected through a series resistor to the Iso_12V bus. This is LED 53.

2773 The anode of the All Power OK LED is tied through a series resistor to the BULK_3V3 bus.
2774 The cathode of this LED is tied to the source of the low active All Power Is OK signal, i.e.
2775 U2961 pin 4. This is LED 54.

Hub Module Front Panel Connectors and Cables



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Figure 38: Illustration of Hub front-panel connections.

Hub - Front Panel Resources for ROD

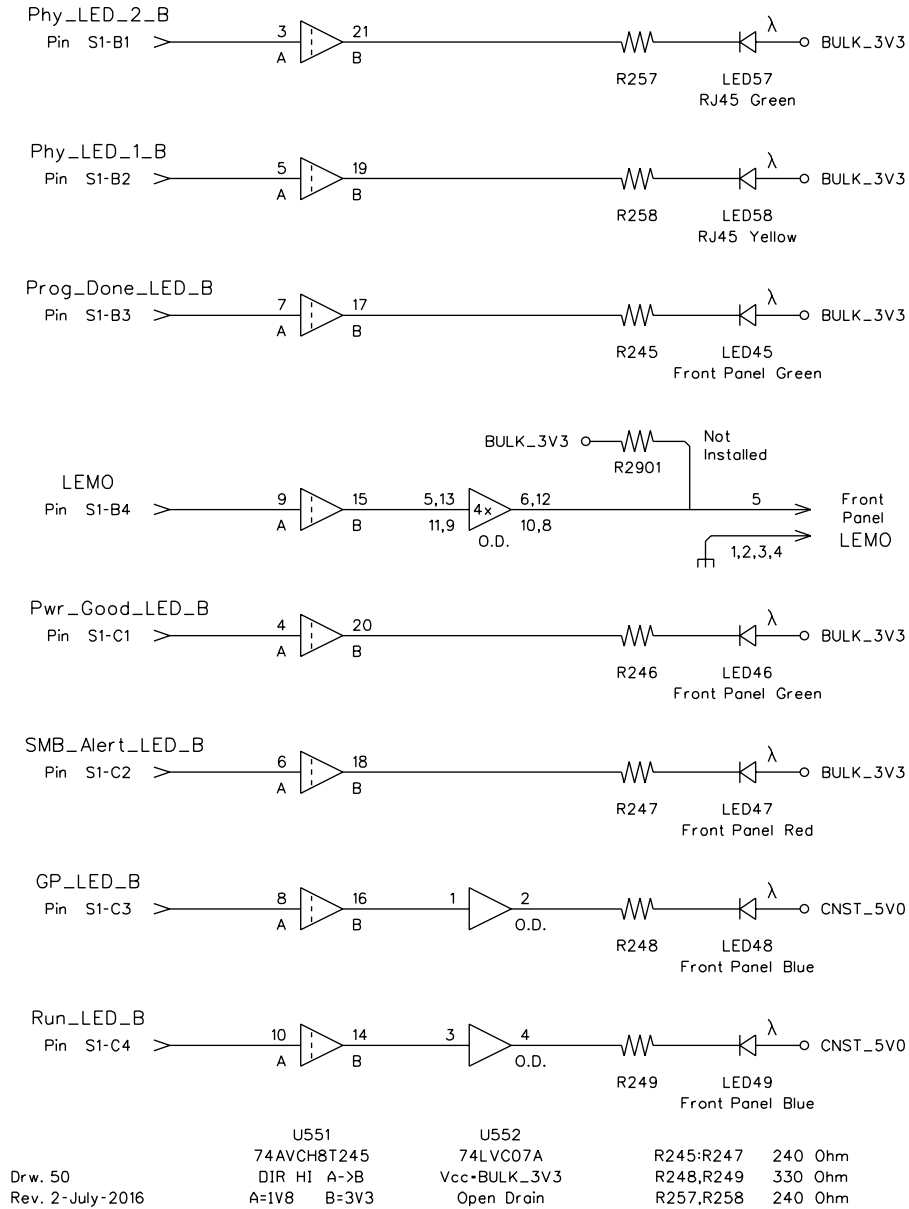
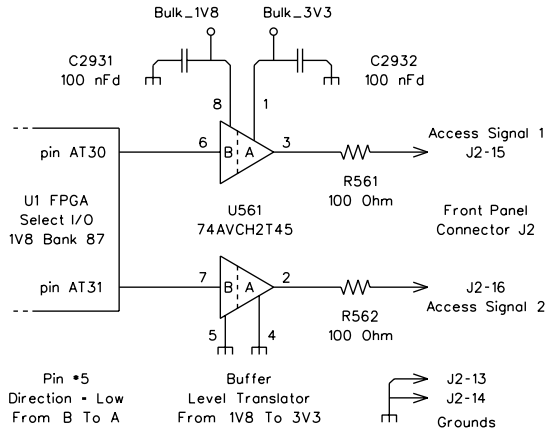


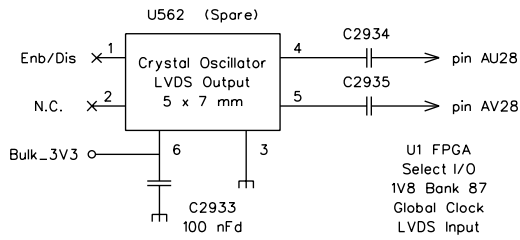
Figure 39: Hub front-panel resources for the ROD mezzanine.

Front Panel Access Signals and Spare Gates

Hub Module Access Output Signals



Hub Module Spare Clock Oscillator



Hub Module Spare Gates

U554 Translator pin 19 In pin 5 out
 U554 Translator pin 20 In pin 4 out
 U554 Translator pin 21 In pin 3 out

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Figure 40: Hub front-panel access signals and spare gates.

2779 **25 Appendix 12: Hub-Module MiniPOD Connections**

2780 The Hub Module includes 2 MiniPODs: 1 Transmitter MiniPOD and 1 Receiver MiniPOD.
2781 Details about the connections to a Hub Module MiniPOD are shown in **Figure 41**.

2782 Only 8 of the 12 channels in the Transmitter MiniPOD are connected to MGT transmitter
2783 outputs on the Hub's FPGA. MiniPOD fibers: 3, 5, 7, 9 are not connected to the FPGA.

2784 The 8 attached MiniPOD fibers are connected to MGT output ports in the following order:

Transmitter MiniPOD Fiber	MGT Quad and Port
0	227 Tx2
1	227 Tx0
2	226 Tx2
4	226 Tx0
6	225 Tx2
8	225 Tx0
10	224 Tx2
11	224 Tx0

2785

2786 These Quads are GTH type MGT transceivers in SLR 0 of the FPGA. These connections are
2787 listed in Section 18 and are shown in **Figure 30**.

2788 Only 4 channels from the Receiver MiniPOD are connected to MGT receivers in the Hub's
2789 FPGA. The connected Receiver MiniPOD fibers are shown in the following table:

Receiver MiniPOD Fiber	MGT Quad and Port
2	224 Rx2
4	224 Rx1
6	224 Rx2
8	124 Rx0

2790

2791 Quad 224 is of the GTH type and Quad 124 is of the GTY type. Both of these Quads are in
2792 SLR 0 of the FPGA. These MiniPOD connections are capacitor coupled using 100 nFd 0201
2793 size coupling capacitors. The trace routing from fiber 8 to Quad 124 Port Rx0 is particularly
2794 complicated and may not support high-speed operation.

2795 The 8 remaining Receiver MiniPOD fibers have no connection on the Hub's FPGA. Recall
2796 that one of these fibers is used to receiver the Optical Felix TTC clock and data signal. These
2797 connections are listed in Section 18 and are shown in **Figure 29** and **Figure 30**.

2798 Monitoring and control of the two MiniPODs is provided by a separate "TWB" from the
2799 Hub's FPGA to each MiniPOD. Both MiniPODs have their TWB Address set at zero. Each
2800 MiniPOD has its own Interrupt_B and Reset_B lines connecting it to the Hub FPGA. Pull-up

2801 resistors are provided for the TWB SDA and SCL lines as well as for the interrupt and reset
2802 lines so the Hub FPGA does not need to provide the pull up current.

2803 Filtered 2.5 Volt and 3.3 Volt power is separately supplied to each MiniPOD from the bulk
2804 supplies on individual isolated power fills.

2805 The design of the heat sinks for these MiniPODs must take into consideration: the ATCA
2806 height limitation, the ROD mezzanine air flow requirements, and the near by Hub FPGA
2807 heat sink.

2808 The two ribbons of optical fibers for these MiniPODs will use the backplane optical MPO
2809 connectors to exit the Hub via its Rear Transition Module. Part numbers for 50 cm single 12-
2810 fiber ribbon Prism to MPO cables are:

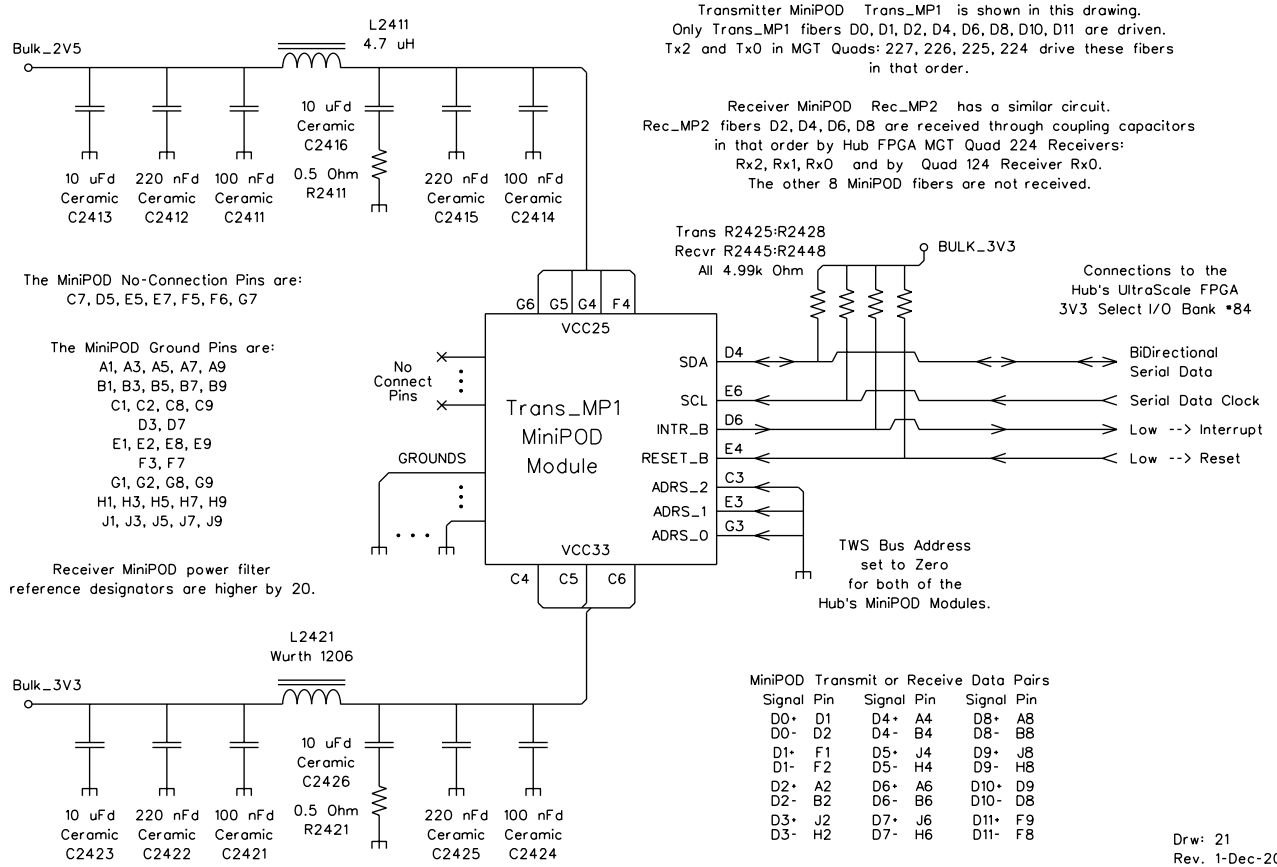
2811 Molex 106267-2011 for the male MPO connector and

2812 Molex 106267-2001 for the female MPO connector

2813

2814

Transmitter and Receiver MiniPOD Modules



Drw: 21
Rev. 1-Dec-2016

Figure 41: Hub MiniPOD module circuit digrams.

2816 **26 Appendix 13: Non-MGT Rod-Hub Connections**

2817 The intent of this note is to describe all of the non-MGT ROD-Hub connection signals. The
2818 Meg-Array pinout of these signals is presented in Ed's document, "ROD Hub Pinout" Rev.
2819 1.4 from 6-May-2015.

2820 **26.1 JTAG**

2821 The Hub Module provides a front panel "Access" connector". One of the functions available
2822 on this J2 access connector is a JTAG string that runs to components on both the ROD and
2823 Hub.

2824 On the ROD this JTAG string connects only to the ROD's FPGA.

2825 On the Hub this JTAG string connects only to the Hub's FPGA.

2826 This JTAG string is not connected to either the IPMC's "Master" or "Slave" JTAG ports.

2827 Manually installed jumpers are provided so that the JTAG string can be jumpered around the
2828 Hub's FPGA. An automatic jumper is provided so that this JTAG string jumpers around the
2829 ROD when the ROD Power Good signal is not asserted.

2830 The JTAG signal level at the Hub's front panel is 3V3 CMOS. The front panel pinout is
2831 standard for Xilinx signal/ground pair type of JTAG wiring and includes a fused 3V3
2832 reference.

2833 On the Hub Module the JTAG signals are buffered and translated to 1V8 levels. The JTAG
2834 signal level to the ROD is 1.8 Volt.

2835 The Hub Module JTAG String is shown in **Figure 37**.

2836 **26.2 Sensor I2C Bus**

2837 The I2C Bus connection to the ROD is normally mastered by the IPMC's Sensor I2C port.
2838 The normal function of the Sensor I2C bus is to allow collection of monitoring information
2839 (e.g. power supply voltages and currents and device temperatures). The IPMC initiates and
2840 masters the Sensor I2C Bus cycles that collect this monitoring data. The Sensor I2C bus
2841 from the IPMC is shared by the ROD and the Hub and is used to collect the Atlas DCS
2842 monitoring information from both of them.

2843 At times either the Hub or ROD FPGA may need to initiate and master a Sensor I2C Bus
2844 cycle for example to set a parameter in one of their GE power supplies. Thus not only
2845 sensors and GE power modules are connected to the Sensor I2C Bus but also both the Hub
2846 and ROD FPGAs make a master connection to this bus. In addition the Hub's FPGA makes a
2847 second slave only connection to the Sensor I2C Bus that provides a port to the System
2848 Monitor in the Hub's FPGA.

2849 The I2C addresses are shared between the Hub and ROD on this IPMC Sensor I2C Bus.

2850 Some parts of the overall Sensor I2C bus are 3V3 level and some parts are 1V8 level. The
 2851 Hub Module provides the required translation and uses buffered translator chips, to provide
 2852 the required drive for the large number of devices that are connected to the Sensor I2C Bus.
 2853 These translators can have their ports enabled or disabled under control of the Hub's FPGA.

2854 The Hub's Sensor I2C Bus is shown in **Figure 36**.

2855 Note that the Sensor I2C Bus can also be accessed from the front panel of the Hub Module
 2856 via its J2 "Access Connector".

2857 The ROD-Hub Sensor I2C bus has the potential problem that when a section of it is either
 2858 powered off or has a power supply problem, that the the ESD diodes in the devices in that
 2859 section of the bus may clamp the I2C signals to ground. Comments on this potential
 2860 problem:

- 2861 • We really only need monitoring information when the ROD Hub are up and running so a
 2862 brief lack of monitoring data at the start of a normal power up is probably OK.
- 2863 • It would be very useful the IPMC could report in its monitoring data when the Sensor I2C
 2864 cycles are not working vs just sending junk data or no data to the DCS monitoring
 2865 system.
- 2866 • The Linear Technology I2C bus translators/buffers may automatically isolate stuck
 2867 sections of the Sensor I2C bus and allow good monitoring data to be read from the
 2868 sections of the bus that are fully powered up.
- 2869 • It may be useful to run the Ready signals from the I2C bus translators/buffers back to the
 2870 Hub FPGA so that it can see if a section of the Sensor I2C bus is stuck.

2871 **26.3 ROD Front Panel Signals**

2872 The ROD provides a total of 8 front panel control signals. The net-names of these signals,
 2873 both old and new netnames are shown in the table below.

- 2874 • **Figure 39** shows the resources on the Hub that are connected to these 8 front panel
 2875 control signals from the ROD.
- 2876 • Two of these front panel signals control the two LEDs in the RJ45 connector for the
 2877 ROD.
- 2878 • One of these front panel signals is the input to the LEMO driver and thus controls the
 2879 output of the ROD's LEMO connector on the Hub's front panel.
- 2880 • Five of these front panel signals control five of the LEDs on the Hub's front panel.
- 2881 • All 7 of the front panel control signals from the ROD that control LEDs are Low active
 2882 1V8 logic signals. When these signals are voltage Low the LED illuminates.
- 2883 • The one front panel control signal from the ROD that controls the LEMO output is also a
 2884 1V8 logic signal. When this control signal is voltage Low the open drain LEMO output
 2885 pulls Low.
- 2886 • All of these front panel signals from the ROD are 1V8 CMOS level, i.e. they do not
 2887 directly drive the LEDs.
- 2888 • Front panel signal table:

2890

MegArray	Old	New	LED
S1 Pin#	Name	Current Name	Color
B1	LED-0	Phy_LED2_B	Green
B2	LED-Y	Phy_LED1_B	Yellow
B3	LED-B	Prog_Done_LED_B	Green
B4	LEMO-0	LEMO	--
C1	LED-1	Pwr_Good_LED_B	Green
C2	LED-R	SMB_Alert_LED_B	RED
C3	LED-G	GP_LED_B	Blue
C4	LEMO-1	Run_LED_B	Blue

2891

2892

- 2893 • GP_LED_B is a General Purpose LED which can be used by firmware to signal some
2894 condition (TBD)
- 2895 • “The Run_LED_B is the “Up and Running” signal that you had proposed a while back. It
2896 indicates to the Hub and to the Front Panel that the ROD is running a functional firmware
2897 image. This will not be turned on if the ROD is running an initialization, error recovery,
2898 or other engineering image.
2899

2900 • My configuration sequence is to always boot an engineering image first. That image
2901 will check to see the board context, and will then trigger the boot of the appropriate
2902 “RUN” image. I’ve allowed for the ROD to carry several images for [efex, gfex, jfex *
2903 hub1, hub2] + the engineering image = 7 configuration images.

2904 • I will turn on “Run” when the second image has booted.”

2905 **26.4 Clock 40.08 MHz**

2906 This is a clock signal from the Hub to the ROD. This 40.08 MHz clock is always running -
2907 even when the Hub is not receiving an Optical Timing reference signal from the LHC. This
2908 is an LVDS signal. It is AC coupled on the Hub before being sent to the ROD. It is
2909 synchronous with the Clock signal that the Hub sends to the other 12 FEX slots in the ATCA
2910 Shelf.

2911 **26.5 Geographic Address**

2912 These 8 lines are 1V8 signals from the Hub to the ROD.

2913 The net-names of these signals are: LOC_ADD1:LOC_ADD8.

2914 These signals indicate a unique Geographic Address within the overall L1Calo system. That
2915 is, these lines indicate both a Slot Number and a Shelf Number within the overall L1Calo
2916 system. These lines are not just the backplane Geographic Address signals from the ATCA
2917 Zone 1 connector.

2918 The details of how the Hub obtains the Shelf Number and encodes the Shelf Nmbr + Slot
2919 Nmbr before sending it to the ROD on these 8 lines are currently being discussed with Ian
2920 and David.

2921 **26.6 Ethernet Connection**

2922 These 8 lines come from the Micrel KSZ9031RNX Phys chip on the ROD. The net-names of
2923 these signals are: TR01_P, TR01_N, through TR04_P, TR04_N. The Hub provides the
2924 “magnetics” and the RJ45 connector for the ROD’s Base Interface Ethernet connection.

2925 The components on the Hub are specified for 10/100/1000 Base-T operation. The
2926 components currently in the Hub design are Pulse Engineering HX5201NL magnetics and TE
2927 Connectivity 1888653-x connectors. The colors of the LEDs in the RJ45 connector are
2928 Green and Yellow.

2929 Careful attention must be paid while routing the Hub to confirm that it correctly implements
2930 the polarity of the Ethernet signals coming from the ROD.

2931 **26.7 Module_Present**

2932 This ROD_PRSENT_B signal is pulled to Ground with a 1k Ohm resistor on the ROD. The
2933 Hub has a high value pull-up resistors on this signal. The resulting logic signal goes Low
2934 when the ROD is plugged in. This signal can be used to let the Hub FPGA know if a ROD
2935 mezzanine card is installed.

2936 **26.8 ROD-Hub Power Control Signals**

2937 All 4 of the Power Control Signals are 1V8 CMOS level logic signals. These are single
2938 ended signals and the direction of each of them is given below.

2939 OK for ROD to Power Up: --- Net PWR_CON1

2940 This is a signal from the Hub to the ROD that tells the ROD when everything on the HUB
2941 has been brought up and is running. By using this signal the ROD can delay its power up
2942 until the Hub is fully running and presenting a stable environment to the ROD.

2943 The ROD includes a 1k Ohm pull-down resistor on this signal.

2944 Before telling the ROD to power up the Hub will have configured its FPGA and will have all
2945 clocks running.

2946 It will take several (many) seconds from the time that the Shelf Manager gives the Hub the
2947 OK to power up until the Hub gives the ROD the OK to power up.

2948 During an overall power up sequence, once the Hub asserts the PWR_CON1 signal voltage
2949 Hi it will not return this signal Low until the Shelf Manager tells the Hub to turn off or the
2950 backplane 48V goes away or a process is started to re-power-up the ROD.

2951 *ROD Power Supplies Are All Running OK: --- Net PWR_CON2*

2952 This is a signal from the ROD to the Hub.

2953 As soon as the ROD has all of its power supplies up and running with their outputs within the
2954 required voltage range then it will assert this signal.

2955 The Hub will not “believe or use” any other signals that it receives from the ROD until this
2956 signal is asserted.

2957 *ROD Has Completed Its Power Up: --- Net PWR_CON3*

2958 This is a signal from the ROD to the Hub.

2959 This signal means that the ROD is fully Configured and ready for normal L1Cal Trigger
2960 operation.

2961 The Hub will not indicate to any other cards that it is ready to operate in the overall L1Calo
2962 system until this signal from the ROD is asserted.

2963 *Spare Power Control Signal: --- Net PWR_CON4*

2964 The spare Power Control signal will be routed to Select I/O pins on both the ROD and Hub
2965 FPGAs.

2966 PWR_CON signals 2, 3, and 4 all run directly between the ROD and Hub FPGAs. The Hub
2967 includes 470 Ohm “isolation” resistors in these line to limit current flow before both FPGAs
2968 are both powered up and configured.

2969 **26.9 Spare Unused ROD-Hub HP IO Signals**

2970 We have a number of spare currently un-assigned signals between the ROD and the Hub. All
2971 of these signals are FPGA to FPGA HP IO lines.

- 2972 • There are 8 spare HP IO lines in the Meg-Array pinout list. These are nicely setup as 4
2973 LVDS pairs so that we can use them as LVDS or as single-ended signals, which ever
2974 may be required in the future.
- 2975 • The net-names of these spare signals are: TBD_LINK0_P, TBD_LINK0_N, through
2976 TBD_LINK3_P, TBD_LINK3_N.
- 2977 • Both ROD and Hub have routed these 8 signals as 4 differential pairs.
- 2978 • When not used for some function, these 8 spare signals are to be operated with 1.8V
2979 single ended CMOS levels with the Hub driving and the ROD receiving. The Hub is
2980 required to tri-state its output drives for these signals any time that the ROD’s Power
2981 Control #2 signal is NOT asserted HI. That is, the Hub will only drive these signals when
2982 the ROD reports that it is fully powered up. In any case, in this stand by service the Hub
2983 should use a low level of Drive current on these lines.
- 2984 • In firmware, these unused spare HP IO lines between the ROD and Hub will be
2985 connected to IPBus visible registers so that we may test them to prove that they are OK,
2986 i.e. prove that our lifeboat floats.

2987 **26.10 Power from the Hub to the ROD**

2988 The Hub provides bulk +12 Volt power to the ROD that is isolated from the backplane 48
2989 Volt power feed.. This power is the same Isolated +12V bus that feeds all of the DC/DC
2990 Converters on the Hub module itself.

2991 The ROD may draw up to 100 Watts of this bulk +12V power, i.e. 8.3 Amps. This +12V
2992 power is sent to the ROD as soon as the Shelf Manager tells the Hub that it may power up.

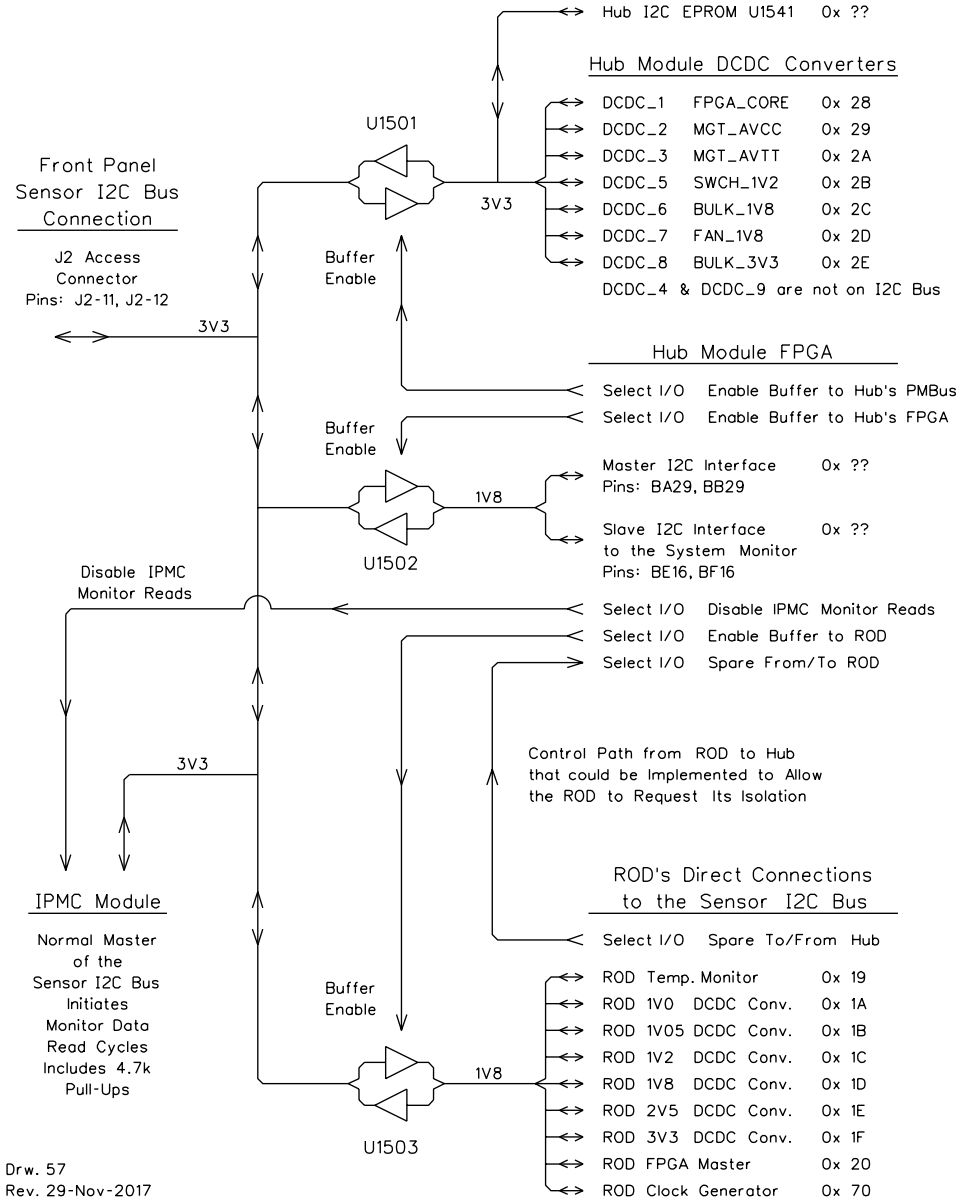
2993 The current parts in the Hub design that provide the bulk Isolated +12V power are: SynQor
2994 IQ65033QMA10SNF-G power entry module and SynQor PQ60120QEA25NNS-G Isolated
2995 +12V supply.

2996 Note that the Isolated +12V supply module has a maximum capacitive load of 12,000 uFd
2997 that it can support when fully loaded with a resistive load. The Hub itself places 3118 uFd
2998 on the output of the Isolated +12V converter or about 26% of the assumed total available
2999 budget.

3000 **26.11 ROD-Hub MGT Signals**

3001 These signals are covered in Section 18.

ROD plus Hub Overall Sensor I2C Bus



3002

3003

Figure 42: Joint ROD and Hub sensor I2C bus circuit diagram.

3004

3005

3006 **27 Appendix 14: Phys Chip Usage on the Hub Module**

3007 The Hub Module requires 2 Phys Chips for the Ethernet Base Interface connections to its
3008 UltraScale Virtex FPGA.

3009 Two Micrel (now Microchip Technology) KSZ9031RNX Phys chips are used to implement
3010 these Ethernet connection. An advantage of this part is that it can operate with a 1.8V
3011 RGMII port and thus directly connect to the Virtex HP I/O pins. The documentation for this
3012 Micrel part looks good and its implementation looks clean.

3013 Two drawings show the implementation of the Micrel Phys chips on the Hub Module,
3014 provided in **Figure 61** and **Figure 62**.

3015 **27.1 Power Supply, ByPass, Power Up, and Reset Requirements**

3016 In the Hub application the KSZ9031RNX Phys chip requires 3 supply buses:

- 3017 • 1.2V supply for: AVDDL = the Analog Core, DVDDL = the Digital Core, AVDD_PLL
3018 = Internal PLL
- 3019 • 1.8V supply for: DVDDH = the Digital I/Os, this bus can be: 1.8V, 2.5V, or 3.3V
- 3020 • *3.3V supply for: AVDDH = Transceiver Analog Power*
3021

3022 The total load on each of these 3 power buses is expected to be the following, per chip, recall
3023 that Hub has 2 chips:

- 3024 • 1.2V supply 265 mA for Cores and PLL
- 3025 • 1.8V supply 65 mA for Digital I/Os
- 3026 • 3.3V supply 82 mA for Transceivers

3027 The Micrel data sheet gives a +-5% tolerance on all of this chip's supply rails.

3028 Note that the KSZ9031RNX includes a “controller” for an external MOSFET pass transistor
3029 so that by itself it can generate the 1.2V bus from the 3.3V bus if the application requires that
3030 function. The Hub Module provide all 3 buses from external supplies.

3031 Total Power Consumption with 1.8 V digital IO and 3.3 V Transceiver supply and 100%
3032 utilization at 1000 Base-T is expected to be about 706 mW per chip.

3033 ByPass and Filter Components recommended for the KSZ9031RNX:

- 3034 • AVDDL Bus: Next to pins 4, 9 bypass with 100 nFd on each pin. Also include one
3035 or two 10 uFd and a 1 uFd on the AVDDL bus.
 - 3036 • DVDDL Bus: Next to pins 14, 18, 23, 26, 30, 39 bypass with 100 nFd on each pin.
3037 Also include a 10 uFd and use a Ferrite Bead to isolate the DVDDL bus.
 - 3038 • AVDDL_PPL Bus: Next to pin 44 bypass with 100 nFd. Also include a 10 uFd and
3039 use a Ferrite Bead to isolate the AVDDL_PLL bus.
-

- 3040 • DVDDH Bus: Pins 16, 34, 40
- 3041 • AVDDH Bus: Pins 1, 12
- 3042 • Ground: Pins 29 and the exposed thermal pad pin 49
- 3043 • All capacitors are X5R or X7R ceramic.
- 3044 • All ferrite beads are <0.1 Ohm DC and >60 Ohm at 100 MHz e.g. TDK MPZ1005S600C
- 3045

3046 This list of Bypass and Filter requirements for the KSZ9031RNX about matches the
3047 schematic of the Micrel Eval Brd for this chip.

3048 The Micrel Eval Brd uses chokes (ferrite beads) on all 5 supply rails to the chip. They use:
3049 Steward HI1206N101R-00 on all rails. These are: 100 Ohm at 100 MHz, 144 Ohm at 500
3050 MHz and 150 Ohm at 1 Ghz with 35 mOhm of DC resistance and 3 Amp max.

3051 Because of space limitation on the Hub module I think that we can use the smaller Würth
3052 782633601 0603 size chokes on 4 of these 5 power rails. The Würth 782633601 has better
3053 AC filtering characteristic, a 1 Amp max, but has 200 mOhm max DC resistance. This
3054 should be OK for the: AVDDL, AVDDL_PLL, DVDDH, and AVDDH rails.

3055 None of these supplies can be over 100 mA and thus the maximum drop with the Würth
3056 782633601 choke is about 20 mV or about 1.6% on the lowest 1.2 Volt rails. I expect the
3057 current draws to be less than 100 mA, and it's possible to measure them on a running card
3058 and replace these parts if necessary so I think that this is OK.

3059 I believe that most of the current for this chip is on its DVDDL rail, probably about 225 mA
3060 so for that I will use the lower DC resistance (60 mOhm) Würth 742792116.

3061 See pages 40 and 65 in the ver 2.2 datasheet for this chip for details about the expected
3062 current requirements.

3063 Power Up Sequence:

- 3064 • Basically the KSZ9031RNX wants its Cores to power up last.
- 3065 • Recommended power up sequence is to have the transceiver AVDDH and the digital
3066 I/O DVDDH voltages power up before the 1.2V buses to DVDDL, AVDDL,
3067 AVDDL_PLL.
- 3068 • There is no required sequence between the transceiver AVDDH and the digital I/O
3069 DVDDH.
- 3070 • The power up waveforms need to be monotonic for all power buses to the
3071 KSZ9031RNX.
- 3072 • After de-assertion of the RESET wait 100 usec before starting to use the part.
- 3073 • At power down it is best to remove the 1.2 V supply first.
- 3074 • For a power down cycle all buses must be less than 0.4V for at least 150 msec.
- 3075 • All power buses must be stable for at least 10 msec before de-assertion of the Reset
3076 signal.
- 3077 • All supply voltages must have a minimum of 200 usec ramp up time and have
3078 monotonic ramp.
- 3079 • The recommended Reset circuit, on page 75 of the data sheet is a combination of the
3080 typical R, C, Diode to guarantee a Reset at power up and another Diode to mix in an
3081 External Reset from a CPU or FPGA.

3082 **27.2 RGMII Interface Port**

3083 The RGMII port on the KSZ9031RNX is its data connection with the Hub's UltraScale
3084 Virtex FPGA. The KSZ9031RNX RGMII connects to HP I/O pins on the FPGA.

3085 The RGMII bus consists of 12 signals:

- 3086 • Transmit Clock to the KSZ9031RNX
- 3087 • Transmit Control (enable) to the KSZ9031RNX
- 3088 • Transmit Data 0:3 to the KSZ9031RNX
- 3089 • Receive Clock from the KSZ9031RNX
- 3090 • Receive Control (enable) from the KSZ9031RNX
- 3091 • Receive Data 0:3 from the KSZ9031RNX

3092 **27.3 MDC/MIIM/MDIO Interface Port**

3093 The KSZ9031RNX includes a MII Management port. This type of port is also called MDIO
3094 Management Data Input/Output. This port allows higher level devices to monitor and control
3095 the KSZ9031RNX. This port allows direct access to the IEEE defined MIIM registers, and
3096 the vendor specific registers. This port also allows indirect access to the MMD address space
3097 and registers.

3098 This port consists of signals:

- 3099 • MDC the clock
- 3100 • MDIO the data line

3101 The MAC in the FPGA provides the connections to this device management port.

3102 **27.4 Jumpers for the KSZ9031RNX (aka Strapping Pins)**

3103 The KSZ9031RNX uses a number of jumpers that are “read” during its power up process and
3104 then the state of these jumpers control its operation of the chip once power up is completed.

3105 Most of these jumpers are the new standard type of jumper, i.e. a weak pull-up or weak pull-
3106 down on a dual purpose I/O pin. Once the jumper is “read” and the KSZ9031RNX completes
3107 its power up then the pin begins its normal function and the weak pull resistor is ignored.

3108 For this chip the pull-up resistors connect to the DVDDH 1V8 rail.

3109

Pin #	Strap Pin Name	Normal Function	Jumper Function - Strapping Option
17	PHYAD0	LED1	Pull-Up = 1 Pull-Down = 0 PHY Address Bits 3 and 4 are always 0, 0. This is the PHYAD of the Management Interface port on the KSZ9031RNX.
15	PHYAD1	LED2	
35	PHYAD2	RX_CLK	
32	MODE0	RXD0	Set operating Mode at Power Up

31	MODE1	RXD1	0100 NAND tree mode
28	MODE2	RXD2	1100 RGMII 1000 Base-T full duplex
27	MODE3	RXD3	1101 RGMII 1000 Base-T full or half duplex
			1110 RGMII 10/100/100 all but 1000 half duplex
			1111 RGMII 10/100/1000 full or half duplex
33	CLK125_EN	RX_DV	Pull-Up --> Enable the 125 MHz Clk Output
			Pull-Down --> Disable the 125 MHz Clk Output
41	LED_MODE	CLK125_NDO	Pull-Up --> Single LED Mode
			Pull-Down --> 3 color or dual LED Mode

3110

3111 *KSZ9031RNX Jumpers implemented on the Hub Module:*

- 3112 • Pins 15, 17, 35 PHYAD Pull-Up and Pull-Down R1901:R1906
- 3113 • Pins 27, 28 MODE Pull-Up Only R1907,R1908
- 3114 • Pins 31, 32 MODE Pull-Up and Pull-Down R1909:R1912
- 3115 • Pin 33, CLK125_EN, Pull-Up Only --> Enable the 125 MHz Clk to the MAC
- 3116 • Pin 41, LED_MODE, Pull-Up Only --> Single LED Mode R1913,R1914

3117

3118 Note that the Pull-Down resistors are 1k Ohm and the Pull-Up resistors are 10k Ohm. Note
 3119 that some of these Pull-Up / Pull-Down resistors are on high-speed RGMII lines. They must
 3120 be placed and routed with minimum parasitic effect on the high-speed signals.

3121 *KSZ9031RNX LEDs:*

3122 The Hub Module runs the KSZ9031RNX LEDs in “Single LED Mode”. That is it does not
 3123 use tri-color or multiple LEDs per LED pin on the chip. With a 1V8 DVDDH rail I do not
 3124 think that the chip can drive the LEDs directly. Rather the standard, 74AVCH8T245 non-
 3125 inverting Hub circuit for controlling LEDs with 1V8 CMOS logic signals is used for the Phys
 3126 chip LEDs.

3127 *KSZ9031RNX ISET Resistor:*

3128 ISET pin #48 requires a 12.1k Ohm 1% resistor to ground to set the transmitter output level.
 3129 This is resistor R1915.

3130 *KSZ9031RNX RESET Circuit:*

3131 The KSZ9031RNX Phys Chips receive a reset signal from the Hub’s Board Startup Reset
 3132 circuits. Currently it is not understood if we want to or should provide the Phys Chips with
 3133 a reset from the Hub’s FPGA that would be controlled from a bit in an IPBus visible register.

3134 *KSZ9031RNX Clocks:*

3135 The KSZ9031RNX contains an internal oscillator circuit for use with a 25 MHz crystal or it
 3136 can use an external clock. Be sure to use the version 2.2 or later data sheet for this Phys chip
 3137 to correctly understand its clock signal requirements.

3138 The Hub supplies the KSZ9031RNX with a quality external 25 MHz 3V3 clock signal. This
3139 external clock is sent into “X1” pin #46. Pin “X0” pin #45 is not connected.

3140 Internally the KSZ9031RNX manipulates this 25 MHz clock as required to sequence its
3141 various functions. One step to to multiply this up to 125 MHz.

3142 The internally generated 125 MHz clock is made available on pin CLK125 pin #41 for use
3143 by the MAC that controls the KSZ9031RNX. This 125 MHz clock is returned to the Hub
3144 FPGA as it provides the MAC for the KSZ9031RNX Ethernet circuits.

3145 Note that this Phys chip has internal series terminator resistors in the CLK125 line and the
3146 other high-speed output lines from it in the RGMII interface. The FPGA pins in its RGMII
3147 port should incorporate the correct type of DCI termination, e.g. series termination in its
3148 output pins.

3149 *KSZ9031RNX RGMII Link to FPGA:*

3150 Reduced Gigabit Media Independent Interface between the KSZ9031RNX Phys chip and the
3151 MAC in the Hub FPGA.

3152 *KSZ9031RNX MII / MIIM Link to the FPGA:*

3153 This is the “Management Interface” between the MAC in the Hub FPGA and the
3154 KSZ9031RNX Phys chip. This separate interface allows an external entity to monitor and
3155 control the KSZ9031RNX via way of its MDC/MDIO Monitor Data Clock and I/O pins.
3156 The address of this port on the KSZ9031RNX is set by the PHYAD strapping jumpers. This
3157 Management Interface can talk to 32 bit registers both directly addressed IEEE defined
3158 registers and indirectly to vendor defined management registers.
3159

Phys Chip - RGMII, MDC/DMIO, and Base-T Circuits

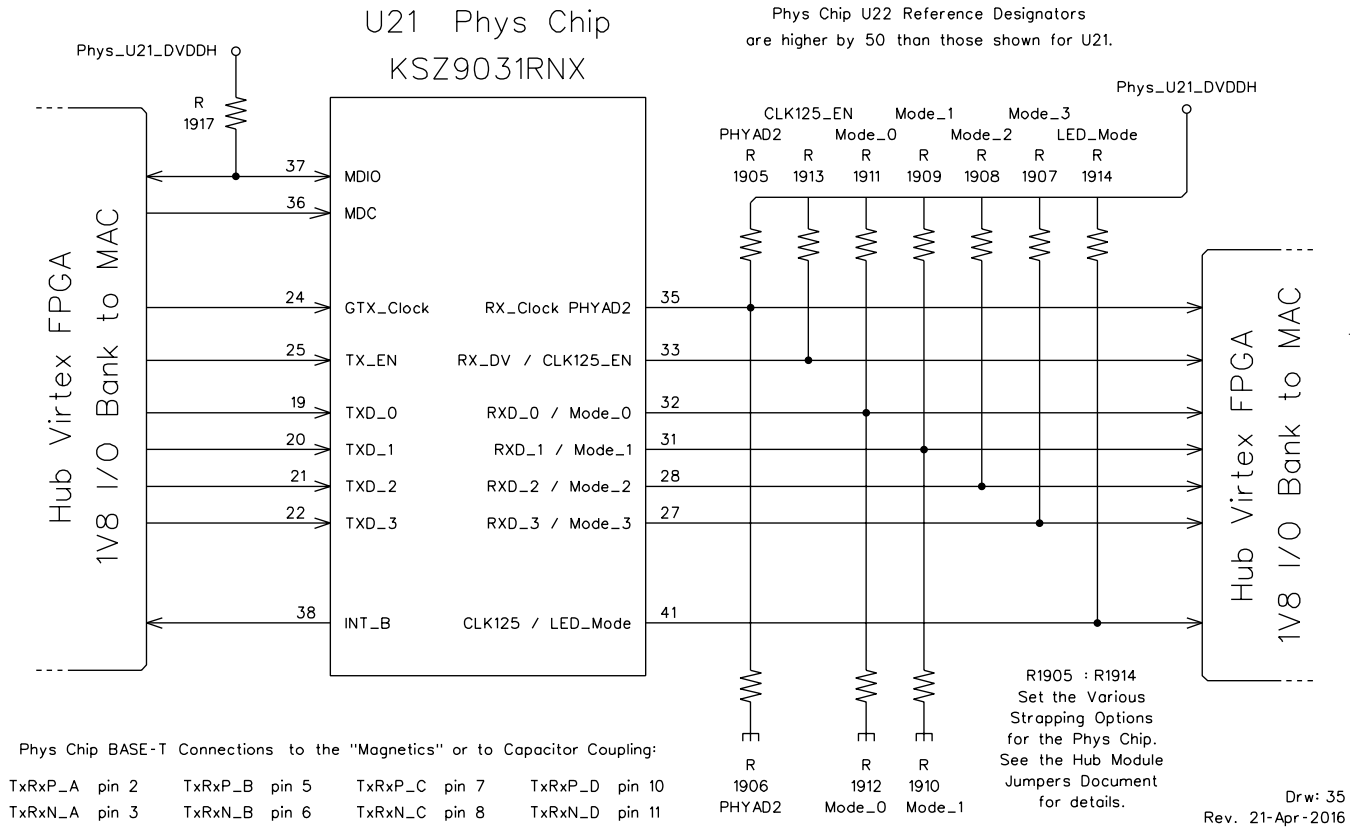


Figure 43: PHY Chip RGMII, MDC/DMIO and Base-T circuit diagrams.

3161 **28 Appendix 15: Hub-Module Power System**

3162 The Hub-Module power system is based on the ATCA architecture. This power system
 3163 supplies both the components on the Hub-Module itself and provides +12V power to the
 3164 ROD mezzanine card. An overall view of the Hub Module power supplies is presented in
 3165 **Figure 47**.

3166 **28.1 ATCA Power Entry and Isolated +12V Supply**

3167 Power reaches the Hub Module's zone 1 connector on redundant negative 48 Volt buses.
 3168 After passing through fuses the bulk -48 Volt power from the backplane enters a SynQor
 3169 "power entry module". This is either a SynQor IQ65033QMA10 10 Amp 300 Watt
 3170 module or a SynQor IQ65033QGA12 12 Amp 350 Watt module. In either case these are
 3171 quarter-brick size modules with the same footprint. The first prototype Hub cards are built
 3172 with the SynQor IQ65033QMA10SNF-G power entry module.

3173 From the power entry module filtered power, monitored by the IPMC, flows to the input of
 3174 an Isolated +12 Volt converter. This converter makes the Isolated +12 Volt power that
 3175 operates everything on the Hub Module except for the power supervision circuits and the
 3176 IPMC mezzanine card. The Isolated +12 Volt power is provided by a SynQor
 3177 PQ60120QEA25NNS-G 12V 25A 300 Watt quarter-brick module. Higher current modules
 3178 are available if needed.

3179 The Isolated +12 Volt power from this SynQor module is the input power to a number of
 3180 non-isolated DC/DC "buck" converters that generate the actual power buses used on the Hub
 3181 Module. This same Isolated +12 Volt power is provided to the ROD mezzanine card on the
 3182 Hub.

3183 The power entry module provides a separate isolated 5V0 supply that is used to operate the
 3184 power supervision circuits on the Hub Module. This isolated 5V0 supply is available
 3185 anytime that the Hub receives backplane 48V power.

3186 The power entry module also provides separate isolated 3V3 power for the IPMC card. This
 3187 separate 3V3 power is available anytime that the input module receives backplane 48V
 3188 power.

3189 The IPMC controls when the Isolated +12V module is allowed to operate. When the IPMC
 3190 and the Shelf Manager have successfully negotiated the power up of the Hub Module then the
 3191 IPMC asserts the enable signal to the Isolated +12V module.

3192 The IPMC the monitors the power entry module using its Management I2C bus which runs to
 3193 both the ATCA power entry module and to the FRU & SDR EEPROM.

3194 The power entry and Isolated +12V section of the overall Hub Module design are shown in
 3195 **Figure 44** and **Figure 45**. **Figure 46** shows the various backplane ground connections that
 3196 are used on the Hub Module.

3197 **28.2 Hub Module Power Bus Table**

3198

Power Bus Net Name	Bus Voltage	Principal Consumers	Anticipated Load	Supply Capacity	Supply Name
FPGA_CORE	0.950 V	FPGA INT & BRAM	20.8 Amps	40 Amps	DCDC-1
MGT_AVCC	1.000 V	FPGA MGT	10.8 Amps	20 Amps	DCDC-2
MGT_AVTT	1.200 V	FPGA MGT	10.0 Amps	20 Amps	DCDC-3
MGT_AVAUX	1.800 V	FPGA MGT	0.60 Amps	3 Amps	DCDC-4
SWCH_1V2	1.200 V	Switch & Phys	4.0 Amps	12 Amps	DCDC-5
BULK_1V8	1.800 V	FPGA & other	3.0 Amps	12 Amps	DCDC-6
FAN_1V8	1.800 V	MGT Fanout	13.0 Amps	20 Amps	DCDC-7
BULK_3V3	3.300 V	Switch & other	4.6 Amps	12 Amps	DCDC-8
BULK_2V5	2.500 V	MiniPOD & Clk FO	1.3 Amps	3 Amps	DCDC-9

3199

3200 Notes:

- 3201
- 3202
- 3203
- 3204
- 3205
- 3206
- The 40 Amp supply is a GE MDT040A0X3-SRPHZ
 - The 20 Amp supplies are GE UDT020A0X3-SRZ
 - The 12 Amp supplies are GE PDT012A0X3-SRZ
 - The 3 Amp linear supplies are LT1764AEQ
 - The low current reference supplies for the FPGA System Monitor are not included in this table.

3207 **28.3 DCDC Converters**

3208 Both GE (Lineage Power) D-Lynx series and TI (Power Trends) PTH08Txyz series

3209 converters were evaluated for use on the Hub Module. The D-Lynx converters were selected

3210 based mostly on the PMBus connection offered by their TI TPS40400 control chip. Concerns

3211 about using the D-Lynx converters remain in the areas of noise, assembly, and rework. Note

3212 that for the 2 low current supplies Linear Technology LDO linear regulators are used both to

3213 save space on the PCB and to insure a low noise supply bus. The amperage capacity of each

3214 of these DC/DC converters was sized to the load that it must drive. During this selection

3215 consideration is also given to minimizing the number of different component types used on

3216 the Hub Module.

3217 The details of the 7 GE DCDC Converters are shown in **Figure 49 - Figure 51**. The

3218 following table and its notes summarize these designs:

3219

3220

3221

3222

3223

Converter Name:	DCDC1	DCDC2	DCDC3
Bus NetName:	FPGA_CORE	MGT_AVCC	MGT_AVTT
Bus Voltage:	0.950 V	1.000 V	1.200 V
Max Bus Amps:	40 A	20 A	20 A
Converter Type:	MDT040A0X3	UDT020A0X3	UDT020A0X3
* Cin Local:	62 uFd	42 uFd	42 uFd
# Cout Local:	220 uFd	580 uFd	580 uFd
Cout Remote:	3822 uFd	1013 uFd	1013 uFd
R V-Set Theory:	34.29k	30.0k	20.0k
R V-Set Real :	34.00k	30.0k	20.0k
R Ramp Series:	20.0k	20.0k	20.0k
R Ramp Shunt :	34.0k	30.0k	20.0k
R Servo:	180 Ohm	180 Ohm	180 Ohm
C Servo:	10 nFd	10 nFd	10 nFd
R ADRS_0:	10k	15.4k	23.7k
R Adrs_1:	84.5k	84.5k	84.5k
I2C Adrs:	0o50	0o51	0o52
Anticipated Load in Watts:	19.8 W	10.8 W	12.0 W
@ Anticipated Input Current:	1.83 A	1.00 A	1.11 A
Design Notes:	--	External Output LC Filter	External Output LC Filter

3224

3225

Converter Name:	DCDC5	DCDC6	DCDC7	DCDC8
Bus Net Name:	SWCH_1V2	BULK_1V8	FAN_1V8	BULK_3V3
Bus Voltage:	1.200 V	1.800 V	1.800 V	3.300 V
Max Bus Amps:	12 A	12 A	20 A	12 A
Converter Type:	PDT012A0X3	PDT012A0X3	UDT020A0X3	PDT012A0X3
* Cin Local:	42 uFd	42 uFd	42 uFd	42 uFd
# Cout Local:	88 uFd	88 uFd	580 uFd	88 uFd
Cout Remote:	1530 uFd	1510 uFd	1929 uFd	1030 uFd
R V-Set Theory:	20.0k	10.0k	10.0k	4.444k
R V-Set Real :	20.0k	10.0k	10.0k	4.420k
R Ramp Series:	--	40.0k	40.0k	40.0k
R Ramp Shunt :	--	20.0k	20.0k	8.87k
R Servo:	180 Ohm	180 Ohm	- Ohm	200 Ohm
C Servo:	10 nFd	15 nFd	- nFd	10 nFd
R ADRS_0:	36.5k	54.9k	84.5k	130k
R Adrs_1:	84.5k	84.5k	84.5k	84.5k
I2C Adrs:	0o53	0o54	0o55	0o56
Anticipated Load in Watts:	4.8 W	5.4 W	23.4 W	15.2 W
@ Anticipated Input Current:	0.44 A	0.50 A	2.17 A	1.41 A
Design Notes:	Delayed Turn On & Self Ramp	--	External Output LC Filter	--

3226 The following symbols were used in the previous table:

3227 * --> The Cin Local capacitors are all ceramic of 3 different values and are located
3228 immediately next to the converter's input terminal.

3229 There is an additional Bulk Cin of 2100 uFd consisting of both ceramic and Tantalum
3230 capacitors that is shared by all 7 DCDC converters. This Bulk Cin is located within a few
3231 cm of the converters and is connected to each converter by a neck of trace typically a one
3232 or two cm wide.

3233 # --> The Cout Local capacitors are all ceramic of 2 different values and are located
3234 immediately next to the converter's output terminal. Note that in the case of converters:
3235 DCDC_2, DCDC_3, and DCDC_7 (the 3 DCDC Converters that include an external LC
3236 output filter) that the Cout Local includes a 470 uFd Tantalum capacitor in addition to
3237 the multiple ceramic capacitors.

3238 Cout Remote consists of ceramic and Tantalum capacitors of multiple values distributed
3239 around the card. In the case of the FPGA supplies these capacitors are all located near the
3240 U1 FPGA.

3241 @ --> The anticipated Input Current in Amps for each supply assumes 90% efficiency
3242 for that converter.

3243 Currently the total anticipated load on the Isolated +12V bus from the Hub itself is 8.46
3244 Amps or about 101.5 Watts. About 91 Watts of this reaches components on the Hub
3245 and about 10 Watts is lost as heat in the DCDC converters.

3246 **28.4 DCDC Converter Input Filter Capacitors**

3247 There is a limit of about 12,000 uFd for the total amount of capacitance that one may have on
3248 the output of the Isolated +12V converter without upsetting its stability. Note that this 12,000
3249 uFd is specified with the Isolated +12V supply running at capacity into a resistive load and I
3250 do not know how running it at less than full output or running it into a chopping DCDC
3251 Converter load affects its stability with the full 12,000 uFd on its output.

3252 This 12,000 uFd must be split between the DCDC Converters on the Hub itself and the
3253 converters on the ROD mezzanine.

3254 On the Hub Module itself, the total capacitance presented to the Isolated +12V supply is:
3255 3118 uFd or about 26% of the assumed total available budget.

3256 **28.5 DCDC Linear Supplies**

3257 Two low current power buses on the Hub Module use linear LDO regulators. One of the
3258 linear supplies is MGT_AVAUX and the other is BULK_2V5. Both of these linear
3259 supplies are powered from the BULK_3V3 bus. Both supplies use an LC filter between the
3260 possibly noisy BULK_3V3 supply and the linear regulator's power input pin. These supplies
3261 include a trim pot with a +-5% adjustment range. These LDO regulators are enabled all of
3262 the time. Their output ramps up as the BULK_3V3 supply ramps with the regulator output
3263 typically trailing the BULK_3V3 supply by about 200 mV. These two supplies do not have
3264 PMBus monitoring and control like the 7 DCDC converters do. Details of these low current
3265 linear supplies are shown in **Figure 52**.

3266 **28.6 DCDC Converter Supervision**

3267 The IPMC supervises the Hub module power system through its control of the Isolated +12V
3268 bus. In addition the IPMC can monitor the ATCA power entry module via its Management
3269 I2C bus and it can monitor the 7 DCDC converters via its Sensor I2C bus.

3270 The only two supplies that can not be directly monitored in this way by the IPMC are the
3271 linear regulators for the MGT_AVAUX and BULK_2V5 power buses. The voltage of these
3272 supplies can be read by the FPGA's System Monitor. The System Monitor can internally see
3273 the MGT_AVAUX supply and the BULK_2V5 is scaled and connected to an analog input to
3274 the System Monitor's ADC.

3275 The voltage of all 9 supplies can be accurately measured with a good DVM plugged into
3276 header J3 in the NE corner of the Hub circuit board. This step is needed to calibrate the
3277 internal monitoring provided by the DCDC Converters.

3278 A number of components on the Hub Module (FPGA, Switch chips, and Phys chips) have
3279 specific power supply sequencing requirements. These requirements are met by ramping up
3280 together on a volt per volt bases all supplies on the Hub module except for the SWCH_1V2
3281 supply. The SWCH_1V2 converter is not started until the other 8 supplies have ramped up
3282 and are stable.

3283 The circuits that control the start-up of the power supplies are shown in **Figure 53, Figure 55**
3284 and **Figure 56**. The start-up process has the following steps:

- 3285 • The process starts when the supervisor sees that the enable signal to the Isolated +12V
3286 supply has been asserted and that the Isolated +12V bus from this supply has reached a
3287 minimum of 8.5 Volts.
- 3288 • At this point a delay of 500 msec is used to allow the Isolated +12V bus to reach its full
3289 value and to stabilise.
- 3290 • Then the enable signal is sent to 6 of the DCDC converters on the Hub Module, all of the
3291 DCDC converters except for the SWCH_1V2 supply.
- 3292 • At this point a delay of 120 msec is used to allow these 6 DCDC converters time to
3293 complete their internal startup routines. Note that the output of these converters does not
3294 begin to ramp during this 120 msec delay because the Ramp Sequence pins on these
3295 converters is being held low.
- 3296 • After this 120 msec delay the Ramp Sequence signal to these 6 converters begins to rise.
3297 The converter outputs follow the Ramp Sequence signal on a volt per volt bases. The
3298 main supplies to the FPGA reach their full output over a 5 to 9 msec period. The
3299 BULK_3V3 supply is the last to reach its full output - taking about 3 times longer than a
3300 1 Volt supply.
- 3301 • About 100 msec after these 6 supplies have reached their full output the SWCH_1V2
3302 converter is enabled. The ramp rate of this converter is internally controlled so that it
3303 reaches its full output in a few msec. This delayed startup of the SWCH_1V2 supply is
3304 required by the Switch chips, not just to prevent cross coupling of the power rails through
3305 the CMOS circuits but rather because the Switch does not want its core to start until its
3306 I/O has been powered up and is stable.

- 3307 • The two linear regulator supplies MGT_AVAUX and BULK_2V5 receive their input
 3308 power from the BULK_3V3 supply. They just ramp up about 200 mV behind the
 3309 BULK_3V3 supply.
- 3310 • Once all 9 supplies are up and stable, as indicated either by their Power Good signals
 3311 being asserted or as measured for the two linear regulator supplies, then there is a delay
 3312 of 500 msec for everything to settle down and then the Board_Startup_Reset_B signal is
 3313 de-asserted. The distribution of the Board_Startup_Reset_B signal is shown in **Figure**
 3314 **58**. This completes the power up of the Hub Module.
 3315

3316 The circuits that supervise this startup process are powered by an isolated 5 Volt output on
 3317 the ATCA power entry module. This 5 Volt output is active anytime that the card receives
 3318 backplane 48 Volt power.

3319 The shutdown of the Hub Module supplies is initiated when either the enable to the Isolated
 3320 +12V supply is dropped (the normal shutdown situation) or when the output of the Isolated
 3321 +12V supply falls below 8.5 Volts. During the shutdown sequence the SWCH_1V2
 3322 converter is immediately stopped and the other 6 converters ramp down quickly in an orderly
 3323 manner for as long as their input power remains available. When the input power falls below
 3324 threshold then all of the converters are immediately stopped. The shutdown sequence is
 3325 shown in **Figure 54**. During shutdown the Board_Startup_Reset_B signal is asserted as
 3326 soon as the enable is removed from the Isolated +12V supply and remains asserted for as
 3327 long as power is available.

3328 **28.7 DCDC Converters with an LC Output Filter**

3329 Three of the DCDC Converters on the Hub Module include an LC Output Filter to reduce the
 3330 switching noise that is present in their output voltage. These 3 converters make power for the
 3331 MGT Transceiver circuits and these circuits specify a peak to peak noise voltage of under 10
 3332 mV on their power supply rails.

3333 The low current MGT_AVAUX supply meets this requirement by using a linear regulator
 3334 with a filter inductor before it to remove the high frequency noise. The higher current
 3335 MGT_AVCC, MGT_AVTT, and FAN_1V8 supplies meet this requirement by using an LC
 3336 filter after these DCDC Converters. The L for this filter is a high current low resistance 680
 3337 nH Würth inductor. The C for the filter consists of large value tantalum capacitors and
 3338 ceramic capacitors of multiple values. Most of these capacitors are located near the load
 3339 point.

3340 A potential issue with using an LC filter after these buck DCDC Converters is that their servo
 3341 control loop may require special compensation for it to be stable. To provide various options
 3342 for how the feedback network is setup in these 3 converters the Hub Module PCB includes a
 3343 set of 4 jumpers for each of these supplies. The jumpers that are associated with each of
 3344 these converters are:

3345 DCDC-2 MGT_AVCC JMP1051, JMP1052, JMP1053, JMP1054

3346 DCDC-3 MGT_AVTT JMP1101, JMP1102, JMP1103, JMP1104

3347 DCDC-7 FAN_1V8 JMP1301, JMP1302, JMP1303, JMP1304

3348

3349 Jumpers JMP1051, JMP1052 (and JMP1101, JMP1102 and JMP1301, JMP1302) control
 3350 whether the the V_SENSE_+ feedback is taken before or after the output filter inductor.
 3351 JMP1051 selects before the output inductor and JMP1052 selects after the inductor.

3352 Jumpers JMP1053, JMP1054 (and JMP1103, JMP1104 and JMP1303, JMP1304) control
 3353 whether the the RC coupled feedback is taken before or after the output filter inductor.
 3354 JMP1053 selects before the output inductor and JMP1054 selects after the inductor.

3355 This jumpers information is also presented in the “as built jumpers” document. In addition to
 3356 these feedback source selection jumpers, the layout for each of these 3 converters also
 3357 includes the SMD pads to mount an 0805 capacitor that directly connects between the
 3358 converters output and its “Trim” input pin.

3359 **28.8 Power Requirements Information for each Section of the Hub**

3360 The following are power supply requirements information about the various components on
 3361 the Hub Module. This information was used to design the overall Hub Module power supply
 3362 and to make the overall list of Hub Module power buses shown above. More details about
 3363 the power requirements of the individual sections can be found in their “as built” documents.

3364 *Power Supply Requirements for the Hub Module UltraScale XCVU125 FPGA:*

FPGA Bus	Bus Volts	Estimated Current Draw
VCCINT+VCCBRAM	0.950 V	20.8 Amps est.
VCCAUX	1.800	147 mA quiescent
VCCAUX_IO	1.800	2 mA quiescent
VCCO	1.800 / 3.300	1 mA per bank quiescent
VCCADC	1.800	few mA
VREFP	1.250	few mA
MGT_AVCC	1.000	8.8 Amps est.
MGT_AVTT	1.200	12.6 Amps est.
MGT_AVAUX	1.800	0.6 Amps est.

3365

3366 Note that this FPGA has power supply sequencing requirements.

3367 See below for more details about the estimates for FPGA MGT power from the Xilinx
 3368 tools.

3369 *Requirements for the Base Interface Switch Power Supplies:*

3370 A separate 12 Amp converter is used for the Switch's 1.2 Volt requirements. To meet the
3371 power supply sequencing requirements of the Switch and Phys chips, this SWCH_1V2
3372 converter is not enabled until after the other DCDC converters on the Hub have ramped
3373 up and stable.

3374 The total draw on the SWCH_1V2 bus from all 3 switch chips is expected to be 3.5
3375 Amps.

3376 The total draw on the BULK_3V3 supply from the 3 Switch chips is expected to be 1.5
3377 Amps.

3378 The total heat dissipation from the 3 Switch chips is expected to be 9.2 Watts.

3379 *Requirements for the GTH Fanout Power Supply:*

3380 The 74 channel FEX Data Fanout (aka GTH Fanout) has its own private power bus
3381 called FAN_1V8. The reasons to have a private converter for this Gb/s speed fanout
3382 include the requirement for low noise and the possible need to adjust this supply
3383 independent of other loads.

3384 The expected load on the FAN_1V8 supply is 13.0 Amps which results in about 23.4
3385 Watts of heat from the 74 fanout chips.

3386 *Requirements for the Micrel KSZ9031RNX Phys Chip Power Supplies:*

3387 In the Hub application the KSZ9031RNX requires 3 supply buses:

- 3388 • 1.2V supply for: AVDDL, the Analog Core, DVDDL the Digital Core, AVDD_PLL
- 3389 Internal PLL
- 3390 • 1.8V supply for: DVDDH, the Digital I/Os
- 3391 • 3.3V supply for: AVDDH, Transceiver Analog Power

3392 The total load on each of these power buses from the 2 Phys Chips on the Hub Module is
3393 expected to be:

- 3394 • 1.2V supply 530 mA from SWCH_1V2 delayed turn on
 - 3395 • 1.8V supply 130 mA from BULK_1V8
 - 3396 • 3.3V supply 164 mA from BULK_3V3
- 3397

3398 Total Power Consumption with 1.8 V digital IO and 3.3 V Transceiver supply and 100%
3399 utilization at 1000 Base-T is expected to be about 1.5 Watts for both Phys chips.

3400 *Requirements for the Clock Generation and Fanout Power Supplies:*

3401 The 25 MHz Ethernet Clock generator and its fanout are expected to use 55 mA from the
3402 BULK_3V3 supply.

3403 The 40.08 MHz and 320.64 MHz Clock generators and their fanouts are expected to use
3404 160 mA from the BULK_3V3 supply and 381 mA from the BULK_2V5 supply.

3405 6. All supplies to these clock generators and fanouts are filtered and distributed to the
3406 clock components on a separate isolated PCB area fills. A total of about 2.0 Watts is
3407 needed for Clock generation and distribution.

3408 *Requirements for the MiniPOD Power Supplies:*

3409 The MiniPODs each require: 2.5 V and 3.3 V power.

3410 The Transmitter MiniPOD requires: from the 2V5 bus 280 mA typical 365 mA
3411 maximum, from the 3V3 bus 105 mA typical 185 mA maximum. This is a heat load of
3412 1.2 Watts typ 1.6 Watts max.

3413 The Receiver MiniPOD requires: from the 2V5 bus 350 mA typical 525 mA maximum,
3414 from the 3V3 bus 48 mA typical 90 mA maximum. This is a heat load of 1.1 Watts
3415 typ 1.6 Watts max.

3416 The total maximum requirements for both MiniPODs are:

3417 Bulk_2V5 bus 890 mA

3418 Bulk_3V3 bus 275 mA

3419 Heat Load 3.1 Watts

3420

3421 Power to both MiniPODs is filtered and distributed on separate isolated PCB area fills.

3422 **28.9 Final best Estimate on FPGA MGT Power from Xilinx Tools**

3423 *Requirements for the MGT AVCC and AVTT Power Supplies*

3424 Ultrascale GTH and GTY channels each draw currents from:

3425 1.0 V AVCC power

3426 1.2 V AVTT power

3427

3428 The Xilinx Power Estimator spreadsheet (XPE) was used to evaluate the expected power
3429 usage for AVCC and AVTT. The current draw on these supplies depends highly on the line
3430 rate and very little on the user data payload. This is quite different from estimating current
3431 usage in the main logic area where user data content and most importantly the toggling ratio
3432 is the driving factor. For MGT channels the toggling ratio for the highest rate circuitry has to
3433 be 50%. XPE thus has all the information it should need to produce an accurate estimate for
3434 MGT AVCC and AVTT.

3435 The goal was to determine a maximum expected power usage.

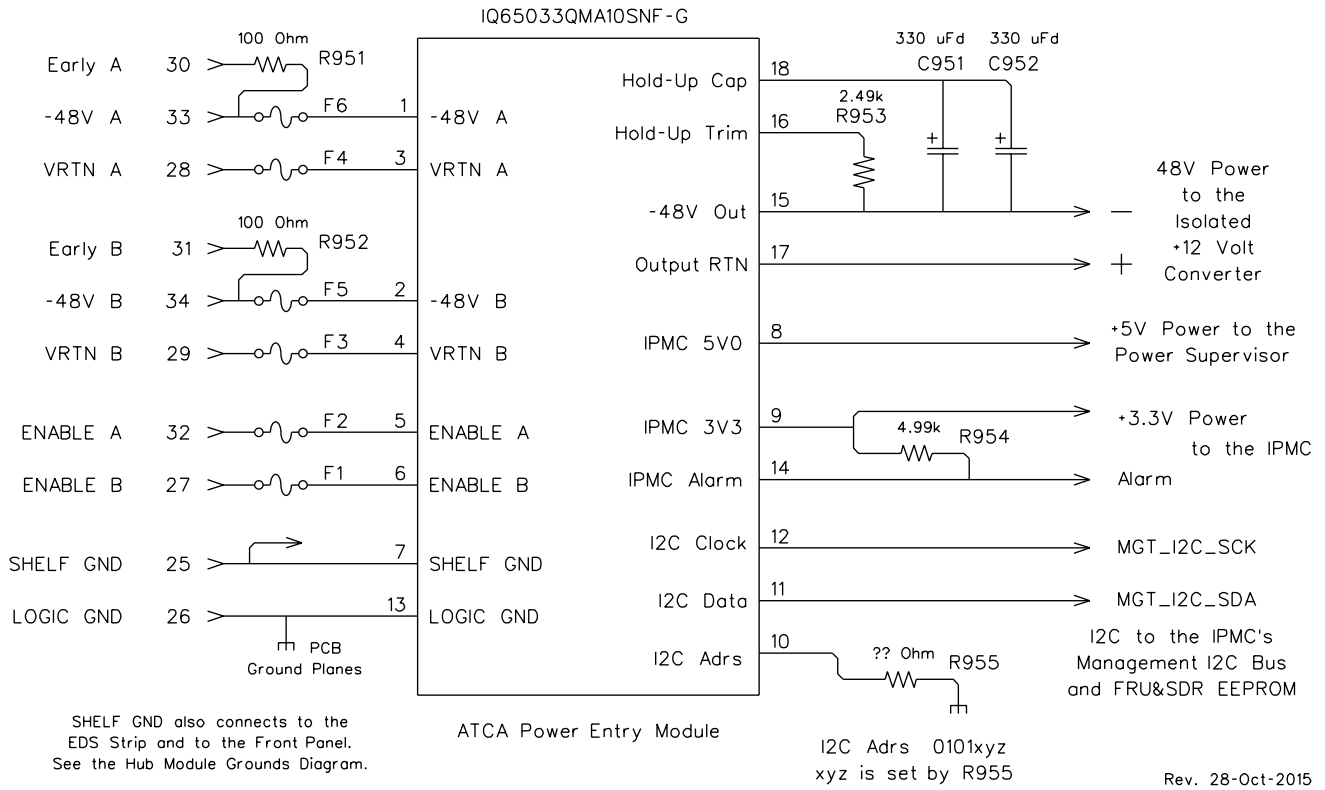
3436 This requires knowing the maximum line rate considered.

3437 The assumptions were

- 3438 • 9.6 Gbps maximum line rate for backplane and all readout channels
- 3439 • 4.8 Gbps maximum line rate for MiniPOD channels, i.e. all TTC, combined data and
3440 FELIX channels
- 3441 • DFE used for all receiver channels (as it uses more power)
- 3442 • 1.0 V differential swing on Hub FPGA readout output channels
- 3443 • 0.5 V differential swing on MiniPOD output channels
- 3444

3445 The MGT channel assignment from 18-Apr-2016 provided the list of GTH and GTY
3446 channels the Hub uses only as transmitters and as full transceivers, grouped by usage and by
3447 corresponding expected line rates. This list was used to configure the XPE GTH and GTY
3448 tabs.

Hub-Module ATCA Power Entry



6

Figure 44: Circuit diagram for Hub power entry.

Hub-Module Isolated +12V Supply

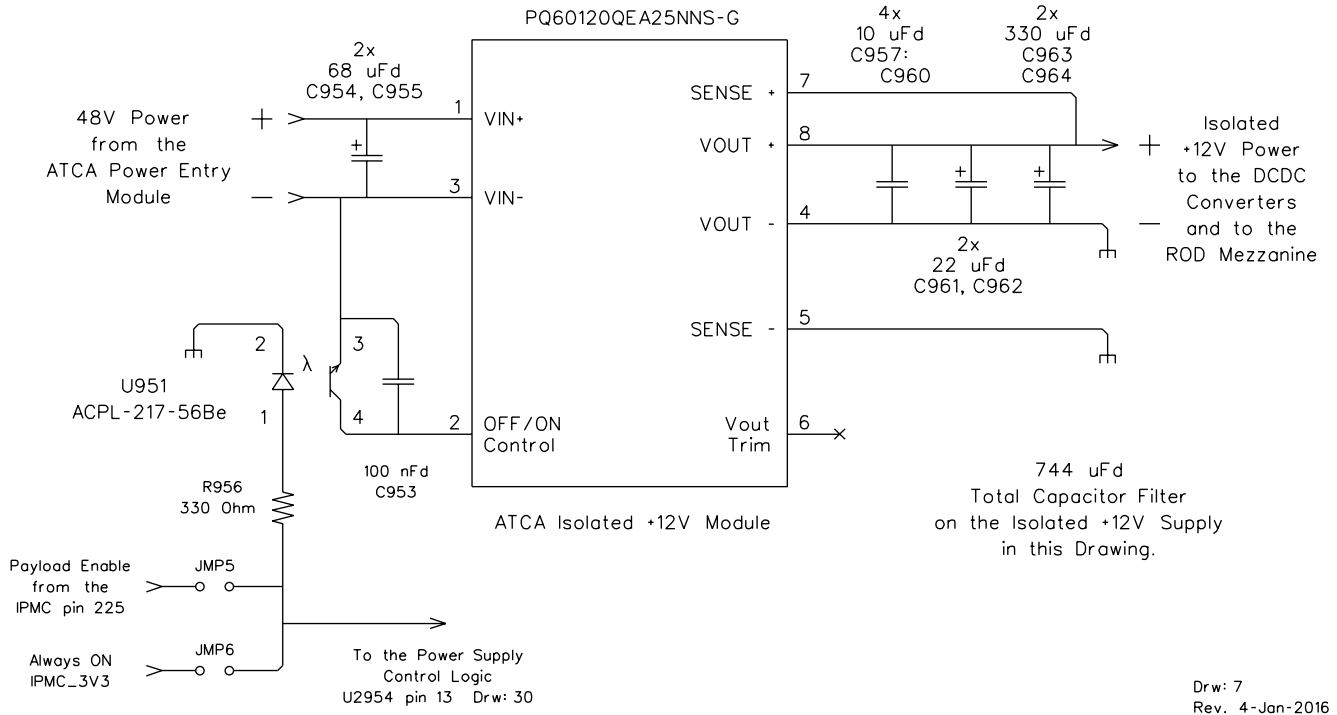
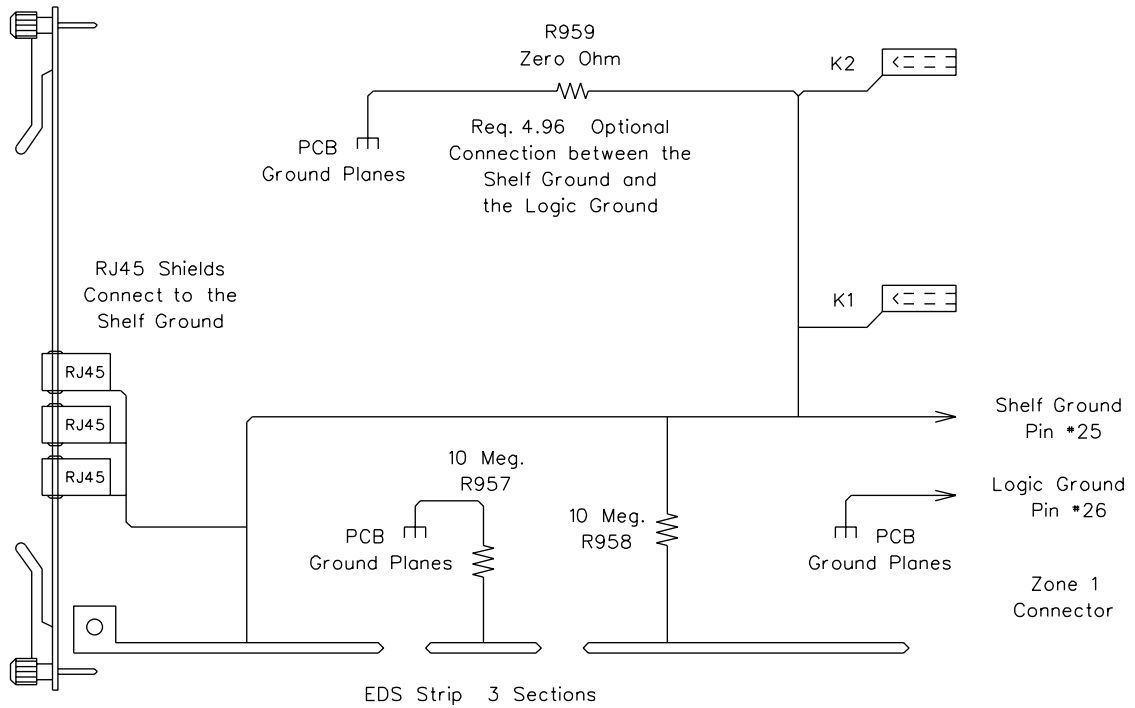


Figure 45: Circuit diagram for Hub +12V supply.

Hub-Module Ground Connections



The Front Panel Connects to the Front Section of the EDS Strip and thus to the Shelf Ground

Not shown are the 400 connections from the Zone 2 Connector Ground Pins to the PCB Ground Planes.

Drawing: 8
Rev. 4-May-2016

Figure 46: Circuit diagram for Hub ground connections.

Hub Module Power Supplies

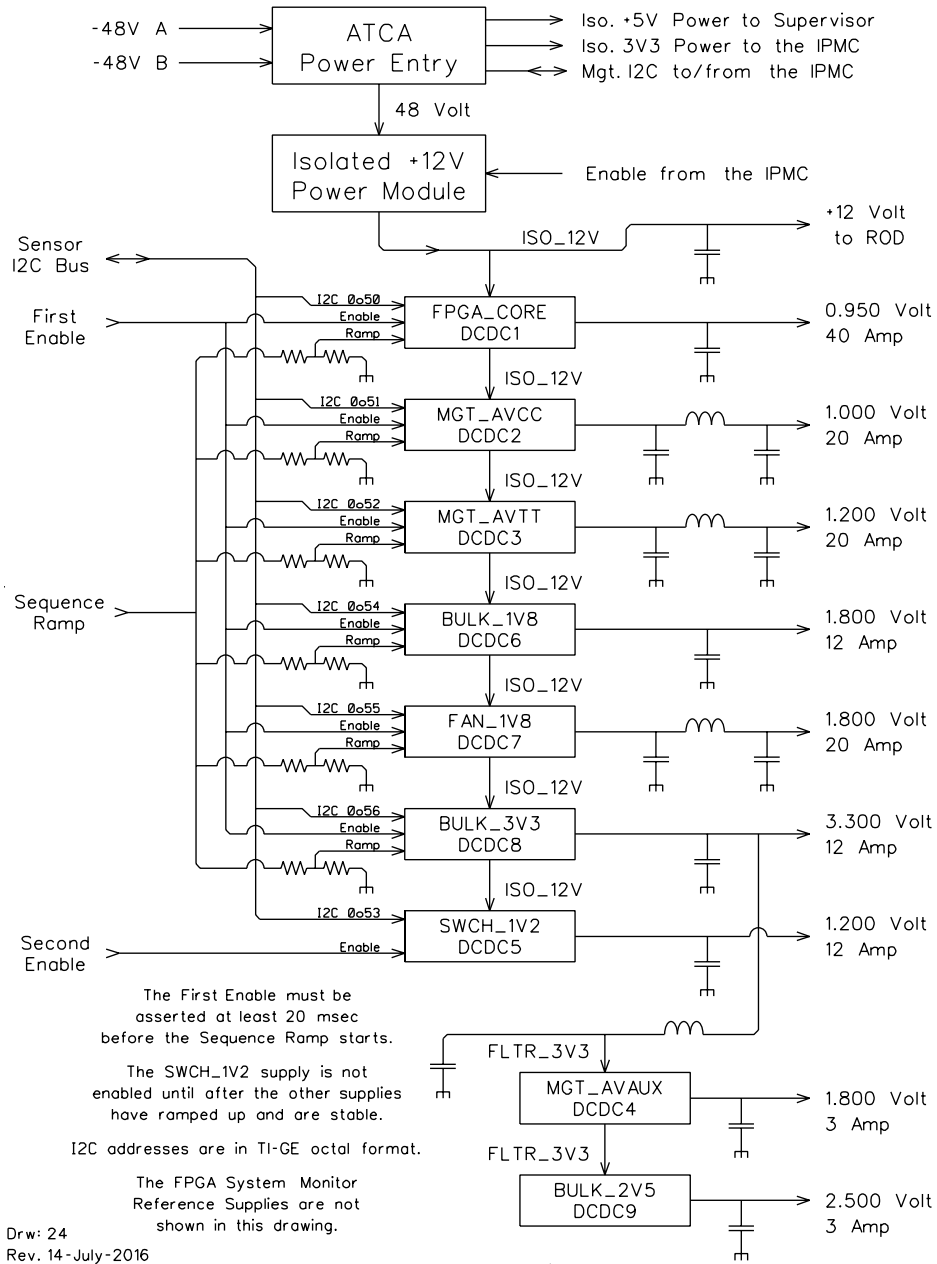
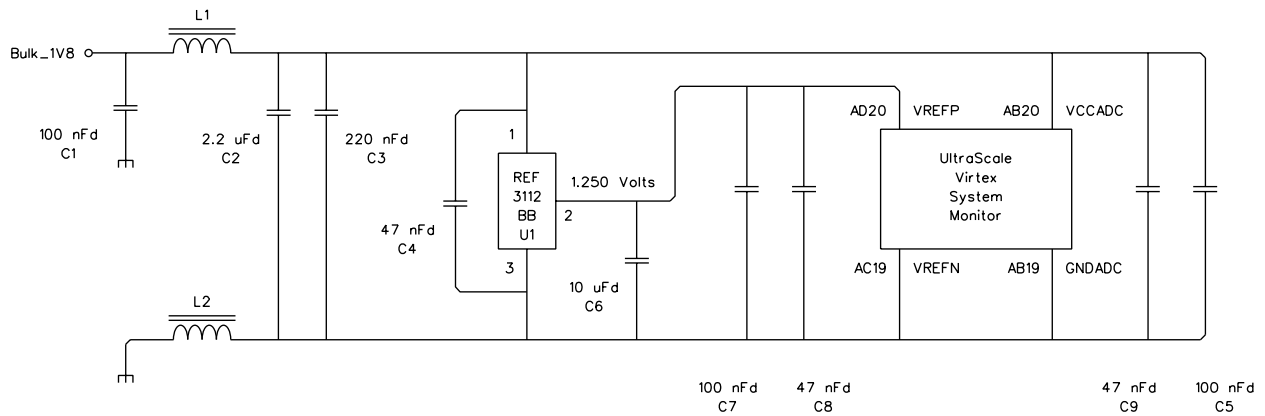


Figure 47: Circuit diagram for Hub power supplies.

HUB System Monitor Reference Supply

UltraScale Virtex FPGA System Monitor Reference



The inductors are Wurth 742792116, 1206, 60 mOhm.
See: SysMon UG580 Pg. 9 and 71, 72.

Actual reference designators are larger by 1850.

Figure 48: Circuit diagram for the Hub monitor reference supply.

Hub Module 40 Amp DC-DC Converter Design

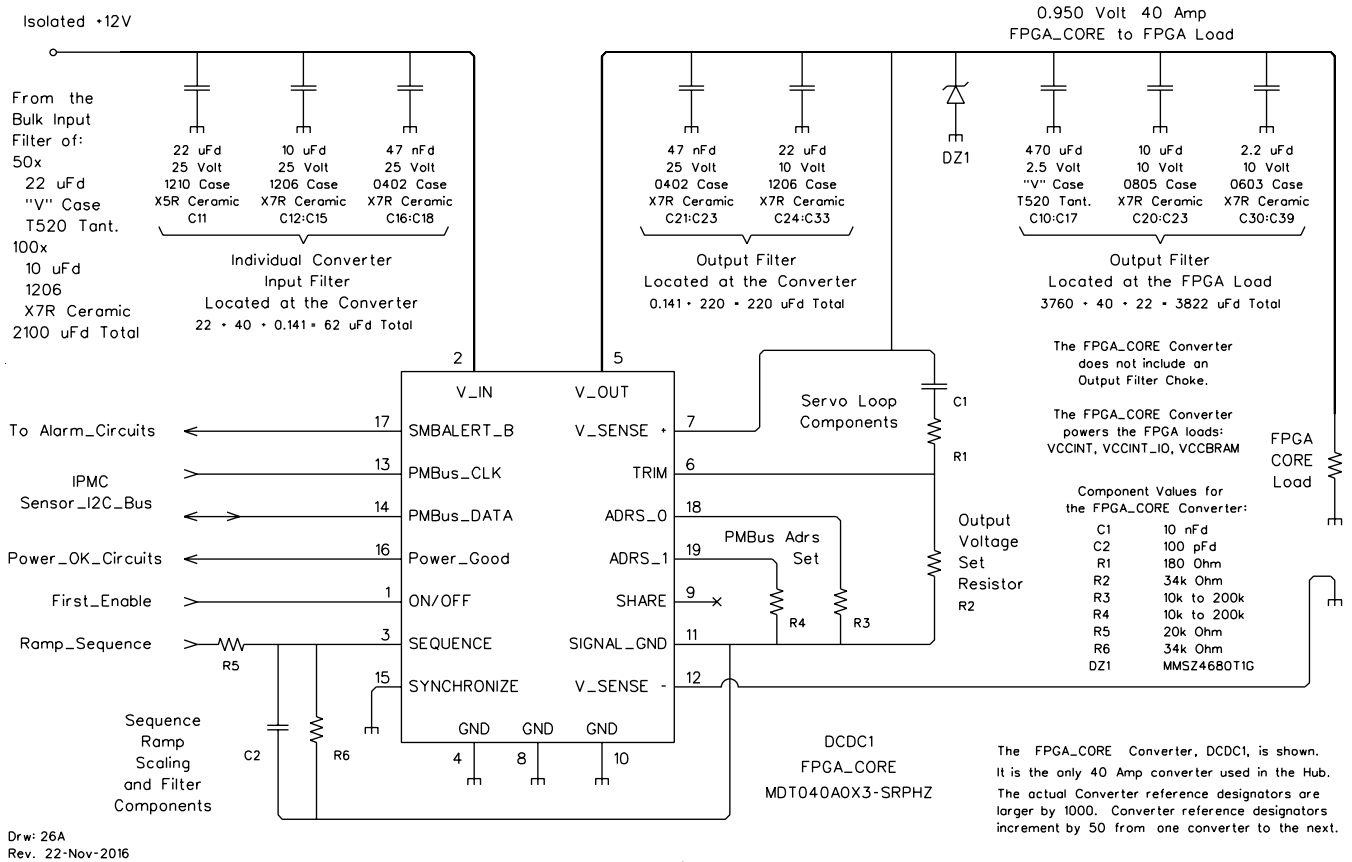


Figure 49: Circuit diagram for Hub 40A DCDC converter

Hub Module 20 Amp DC-DC Converter with External Filter

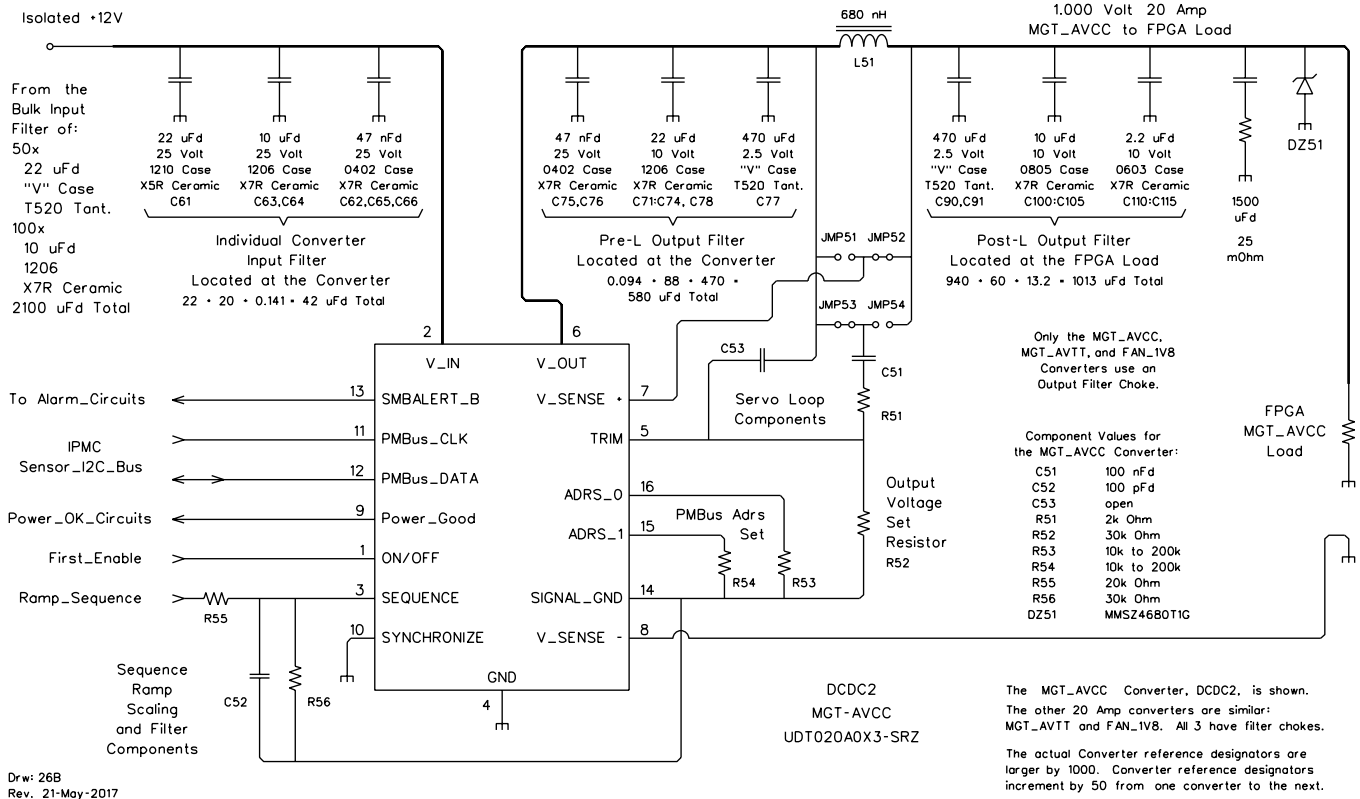


Figure 50: Circuit diagram for Hub 20A DCDC converter

Hub Module 12 Amp DC-DC Converter Design

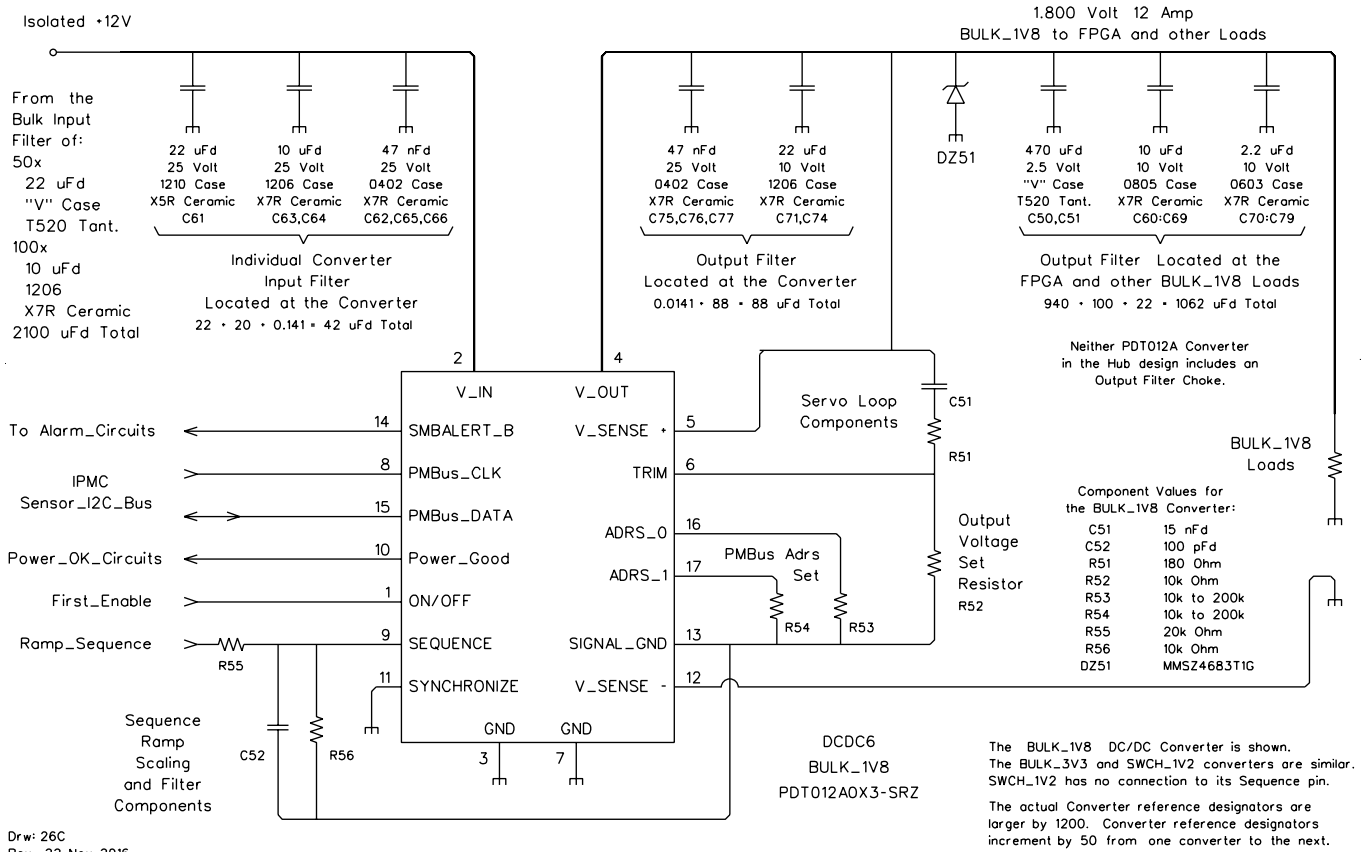
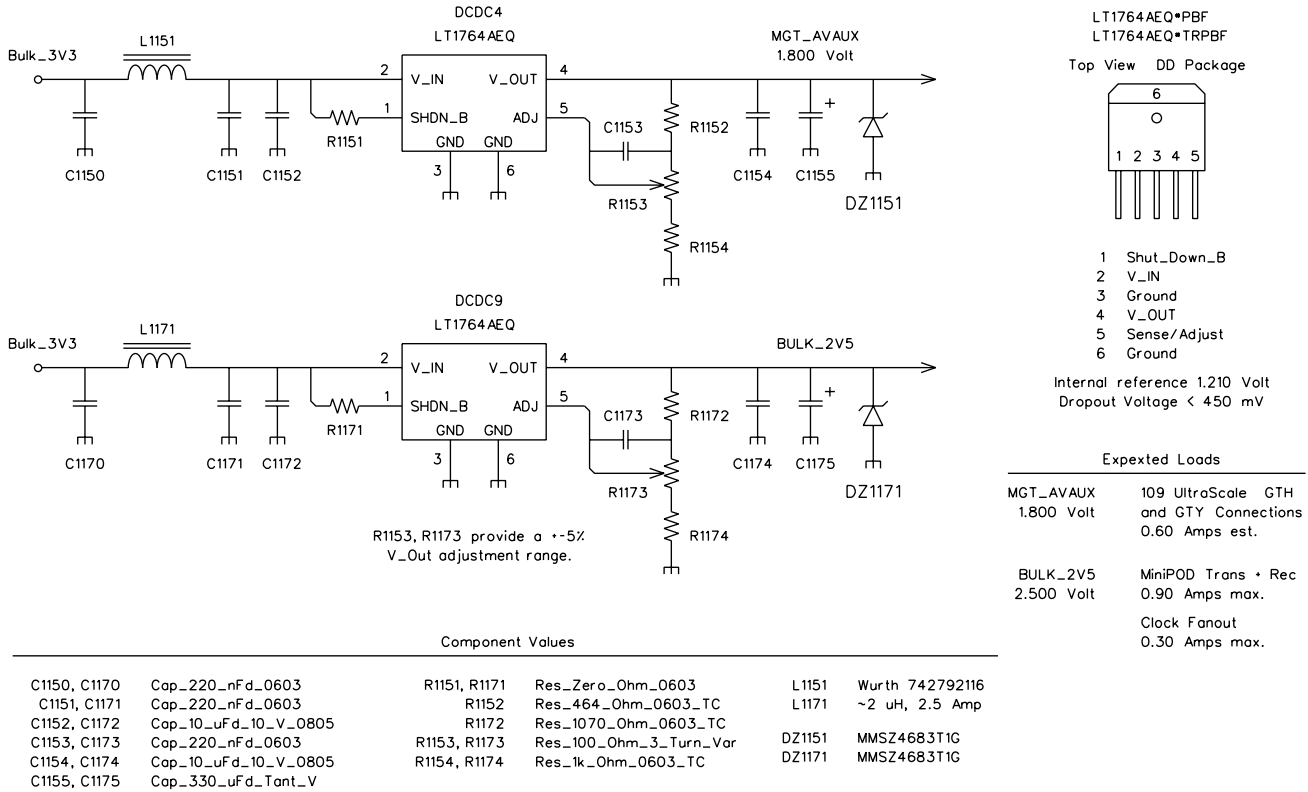


Figure 51: Circuit diagram for Hub 12A DCDC converter.

Hub Module Linear Regulators

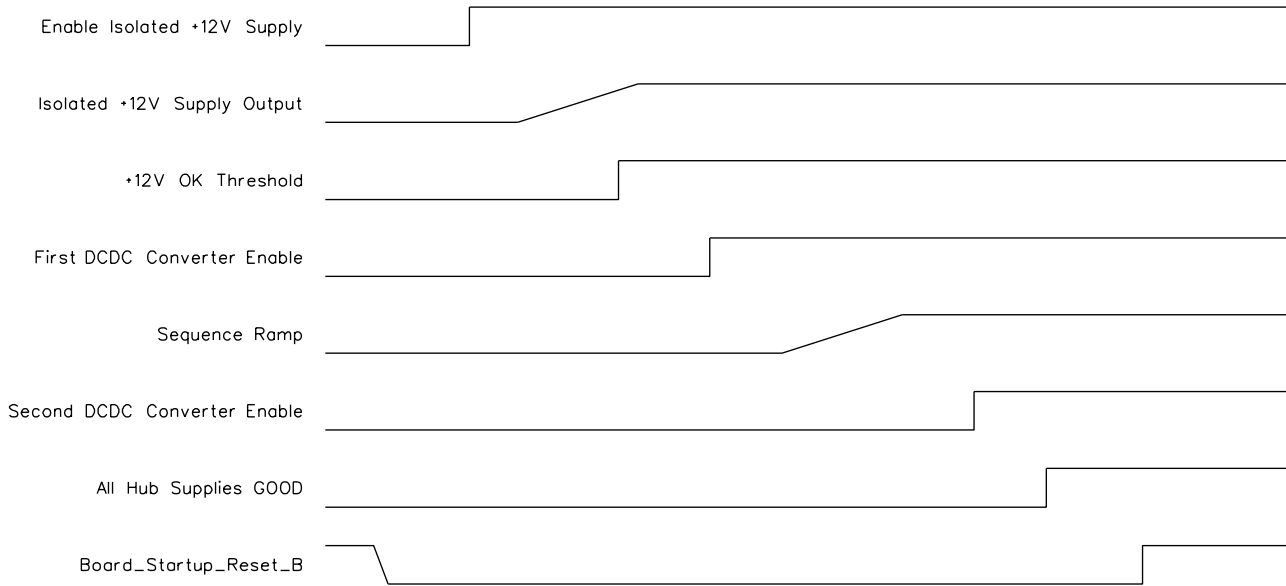


Drw: 27

Rev. 28-Sept-2016

Figure 52: Circuit diagram for Hub linear regulators.

Hub Power Supply Startup



Requirements

Allow the Isolated +12V Supply to stabilize for 500 msec before asserting the First DCDC Converter Enable.

First DCDC Converter Enable must be asserted for 20 msec minimum before the Sequence Ramp starts.

The Sequence Ramp should bring up the FPGA supplies in about 5 to 9 msec.

Once the Sequence Ramp is complete must wait a minimum of 10 msec before asserting the Second DCDC Converter Enable.

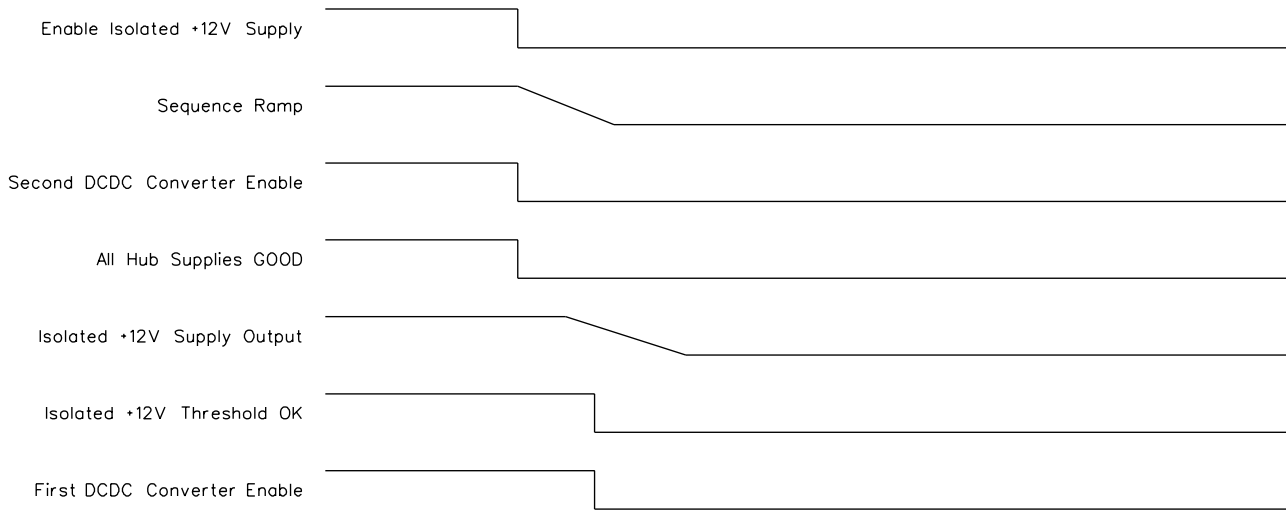
The SWCH_1V2 supply must ramp up within 2 msec maximum.

All supplies must be up and stable for 100 msec minimum before the Startup Reset is dropped.

Draw: 28
Rev. 11-Feb-2016

Figure 53: Hub power supply startup timing diagram.

Hub Power Supply Shutdown



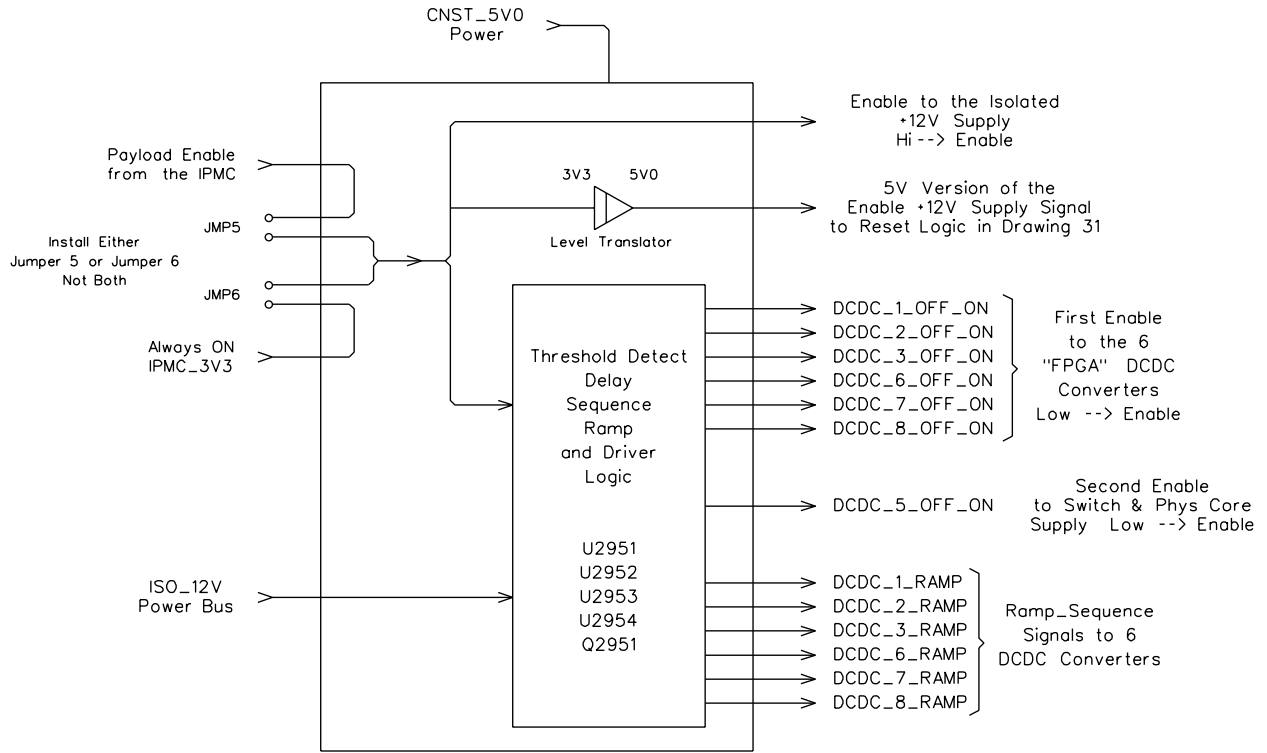
Sequence

When the Enable signal to the Isolated +12V Supply is dropped the Sequence Ramp will immediately begin to fall. The supplies will ramp down in an organized manner for as long as the Isolated +12V remains above threshold. Once the Isolated +12V bus falls below threshold then the First Enable signal to the 6 FPGA DCDC Converters is dropped. The Second Enable (to the SWCH_1V2 converter) is dropped as soon as the Isolated +12V Enable is deasserted.

Draw: 29
Rev. 11-Feb-2016

Figure 54: Hub power supply shutdown timing diagram.

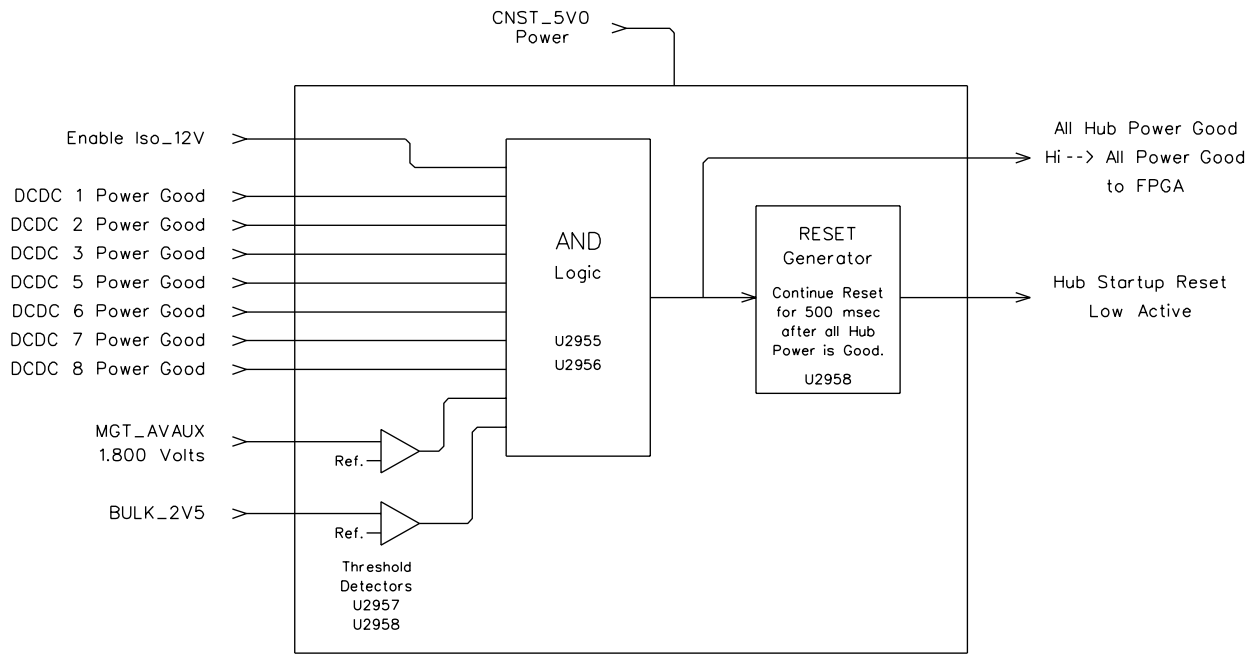
Block Diagram of Power Control Drawing #30



Drw: 30_Blk
Rev. 31-May-2016

Figure 55: Block diagram of Hub power control (1/2)

Block Diagram Power Good & Reset Drawing #31



Draw: 31_Blk
Rev. 28-Dec-2016

3492

3493

Figure 57: Block diagram of Hub power ready/reset (1/2).

3494

3495

3496

3497

3498

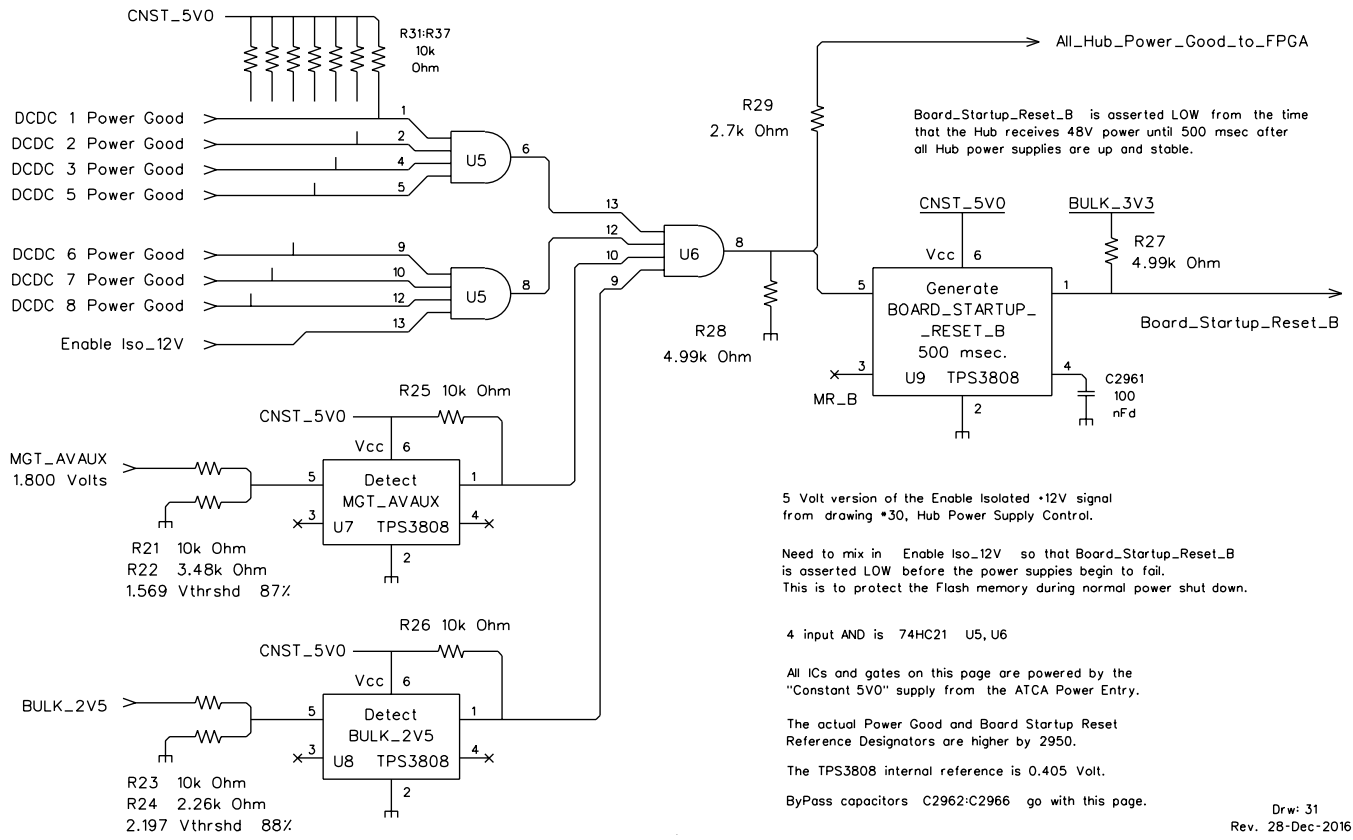
3499

3500

3501

3502

Hub Power Good and Board Startup Reset



3503

3504

3505

3506

3507

3508

Figure 58: Circuit diagram for Hub power ready/reset (2/2).

Board Reset Distribution - ROD Power Control

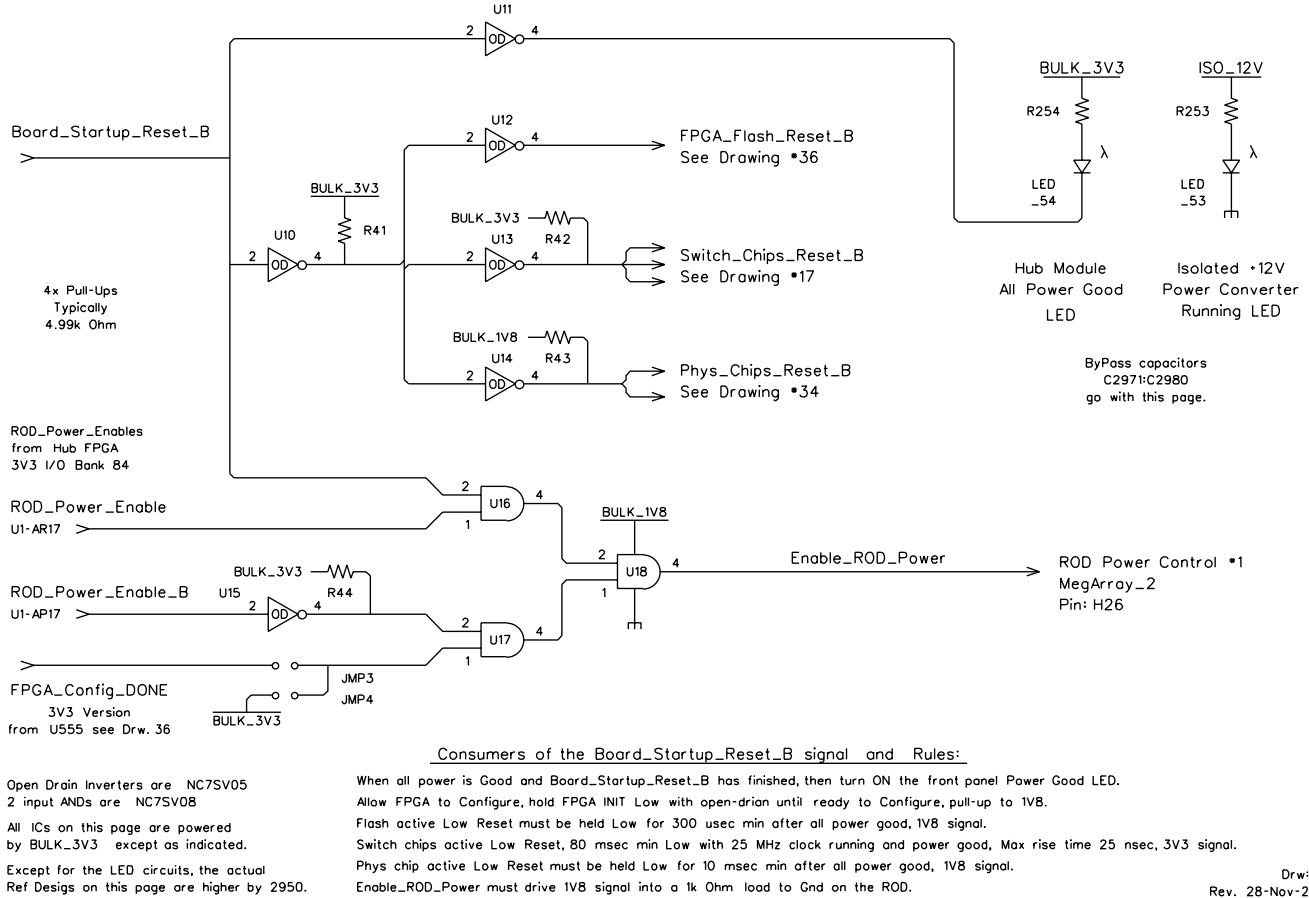


Figure 59: Circuit diagram for Hub board reset distribution.

3510 **29 Appendix 16: Hub-Module Base Interface Ethernet Switch**

3511 The Hub Module contains a Base Interface Ethernet Switch that is built from 3 Broadcom
3512 BCM 53128 KQLE switch chips. The Hub Module Ethernet switch provides ATCA Base
3513 Interface Ethernet connections to the following:

- 3514 • 12 to the FEX Cards via the backplane
- 3515 • to the Other Hub's FPGA via the backplane
- 3516 • to This Hub's FPGA via capacitor coupling
- 3517 • 4 Front Panel RJ-45s 1x to Switch Chip "A",
- 3518 • 2x to Switch Chip "B",
- 3519 • 1x to Switch Chip "C"

3520

3521 During normal operation the 4 front panel RJ-45 connections to the Ethernet Switch are used
3522 in the following way:

- 3523 • one is used for the "up-link" connection,
 - 3524 • one is used for the connection to the ROD or IPMC mezzanine on This Hub Module.
 - 3525 • one is used for the connection to the ROD or IPMC mezzanine on the Other Hub Module.
- 3526

3527 and there is one spare front panel RJ-45 connection to the Ethernet Switch.

3528 Internally there are 4 switch ports used to connect the 3 BMC53128 switch chips: Chip "A"
3529 <--> Chip "B" and Chip "B" <--> Chip "C".

3530 The Hub Module does not provide a Base Interface Ethernet connection to the Shelf
3531 Manager.

3532 With 2 Hub Modules in an ATCA Shelf the intent is that the switch in one module will
3533 provide connection to the "Control" Ethernet and the switch in the other Hub Module will
3534 provide connection to the "DCS" Ethernet.

3535 The FEX modules have an ethernet connection to both switches and thus to both
3536 networks.

3537 The Hub FPGAs also have an ethernet connection to both switches and thus to both
3538 networks.

3539 The RODs have only one ethernet connection and both the ROD on This Hub and the
3540 ROD on the Other Hub are connected to the Control network switch.

3541 The IPMCs have only one ethernet connection and both the IPMC on This Hub and the
3542 IPMC on the Other Hub are connected to the DCS network switch.

3543 Test systems may be operated with a single Hub Module that handles the Ethernet connects
3544 to both the single ROD and single Hub IPMC in the Shelf.

3545 The Hub's ethernet switch supports 10/100/1000 Base-T operation. The switch is based on 3
3546 Broadcom BCM53128 switch chips. These 3 chips are connected together to form one
3547 switch but can also be operated as 2 separate switches. Note that the part used is a
3548 BCM53128 not a BCM53128v

3549 **29.1 Power Supply for the BCM53128 Switch Chip**

3550 The BCM53128 Switch chip has some rather specific power supply requirements in terms of
 3551 the number of supplies, their noise level, and the order in which they are ramped up at power
 3552 on.

3553 The naming of the power buses to this switch chip does not seem to be consistent in all of the
 3554 BCM53128 documentation so one must be very careful. In the Hub design I have used
 3555 unambiguous versions of the BMC53128 power supply net names.

3556 Using the power supply net-names from the Data Sheet the required power rails are:

Data Sheet Power Net	Supplies Power to	Details
AVDDH	Analog I/O	3.3V from BULK_3V3 Net-name matches in the Design Guide the Demo Brd Sch and Data Sheet tables and Pin Lists.
AVDDL	Analog Core	1.2V from SWCH_1V2 DCDC Conv. Ferrite isolated on Demo Board. Net-name matches in the Design Guide the Demo Brd Sch and Data Sheet tables and Pin Lists.
DVDD	Digital Core	1.2V from SWCH_1V2 DCDC Conv. Called DVDD in Data Sheet and Sch. Called VDDC in the Design Guide.
OVDD	GMII-RGMII Port	Can be: 1.5V or 2.5V or 3.3V from BULK_3V3 on the Hub. This port is not used on the Hub. Called OVDD in Data Sheet and Sch. Called VDDO1 in the Design Guide.
OVDD2	Digital 3V3 I/O	3.3V from BULK_3V3 Called OVDD2 in Data Sheet and Sch. Called VDDO3 in the Design Guide.
GPHY1_BAVDD	Phys Analog	3.3V from BULK_3V3 Ferrite isolated on Demo Brd. Called GPHY1_BAVDD in Data Sheet Table 32 Signal Definitions and Design Guide Pg 62. Called GPHY1_BVDD in the Schematic and the Data Sheet Pin Lists. Called QGPHY1_BVDD1 in the Design Guide Pg 61.
GPHY2_BAVDD	Phys Analog	3.3V from BULK_3V3 Ferrite isolated on Demo Brd. Called GPHY2_BAVDD in Data Sheet Table 32 Signal Definitions and Design Guide Pg 62. Called GPHY2_BVDD in the Schematic and the Data Sheet Pin Lists. Called QGPHY2_BVDD1 in the Design Guide Pg 61.
PLL_AVDD	PLL Analog	1.2V from SWCH_1V2 DCDC Conv. Ferrite isolated on Demo Brd. Called PLL_AVDD in all documents but not listed Pg 61 Design Guide.
GPHY1_PLLDVDD	Phys Analog	1.2V from SWCH_1V2 DCDC Conv. Ferrite isolated on Demo Brd. Called

3576 As such I do not think that there are any Gnd pins on this part. Its one and only ground
3577 connection is through its center Exposed Thermal Pad.

3578 The power supply connections to a Switch Chip on the Hub Module are shown in **Figure 60**.

3579 **29.2 Power-Up Supply Sequencing**

3580 The required power supply ramp up sequence is discussed on page 62 and 63 of the Design
3581 Guide. They say that failure to properly sequence the supplies will not damage the device but
3582 the for “successful” power up the proper supply sequence must be followed and the Reset
3583 line used in the proper way.

3584 The BCM53128 device requires specific power sequencing between the core and I/O
3585 supplies.

3586 The device power sequence requires I/O power (3.3V, 2.5V) to come up first, followed by
3587 the core power (1.2V). The requirement is that the core power (1.2V) should not be on
3588 until the I/O power (3.3V, 2.5V) reaches at least 1.0V.

3589 When the core power reaches nominal core voltage (1.2V \pm 5%), the I/O power should
3590 be stable at nominal I/O voltage (3.3V \pm 5% or 2.5V \pm 5%).

3591 The max ramp-up time for core power 1.2V (from 0V to nominal voltage \pm 5%) is 2
3592 msec. See page 63.

3593 Additionally, for successful power-up, Broadcom recommends that the external hardware
3594 reset be active for at least 80 msec after both I/O and core power are stable. See page
3595 63.

3596 Note that the required power-up sequence rules out ramping all supplies Volt for Volt
3597 because they do not want any power on the core until the I/O is up to at least 1.0V.

3598 Thus the Hub Module needs a separate delayed 1.2V Core supply for the Switch Chips.
3599 Having a separate 1.2V supply for the Switch Chips was kind of in the cards anyway because
3600 clearly it can not be shared with the 1.2V Virtex MGT supply.

3601 The power supply current requirements on page 298 of the data sheet appear to be total
3602 current from the various voltage buses. I don't know if there are extra start up requirements.

3603 1.2 Volt 1130 mA
3604 2.5 Volt 26 mA (if used)
3605 3.3 Volt 496 mA

3606 **29.3 Hub Module Power Supply Design for Its Switch Chips**

3607 A separate 12 Amp supply is used for the Switch's 1.2 Volt requirements. This is a GE
3608 UDT020A0X1 DCDC Converter and it is enabled after the other DCDC Converters on the
3609 Hub Module have all ramped up and specifically after the BULK_3V3 converter has ramped
3610 up.

3611 The typical draw on this SWCH_1V2 bus for all 3 switch chips is expected to be 3.5 Amps.
 3612 The typical draw on the BULK_3V3 bus for all 3 switch chips is expected to be 1.5 Amps.
 3613 The expected heat load for all 3 switch chips is 9.2 Watts.

3614 The OVDD power bus to the Switch Chips can be either 2.5 Volt or 3.3 Volt. The OVDD
 3615 rail powers the GMII - RGMII port I/O pins. On the Hub Module the GMII-RGMII port is
 3616 not used and for convenience the OVDD rail is powered from the BULK_3V3 supply.

3617 The sources of the 11 supply rails to the BCM53128 Switch Chips on the Hub Module are the
 3618 following:

3619	AVDDL	1.2V	from SWCH_1V2 DC/DC Converter
3620	DVDD	1.2V	from SWCH_1V2 DC/DC Converter
3621	PLL_AVDD	1.2V	from SWCH_1V2 DC/DC Converter
3622	GPHY1_PLLDVDD	1.2V	from SWCH_1V2 DC/DC Converter
3623	GPHY2_PLLDVDD	1.2V	from SWCH_1V2 DC/DC Converter
3624	AVDDH	3.3V	from BULK_3V3 DC/DC Converter
3625	OVDD	3.3V	from BULK_3V3 DC/DC Converter
3626	OVDD2	3.3V	from BULK_3V3 DC/DC Converter
3627	GPHY1_BAVDD	3.3V	from BULK_3V3 DC/DC Converter
3628	GPHY2_BAVDD	3.3V	from BULK_3V3 DC/DC Converter
3629	XTAL_AVDD	3.3V	from BULK_3V3 DC/DC Converter

3630 **29.4 Switch Chip Bypass Capacitors and Filter Chokes**

3631 Recall the power supply bypass capacitors recommended by Broadcom. The following is a
 3632 combination of the BCM53128 Design Guide and the Demo Board Schematic.

- 3633 • PLL_AVDD pin (each one) is connected to the Analog 1.2V plane via the ferrite bead.
 3634 Each pin is bypassed with 22 uFd and 100 nFd capacitors.
 - 3635 • AVDDL pins are connected to the Analog 1.2V plane and bypassed with a 33 uFd
 3636 capacitor. Each pin is decoupled with a 1.0 uFd capacitor.
 - 3637 • DVDD pins are connected to the Digital 1.2V plane and bypassed with a 10 uFd
 3638 capacitor. Each pin is bypassed with a 100 nFd capacitor.
 - 3639 • GPHY1_PLLDVDD pins are connected to the Digital 1.2V plane and bypassed with a 10
 3640 uFd capacitor. Each pin is bypassed with a 100 nFd capacitor.
 - 3641 • GPHY2_PLLDVDD pins are connected to the Digital 1.2V plane and bypassed with a 10
 3642 uFd capacitor. Each pin is bypassed with a 100 nFd capacitor.
 - 3643 • XTAL_AVDD pins are connected to the 3.3V plane and bypassed with a 100 nFd
 3644 capacitor.
-

- 3645 • AVDDH pins are connected to the 3.3V plane and bypassed with a 33 uFd capacitor.
3646 Each pin is bypassed with a 1.0 uFd capacitor.
 - 3647 • OVDD2 pins are connected to the 3.3V plane and bypassed with a 10 uFd capacitor.
3648 Each pin is bypassed with a 100 nFd capacitor.
 - 3649 • OVDD pins are connected to either the 2.5V or 3.3V plane and bypassed with a 10 uFd
3650 capacitor. Each pin is bypassed with a 100 nFd capacitor.
 - 3651 • GPHY1_BAVDD pins are connected to the 3.3V plane and bypassed with a 10 uFd
3652 capacitor. Each pin is bypassed with a 100 nFd capacitor.
 - 3653 • GPHY2_BAVDD pins are connected to the 3.3V plane and bypassed with a 10 uFd
3654 capacitor. Each pin is bypassed with a 100 nFd capacitor.
- 3655 On the Hub Module the following 7 supply rails to the switch chips are isolated with a ferrite
3656 filter chokes:
- | | | |
|------|---------------|------|
| 3657 | AVDDL | 1.2V |
| 3658 | PLL_AVDD | 1.2V |
| 3659 | GPHY1_PLLDVDD | 1.2V |
| 3660 | GPHY2_PLLDVDD | 1.2V |
| 3661 | GPHY1_BAVDD | 3.3V |
| 3662 | GPHY2_BAVDD | 3.3V |
| 3663 | XTAL_AVDD | 3.3V |

3664

3665 From the demo board schematics I believe that ferrite chokes with a reactance of 600 Ohms
3666 at 100 MHz and a 2 Amp capacity with less than 100 mOhm resistance is adiqute for all 7 of
3667 these applications.

3668 On the Hub Module the following 4 supply rails to the switch chips are not isolated with a
3669 filter choke:

3670	DVDD	1.2V
3671	AVDDH	3.3V
3672	OVDD	3.3V
3673	OVDD2	3.3V

3674 **29.5 The BCM53128 Switch Capacitive Coupling**

3675 Page 29 of the BCM53128 Design Guide explains that capacitive coupling can be used
3676 between pairs of BCM53128 chips for all 3 ethernet speeds. Capacitive coupling works
3677 between BMC53128 chips because the BCM53128 uses Voltage Mode Phy technology.

3678 Capacitive coupling should also work between the BMC53128 and other parts that use
3679 Voltage Mode Phy technology.

3680 There are termination schemes that use capacitive coupling between the BCM53128 and parts
3681 with older Current Mode Phys parts but this is probably speed dependent and is not needed
3682 on the Hub Module.

3683 The Micrel KSZ9031 Phys has a voltage mode transmitter connection to the medium so it
3684 can probably work with capacitive coupling. The KSZ9031 data sheet talks only about
3685 connection with magnetics. Because the KSZ9031 has voltage mode transmitters, the center
3686 tap on the chip's side of the transformer should just be tied to ground with a 100 nFd
3687 capacitor (i.e. not connection to a power bus). This is just like the transformer connection to
3688 the BCM53128 switch chip.

3689 The Hub Module design uses capacitive coupling between the 3 BCM53128 Switch chips
3690 and between the BCM53128 and the KSZ9031RNX Phys for the Hub's FPGA.

3691 **29.6 Switch Chip Orientation and Port Connections**

3692 For all 3 Switch Chips their pin #1 will be in the SE corner.

3693 The 1:64 edge is to the East with its Clock, JTAG, 3 LED, and unused IMP connections.

3694 The 65:128 edge is to the North. This is Ports 4:7 with Port 4 closest to the Hub's back edge.

3695 The 129:192 edge is to the West. This is a bunch of unused IMP stuff and then the bulk of
3696 the LED connections.

3697 The 193:256 edge is to the South. This is a few LED connections and then Ports 0:3 with
3698 Port 3 closest to the back edge of the Hub.

3699 Based on the placement of the Switch Chips running B, A, C across the card from front to
3700 back and based on the Switch Chip's orientation the following Port assignments are the most
3701 straight forward to route.

3702 Chip "A" U31 is in the center of the row:

3703 Port 0 to J24 Row 8 BI Channel 14 Slot 14 FEX

3704 Port 1 to J24 Row 7 BI Channel 13 Slot 13 FEX

3705 Port 2 to J24 Row 6 BI Channel 12 Slot 12 FEX

3706 Port 3 to J24 Row 5 BI Channel 11 Slot 11 FEX

3707 Port 4 to J24 Row 4 BI Channel 10 Slot 10 FEX

3708 Port 5 to J24 Row 3 BI Channel 9 Slot 9 FEX

3709 Port 6 to Front Panel RJ-45 Connector RJ2 Lower/Left

- 3710 Port 7 to Switch Chip “B” Capacitor Coupled
- 3711
- 3712
- 3713
- 3714 Chip “B” U32 is the “center” Switch Chip:
- 3715 Port 0 not used
- 3716 Port 1 not used
- 3717 Port 2 to Switch Chip “A” Capacitor Coupled
- 3718 Port 3 to Switch Chip “C” Capacitor Coupled
- 3719 Port 4 to This Hub’s FPGA Capacitor Coupled
- 3720 Port 5 to J20 Row 3 Update Channel to Other Hub
- 3721 Port 6 to Front Panel RJ-45 Connector RJ3 Lower/Left
- 3722 Port 7 to Front Panel RJ-45 Connector RJ3 Upper/Right
- 3723
- 3724
- 3725 Chip “C” U33 is near the cards backplane edge:
- 3726 Port 0 to J24 Row 2 BI Channel 8 Slot 8 FEX
- 3727 Port 1 to J24 Row 1 BI Channel 7 Slot 7 FEX
- 3728 Port 2 to J23 Row 10 BI Channel 6 Slot 6 FEX
- 3729 Port 3 to J23 Row 9 BI Channel 5 Slot 5 FEX
- 3730 Port 4 to J23 Row 8 BI Channel 4 Slot 4 FEX
- 3731 Port 5 to J23 Row 7 BI Channel 3 Slot 3 FEX
- 3732 Port 6 to Front Panel RJ-45 Connector RJ2 Upper/Right
- 3733 Port 7 to Switch Chip “B” Capacitor Coupled
- 3734
- 3735
- 3736

3737 **29.7 Assignment of Ethernet “Magnetics”**

3738 These assignments are given in Section 17.

3739 **29.8 Assignment of Front Panel RJ-45 Connectors**

3740 These assignments are given in Section 17.

3741 **29.9 Resistor Set Pin**

3742 The RDAC pins, GPHY1_RDAC pin 228 and GPHY2_RDAC pin 96 must be connected
3743 to Ground with 1.24k Ohm 1% resistors.

3744 **29.10 Unused Tie Hi, Tie Low, Float Pins**

3745 There are a number of un-used and no-connect pins on the switch chips. Some of the un-used
3746 pins must be tied Hi or Low - others must be left floating.

3747 IMP_VOL_REF pin 146 must be tied to Ground.

3748

3749 CLK_FREQ0/GPIO0 pin 14 must be left floating

3750 CLK_FREQ1/GPIO1 pin 15 must be left floating

3751

3752 IMP RGMII Inputs: RXCLK, RXD(3:0), RXCTL (aka RXDV)

3753 should all be Pulled-Down These are pins:

3754 144, 154, 152, 151, 150, 149

3755

3756 LOOP_DETECTED pin 58 warning buzzer if a Loop

3757 *is Detected - float*

3758 No Connect Pins from BCM Datasheet:

3759 NC 5 this is a second MDIO aka MDIO2

3760 NC 6 this is a second MDC aka MDC2

3761 NC 20

3762 NC 28

3763 NC 37

3764 NC 39

3765 NC 41

3766 NC 42

3767 NC 45

3768 NC 46

3769 NC 69

3770 NC 70

3771 NC 99

3772 NC 225

3773 Other unused pins, e.g.

3774 LEDCLK 167 HP has small cap to gnd Kit has 100 pFd to gnd

3775 LEDDATA 166 HP has small cap to gnd Kit floats

3776

3777 TRST pin 36 has an internal Pull-Up but Must be pulled Low

3778 7. for normal operation. See datasheet page 129.

3779 8. Kit has a DNI pull-down. HP has a pull-down.

3780 **29.11 EEPROM Connection to the Switch Chip**

3781 The BCM53128 contains about 200 internal registers. The initial running state of many of
3782 these registers may be set at power up by the contents of an attached EEPROM.

3783 **Figure 61** shows the connection of this EEPROM to the BCM53128 switch. This drawing
3784 also shows the Clock, Reset, and management connections to the Switch Chip.

3785 The EEPROM is an AT93C66B device with 8 pins. Note that an earlier Atmel device
3786 (AT93C66A-2.7) had originally been specified for use with the BCM53128. This EEPROM
3787 is powered from the 3V3 bus and 4 of its pins connect to the switch chip:

3788 SS slave select pin 160 Low active to the EEPROM

3789 SCK SPI Clock pin 163 to the EEPROM

3790 MOSI Master Out Slave In pin 164 input to the EEPROM

3791 MISO Master In Slave Out pin 161 output from EEPROM

3792

3793 All 4 of these pins use series damping resistors, e.g. 22 Ohm. In addition to these 4 signal
3794 pins this EEPROM has one power pin and one ground pin and one not connected pin.

3795 The ORG pin on the EEPROM is pulled up to set it for 16 bit words. The AT93C66B
3796 stores 256 16 bit words.

3797 Note that this: SS, SCK, MOSI, MISO interface to the switch chip can be used for either:
3798 EEPROM or SPI bus - but not for both. It's use is set for ever more at power up by the
3799 CPU_EEPROM_SEL strapping pin, pin 18. Pull it down to enable use with the EEPROM.
3800 At power up I think it's basically an issue of setting up the switch's SPI port as a SPI master
3801 or a slave.

3802 We still have the questions of what content to put into this EEPROM for the Hub application,
3803 can all 3 EEPROMs contain exactly the same data, how to program them, and how to change
3804 their data if there is a problem in the future.

3805 Because of these uncertainties I want to put the EEPROMs on the back side of the Hub PCB
3806 and keep them open and easy to change. To facilitate this I will use an SOIC-8 part. This
3807 should be part number: AT93C66B-SSHM -B or -T. Both are good DK numbers. This is a
3808 normal SOIC with a 3.90 mm wide body, i.e. feet about 6.00 mm wide. Atmel says that its
3809 maximum height is 1.75 mm so it fits within the Hub's 2.00 mm side 2 comp height rule.

3810 **29.12 SPI Bus Connection**

3811 The BCM53128 switch chip includes a serial SPI bus connection. This SPI serial bus allows
3812 control and monitoring of the chip through its various registers. The problem is that the SPI
3813 serial bus and the EEPROM share the same pins on the device. At power up, a strapping
3814 option sets these pins to operate as either an SPI bus interface or as an EEPROM interface.
3815 Once this option is set it can not be changed.

3816 In the Hub Module we need to use these pins for EEPROM setup of the switch chips. For
3817 subsequent control and monitoring of the switch chips from the Hub's FPGA we need to use
3818 the MDC MDIO management interface to the device.

3819 **29.13 MDC MDIO Connection to the Hub's Virtex FPGA**

3820 The Hub uses the Switch Chip's MDC MDIO port in slave mode so that an external entity,
3821 i.e. the Hub's FPGA, can access registers within the Switch. See the Datasheet starting at
3822 page 112 and on page 128. See the Design Guide starting on page 56.

3823 MDIO pin 61 Data I/O pin

3824 "In slave mode, it is used by an external entity to read/write to the switch registers via the
3825 Pseudo-PHY."

3826 MDC pin 62 Clock pin

3827 "In slave mode (the clock) is sourced by an external entity."

3828 **29.14 Switch Chip Reset**

3829 The BCM53128 Switch Chip needs a Reset signal that remains asserted until 80 msec after
 3830 all of its power supply rails are fully ramped up. We may also want to be able to reset one or
 3831 all of the Switch Chips from a protected register in the Hub Module's Virtex FPGA. The
 3832 minimum pulse width of the Reset signal is 1 msec. One must wait 50 msec after the end of
 3833 the Reset signal before trying to talk to the switch chip via its SPI bus. The Reset signal is
 3834 pin 17. The Reset signal is Low active.

3835 **29.15 Clock to the Switch Chip**

3836 The Hub Module uses an external 25 MHz clock source to provide the clock to all 3 of its
 3837 Switch Chips. This external clock enters the chip on its XTAL1 pin 34 and the XTAL0 pin
 3838 33 is left floating. The clock source for the Switch Chips must be:

3839 25 MHz +/- 50 ppm,
 3840 50% duty cycle,
 3841 1 to 4 nsec edge speed,
 3842 3V3 CMOS level,
 3843 5 ppm per year,
 3844 10 ppm over temperature,
 3845 less than 100 psec jitter
 3846 very low jitter in the 5 kHz to 1 MHz band.
 3847

3848 The Hub Module supplies this clock from a Connor Winfield CWX813-025.0M oscillator
 3849 with a 6x fanout and series terminator resistors.

3850 **29.16 Switch Chip Functions That Are Not Used on the Hub**

3851 One must understand whether or not any pull-up / pull-downs are needed to not use these
 3852 functions so that they just sit quietly as good citizens.

- 3853 • Flash Memory, pins: FSO 64, FCSB 65, FSCLK 66, FSI 67 Note that the Flash
 3854 Memory is for 8051 code only.
- 3855 • JTAG, pins: TDO 22, TDI 23, TCK 24, TMS 25, TRST 36
- 3856 • IMP Interface - this is the Inband-Management-Port, i.e. a PhysLess port that can
 3857 operate as: GMII, RGMII, MII, TMII, RxMII or whatever to manage the switch chip.
 3858 We do not want it at all - thus we must tie DIS_IMP strap pin Hi. The IMP pins - note
 3859 that the Design Guide says to tie Low unused IMP pins: RXCLK, RXD(3:0), RXCTL but
 3860 that neither the Kit or HP does this.
- 3861 • List of IMP pins:
 3862

3863 IMP_VOL_REF 146 must be tied Low

3864 IMP_VOL_SEL1 48, IMP_VOL_SEL0 49

3865 IMP_COL 159, IMP_CRS 143

3866 IMP_DUPLEX 52, IMP_LINK 54

3867 IMP_MODE0/GPIO5 7, IMP_MODE1/GPIO6 8
 3868 IMP_PAUSECAP_RX 55, IMP_PAUSECAP_TX 56
 3869 IMP_SPEED1 50, IMP_SPEED0 51
 3870 IMP_GTXCLK 132, IMP_RXCLK 144
 3871 IMP_RXD0 150, IMP_RXD1 151
 3872 IMP_RXD2 152, IMP_RXD3 154
 3873 IMP_RXD4 155, IMP_RXD5 156
 3874 IMP_RXD6 157, IMP_RXD7 158
 3875 IMP_RXDV 149, IMP_RXER 147
 3876 IMP_TXCLK 141, IMP_TXD0 137
 3877 IMP_TXD1 136, IMP_TXD2 134
 3878 IMP_TXD3 131, IMP_TXD4 130
 3879 IMP_TXD5 128, IMP_TXD6 127
 3880 IMP_TXD7 126, IMP_TXEN 139
 3881 IMP_TXER 140

3882 **29.17 Switch Chip Bypass Capacitor and Filter Update**

3883 During the tentative final placement of the 100 or so RCL comps for each Switch chips the following
 3884 changes were made:

3885
 3886 PLL_AVDD C01 C02 L01 no-change
 3887 GPHY1_PLLDVDD C03 C04 L02 no-change
 3888 GPHY2_PLLDVDD C05 C06 L03 no-change
 3889 GPHY1_BAVDD C07 C08 L04 no-change
 3890 GPHY2_BAVDD C09 C10 L05 no-change
 3891 XTAL_AVDD C11 C12 L06 no-change
 3892
 3893 DVDD SWCH_1V2 C36,C37 C38:C47 no-change
 3894

3895 AVDDL 1V2 C13,C14 C16:C30 L07

3896 remove from set: C15 C33,C34,C35

3897

3898

3899 AVDDH \ C48, C49, C50

3900 OVDD | BULK_3V3 C51:C62

3901 OVDD2 / C78:C85

3902

3903 remove from set: C67, C68, C76, C77

3904 C63, C64, C65, C66

3905 C69:C75

3906 C86:C90

3907

3908 The components that have been removed from the relatively positioned component set are now in
3909 their own comps file for manual positioning.

3910

3911 Other Changes in Switch Comps:

3912

3913 R2x19 the clock series terminator has been moved

3914 out of the Switch Chip Comps files and into

3915 the 25 MHz Enet Clock Generator comps file.

3916

3917 C2x91 for the Switch EEPROM has been moved to the

3918 top side of the card.

Switch Chip - Support Circuits 1

Signals to/from pins in the Hub's
UltraScale FPGA 3V3 Select I/O Banks

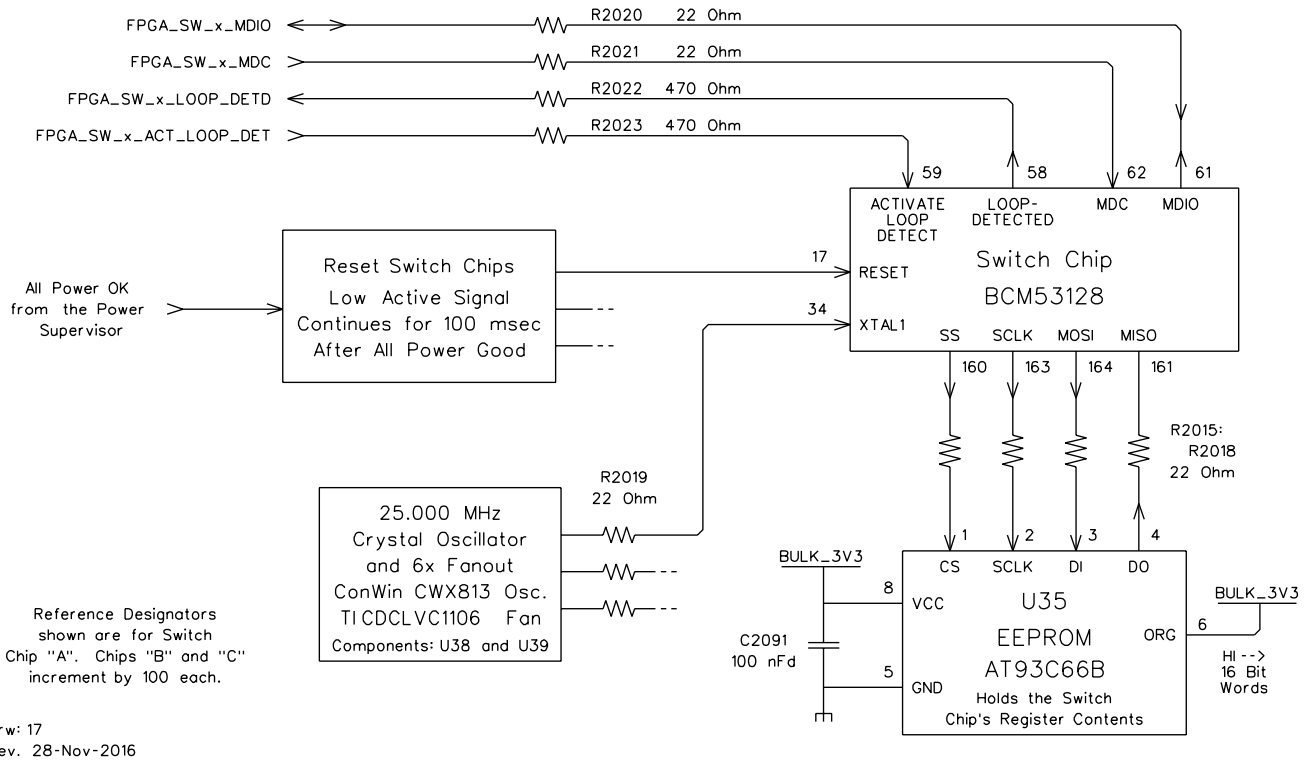
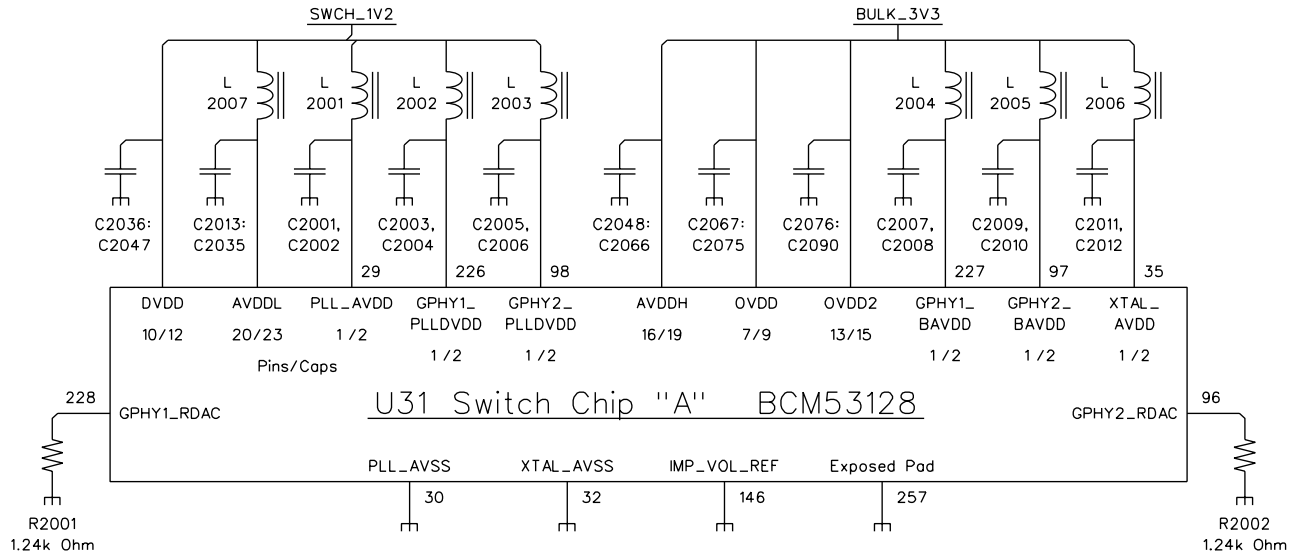


Figure 60: Hub switch chip support circuit diagram (1/3).

Switch Chip - Support Circuits 2



DVDD Pins: 16, 27, 31, 40, 53, 135, 148, 162, 169, 183

AVDDL Pins: 71, 77, 83, 89, 95, 100, 106, 112, 118, 124, 200, 206, 212, 218, 224, 229, 235, 241, 247, 253

AVDDH Pins: 74, 80, 86, 92, 103, 109, 115, 121, 203, 209, 215, 221, 232, 238, 244, 250

OVDD Pins: 125, 129, 133, 138, 142, 145, 153

OVDD2 Pins: 3, 11, 19, 43, 44, 57, 63, 68, 165, 173, 180, 187, 193

Reference Designators are shown for U31 Switch Chip "A".

Reference Designators increment by 100 going to chips "B" and "C".

10 uFd Capacitors: C2001, C2003, C2005, C2007, C2009, C2011, C2013:C2015, C2036, C2037, C2048:C2050, C2067, C2068, C2076, C2077

1 uFd Capacitors: C2016:C2035, C2051:C2066

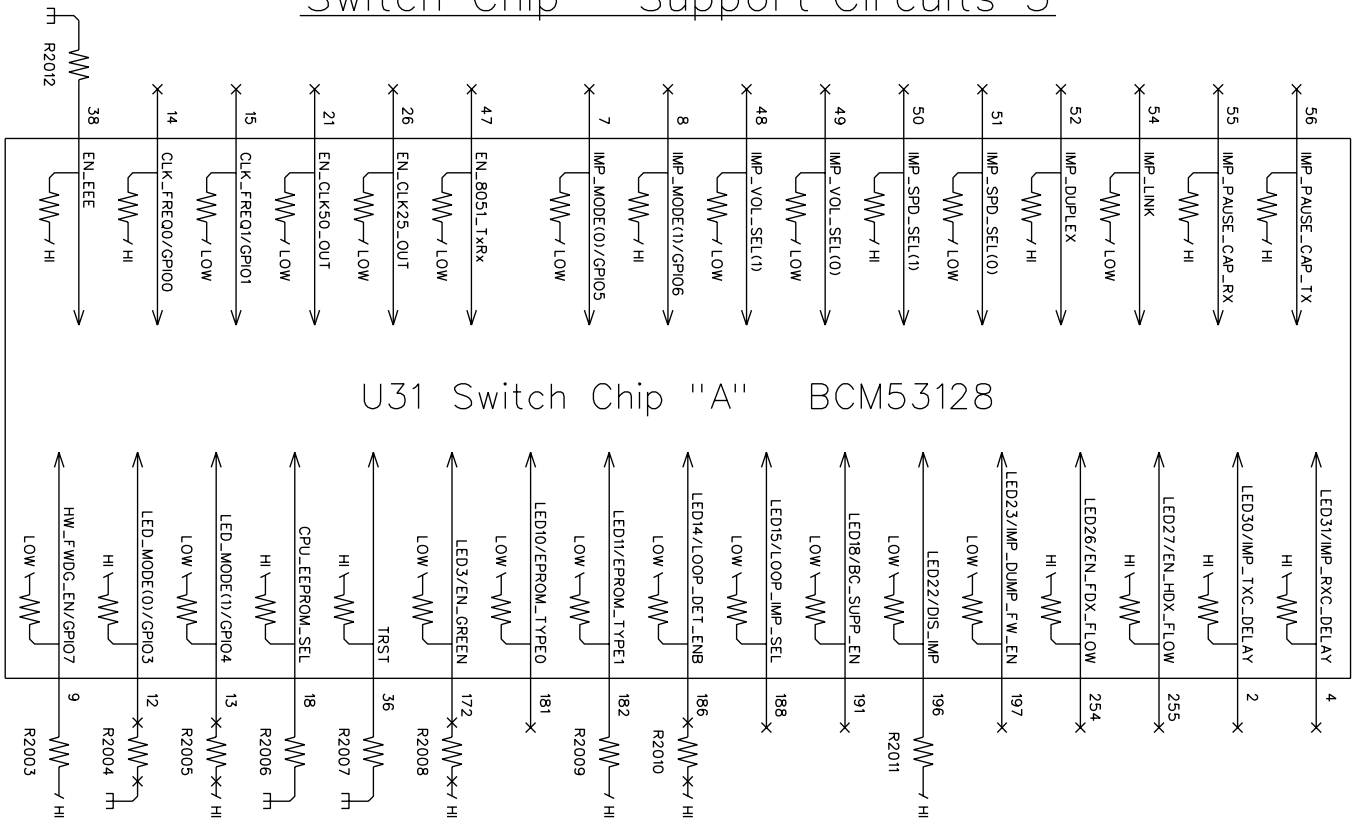
100 nFd Capacitors: C2002, C2004, C2006, C2008, C2010, C2012, C2038:C2047, C2069:C2075, C2078:C2090

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18

Figure 61: Hub switch chip circuit diagram (2/3).

Switch Chip - Support Circuits 3



U31 Switch Chip "A" BCM53128

Drw: 19

Jumper Reference Designators Increment by 100 for U32 and by 200 for U33.

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Figure 62: Hub switch chip circuit diagram (3/3).

3922 **30 Appendix 17: Switch Chip Associated Jumpers**

3923 The BMC53128 switch chip has a large number of “strapping” pins (33) to provide basic
 3924 control its various functions. The use of these strapping pins is complicated because there are
 3925 interactions between them and because the documentation seem incomplete and different
 3926 sections of the documentation frequently call the same object by different names and
 3927 frequently use slang names, e.g. green means don’t use the 8051.

3928 On the Hub Module, to the extent that space limitations allow, the approach taken (same as
 3929 HP used) is to provide a 0603 jumper site for each strapping pin that is tied to the opposite
 3930 rail than the default internal pull up/down resistor for that pin. This gives us a way to make
 3931 post production changes if necessary.

3932 The 0603 site has not been provided for some strapping pins where their functions were clear
 3933 and where we wanted the default provided by the internal pull up/down resistor. In these
 3934 cases trace routing is such that access can be made to the signal if necessary.

3935 The 33 strapping pins and their internal pull up/down resistors and their external 0603 jumper
 3936 sites are shown in **Figure 62**.

3937 **30.1 Enumeration of All Strapping Options on the BCM53128**

3938

Signal Name	Pin #	Int’l Default	BCM Docs Say	Kit	HP	Hub
CLK_FREQ1/GPIO1	15	PD	Must Float in all designs DG pg 39	DNI PU	Float	---
CLK_FREQ0/GPIO0	14	PU		DNI PD	Float	---
EN_CLK25_OUT/CLK_25_OUT	26	PD	Low --> Disable	Float	Float	---
EN_CLK50_OUT/CLK_50_OUT	21	PD		Float	Float	---
EN_EEE	38	PU	Hi->Enable	Float	Float	YID
EN_8051_TxRx	47	PD	Hi->Enable	Float	Float	---
IMP_MODE(1)/GPIO6	8	PU	Sets IMP Mode	Float	Float	---
IMP_MODE(0)/GPIO5	7	PD		Float	Float	---
IMP_VOL_SEL(1)	48	PD	Both Low --> 3V3	Float	Float	---
IMP_VOL_SEL(0)	49	PD		Float	Float	---
IMP_SPD_SEL(1)	50	PU	Default for normal operation	Float	Float	---
IMP_SPD_SEL(0)	51	PD		Float	Float	---
IMP_DUPLEX	52	PU	Hi->Duplex	Float	Float	---
IMP_LINK	54	PD	Hi->LinkUp	Float	Float	---
IMP_PAUSE_CAP_RX	55	PU	Hi->EnbPause	Float	Float	---
IMP_PAUSE_CAP_TX	56	PU	Hi->EnbPause	Float	Float	---
HW_FWDG_EN/GPIO7	9	PD	HI to Enb Frame Fwd	has PU	has PU	YIU

LED_MODE(1)/GPIO4	13	PD	Set LED Mode	DNI PD	has PD	YBU
LED_MODE(0)/GPIO3	12	PU		DNI PU	Float	YBD
CPU_EEPROM_SEL	18	PU	Low to Enb EEPROM	has PD	has PD	YID
TRST	36	PU	Pull Low for normal operation	DNI PD	has PD	YID
LED3/EN_GREEN	172	PD	Hi->Enable Green Mode DS Pg 133 DG pg 56	has PU	Float	YBU
LEDP11/EPROM_TYPE1	182	PD	10b is PROM type 93C66	has PU	has PU	YIU
LEDP10/EPROM_TYPE0	181	PD		Float	Float	---
LEDP14/LOOP_DETECT_EN	186	PD	Hi->Enable	has PU	Float	YBU
LEDP15/LOOP_IMP_SEL	188	PD	Hi->Include	Float	Float	---
LEDP18/BC_SUPP_EN	191	PD	Hi->Enable Rate Brdcast Supp	Float	Float	---
LEDP22/DIS_IMP	196	PD	Hi->Disable	has PU	has PU	YIU
LEDP23/IMP_DUMB_FWDG_EN	197	PD	Hi->Allow Dumb Forward	Float	Float	---
LEDP26/ENFDXFLOW	254	PU	Hi->Not Clear from DS or DG	Float	Float	---
LEDP27/ENHDXFLOW	255	PU	Hi->Enable	Float	Float	---
LEDP30/IMP_TXC_DELAY	2	PU	Hi->Enable	Float	Float	---
LEDP31/IMP_RXC_DELAY	4	PU	Hi->Enable	Float	Float	---

3939

3940

3941

3942 Hub Notation Key:

- 3943 • YIU -> Yes Hub has an Installed jumper and it's a Pull-Up
- 3944 • YID -> Yes Hub has an Installed jumper and it's a Pull-Dowm
- 3945 • YBU -> Yes Hub has a Not-Installed jumper and it's a Pull-Up
- 3946 • YBD -> Yes Hub has a Not-Installed jumper and it's a Pull-Dowm
- 3947 • --- -> For these, the Hub does not have a jumper for this function

3948 **31 Appendix 18: Hub-Module Xilinx FPGA**

3949 The UltraScale Virtex device on the Hub Module is a: XCVU125-1FLVC2104I

3950 This is speed grade “1”, i.e. the normal common slowest speed grade and it is the “Industrial”
3951 temperature range which is the common temp range for most of these UltraScale parts.

3952 This part has: 40 GTH Transceivers and 40 GTY Transceivers. These are spread across 2
3953 SLRs with 20 of each kind of transceiver in each SLR.

3954 This part has 7 HP Select I/O Banks with 52 I/O signals in each. 4 of the HP banks are in
3955 SLR #0 and 3 of the HP banks are in SLR #1.

3956 This part also has 2 HR Select I/O Banks with 26 I/O signals in each. Both of the HR banks
3957 are in SLR #0. The Hub Module uses both of the HR Banks for 3V3 I/O and it uses most of
3958 the signals in these Banks.

3959 The FLVC2104 package has 2104 pins in a 1mm by 1mm square array with 46 pins on each
3960 side and 3 pins missing at each corner. This is a No-Lead package.

3961 **31.1 FPGA Configuration:**

3962 The Hub’s UltraScale Virtex FPGA is configured in Master BPI mode from a Micron
3963 MT28GU01GAAA1EGC-OSIT NOR Flash memory. This method of configuration requires
3964 pins in both the special Bank #0 and most of the pins in Select I/O Bank #65.

3965 **Figure 63** shows the details of this configuration setup.

3966 The MT28GU01GAAA1EGC-OSIT Flash memory holds 1 Gb of data. The XCVU125
3967 FPGA requires 401,441,280 bits to configure so the Hub Module can hold 2 versions of
3968 FPGA Firmware.

3969 **31.2 FPGA JTAG Connection**

3970 The Hub Module provides a front panel JTAG connection via its J2 “Access Connector”. A
3971 1V8 version of this JTAG string is routed to the Hub’s FPGA as shown in **Figure 37**.

3972 **31.3 FPGA System Monitor Reference and Connections**

3973 The hub provides an external precision reference and filtered power for the FPGA System
3974 Monitor. This is shown in **Figure 64**. The IPMC’s Sensor I2C bus is routed to the slave I2C
3975 port to the System Monitor as shown in **Figure 36**.

3976 **31.4 FPGA MGT Transceivers**

3977 The Hub design uses all 80 MGT Receivers and 29 of the MGT Transmitters. Note that this
3978 FPGA’s MGT transceivers are shared across both of its SLRs.

3979 The assignment of the MGT transceivers is listed in Section 18. The connections to the GTY
3980 and GTH Banks are shown in **Figure 29** and **Figure 30**.

3981 **31.5 FPGA RGMII Ethernet Base Interface Connection**

3982 The Hub Module FPGA is connected to 2 Micrel KSZ9031RNX Phys chips. These Phys
3983 chips provide 10/100/1000 speed ethernet connection between the FPGA and the Switch on
3984 This Hub and via the backplane to the Switch on the Other Hub.

3985 The Phys RGMII to FPGA connections are made to HP Bank #68.

3986 Besides the MACs to run these connections the FPGA firmware may want MACs to run the
3987 MDC MDIO management links to the 3 Switch chips.

3988 **31.6 FPGA Clock Sources**

3989 The Hub's FPGA is provided with the following clocks:

- 3990 • 25.000 MHz Ethernet Clock single ended 3V3 to Bank 94
- 3991 • 40.08 MHz LHC Clock LVDS Logic Clock to Bank 71
- 3992 • 320.64 MHz LHC Clock Cap Coupled LVPECL Logic Clk to Bank 71
- 3993 • 8x 320.64 MHz LHC Clock Cap Coupled LVPECL MGT Reference Clk
- 3994 • 2x 125.000 MHz Ethernet Clock single ended 1V8 level
- 3995 • Each Phys Chip returns its 5x multiplied Clk to Bank 68 in the FPGA

3996 **31.7 The Select I/O Signals**

3997 The Hub design currently uses about 166 Select I/O signals. Both 1V8 and 3V3 levels are
3998 used. The 3V3 levels are from HR Select I/O Banks 84 and 94.

3999 The Hub's use of FPGA Select I/O signals is listed in Sections 19 and 20.1.

4000 **31.8 FPGA Power Supply Requirements**

4001 The intent here is to list the full details of this FPGA's power supply and bypass capacitor
4002 requirements. Then in the Hub Power Supply Design document only a short summary of
4003 these FPGA's power requirements will be presented along with a summary of the power
4004 supply requirements of the other components on the Hub Module.

4005 *UltraScale XCVU125-FLVC2104 Recommended Operating Conditions:*

- 4006 • VCCINT 0.950 V +/- 3.0%
 - 4007 • VCCINT_IO 0.950 V +/- 3.0%
 - 4008 • VCCBRAM 0.950 V +/- 3.0%
 - 4009 • VCCAUX 1.800 V +/- 3.0%
-

- 4010 • VCCAUX_IO 1.800 V +- 3.0%
- 4011 • VCCO HR 1.140 V to 3.400 V
- 4012 • VCCO HP 0.950 V to 1.890 V
- 4013 • VBATT
- 4014 ○ MGTAVCC 1.000 V +- 3.0%
- 4015 ○ MGTAVTT 1.200 V +- 2.5%
- 4016 ○ MGTVCCAUX 1.800 V +- 2.8%
- 4017

4018 VCCINT_IO must be connected to VCCINT

4019 VCCAUX_IO must be connected to VCCAUX

4020 If VBATT is not used then connect VBATT to either ground or to VCCAU, then
4021 VCCO_0 must be a minimum of 1.425V during configuration.

4022 *Quiescent Supply Currents:*

- 4023 • VCCINT 2875 mA
- 4024 • VCCINT_IO 178 mA
- 4025 • VCCBRAM 162 mA
- 4026 • VCCAUX 373 mA
- 4027 • VCCAUX_IO 148 mA
- 4028 • VCCO 1 mA (assume per Bank)

4029 *Power Supply Sequencing and Common Supplies:*

4030 At Power ON:

4031 VCCINT / VCCINT_IO then VCCBRAM then

4032 VCCAUX / VCCAUX_IO then VCCO

4033 Power OFF is the reverse.

4034 VCCINT / VCCINT_IO and VCCBRAM can all be powered from the same supply and
4035 ramped simultaneously.

4036 VCCAUX / VCCAUX_IO and VCCO can all be powered from the same supply and
4037 ramped simultaneously.

4038 VCCINT and MGTAVCC may be ramped simultaneously.

4039 MGTAVCC should ramp before MGTAVTT.

4040 No recommended sequencing for MGTVCCAUX.

4041 Besides the Quiescent currents listed above the supplies must be able to provide the
4042 following minimum currents during power up:

- 4043 • VCCINT / VCCINT_IO supply 4397 mA minimum additional current
- 4044 • VCCBRAM 200 mA
- 4045 • VCCAUX / VCCAUX_io supply 533 mA
- 4046 • VCCO supply 54 mA
- 4047

4048 *All ramp times are 200 usec minimum and 40 msec max.*

4049 3.0 msec is about in the middle 16x from either side.

Hub FPGA - Banks 0 & 65 - Configuration

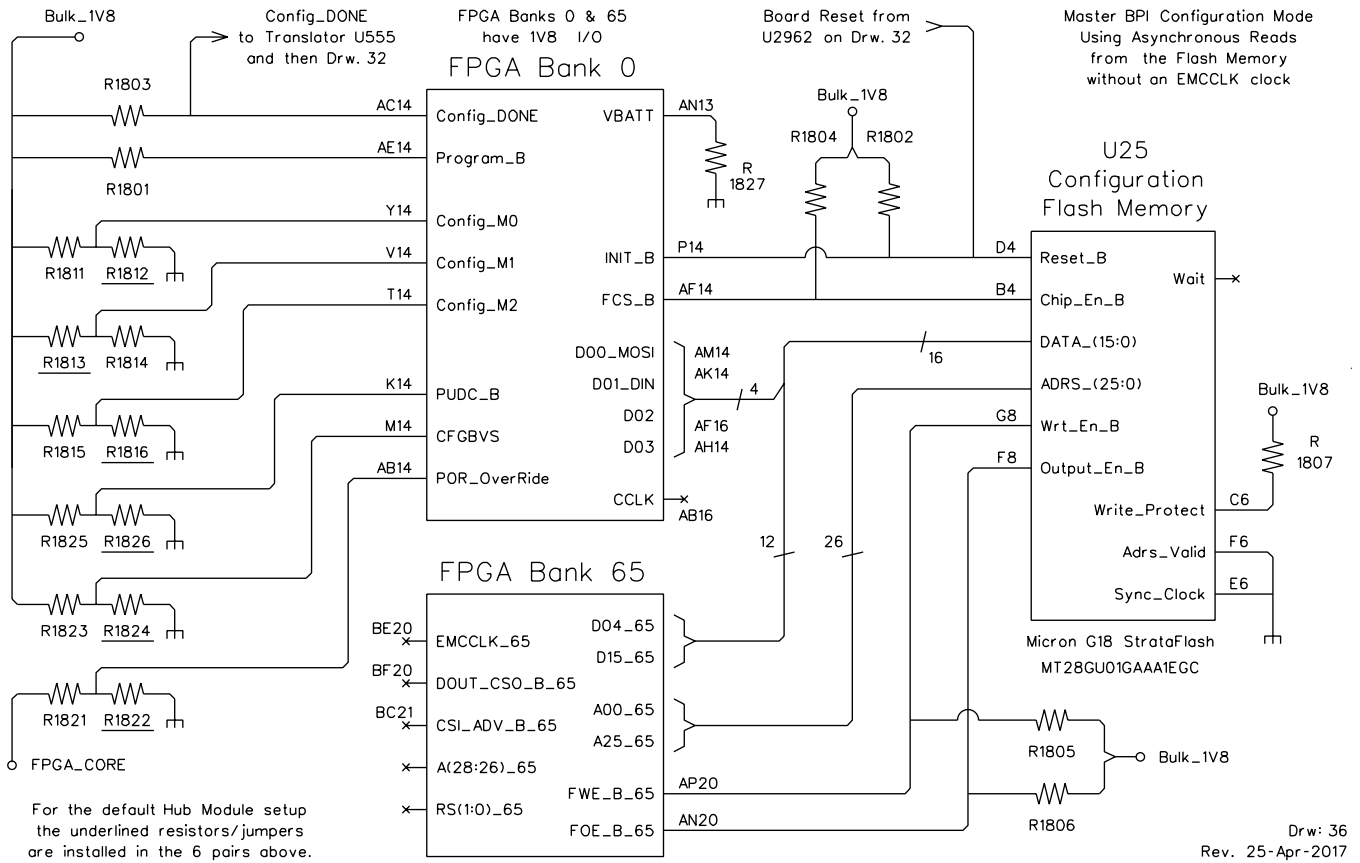


Figure 63: Hub FPGA configuration, banks 0 & 65.

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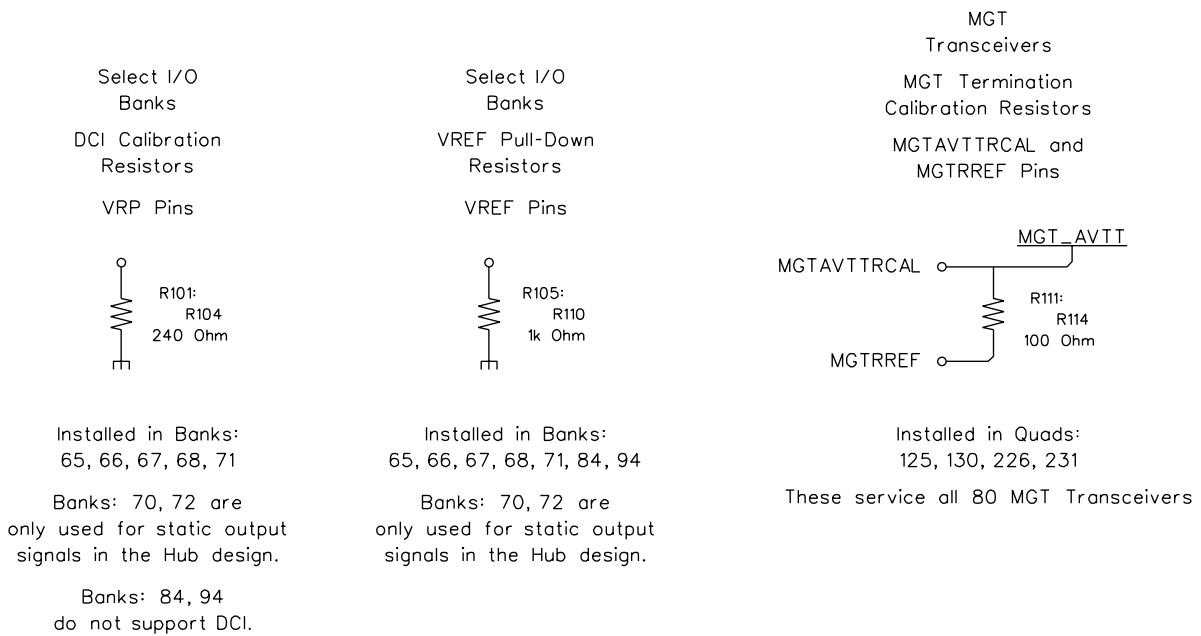
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Hub FPGA DCI, VREF, MGT Calibration Resistors



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Figure 64: Hub FPGA calibration resistors.

4081 **32 Appendix 19: Hub Commissioning Test Plan**4082 External inputs:

- 4083 • Requirements from ROD, FEX and FELIX interfaces are assumed to be defined by
4084 the prior review outcomes and module specifications.
- 4085 • An engineering definition should be provided for the maximum changes in LHC input
4086 reference clock (eg, “We must be able to track a slew rate of 220 Hz/sec while our
4087 recovered clock does not shift in phase by more than 30 degrees from its normal
4088 position with respect to a static center frequency reference input.”)
4089

4090 Definitions:

- 4091 • “This Hub” / “Other Hub”
- 4092 ○ Hub modules do not have a physical difference of whether they are in logical
4093 slot 1 or logical slot 2. The only difference is that the Hub in slot 1 transmits
4094 the master clock to the FEX, ROD and slot-2 Hub modules.
- 4095 ○ Thus, each Hub can view the world from its own internal reference point and
4096 must be able to achieve satisfactory operation from both logical slots.
- 4097 ○ “This Hub” corresponds to a Hub module in a reference slot (eg, Slot 1)
- 4098 ○ “Other Hub” thus corresponds to the Hub in the implied alternate slot relative
4099 to “This Hub” (eg, Slot 2 relative to Slot 1 and vice versa)
- 4100 • Combined Data
- 4101 ○ The Hub module receives TTC information from FELIX and extracts the
4102 clock and configuration data. It then combines local control signals from the
4103 ROD(s) present and distributions this Combined Data to all modules in the
4104 ATCA shelf.
- 4105 • GbE = Gigabit Ethernet

4106 **32.1 Power Supplies and Hub Component Cooling Tests**

- 4107 1. During MSU Final Assembly and Bench Testing
- 4108 a. Verify (measure) 11 power supply output voltages and 7 power supply output
4109 currents while the FPGA is configured with test firmware.
- 4110 b. The 7 DCDC Converters on each Hub are tested and setup for: Vin_On,
4111 Vin_Off, Vout_Margin_High, Vout_Margin_Low, and Vout_Scale_Loop.
- 4112 2. Verify that the I2C PMBus monitoring of the 7 DCDC Converter output voltages and
4113 currents is working OK by reading them from the Front Panel I2C Bus connector. The
4114 intent is to verify that the IPMC has access to this data.
- 4115 3. Verify that the FPGA's System Monitor reads out correct data for the Si Temperature,
4116 1V8 Aux power, and 0V95 Core power.
- 4117 4. Verify the sequencing and ramp rate for at least two of the power supply voltages, e.g.
4118 DC/DC-1 FPGA_Core, DC/DC-5 SWCH_1V2, and DC/DC-8 Bulk_3V3.
- 4119 5. Verify that the board power enable circuit, the board start-up reset circuit and the two
4120 front panel board power status LEDs are all working correctly.
- 4121 6. Verify the expected Hub FPGA Si Temperature with the Hub running in the Shelf
4122 with standard air flow rate and the highest wattage FPGA firmware that we have
4123 available (currently about 32 Watts).

- 4124 7. Verify that the expected operating temperature is readout from the two MiniPODs via
4125 their control/monitoring serial bus connection to the Hub FPGA.

4126 **32.2 IPMC and Slow Control & Monitoring Bus Tests**

- 4127 1. Verify that the IPMC can negotiate via the IPMB Buses with the Shelf Manager and
4128 turn On or Off the Hub card appropriately.
- 4129 2. Verify that the IPMC can detect the front panel handle switch position and correctly
4130 follow the protocol to turn the Hob module power On and Off.
- 4131 3. Verify that the IPMC can correctly read the Slot Address from the backplane pins for
4132 both Hub Slots.
- 4133 4. Verify that the IPMC can correctly get the Crate Address from the Shelf Manager and
4134 make this address data available on the IPMC's general purpose I/O pins.
- 4135 5. Verify that the IPMC can correctly gather the Hub's voltage, current, and temperature
4136 Monitoring Data by initiating the required cycles on the Sensor I2C Bus and that it
4137 can forward this Monitoring Data to the Shelf Manager where it is made available to
4138 the DCS system.
- 4139 6. Verify that by one of its general purpose I/O pins the IPMC can be told to suspend its
4140 Reads of Monitoring Data over the Sensor I2C Bus and then later to resume its
4141 normal reads of the Hub Monitoring Data.
- 4142 7. Verify that the IPMC can correctly read FRU and SDR data from the PROM on the
4143 Hub card via the Management I2C bus so that a generic Hub type L1Calo IPMC can
4144 be used on any Hub card.
- 4145 8. Verify that the IPMC can correctly read the Monitoring Data from the Hub's ATCA
4146 Power Entry Module via the Management I2C Bus.
- 4147 9. Verify that the three I2C buffers in the overall Sensor I2C Bus are working and be
4148 enabled or disabled via their control lines that run to the Hub's FPGA.
- 4149 10. Verify that the Front Panel JTAG connector has access to the Hub's FPGA and that
4150 when the ROD is installed and powered up that the ROD's FPGA also appears in this
4151 JTAG string.
- 4152 11. Verify that the two MiniPOD serial control & monitoring I/O buses are working and
4153 communicating with the Hub's FPGA.

4154 **32.3 MGT Link Tests**

- 4155 1. Verify that the 13 Equalization Group Enable Signals are all working OK and routed
4156 to the correct sets of MGT Fanout Chips.
- 4157 2. Verify that the 4 MiniPOD Receiver MGT channels and the 8 MiniPOD Transmitter
4158 MGT channels are all working OK.
- 4159 3. Verify that the Hub FPGA can receive 6 lanes of MGT data from all 12 of the FEX
4160 slots.
- 4161 4. Verify that the Hub can receiver 6 lanes of MGT data from all 12 of the FEX slots and
4162 correctly pass this data to the ROD.
- 4163 5. Verify that the Hub FPGA can send out Combined Data to the 12 FEX slots, to the
4164 ROD on This Hub, and to the Other Hub.
- 4165 6. Verify that This Hub can Receive Combined Data that was sent out by the Other Hub.
- 4166 7. Verify that This Hub can Receive the Readout Control data that was sent out by the
4167 ROD on This Hub.
- 4168 8. Verify that This Hub can send out two lanes of Readout data to the Other Hub.
- 4169 9. Verify that This Hub can Receive two lanes of Readout data from the Other Hub.
-

- 4170 10. Verify that This Hub can Receive and correctly pass to its ROD one lane of readout
4171 data from the Other Hub.
4172 11. Verify that the FPGA on This Hub can send one lane of its readout data to the ROD
4173 on This Hub.

4174 **32.4 Clock Tests**

- 4175 1. Verify that the 25.0 MHz and 40.0787 MHz oscillators are running at the correct
4176 frequency and are stable.
4177 2. Verify the 40.0787 and 320.6296 MHz PLLs have the correct LHC frequency
4178 tracking range.
4179 3. Verify both sides of the First 40 MHz Fanout to the: Hub FPGA, ROD, 320 MHz
4180 PLL, and Second 40 MHz Fanout.
4181 4. Verify both sides of the 13 outputs from the Second 40 MHz Fanout: 12 to the FEXs
4182 and 1 to Other Hub.
4183 5. Verify both sides of the outputs from the 320 MHz Fanout: 8 connections to MGT
4184 Reference Inputs and 1 Logic Clock to the Hub FPGA.
4185 6. Verify that when operated as the Other Hub (i.e. the Hub that does not directly receive
4186 an optical TTC signal from FELIX), that the Hub card can correctly receive its LHC
4187 Reference Clock from the backplane.

4188 **32.5 Ethernet Connection and Ethernet Switch Tests**

- 4189 1. Verify that both GbE links to the Hub's FPGA are working correctly (link to the GbE
4190 Switch on This Hub and link via the backplane Base Interface to the GbE Switch on
4191 the Other Hub).
4192 2. Verify that all 22 GbE Switch Ports that are used on the Hub card carry GbE traffic
4193 OK.
4194 3. Verify that the Hub's Front Panel GbE connection and GbE Magnetics for the ROD
4195 are all working OK.
4196 4. Verify that the Hub's Front Panel GbE connection and GbE Magnetics for the IPMC
4197 are all working OK.
4198 5. Verify that the current GbE Switch PROM content is OK and Final and start installing
4199 GbE Switch PROMs with this content on all Hub Modules.
4200 6. Characterize the performance of the GbE Switch, i.e. test in isolation the data flow
4201 rate to each of the Switch's 18 external ports and test the switch when all 18 of its
4202 external ports are trying to flow data at the same time.

4203 **32.6 Miscellaneous Tests**

- 4204 1. Verify that all 66 Front Panel LEDs are working and are of the correct color.
4205 2. Verify the Physical aspects of this Hub card:
4206 a. Dimensions look correct (e.g. none of the brackets are in backwards).
4207 b. The board's corners are in good shape.
4208 c. The Insertion and Extraction forces feel correct and are smooth.
4209 d. The Front Panel Labels are clear and not scratched.
4210 e. All of the backplane connectors line up in a straight row and are fully inserted.
4211 f. Nothing is loose or likely to vibrate in the air flow (e.g. the discrete power
4212 wires or fiber optic ribbons, or power supply LC filter comps).
4213 g. MiniPOD and FPGA heat sinks are correctly installed.
-

- 4214 h. The MiniPODs are fully seated and screwed down.
- 4215 i. The MiniPOD Fiber Optic Ribbon Cables are correctly routed and not
- 4216 blocking air flow.
- 4217 3. Verify that all 9 ESD ground points are correctly connected so that the card is safe to
- 4218 handle.
- 4219 4. Verify that the card auto-configures its FPGA from its Flash memory at power up.
- 4220 5. Verify that the ROD can control the open collector output signals from the Hub's
- 4221 Front Panel LEMO Connector.
- 4222 6. Verify the correct operation of the 4 Power Control signals and the 8 Spare TBD
- 4223 signals between the Hub and ROD cards.
- 4224 7. Verify the correct fuses are installed.
- 4225 8. Verify that both Front Panel FPGA output Access Signals are working OK.