FEX System
ATCA Hub Module:
FDR Follow-up

Hub Team
Michigan State University

10 December 2018

Overview & Goals

❖ Hub Production Plan:

- Hub production run will be 20 cards, no pre-production run is planned.
- Goal: Delivery to CERN by June 2019. More on this in the next presentation(s).

❖ Hub PRR Goals:

- Action items identified during FDR will be reviewed.
- Additional tests beyond those identified at FDR will be presented for review.
- Firmware aspects directly impacting hardware function, performance and capability will be presented for review.
- If no hardware issues are identified during the PRR, production PCBs will be scheduled for manufacture.
- If any hardware-sensitive firmware issues are identified during the PRR, a post-PRR review will be scheduled.
- If/when the PRR and any follow-ups are passed, Hub production modules will be assembled.

❖ Today's Presentation Material:

- This talk: Introduction and follow-up of FDR action items
- Next talk: Review of "beyond FDR" Hub test results & firmware implementation
- Last talk: Hub production schedule and scope

Outline of this Presentation

- Introductory & background material
  - Very brief review & status
- Description of Hub test apparatus
  - Primary source of test data for this review
- Follow-up responses to Final Design Review action items
  - Clock generation and distribution
  - Firmware items
  - Remaining hardware items

Hub Team

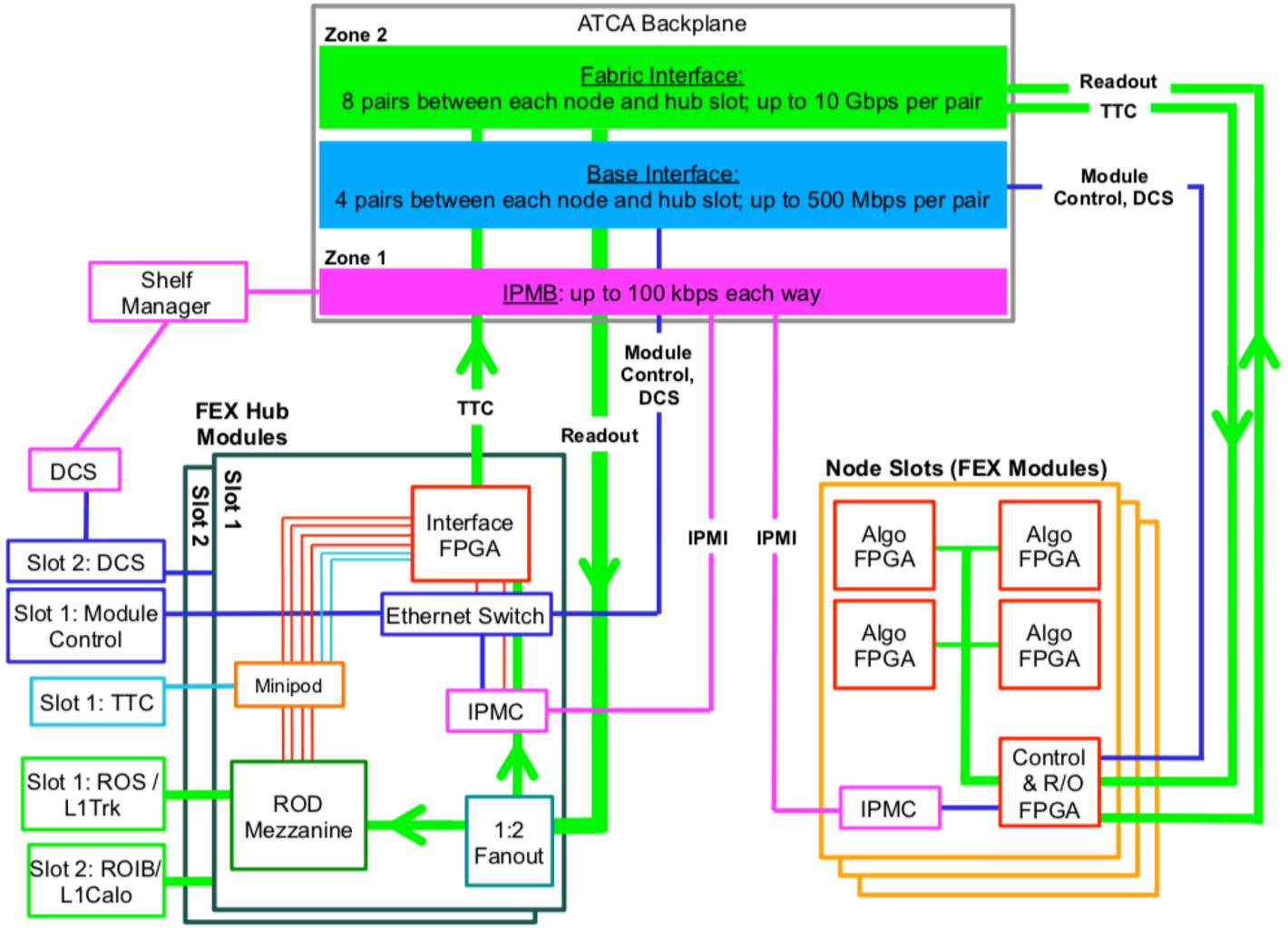
- Many years of experience on the MSU team
  - Dan Edmunds, EE
  - Yuri Ermoline, EE
  - Brian Ferguson, EE
  - Philippe Laurens, EE
  - Pawel Plucinski, PhD

  - Spencer Lee, student
  - Kuan Yu Lin, student
  - Gabriel Moreau, student

  - Wade Fisher, faculty

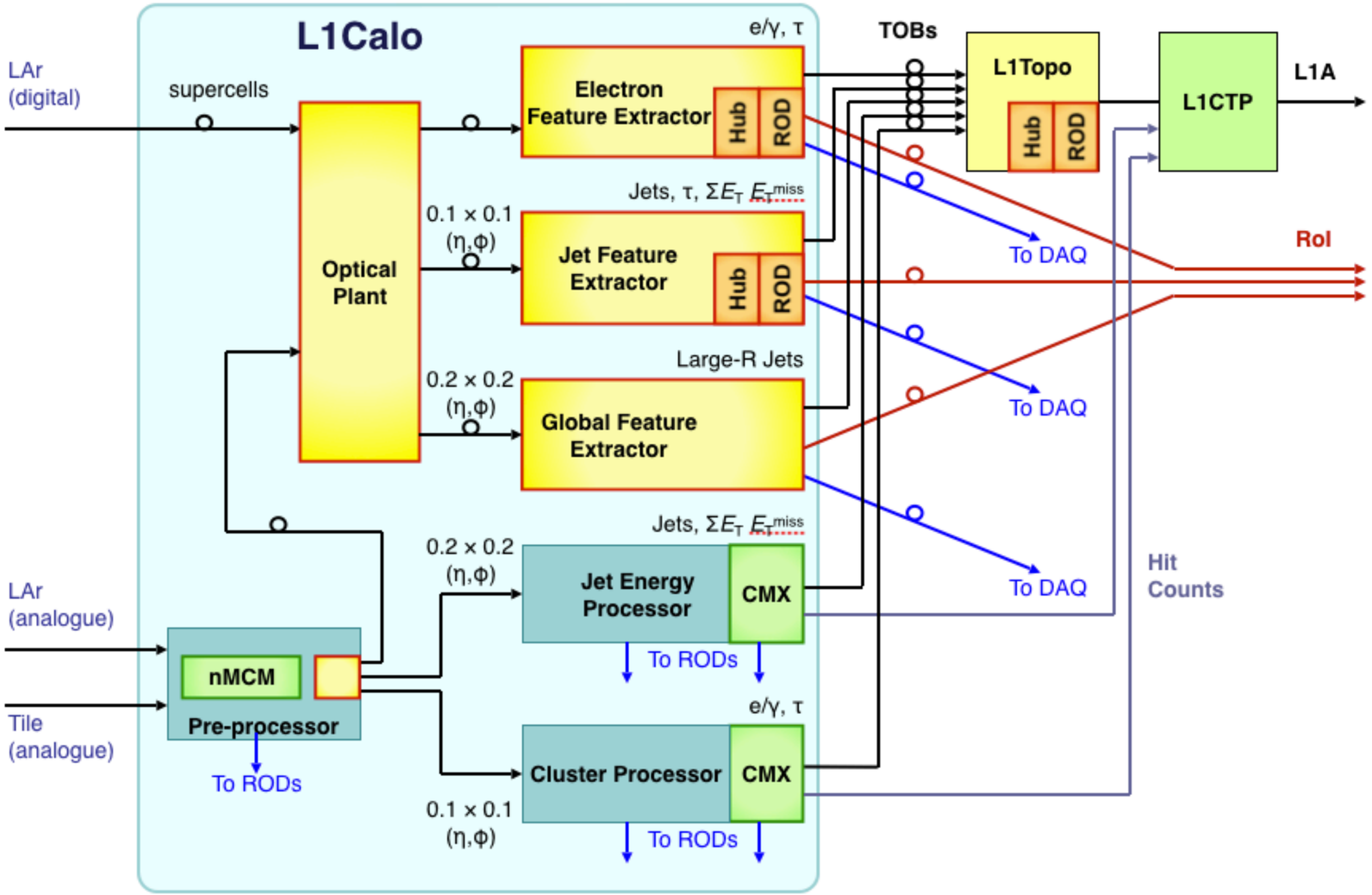
Introduction

- FEX ATCA Hub module provides a readout interface for L1Calo trigger electronics



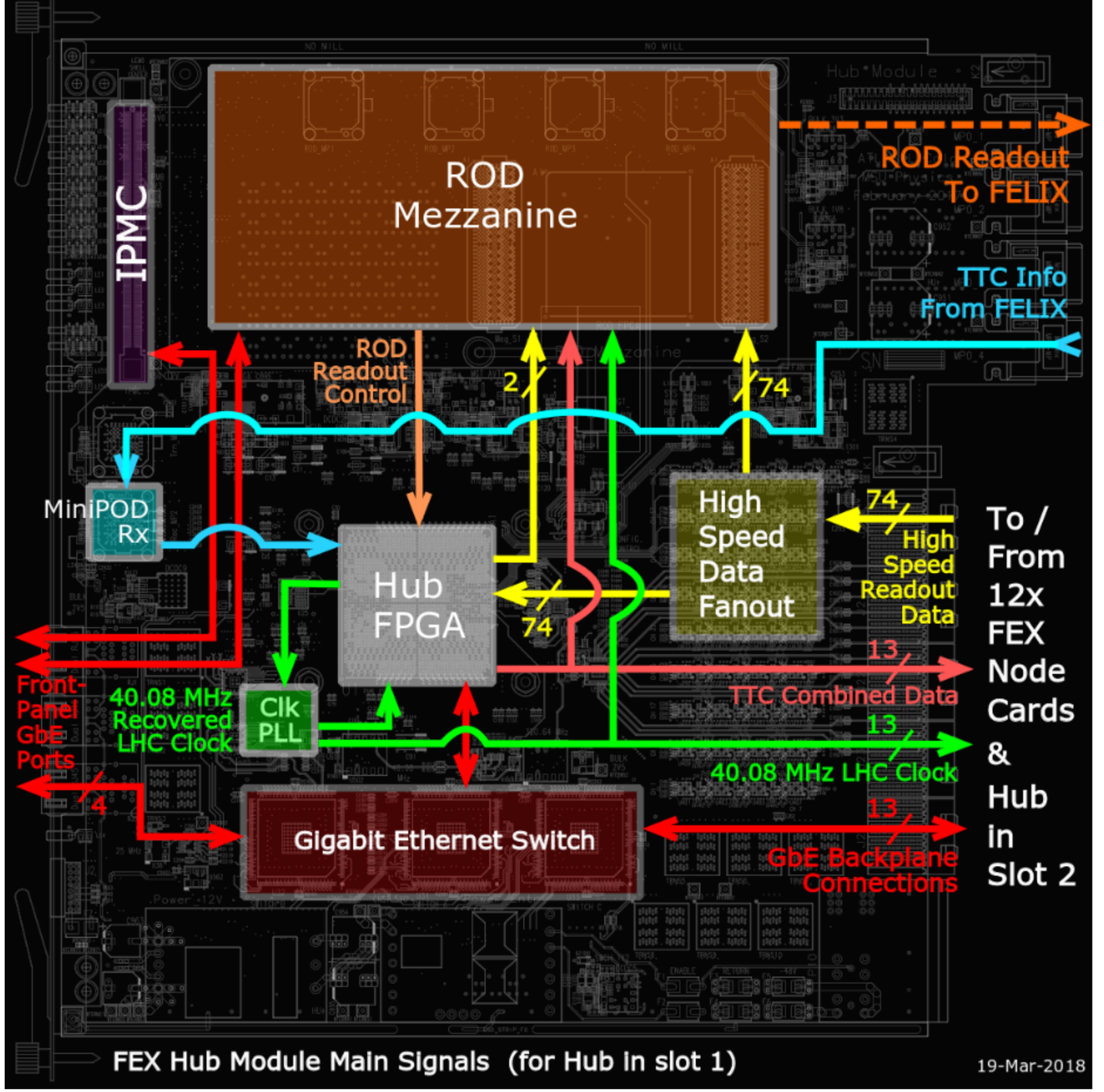
External Interfaces

1. eFEX Modules, 2 shelves
2. jFEX Modules, 1 shelf
3. L1Topo Modules, 1 shelf
4. ROD Mezzanine, 1 per Hub
5. DAQ/HLT [FELIX]
   a) TTC
   b) ROD-busy LEMO
6. Ethernet
   a) DCS
   b) Run control
7. IPMC
8. Board-level
   a) JTAG/I2C



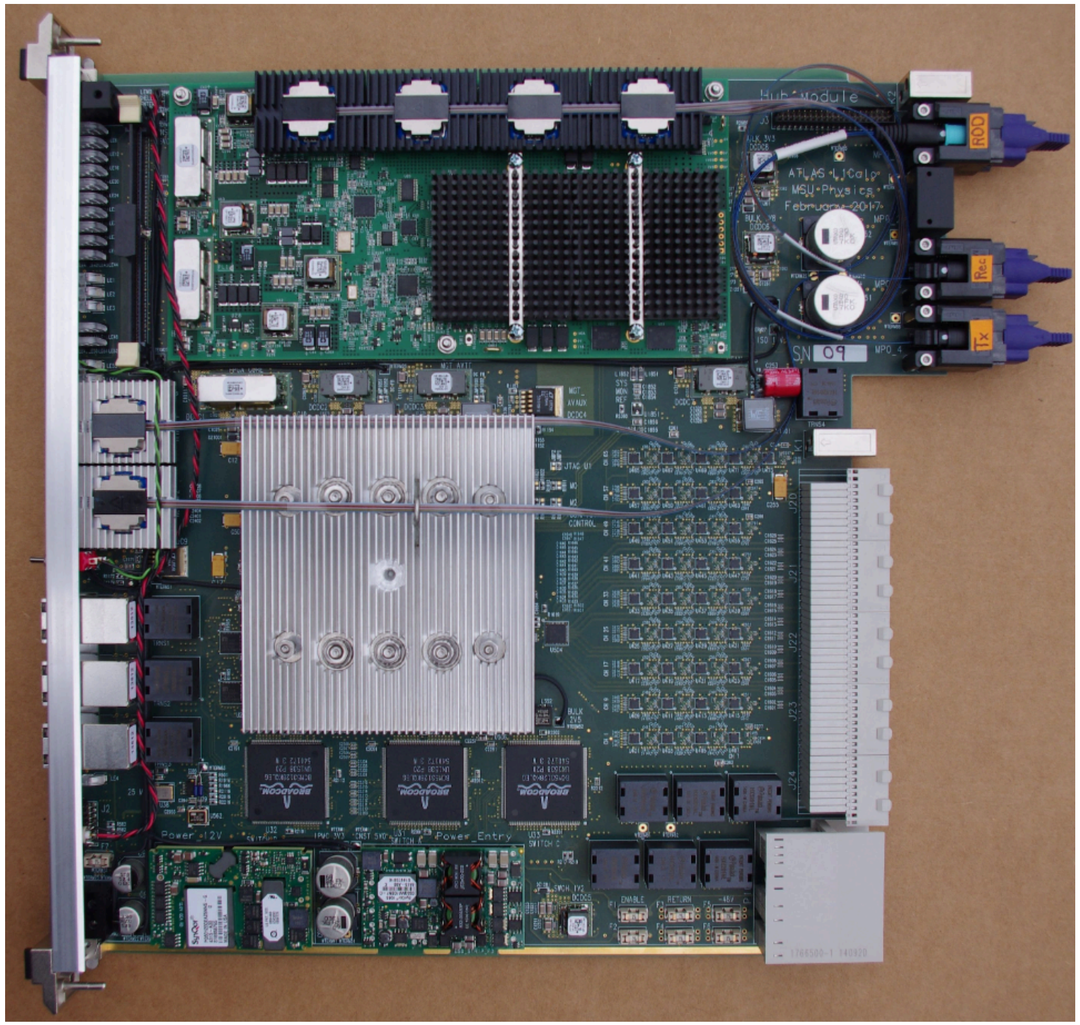
Board Layout

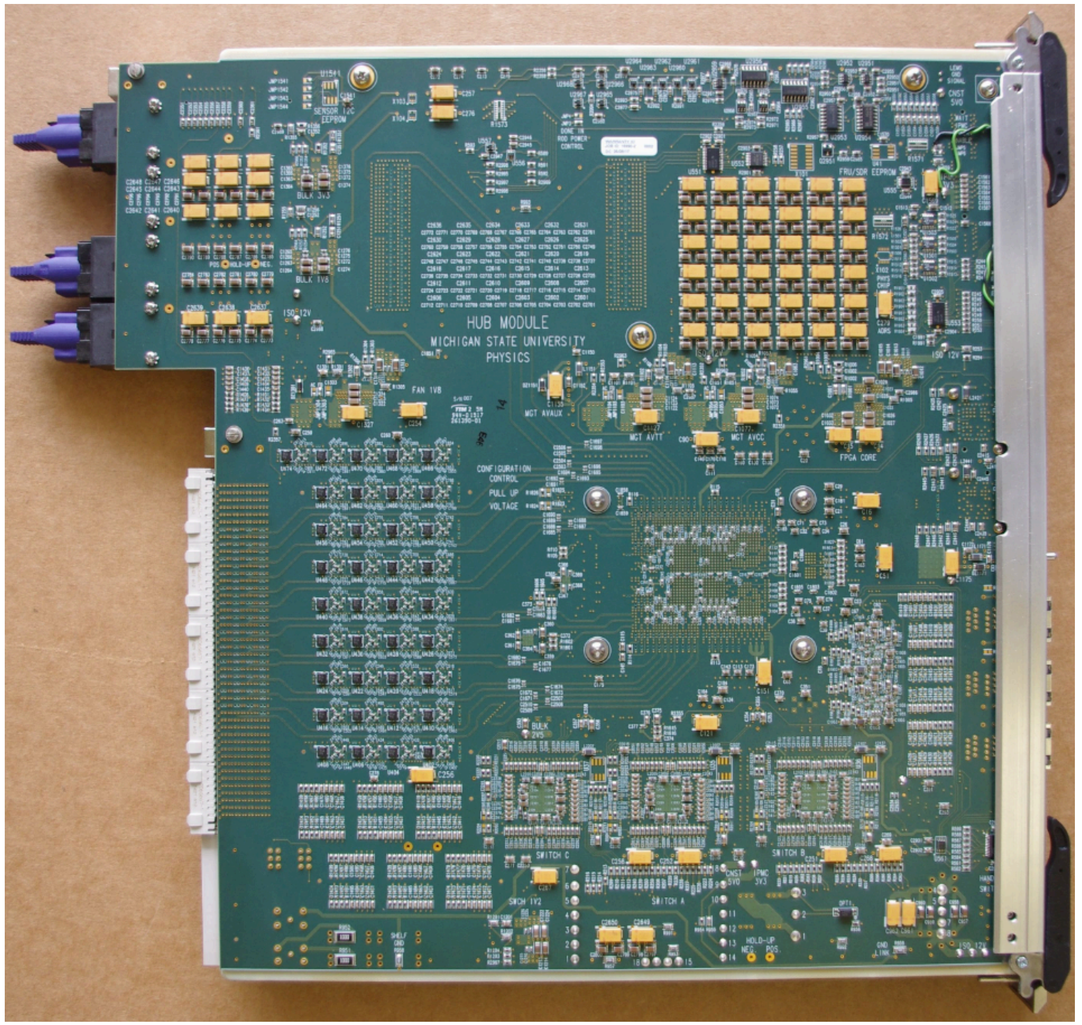
- Core functions of the Hub hardware
  1) Host the ROD Mezzanine
  2) Aggregate Zone-2 FEX readout data and provide to the ROD
  3) Distribute LHC master clock to FEX, Hub and ROD modules
  4) Distribute TTC and ROD control data to FEX, Hub and ROD modules
  5) Provide Ethernet switch for the ATCA shelf via the Base Interface



Prototype Hub Modules

- 9 Hub prototypes were build (8 with FPGAs)
  - Here: Hub S/N 09 with ROD and optical cabling included to illustrate final installation assembly.





Hub Firmware

- There are four core firmware requirements for the Hub module
  1) ROD power-up and control data interfaces
  2) TTC/GBT clock recovery and distribution
  3) TTC/Combined data distribution
  4) IPbus interfaces for ROD & Hub functionality

- These functions will be described both here and in the Hub firmware specification
  - Details pertinent to the Hub FDR will be in this presentation
  - Details related to Hub production readiness in the second presentation
    - Allowing to focus on specifics of the FDR action items in this presentation

Review Documentation

- Hub hardware details
  - Specification: Very minor language changes relative to what was presented at the FDR
    - No relevant changes to the Hub PCB or other hardware aspects.
    - *We did swap out our green indicator LEDs for LEDs with lower light intensity, allowing for better reading of dense switch status LED patterns.*
  - PCB Stackup: No changes WRT what was shown at the FDR
  - PLL Chip data sheet: No changes WRT what was shown at the FDR

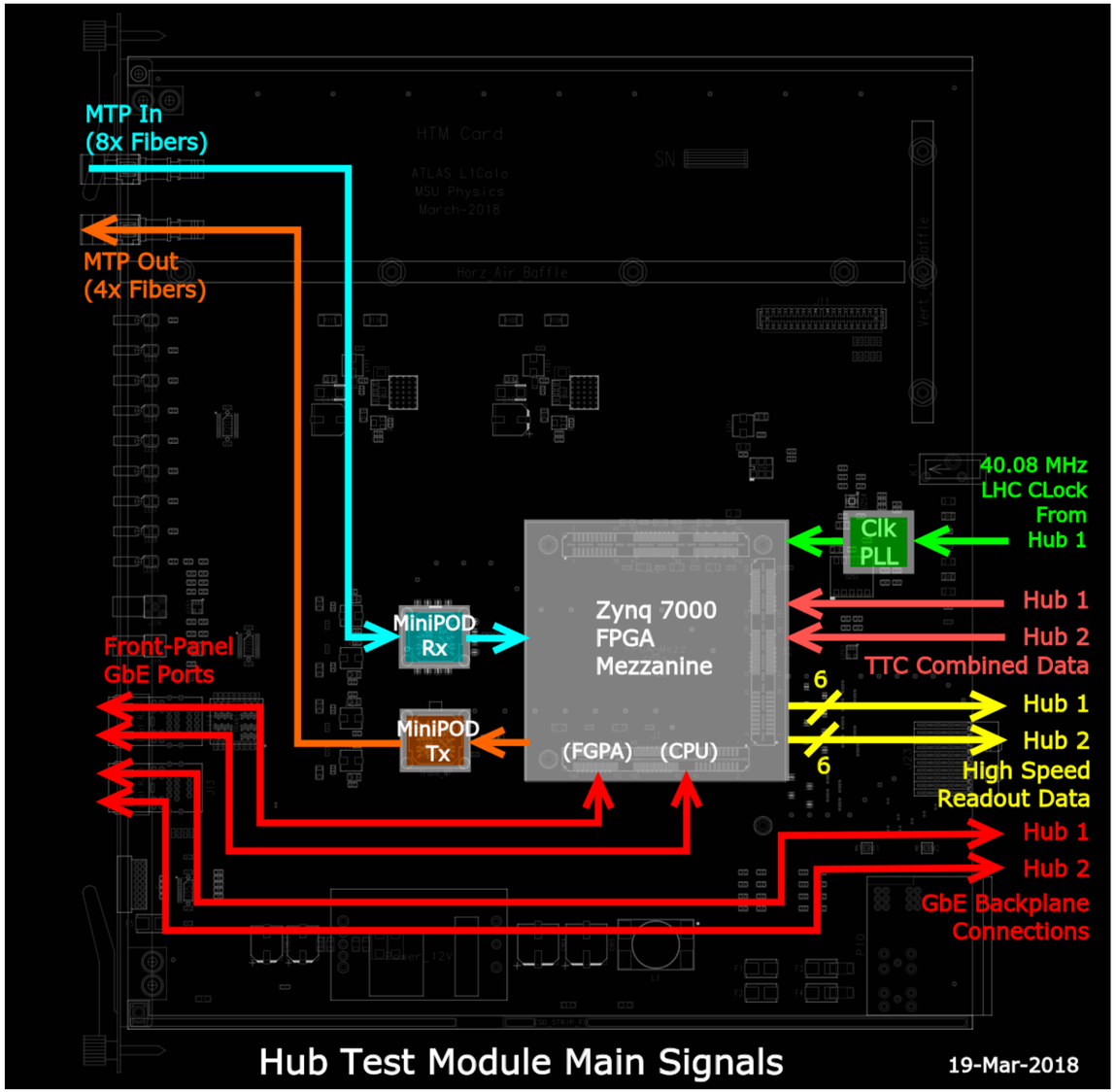
- Hub firmware specification
  - Significant overhaul since FDR
    - New descriptions of core Hub firmware
  - Details of firmware implementation
    - Focus on external interfaces, includes internal details

- Hub GbE test reports
  - Full details of Hub GbE switch tests

- Links to MSU L1Calo webpages
  - All the details of the build, test results, etc
  - https://web.pa.msu.edu/hep/atlas/l1calo/
    - Links for Hub and HTM can be found there

Hub Test Apparatus

Hub Test Module



- Hub Test Module (HTM) designed to allow full system tests far in advance of a full shelf of FEX/FTM cards
  - Developed at MSU. 20 cards delivered July 2018.
- HTM design specifics
  - ATCA form factor, 10 layer board
  - Hosts a commercial mezzanine card with a 7-series Zynq
  - Receives Hub TTC & clock via Zone-2
  - Sources 6 lanes of “FEX” data to each Hub slot, up to 10.26 Gbps
  - Optional MiniPods to emulate all Hub/ROD optical interfaces
  - Connections to both Hub GbE networks

TTM Technologies

Viasystems Technologies Corp. LLC
8150 Sheppard Ave E
Toronto, ON, M1B 5K2

Job Name : 181875
Customer : DEBRON INDUSTRIAL ELECTRONICS
Part Num : 40-00643-00LF
Part Rev : -
Engineer : Yogi Perin

Layer	Cust Thickness	Calc Thickness	Primary Stack	Description	Dk / Df
		0.0005		Taiyo 4000-HFX DI	3.50 / 0.0190
Layer - 1		0.0020		1/2oz Mix (Std Plt)	
		0.0038	1080 - 71%	FR408HR	3.42 / 0.0098
Layer - 2		0.0006		1/2oz P/G	
		0.0100	0.0100 (2-2116)	FR408HR	3.69 / 0.0089
Layer - 3		0.0006		1/2oz Sig	
		0.0040	3313 - 63%	FR408HR	3.48 / 0.0096
Layer - 4		0.0006		1/2oz P/G	
		0.0210	0.0210 (2-2116/2-1652)	FR408HR	3.79 / 0.0086
Layer - 5		0.0012		1oz Mix	
		0.0034	3313 - 63%	FR408HR	3.48 / 0.0096
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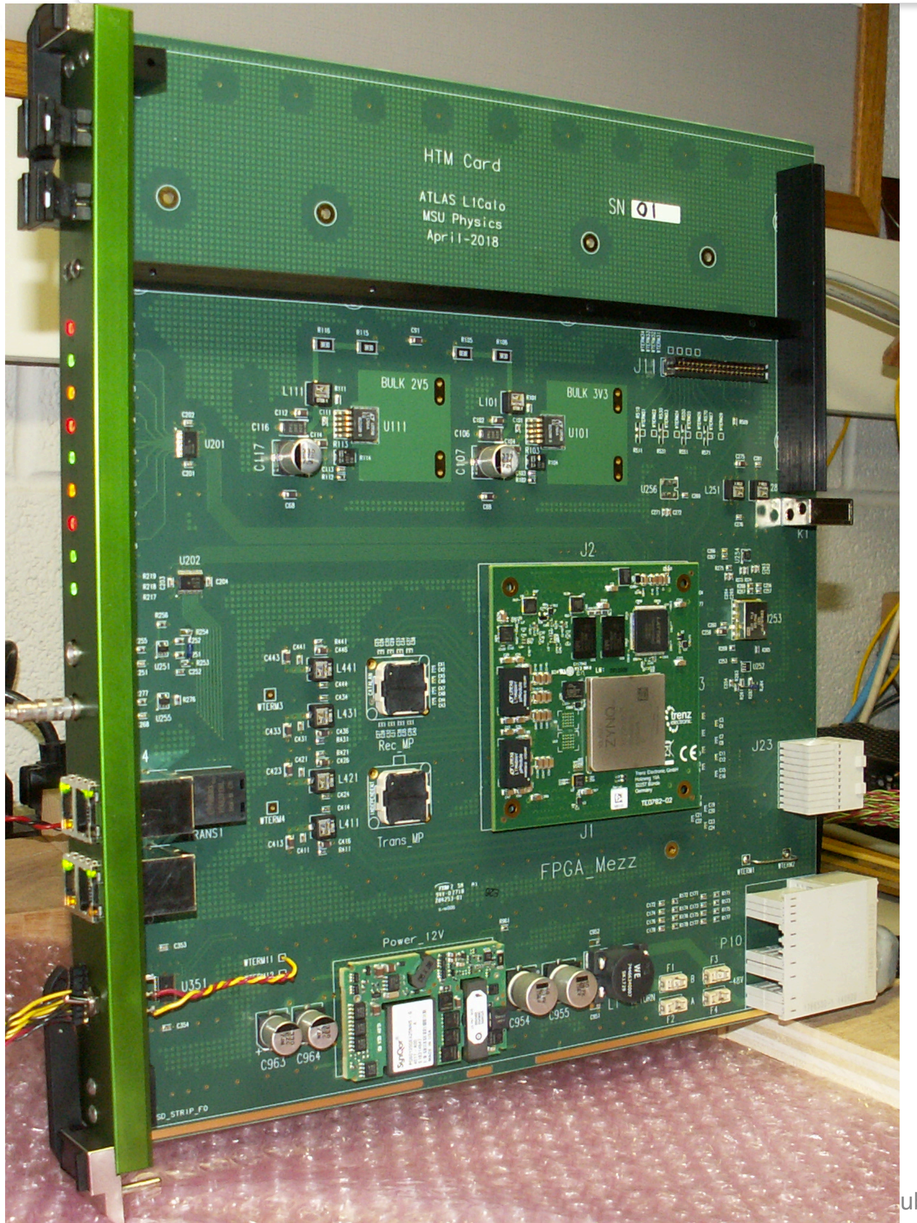
Layer - 8		0.0006		1/2oz Sig	
		0.0100	0.0100 (2-2116)	FR408HR	3.69 / 0.0089
Layer - 9		0.0006		1/2oz P/G	
		0.0038	1080 - 71%	FR408HR	3.42 / 0.0098
Layer - 10		0.0020		1/2oz Mix (Std Plt)	
		0.0005		Taiyo 4000-HFX DI	3.50 / 0.0190

Materials: Isola FR408HR High Speed High-Tg FR4

Hub Test Module



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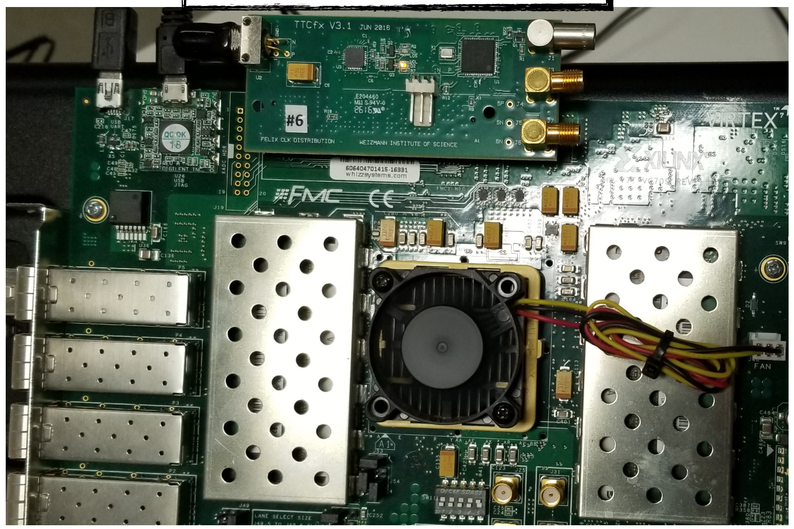
Materials: Isola FR408HR High Speed High-Tg FR4

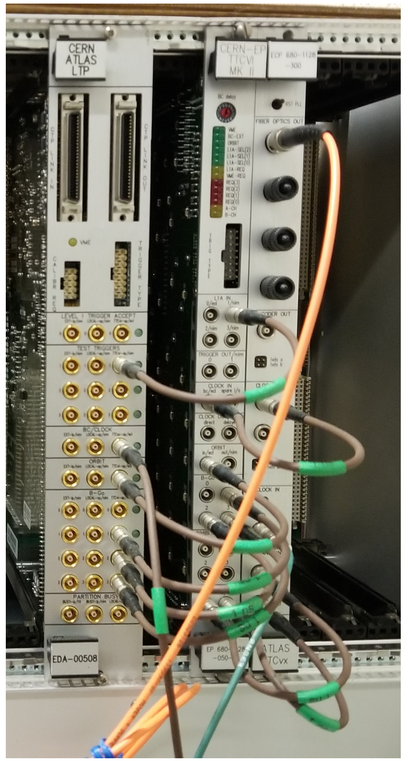
MSU Test Stands

- MSU has two Hub/HTM test stands available for system tests
  - 14 slot ATCA shelf (40G qualified), primarily used for bandwidth tests. Shown here with 12 HTM cards.
  - 6 slot ATCA shelf (40G qualified), primarily used for firmware development.
- System test capabilities
  - VME TTC system providing 40.08 MHz master clock, L1A, ECR, BCR, etc.
  - FELIX functions via TTCfx v3.1 mezzanine on VC709 Xilinx dev board.
  - Optical connections between HTMs and Hub/ROD cards
  - Full backplane link population with 8 lanes to/from each slot
  - 16 PCs to source & sink GbE throughput tests

TTCfx v3.1 + VC709



TTCvi
TTCvx
***Modified to deliver 40.08 MHz clock**



MSU Test Stands

MSU Test Stands

- A ***very*** quick word on current test results
  - MSU has tested a full shelf of 2 Hubs, 1 ROD and 12 HTMs for long-duration signal reception tests.
  - Tests run using Xilinx IBERT firmware with pseudo-random bit sequences of 31 bits in length and at 6.4 Gbps line rates.

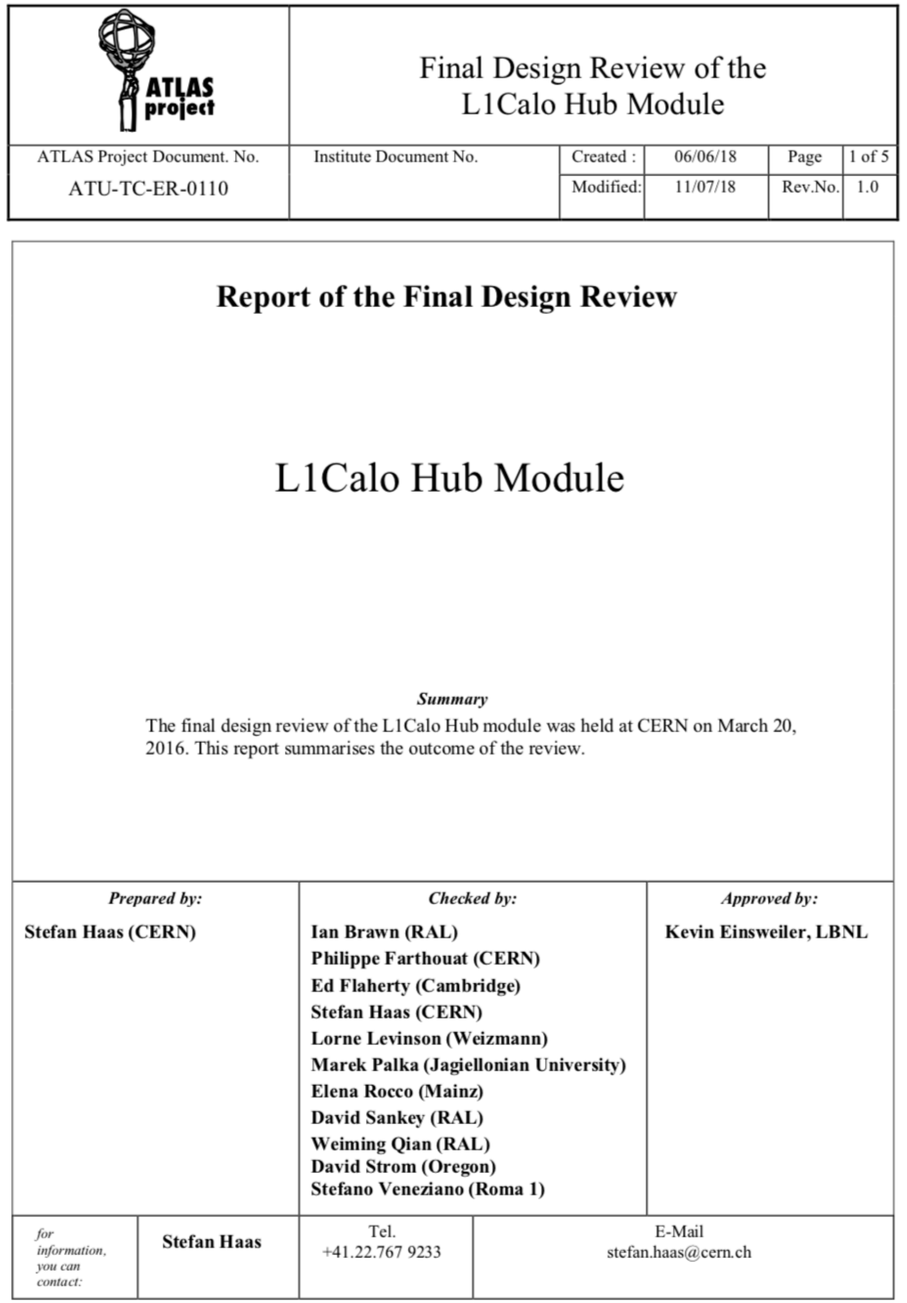
- Two long runs have been performed with different Hub modules each run.
  - First ran ~30 days to BER<6E-17, no errors observed
  - Second ran ~18 days to BER<1E-16, no errors observed
  - In reality, these modules never stopped running for 2+ months with no errors. The real metric is more like ~ <2E-18

Much more on this later and in the next presentation, but this data is relevant throughout this presentation.

Final Design Review Follow-up

Hub Final Design Review

- Hub final design review (FDR)
  - Held 20 March 2018
    - https://indico.cern.ch/event/713755/
- Report issued 12 July 2018
  - Available in EDMS:
    - https://edms5.cern.ch/document/1996657/1
  - Several recommendations and action items identified
    - Clock recovery & distribution
    - PCB & Signal fidelity
    - FW & SW performance
  - FDR Report response document circulated 10 Oct 2018



ATLAS project

Final Design Review of the L1Calo Hub Module

ATLAS Project Document. No.	Institute Document No.	Created :	06/06/18	Page	1 of 5
ATU-TC-ER-0110		Modified:	11/07/18	Rev.No.	1.0

Report of the Final Design Review

L1Calo Hub Module

Summary

The final design review of the L1Calo Hub module was held at CERN on March 20, 2016. This report summarises the outcome of the review.

Prepared by:	*Checked by:*	*Approved by:*
Stefan Haas (CERN)	**Ian Brawn (RAL)** **Philippe Farthouat (CERN)** **Ed Flaherty (Cambridge)** **Stefan Haas (CERN)** **Lorne Levinson (Weizmann)** **Marek Palka (Jagiellonian University)** **Elena Rocco (Mainz)** **David Sankey (RAL)** **Weiming Qian (RAL)** **David Strom (Oregon)** **Stefano Veneziano (Roma 1)**	**Kevin Einsweiler, LBNL**

for information, you can contact:	**Stefan Haas**	Tel. +41.22.767 9233	E-Mail stefan.haas@cern.ch

Hub FDR Action Items & the ROD

FDR Action Item(s):

1) *Reception of readout data in the ROD mezzanine installed on the Hub has to be tested from all the FEX slots (could be one at a time). Tests should be performed using IBERT as wells with the Aurora protocol and full data format implemented in the firmware.*

2) *It is recommend that a combined ROD/Hub intermediate design review be held prior to launching the pre-production of either module. (…) In addition, a full chain slice test should have been demonstrated, including the transmission of a TTC stream from FELIX through the Hub to a FEX modules as well as readout data transfer from a FEX through the Hub and ROD to FELIX. The test should be performed in a full-size ATCA shelf loaded with the Hub/ROD and at least one FEX module prototypes.*

3) *Since many of these tests involve the ROD and since the performance of the ROD heavily depends on various features of the Hub, it is strongly recommended to perform a common PRR of the Hub and the ROD.*

Hub FDR Action Items & the ROD

- It is clear by now that this is not a joint review of the Hub and ROD. There are good reasons for this.
  - Availability of ROD prototypes has limited the ability to perform many of the requested tests.
  - The current demands on the ROD primary engineer are already very high.
    - We have thus focused on the independent areas that impact the Hub hardware design, and those which provide critical feedback to the ROD design.
    - Using HTMs as stand-ins for FEX/L1Topo cards should be sufficient, as the electrical & optical interfaces are identical.
  - The full slice test with FELIX, ROD and eFEX modules is planned for mid-Dec or early January.
    - The Hub team will provide FW support, on site if required.
  - The US funding profile does not admit a long delay to wait for the ROD project to be ready for PRR.
    - As noted, the demands on the ROD effort are substantial and pressure to cut corners to meet the Hub review needs is not within L1Calo's best interests.

We therefore have proposed to move forward with the Hub review, identifying areas which require follow-up at the ROD PRR or in a post-PRR Hub follow-up.

ROD Back-pressure

FDR Action Item:

A scheme for asserting back-pressure to throttle the readout to prevent buffer overflows needs to be defined and documented. The function required on the Hub have to be implemented.

- The ROD can assert back-pressure to FELIX through both:
  1) Its optical connection to FELIX
  2) Via a LEMO connector to the Hub front panel

- The LEMO connection has been shown to have proper electrical connectivity to the ROD, but there has been no systematic test in which the ROD has controlled this signal at MSU.

Clock-related Action Items

Clock Distribution: Hub PLL Chip

FDR Action Item:

…[the Hub PLL chip] has to be fully qualified in terms of input-to-output phase variation, including the effect of temperature. The input-to-output skew of the Silicon Labs Si5344 has been measured to be about 20 ps (over 10000 reset cycles) at room temperature. The performance of the selected jitter cleaner should match this figure. The phase-noise spectrum of the output clock used for the MGT reference also needs to be analysed against the requirements from the Xilinx specifications.

- FDR reviewers had the impression that the clock PLL chip chosen for the Hub was not sufficiently characterized and, thus, qualified for the project.
  - The Hub uses the Conner Winfield SFX-524G.

- Furthermore, this chip provides only one MGT reference clock frequency at 320.64 MHz. If more reference clock frequencies are required, this chip would not be adequate.

Clock Distribution: Hub PLL Chip

- The stability of the L1Calo FEX system is in part driven by the quality of the distributed clock. Thus, the Conner Winfield SFX-524G was chosen because it has an extremely high-quality quartz VCO, rather than a PLL device with an LC VCO.

  - The choice of quartz yields a Q value of O(50,000) rather than O(50)
    - This high Q value does imply a narrower frequency tracking range of ±40 ppm: 40.077097 - 40.080303 MHz
    - This satisfies the PLL operating range in **FELIX requirement 2.3.5**: 40.078886-40.078973 (proton runs) and 40.078422-40.078973 (heavy ion runs).

  - The high Q value gives rise to excellent RMS jitter generation specification for the ConWin SFX-524G
    - 0.20 ps RMS jitter for a 156.25 MHz clock input

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
J_{GEN2}	Jitter Generation RMS (12 kHz - 20 MHz)		0.20	-	ps	4.0
J_{TRAN}	Jitter Transfer Function	-	-	0.1	dB	5.0
TF	Input Frequency Tracking	±40	-		ppm	

http://www.conwin.com/datasheets/sg/sg186.pdf

Clock Distribution: Hub PLL Chip

- The stability of the L1Calo FEX system is in part driven by the quality of the distributed clock. Thus, the Conner Winfield SFX-524G was chosen because it has an extremely high-quality quartz VCO, rather than a PLL device with an LC VCO.

  - Because this PLL has a quartz VCO (rather than LC), the performance over temperature variations expected in the L1Calo operations is negligible.

  - The phase noise specification provides plenty of margin relative to the Xilinx MGT specification requirements
    - Similar to the Si5345 data sheet

Symbol	Parameter	7-Series	Ultrascale	Si5345	Nominal	Maximum	Units	Notes
SSB Phase Noise (for SFX-524G-DFF-A10Z								6.0
	at 10Hz offset	-	-	n/a	-57	-45	dBc/Hz	
	at 100Hz offset	-	-	-91	-92	-80	dBc/Hz	
	at 1kHz offset	-	-	-123	-120	-110	dBc/Hz	
	at 10kHz offset	-116	-105	-135	-138	-135	dBc/Hz	
	at 100kHz offset	-124	-124	-140	-150	-145	dBc/Hz	
	at 1MHz offset	-131	-130	-153	-157	-147	dBc/Hz	
	at 10MHz offset	-	-	-162	-160	-150	dBc/Hz	

http://www.conwin.com/datasheets/sg/sg186.pdf

Bottom line: 2 Hub + 12 HTM have run with BER<6E-17.

Clock Distribution: GBT Clock Recovery

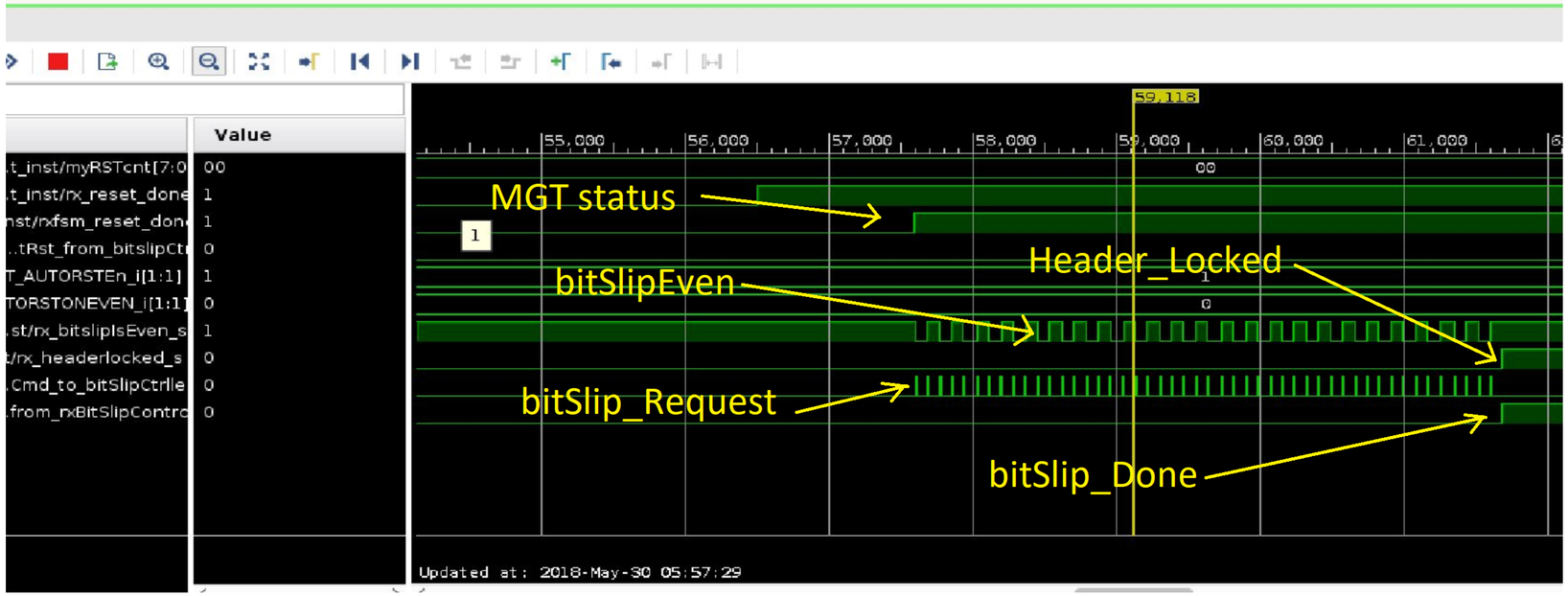
FDR Action Item:

The fixed phase of the clock extracted from the FELIX TTC stream needs to be demonstrated across modules resets, FPGA re-configuration and power-cycles. Since the standard GBT-FPGA implementation in a Xilinx Ultrascale FPGA can achieve a delay variation better than 100 ps (60 ps peak-to-peak over 1000 reset cycles), this is the performance figure to be met.

- Concern primarily related to the 320 MHz MGT reference clock provided by the Hub, rather than 120 MHz or 240 MHz.
- The Hub design restricts clocks to avoid domain crossings and to simplify board design.

Clock Distribution: GBT Clock Recovery

- The Hub module successfully recovers the 40.08 MHz LHC clock using the GBT-FPGA core in “latency-optimized” mode
  - Implemented by generating a 120 MHz MGT reference clock via QPLL
    - The MGT eventually tracks the 4.8 Gbps serial data stream, no relevant phase noise due to rate conversion.
  - “Frame Aligner” status and “Bit Slip Control” status are monitored to ensure proper GBT functionality
- Clock phase observed to be constant (to better than 100 ps) over a range of repeated tests
  - Monitored via comparison of TTC input clock to Hub output clock

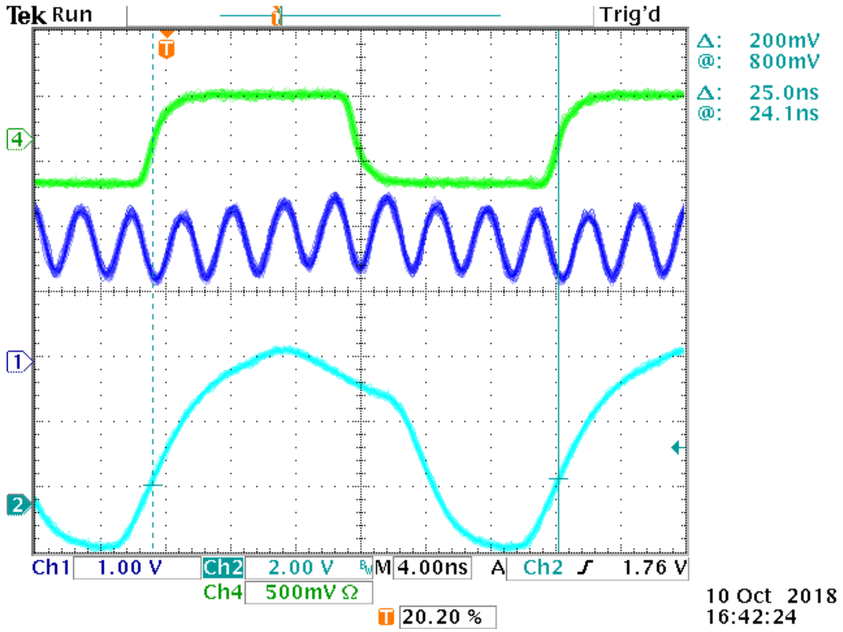


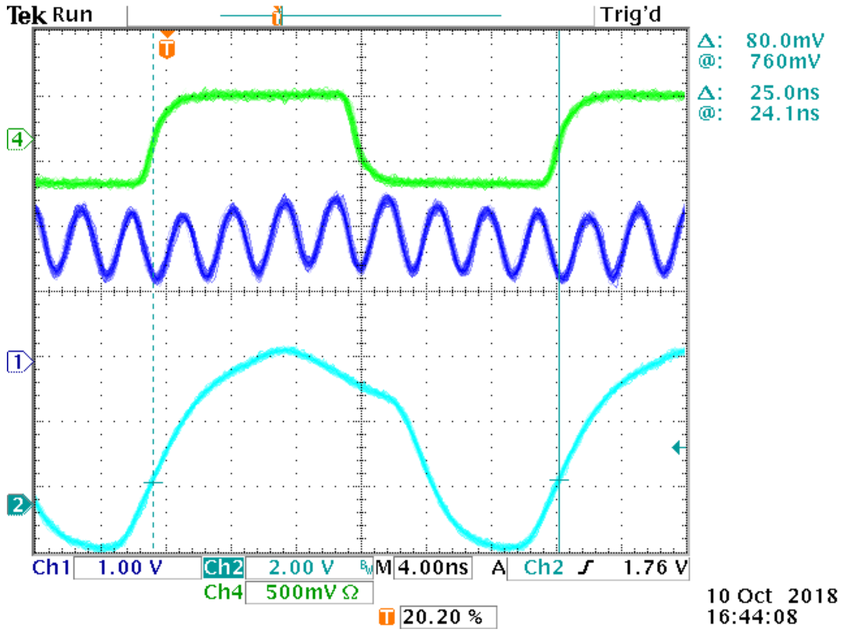
- Manual intervention, force GBT realignment
- Reset receiver MGT on Hub
- Power cycle Hub
- Reconfigure Hub FPGA
- Unplug/reinsert TTC fiber @ TTCfx/VC109
- Reconfigure TTCfx/VC709
- Re-initialize the TTCfx/VC709
- Reset of the TTCfx/VC709

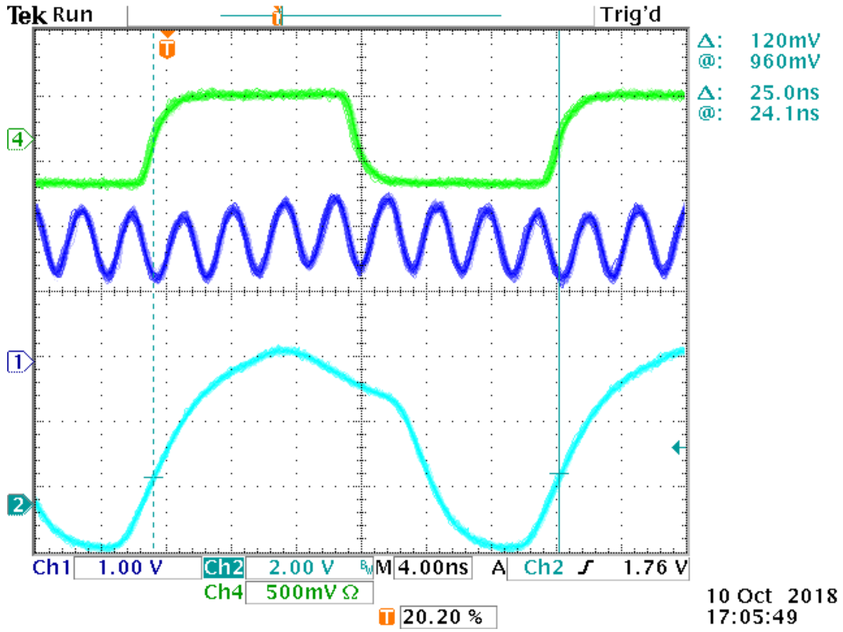
Clock Distribution: GBT Clock Recovery

- Here we have example scope captures of the recovered clock from the Hub over a few example interventions to the FELIX TTC clock.

Channel 1: 160 MHz ref clock
Channel 2: Recovered Hub clock
Channel 4: TTC input clock



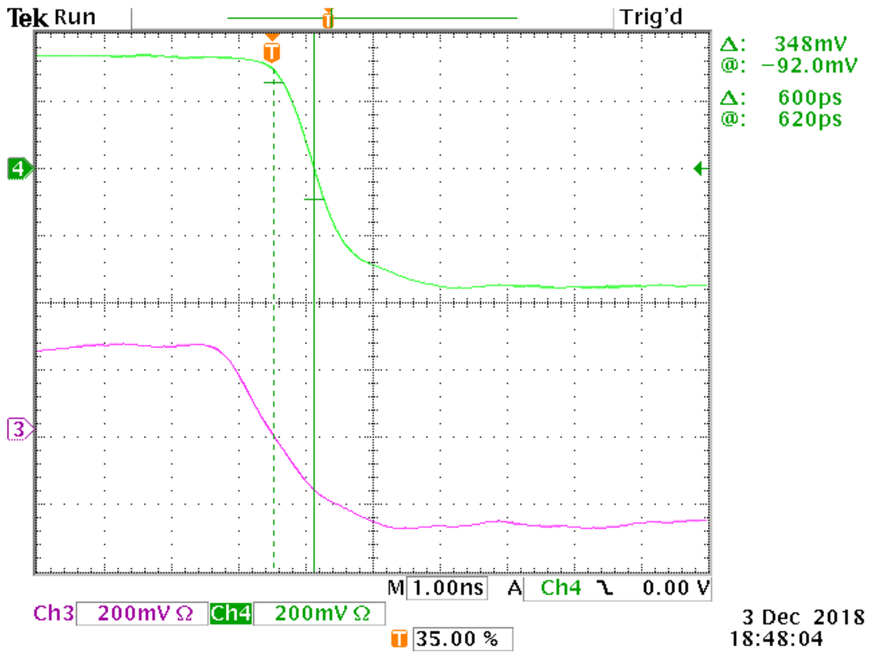




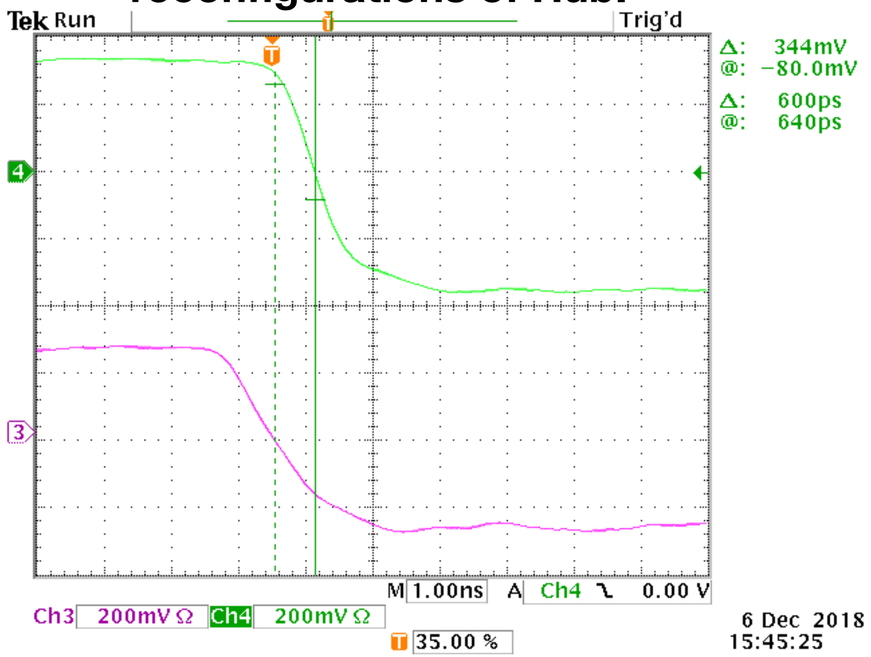
Clock Distribution: GBT Clock Recovery

- Stability of the clock latency at the FEX (HTM) has also been tested
  - The two scope traces below test latency stability between the 40.08 MHz clock:
    1) Starting at the TTC VME crate,
    2) through the VC-709 FELIX system,
    3) through the GBT Receiver, PLL jitter cleaner and reference clock fanout on the Hub,
    4) Across the ATCA shelf backplane,
    5) Received on the HTM (FEX) card where it passes through a PLL jitter cleaner to a front-panel clock monitor.

Initial Reference



Test 3 days later after random resets, reconfigurations of Hub.



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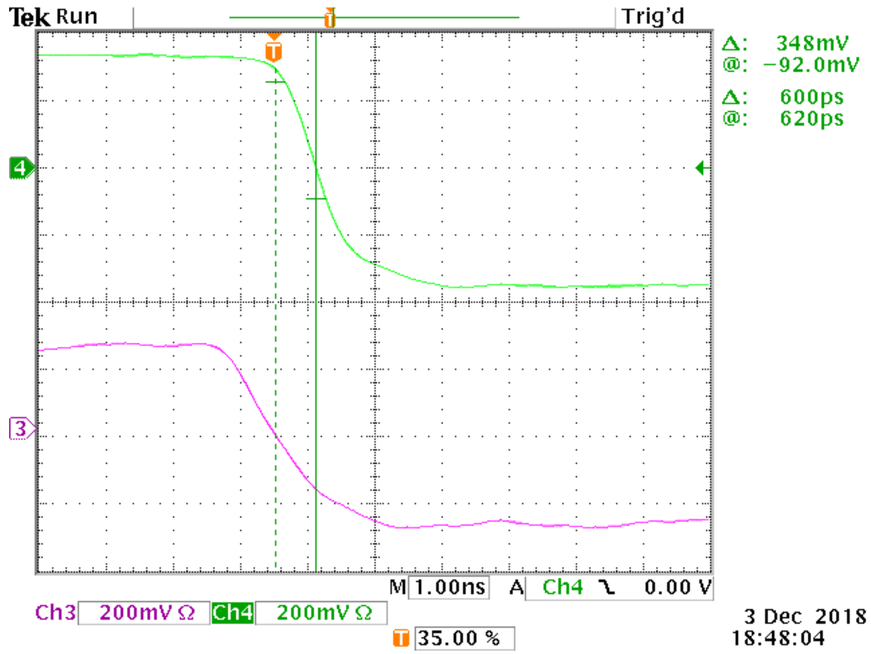
    5) Received on the HTM (FEX) card where it passes through a PLL jitter cleaner to a front-panel clock monitor.

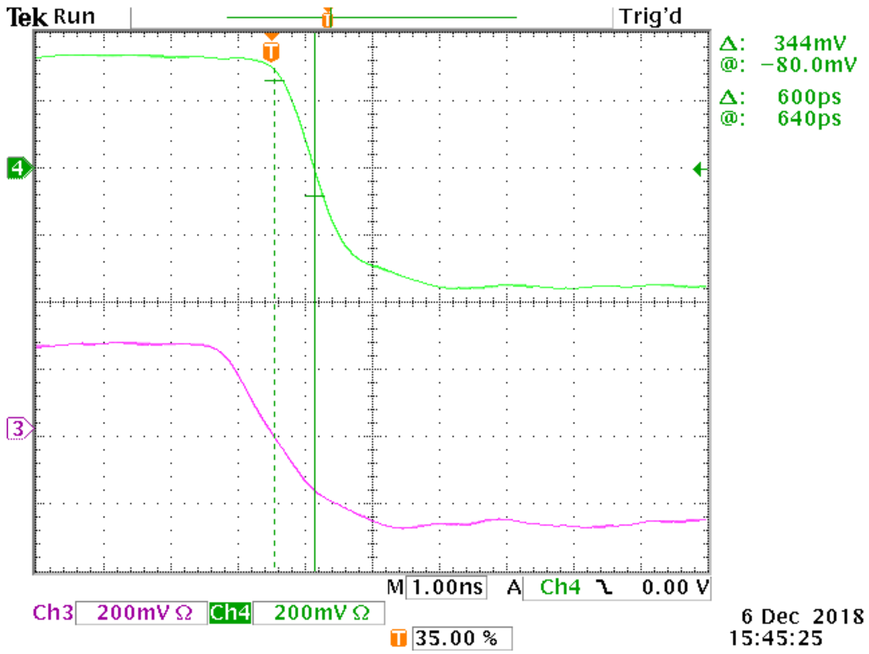
Initial Reference



Clock Distribution: GBT Clock Recovery

- Stability of the clock latency at the FEX (HTM) has also been tested
  - The two scope traces below test latency stability between the 40.08 MHz clock:
    1) Starting at the TTC VME crate,
    2) through the VC-709 FELIX system,
    3) through the GBT Receiver, PLL jitter cleaner and reference clock fanout on the Hub,
    4) Across the ATCA shelf backplane,
    5) Received on the HTM (FEX) card where it passes through a PLL jitter cleaner to a front-panel clock monitor.

Test 3 days later after random resets, reconfigurations of Hub.



Clock Distribution: Clock Fanout Logic Level

FDR Action Item:

There were some questions concerning the logic levels for the fan-out of the bunch clock over the backplane: the Hub uses an LVDS fan-out chip, however it seems that the eFEX would prefer LVPECL levels. The compatibility of the signal level from the Hub with the eFEX, jFEX and L1Topo should be checked and interoperability tests performed.

- Preference from FEX groups to use LVPECL to hopefully improve margin at their MGTs, due to better jitter performance.
- Preference from the Hub group to minimize the noise crossing the FEX data fanout, reduced in LVDS wrt LVPECL due to smaller edge rise.

Clock Distribution: Clock Fanout Logic Level

- The current Hub and FEX/L1Topo card designs are compatible
  - Existing FEX/L1Topo designs use PLL chips with universal inputs
    - No design changes required to use either source
- L1Calo system is not the characteristic use case for LVPECL
  - Benefits of LVPECL are found when both ends of the LVPECL link are on the same board (ie, full run of the link)
    - ie, full run of the link is over one ground plane and both Rx & Tx are operated from the same positive power plane.
    - ECL logic levels are WRT its positive power supply terminal and any trace imperfection spoils the common mode rejection at high enough frequency.
  - When done right, LVPECL can indeed have an advantage over LVDS
    - However, when operating over a backplane, with separate positive and ground planes at Tx and Rx, then LVPECL is at a disadvantage WRT LVDS.
- To resolve the issue, eye diagrams at the eFEX MGTs have been studied for the different clock sources.
  - LVPECL when using FTM and LVDS when using the Hub
    - No discernible difference in BER or open eye area reported. **L1Calo has agreed on the LVDS logic level.**

Firmware-related Action Items

Firmware: Core Hub Firmware Items

FDR Action Item(s):

1) Firmware for the essential functions of the Hub needs to be ready and fully tested. This includes the interface to FELIX as well as to the ROD and the FEX modules with close to final data formats. IPbus should also be fully working.

2) The TTC interface with FELIX need to be fully implemented and characterized.

3) In addition the firmware does not seem to be under revision control yet, the overall L1Calo guidelines on this should be followed.

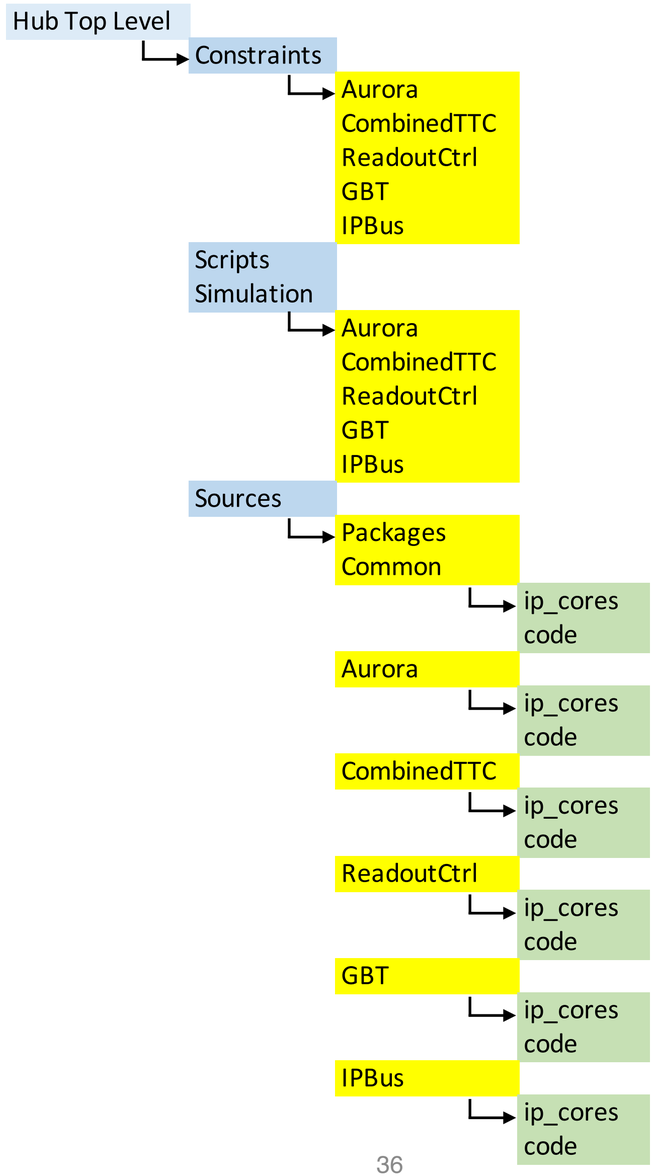
- There are four core firmware aspects for the Hub project.

(a) ROD power-up sequence state machine
(b) GBT/FELIX TTC clock recovery with deterministic phase
(c) TTC/Combined data transmission to node slots with deterministic phase.
(d) IPbus functionality to control ROD/Hub configurations and retrieve monitoring data.

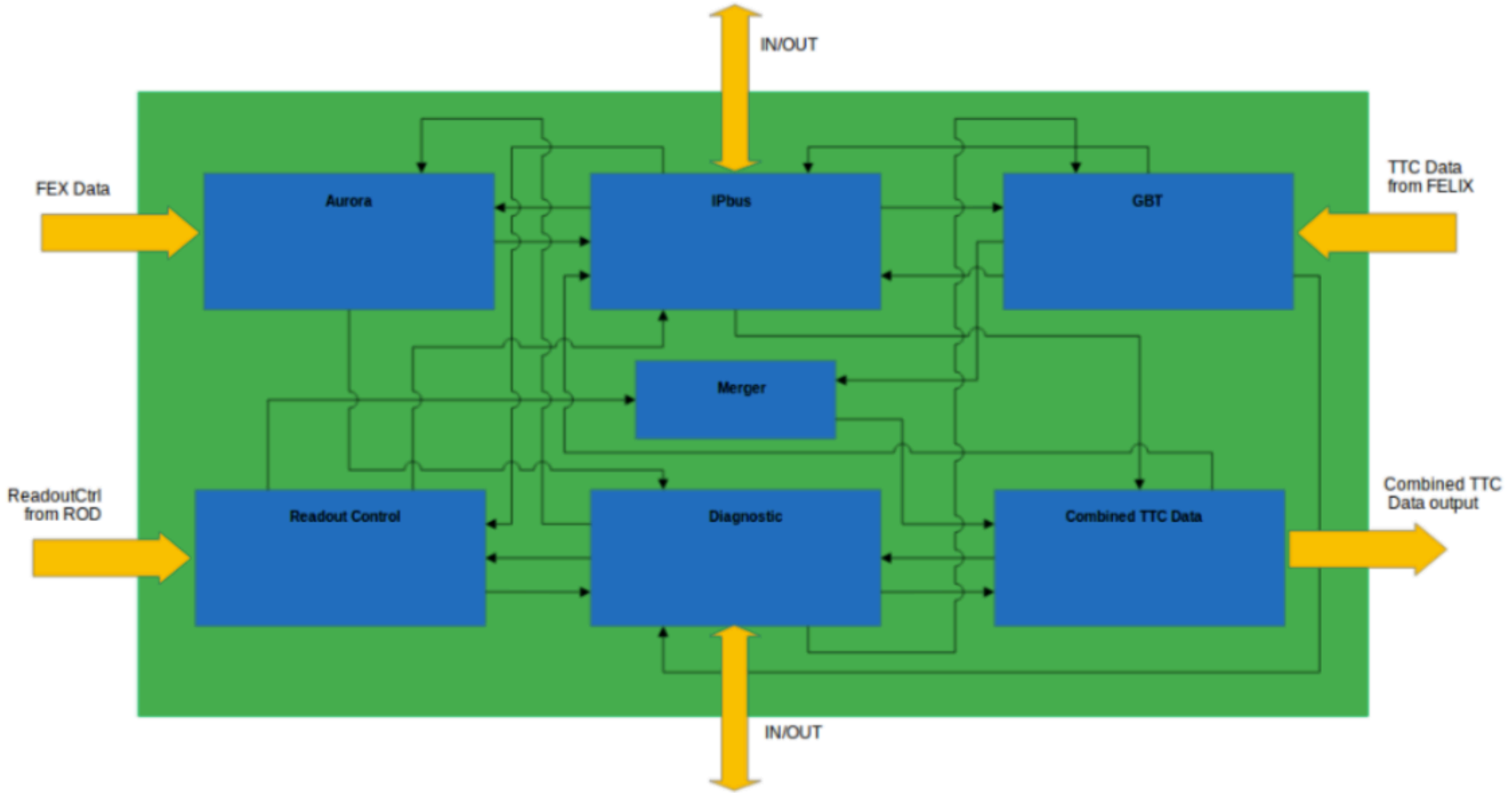
Firmware Management

The versioning control of the Hub firmware is currently maintained in CERN gitlab in private repositories, and is being migrated to the CERN gitlab project `atlas-llcalo/firmware/hub`.

There is a similar structure for the HTM firmware, and a parallel repository for the Hub and HTM software.



Firmware Block Diagram



Firmware: IPbus Implementation

- Both the Hub and HTM cards have successfully integrated IPbus firmware into their respective designs, allowing register-level control of all card functions.
  - Full set of status/control and test/monitoring registers
    - Equalizers, LEDs, I2C buffers, ROD control, IPbus lock, clock selector, HW/FW revision, etc
  - XILIX AXI4 subsystem IPs (via IPbus to AXI4 bridge, similar to ROD)
    - 3 AXI IIC Master IP (22 internal registers)
      - MiniPODs (temp, light level), DC/DC supplies (temp, voltage, current)
    - 3 AXI EthernetLight IP (11 internal registers)
      - 3 Broadcom GbE switch chips
    - AXI System Management Wizard IP (~100 internal registers)
      - FPGA System Monitor (temp, voltage)

Addr	Type	Name	Content		Bit	Comment
00000000	RW	control	other_hub_clk		[31]	FPGA internal, selects clock from other Hub
			fex_clk_en		[30]	Enable clock to FEXs
			mgt_equ_en		[29:17]	Enable equalization in MGT Fanout chips
			i2c_buf_en		[16]	I2C_Buf_1501_ENABLE
					[15]	I2C_Buf_1502_ENABLE
					[14]	I2C_Buf_1503_ENABLE
			spare		[13-11]	spare bits
			rod_pwr_en	?	[10]	ROD may turn ON its power supplies
			rod_pwr_en_b	?	[9]	ROD may turn ON its power supplies
			spare		[8:6]	spare bits
			mpod_rst_b	*	[5]	Trans_MiniPOD_RESET_B
				*	[4]	Recvr_MiniPOD_RESET_B
			spare		[3:0]	spare bits

This is control register for the individual pins (exeption - other_hub_clk, Drw: 40A)
All bits set to '0' after power-on.

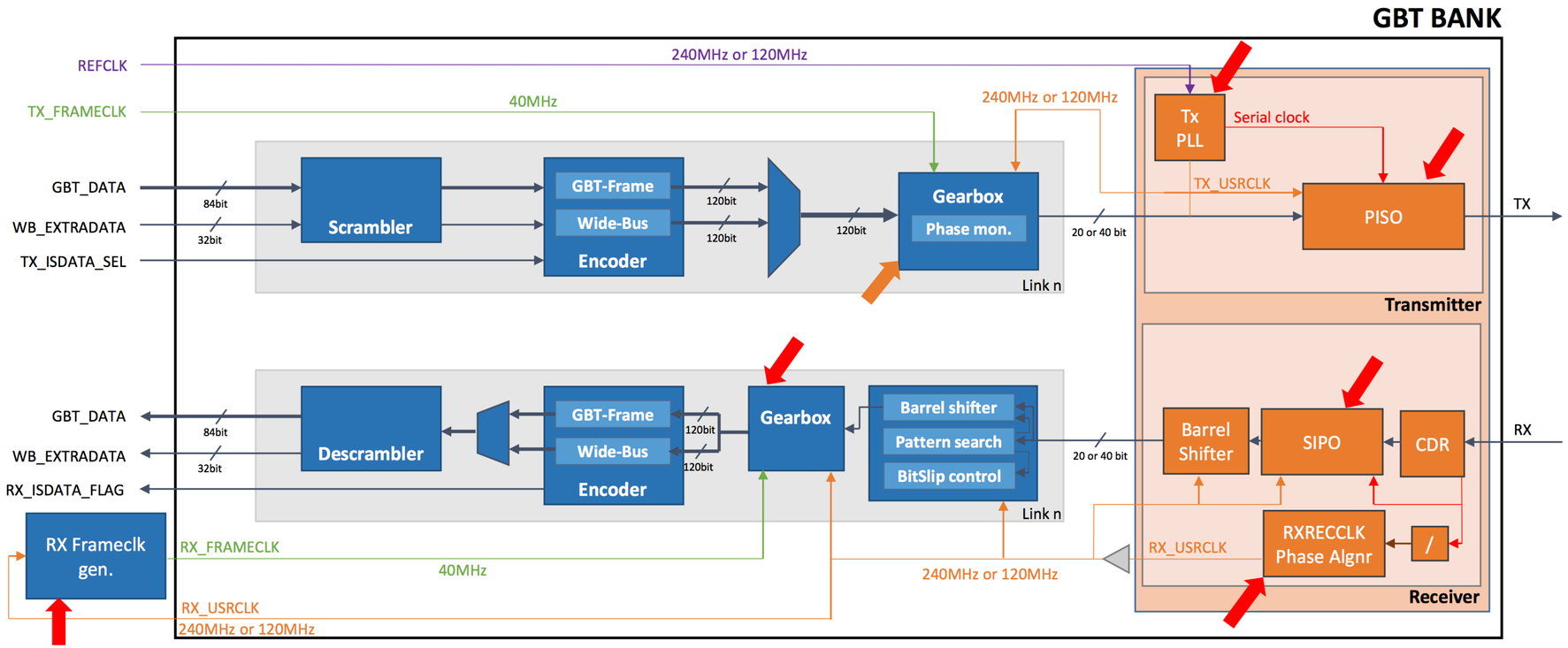
HUB: all bits are implemented
HTM: only bits with (*) are implemented - mpod_rst_b

Addr	Type	Name	Content		Bit	Comment
00000006	RO	status	pll_lock	*	[31]	From PLL lock circuits - pll40_lock
					[30]	From PLL lock circuits - pll320_lock
			phy_int	*	[29]	From Eth Phy chips - phyU21_int_b
					[28]	From Eth Phy chips - phyU22_int_b
			mpod_int	*	[27]	From the MiniPODs - trans_mpod_intr_b
				*	[26]	From the MiniPODs - recvr_mpod_intr_b
			hub_smb_alert		[25]	From 7 DCDC Converters
			hub_pwr_good		[24]	From the Power Control circuits
			rod_present_b		[23]	ROD is present
			rod_smb_alert_b		[22]	Power supply problem on the ROD
			rod_status		[21]	ROD power
					[20]	ROD config
			rod_status		[19]	spare rod_power_ctrl4
			sw_loop_det		[18]	Broadcom Switch chips switch_a_loop_det
					[18]	Broadcom Switch chips switch_b_loop_det
					[18]	Broadcom Switch chips switch_c_loop_det
			spare		[15:0]	spare bits, set to all zeros

This is a status information from individual pins.
HUB: all bits are implemented
HTM: only bits with (*) are implemented - [31] PLL_40_MHZ_LOCKED_MON
[29] ETH2_INT
[27] MP_TRANS_INTR
[26] MP_REC_INTR

Firmware: GBT/TTC Clock Recovery

- As stated previously, the LHC clock is recovered from the TTC signal provided via FELIX and decoded via the GBT firmware.
  - 120 MHz reference clock generated at MGT quad QPLL
  - All features of the firmware behave as expected
    - Stable, deterministic latency clock recovered and fanned out.



https://indico.cern.ch/event/489996/contributions/2291863/attachments/1345764/2028939/GBTTutorial_-_TWEPP2016.pdf

Firmware: TTC/Combined Data Fanout

FDR Action Item(s):

1) Tests of the TTC clock reception on the each of the FEX slots as well as the TTC/control link to and from the FEX slots have to be performed under the same conditions as above.

2) The TTC interface with FELIX need to be fully implemented and characterized.

- The L1Calo requirement is that the TTC combined data is provided at the receiving end with a deterministic latency.

Firmware: TTC/Combined Data Fanout

- To define the phase of the arrival of the TTC/Combined data, we use the LHC master clock as the reference. This minimizes the variation across the system and provides an easily-to-verify, stable reference.
  - 128 bits of control data are received from the ROD at a 6.4 Gbps line rate
    - This data is translated and merged with TTC data in the Hub (L1A, ECR, BCR)
  - 128 bits of TTC/Combined data are transmitted from the Hub at a 6.4 Gbps line rate
    - At the receiver, the data is transferred into a parallel register
  - The 128 bits of the TTC/Combined data are provided to the users at the output of a 128 bit wide D register.
    - The D register is updated on the positive edge of the FPGA's 40.08 MHz clock that is locked to the LHC backplane reference clock.
    - These 128 bits are stable at all times except during the update.

- Receiver FPGA requirements
  - MGT reference clock to receive the 6.4 Gbps link
  - 40.08 MHz clock locked to the LHC backplane reference clock

** The Readout Control and Combined TTC Specification (v0.5) is linked to the indico page.

Other Hardware-related Action Items

Hardware: Backplane Link Testing

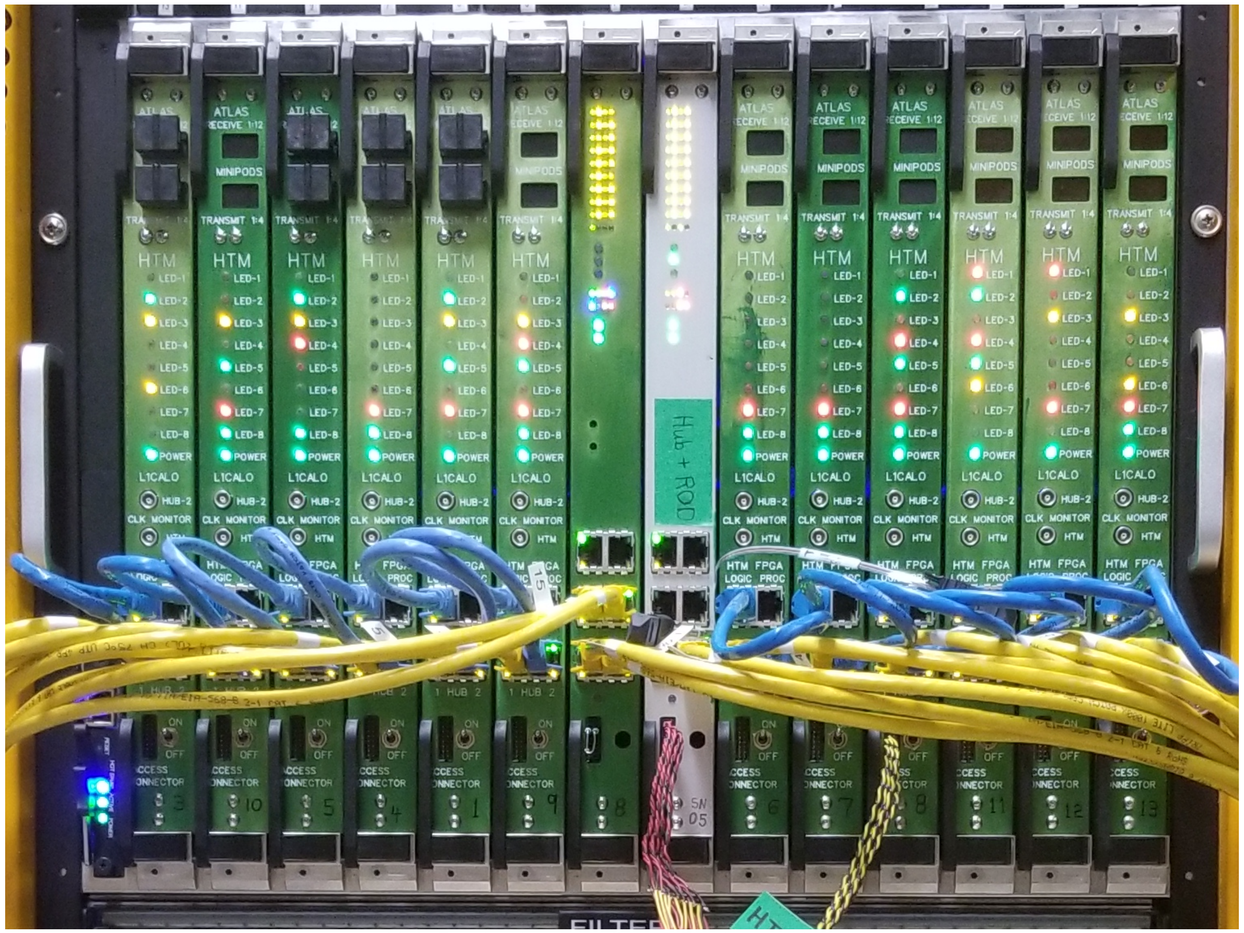
FDR Action Item(s):

1) A full-size ATCA shelf should be fully populated with Hub Test Modules and two Hub modules in order to run traffic on all the backplane links to and from the Hub concurrently.
2) BER tests should be performed in this configuration to check for potential crosstalk issues.
3) The test should be performed with a ROD mezzanine installed in order to also cover the backplane links to the ROD.

- At the time of the FDR, no full-shelf bandwidth tests had been performed. The primary concern is whether the dense design of the FEX data fanout, clock and TTC/Combined data routing is susceptible to crosstalk.

Hardware: Backplane Link Testing

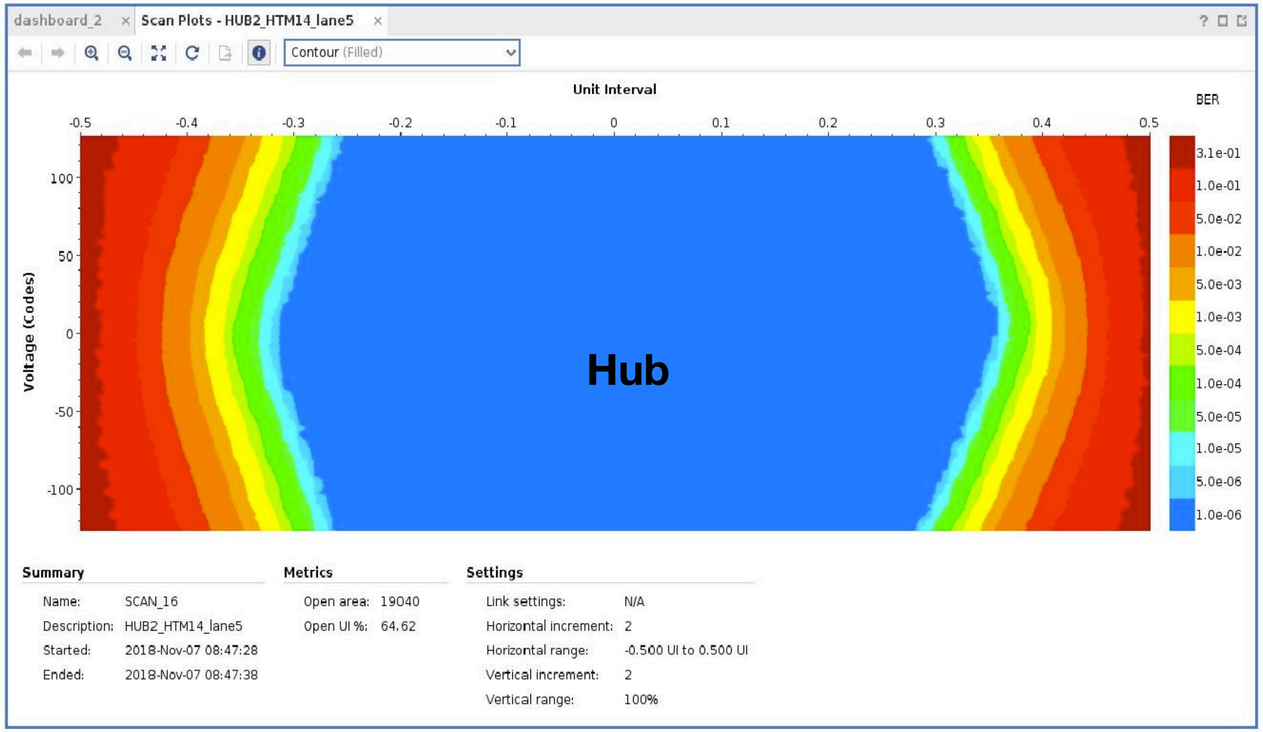
- As noted earlier in this presentation, Hub Test Modules (HTMs) have been produced by MSU.
  - The HTMs emulate the relevant subset of FEX interfaces to the Zone-2 and optical interfaces for Hub and ROD.
  - The MSU 14-slot shelf and 6-slot shelf both are populated with HTMs.

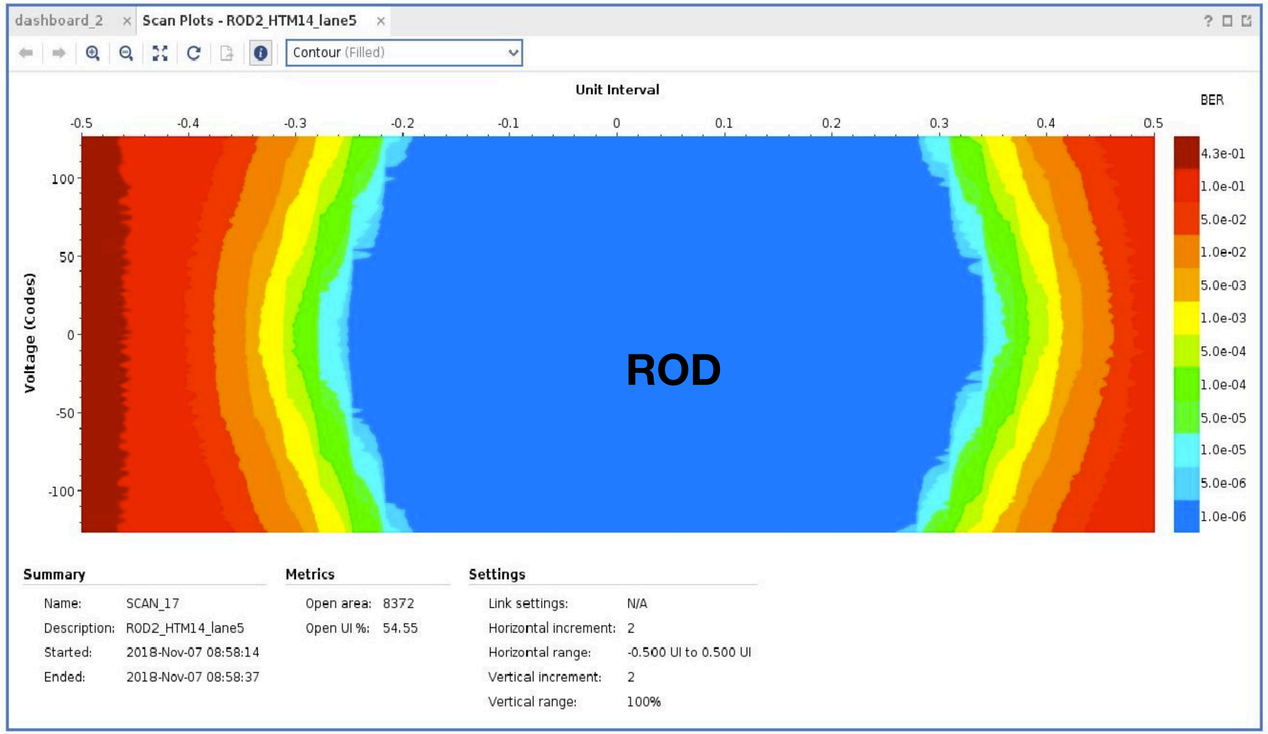


Hardware: Backplane Link Testing

- BER tests have been performed with Xilinx IBERT firmware at a line rate of 6.4 Gbps and using PRBS31
  - Two separate, long-duration runs have been performed and find the full system capable of **BER<6E-17**. No errors observed.
  - Eye diagrams have been produced for both Hub and ROD data links. <u>They all look very good.</u>
  - Relevant data shown here, much more analysis shown in the next talk.

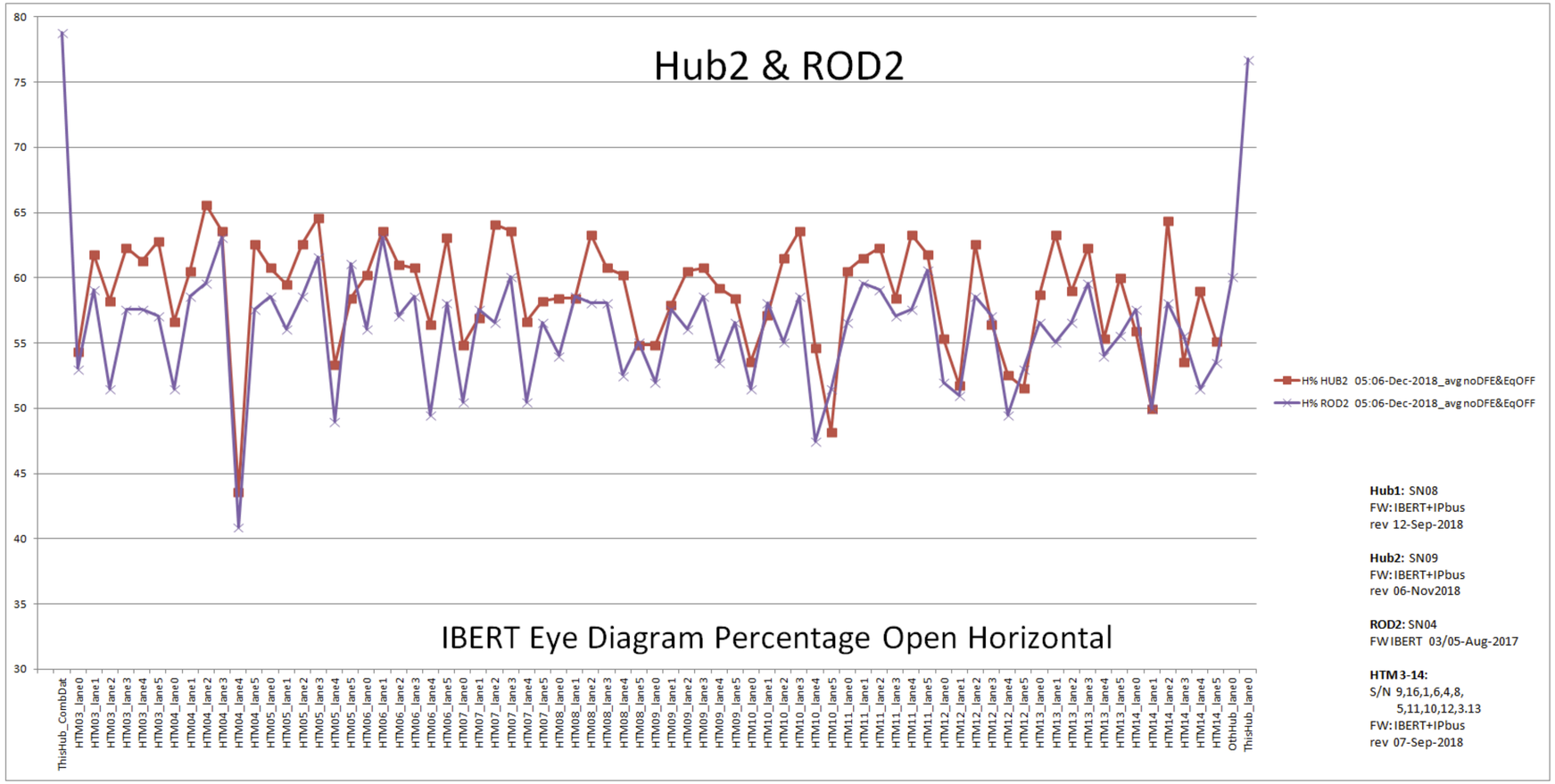
Hub Slot 2, HTM Module 14, Data Lane 5: DFE off, Fanout Eq on





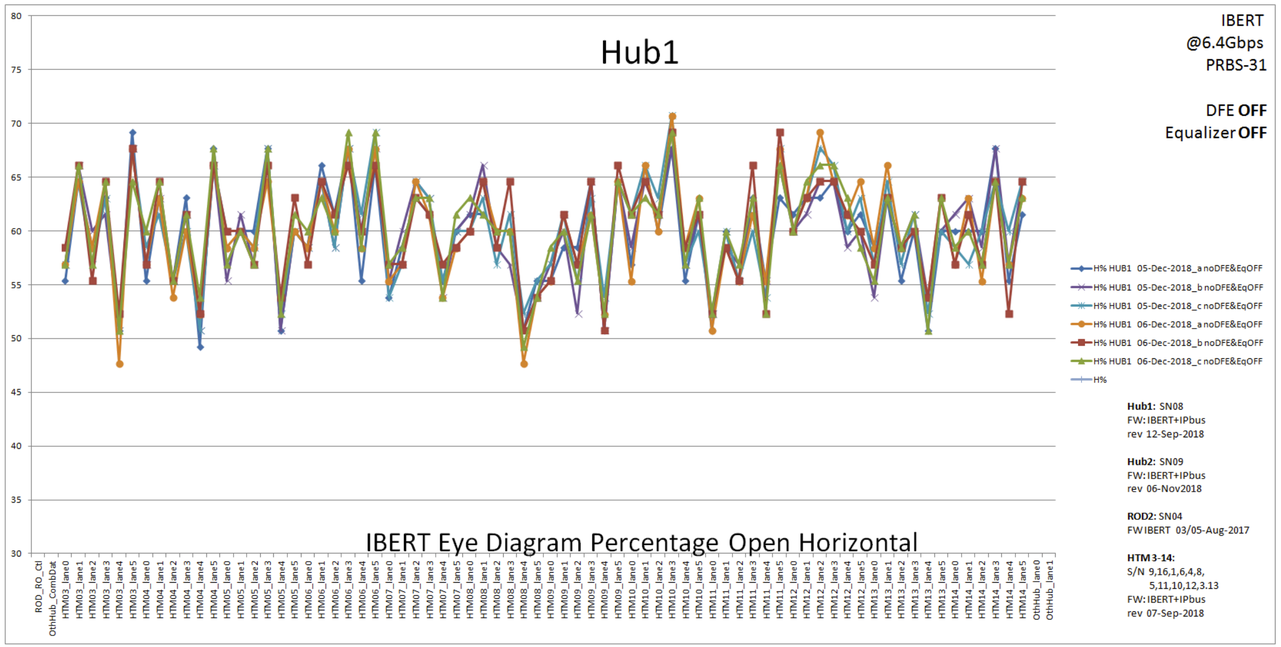
Hardware: Backplane Link Testing

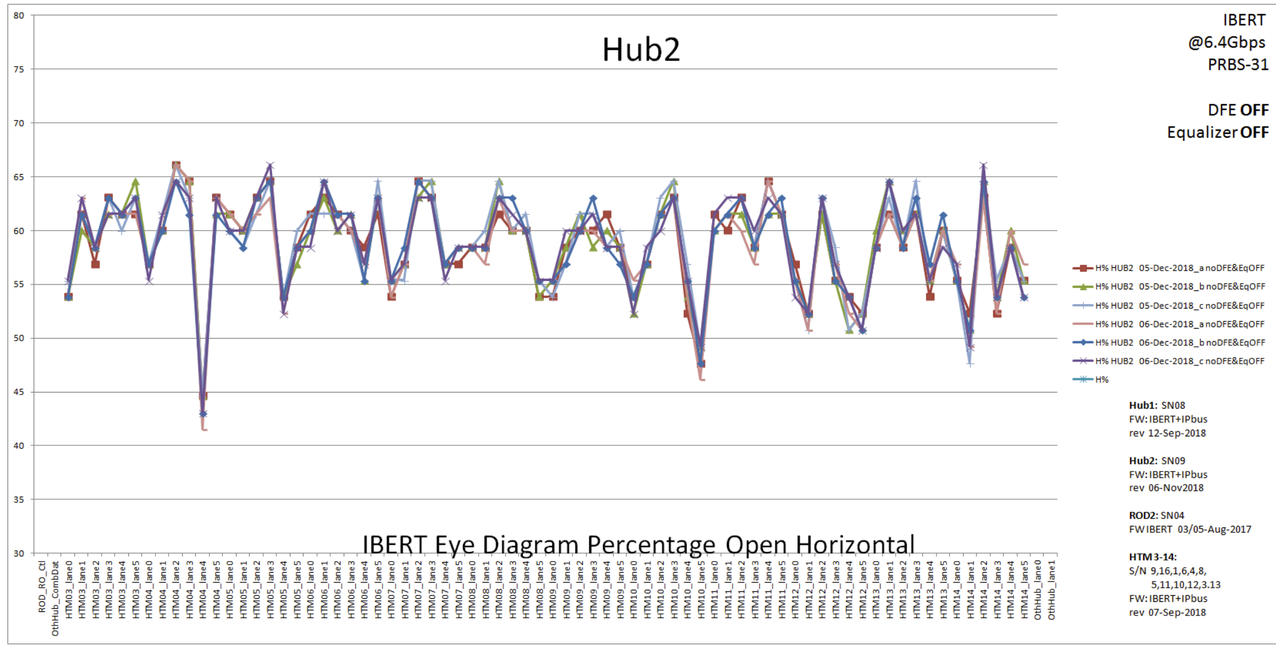
- BER tests have been performed with Xilinx IBERT firmware at a line rate of 6.4 Gbps and using PRBS31, including all FEX Zone-2 links for Hub and ROD.
  - Two separate, long-duration runs have been performed and find the full system capable of **BER<6E-17**. No errors observed.
  - Relevant data shown here, much more analysis shown in the next talk.



Hardware: Backplane Link Testing

- Repeated tests of the Hub eye diagrams illustrate very high uniformity over Hub modules.
  - Repeated tests of the same card also show zero variation.
  - Quality and uniformity of the Hub PCB manufacturing and assembly processes is very high.
  - 6 Hubs shown here, 2 remaining in UK will be tested once we can swap them out.





Hardware: PCB Laminate

FDR Action Item(s):

1) *The Hub blade uses a 22-layer PCB. The dielectric material chosen is Isola FR408HR, which is not a dedicated high-speed laminate. For instance the dissipation factor (Df) of FR408HR is about 2.5 times higher than the one of Megtron-6 or Isola I-Tera, which are the dielectric materials used for the FEX blade PCBs. There was no technical justification given for this choice, in particular since the PCB production house is the same than the one used for the gFEX, Megtron-6 would clearly have been a possible choice. The choice of the dielectric should be reconsidered for the pre-production modules.*

2) *A signal integrity analysis of the most critical high-speed tracks (probably from the fan-out buffers to the ROD) should be done to assess the impact of the chosen dielectric with respect to a high-speed material such as Megtron-6.*

- Concern expressed that the Hub PCB laminate will not support the required signal integrity of the high-speed data links.

Hardware: PCB Laminate

- The choice of Isola FR408HR was intentional, not an oversight. There were three primary considerations:
  1) Based on consultation with the PCB manufacturer and assembly house, and with a clear understanding of our use case, this laminate was recommended to give the highest chance of uniformity over a build of 20 PCBs.
  2) Our observation of other attempts to use Tachyon/I-Tera/Megtron-6 laminates is a high frequency of delamination. Given that delamination may only be apparent after years of use, the risk was very high to use these laminates.
     - There are numerous examples in ATLAS & CMS, notably in L1Calo. MSU's first run with the CMX had delamination issues.
  3) MSU's primary electronics design engineer has decades of experience in high-speed digital design. He understood very clearly the goal of 10+ Gbps bandwidth to all FEX slots and designed to meet that requirement.

Bottom line(s):

- **2 Hubs + 12 HTMs have run with BER<6E-17.**
- **8 prototype Hubs have been built with extremely high uniformity.**

Hardware: IPMC & Monitoring

FDR Action Item(s):

1) Monitoring on-board sensors (at the very least for the Hub and ROD FPGA temperatures) using the IPMC has to be tested. The sensor values have to be read out through the ATCA shelf-manager.

2) The I2C bus to access the on-board sensors is shared between two masters: the Hub FPGA and the IPMC. It is unclear how the arbitration will work and access from the IPMC to the sensor bus appears not to have been tested yet. The IPMC requires access to some critical temperature sensors (Hub FPGA and ROD FPGA on-chip temperature) in order for the ATCA shelf speed regulation through the shelf manager to work. This needs to be demonstrated.

- Concern expressed regarding I2C multimastering and ability of proper IPMC functions.

Hardware: I2C Multimastering

- The Hub I2C bus can be isolated from the IPMC I2C bus and we do not require I2C multimastering during “normal” L1Calo operations.
  - Outside debugging, commissioning and bench testing, only the IPMC will master the I2C bus.

- All Hub & ROD components on the I2C bus are able to be accessed & monitored
  - DCDC converters, FPGA sysmon are primary targets.

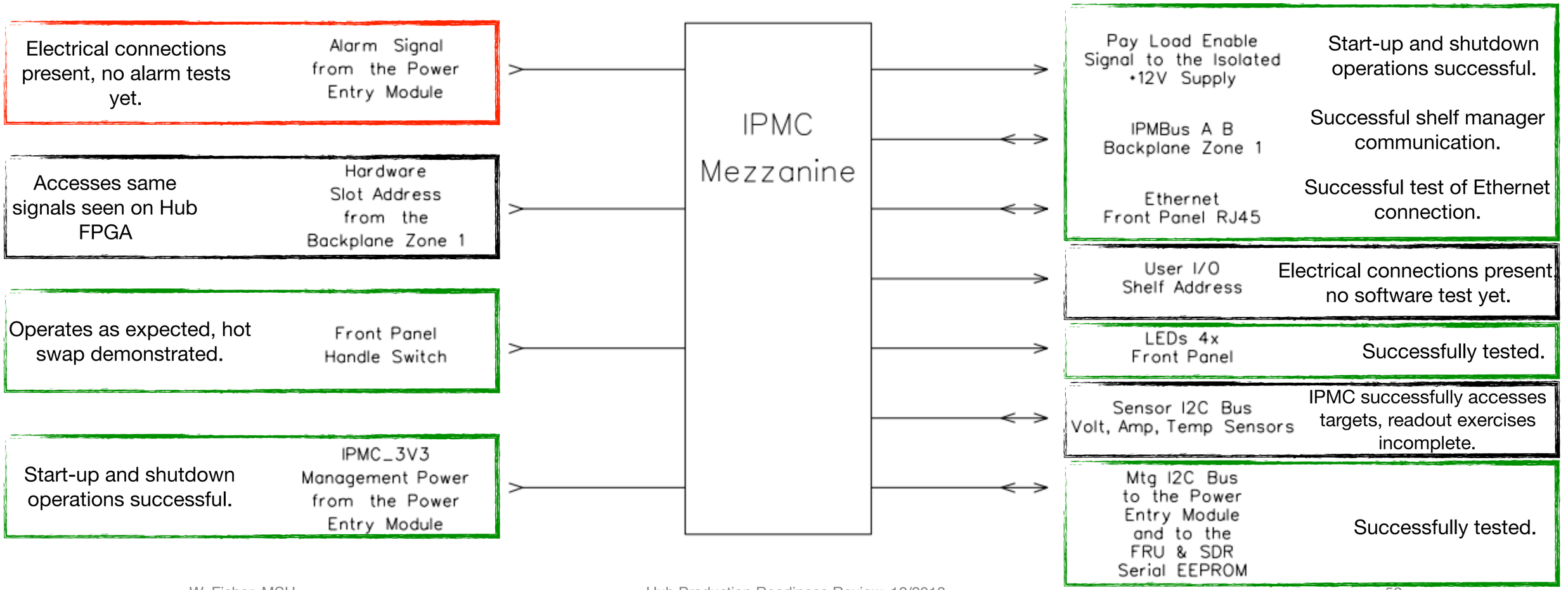
- We have tested our ability to perform I2C arbitration with the IPMC
  - Successfully able to detect bus busy and data FIFO status on the I2C bus.
  - Hub IPbus/I2C software reliably detects IPMC cycles, with a state machine designed to wait for successful I2C mastering arbitration.
  - O(300k) cycles executed without I2C error in a long test run.

Example read of Hub miniPOD transmitter

```
MiniPod type verified to be: trans_mpod
 Minipod internal temperature is 32.22 C
 The voltage on the 2.5 Vcc power supply is 2.4657 V
 The voltage on the 3.3 Vcc power supply is 3.2596 V
 The serial number of the current device: trans_mpod is : A17285016
 The operating time is 3038.0 hours or 126.583333333 days
 Optical power for channel number trans_mpod is: 0.14646524684 dBm or 1034.3 µW
 Optical power for channel number trans_mpod is: 0.911039440903 dBm or 1233.4 µW
 Optical power for channel number trans_mpod is: -0.00130307891732 dBm or 999.7 µW
 Optical power for channel number trans_mpod is: 1.06496870139 dBm or 1277.9 µW
 Optical power for channel number trans_mpod is: 0.137217780511 dBm or 1032.1 µW
 Optical power for channel number trans_mpod is: 1.09646031091 dBm or 1287.2 µW
 Optical power for channel number trans_mpod is: 0.152759066819 dBm or 1035.8 µW
 Optical power for channel number trans_mpod is: 1.0510124455 dBm or 1273.8 µW
 Optical power for channel number trans_mpod is: -0.220935723629 dBm or 950.4 µW
 Optical power for channel number trans_mpod is: 1.3165073809 dBm or 1354.1 µW
 Optical power for channel number trans_mpod is: 0.262471814778 dBm or 1062.3 µW
 Optical power for channel number trans_mpod is: 1.20080134129 dBm or 1318.5 µW
 The nominal wavelenght for device trans_mpod is 845.0 nm ( ± 15.015  nm)
```

Hardware: IPMC

- We have successfully tested all relevant electrical connections to/from the IMPC, and verified their proper operation.
  - Due to limitations in obtaining IPMC software, however, this area has not been fully explored.
  - L1Calo uncertainty in IPMC choice has not helped clarify how to proceed in this area.
  - We are working with both LAPP and CERN IPMCs, possess sufficient LAPP IPMCs for the production run.



Hardware: Shelf Temperatures

FDR Action Item:

Temperature (FPGA and MiniPOD) and power dissipation tests with a Hub carrying a ROD mezzanine in a target ATCA shelf, if possible with all slots populated (e.g. with Hub Test Modules), have to be performed.

❖ FPGA silicon temperatures are measured with a full 14-slot shelf of 12 HTMs, 2 Hub modules and 1 ROD.

• Shelf fan speed set to 6/15 and ambient air used for cooling.

FPGA temperature ---------------->	Hub2		ROD2	
V------------ Configuration Stage	temp C		temp C	
---	---	---	---	---
Hub2 power up with safe foundation	26		--	
Hub2 Config with ibert+ipbus V1.2	46	+20	--	
ROD2 power ON	46		26.5	
Hub2 Turn OFF unused TX	43.5	-2.5	26.5	
Hub2 Define links (DFE ON)	43.5		26.5	
Hub2 Turn DFE OFF all links	42.5	-1	26.5	
ROD2 Config FPGA with Ed's ibert	42.5		54.3	+28
ROD2 Define links (DFE ON)	42.5		54	
ROD2 Turn OFF all TX except R0 Ctrl	42.5		52	-2
ROD2 Turn DFE OFF all links	42.5		49.5	-2.5

Hardware: Shelf Temperatures

- Hub MiniPOD temps are read via IPbus/AXI interface to I2C
  - Temps are quite low, typically around 30C. The Tx MiniPOD is in the Rx MiniPOD shadow, so a bit warmer.
  - NB: Hub and ROD MiniPODs are not on the sensor I2C bus that the IPMC monitors. Rather, they are on an isolated I2C bus accessed via their FPGAs.
    - Thus, while we can read the ROD DCDC supplies and FPGA SysMon, we do not see the ROD MiniPODs directly.

Example read of Hub miniPOD transmitter

```
MiniPod type verified to be: trans_mpod
 Minipod internal temperature is 32.22 C
 The voltage on the 2.5 Vcc power supply is 2.4657 V
 The voltage on the 3.3 Vcc power supply is 3.2596 V
 The serial number of the current device: trans_mpod is : A17285016
 The operating time is 3038.0 hours or 126.583333333 days
 Optical power for channel number trans_mpod is: 0.14646524684 dBm or 1034.3 µW
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 Optical power for channel number trans_mpod is: 1.20080134129 dBm or 1318.5 µW
 The nominal wavelenght for device trans_mpod is 845.0 nm ( ± 15.015  nm)
```

Example read of Hub miniPOD receiver

```
MiniPod type verified to be: recvr_mpod
 Minipod internal temperature is 28.45 C
 The voltage on the 2.5 Vcc power supply is 2.4807 V
 The voltage on the 3.3 Vcc power supply is 3.2876 V
 The serial number of the current device: recvr_mpod is : A1719407F
 The operating time is 3052.0 hours or 127.166666667 days
 Optical power for channel number recvr_mpod is: 0 dBm or 0 µW, is module connected?
 Optical power for channel number recvr_mpod is: 0 dBm or 0 µW, is module connected?
 Optical power for channel number recvr_mpod is: 0 dBm or 0 µW, is module connected?
 Optical power for channel number recvr_mpod is: 0 dBm or 0 µW, is module connected?
 Optical power for channel number recvr_mpod is: 0 dBm or 0 µW, is module connected?
 Optical power for channel number recvr_mpod is: 0 dBm or 0 µW, is module connected?
 Optical power for channel number recvr_mpod is: 0 dBm or 0 µW, is module connected?
 Optical power for channel number recvr_mpod is: 0 dBm or 0 µW, is module connected?
 Optical power for channel number recvr_mpod is: 0 dBm or 0 µW, is module connected?
 Optical power for channel number recvr_mpod is: 0 dBm or 0 µW, is module connected?
 Optical power for channel number recvr_mpod is: 0 dBm or 0 µW, is module connected?
 Optical power for channel number recvr_mpod is: 0 dBm or 0 µW, is module connected?
```

Hardware: Interoperability Tests

FDR Action Item:

Interoperability tests with close to final jFEX and eFEX prototype modules need to be performed. These tests have to done in a full size ATCA shelf with a backplane with the same characteristics as the one to be used in the experiment (ideally with the target shelf). Depending on the availability, interoperability tests with L1Topo should also be performed.

- At the time of this review, the following interoperability tests have been performed on 40G qualified ATCA shelves:
  - FTM:
    - @MSU: IBERT using the Hub clock as input. ROD also present for many tests.
    - These tests have also been performed at RAL and Cambridge.
  - eFEX:
    - @RAL & Cambridge: IBERT using the Hub clock as input. ROD also present for most tests.
  - jFEX:
    - @CERN: IBERT using the Hub clock as input. ROD also present for these tests.
  - L1Topo:
    - No tests performed yet due to availability of hardware. Tests planned for this week.

Summary

- Action items identified during the Hub Final Design Review have been presented.
  - Nearly all items have been addressed
    - Notably there are 3 FDR action items related to the ROD which must be addressed in ROD reviews
  - Performance of Hub + ROD core features in a fully-populated shelf is very encouraging.
    - Excellent BER performance and open eye diagrams
    - FELIX→Hub→HTM clock and TTC/Combined data requirements are met
- Next presentation will cover tests of the Hub prototype modules that extend beyond the scope of the FDR report and further address Hub production readiness.

Backup Slides