FEX System
ATCA Hub Module:
Production Readiness

Hub Team
Michigan State University

10 December 2018

Overview & Goals

❖ Hub PRR Goals:

- Action items identified during FDR will be reviewed.
- Additional tests beyond those identified at FDR will be presented for review.
- Firmware aspects directly impacting hardware function, performance and capability will be presented for review.
- If no hardware issues are identified during the PRR, production PCBs will be scheduled for manufacture.
- If any hardware-sensitive firmware issues are identified during the PRR, a post-PRR review will be scheduled.
- If/when the PRR and any follow-ups are passed, Hub production modules will be assembled.

❖ Today's Presentation Material:

- Previous talk: Introduction and follow-up of FDR action items
- This talk: Review of "beyond FDR" Hub test results & firmware implementation
- Next talk: Hub production schedule and scope

Outline of this Presentation

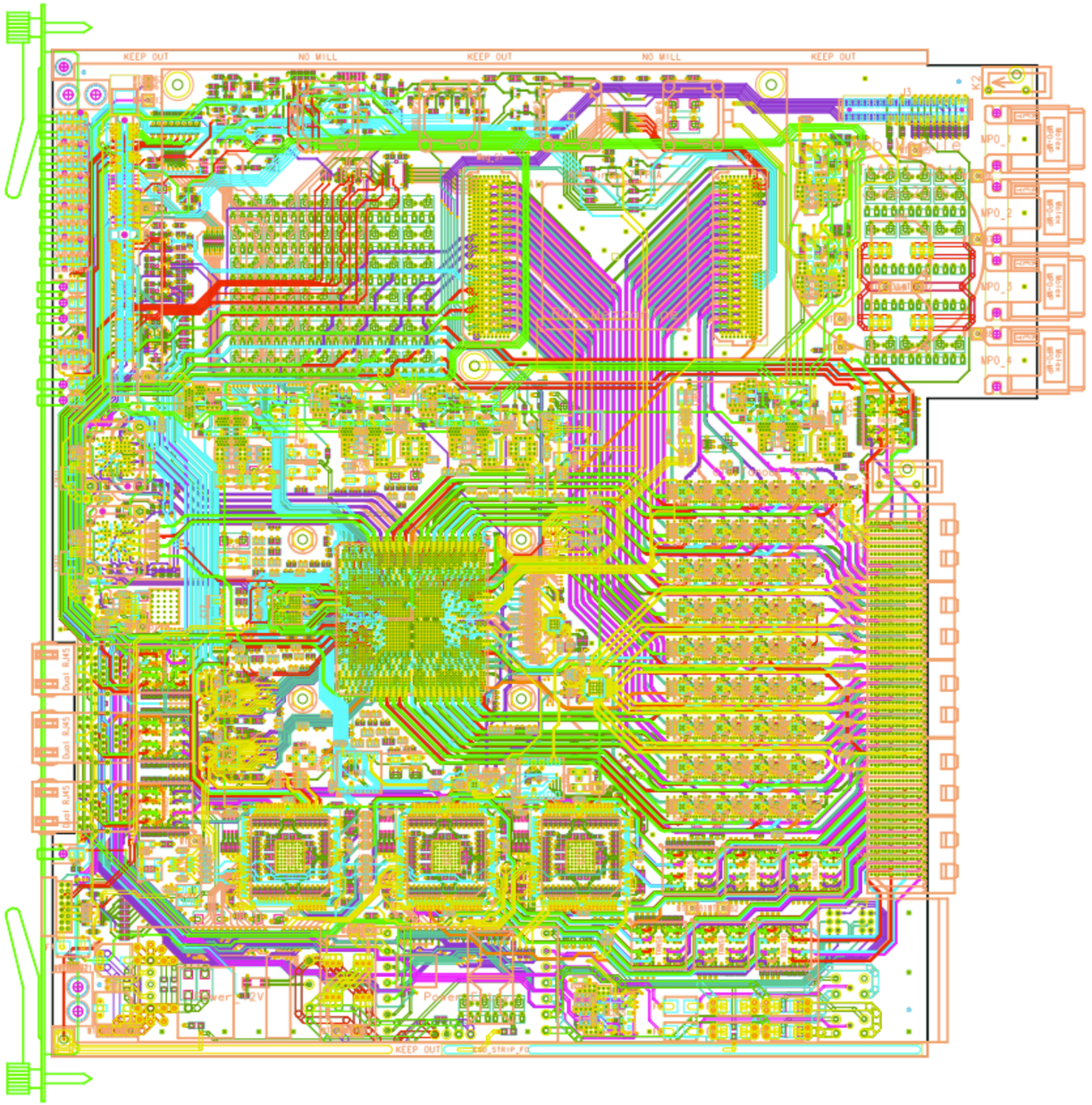
- Overview of tests performed on Hub modules
  - Focus on tests beyond basic input to FDR follow-up
- Core areas of Hub functionality are presented
  - Power and cooling
  - Clock
  - High speed links
  - GbE switch
  - Slow control & monitoring
  - Miscellaneous hardware
  - Firmware

Hub Prototype Card

HUB PCB is a 22 layer IPC* class 2 card, 3.05 mm thick.

IPC, the **Association Connecting Electronics Industries (**initial name: **Institute for Printed Circuits)**

- 10 of the layers are 1/2 oz Ground planes
- 8 of the layers are 1/2 oz signal routing
- 2 of the layers are 1 oz mixed signal/power fills
- 2 of the layers are 1 oz power fills/routing



Hub Prototype Manufacturing

The Hub PCB was manufactured by TTM Technologies
- Same PCB company as gFEX and CMX
- Laminate is Isola FR408HR
- Extra care taken to ensure a reliable design (eg, back drilling instead of blind vias)

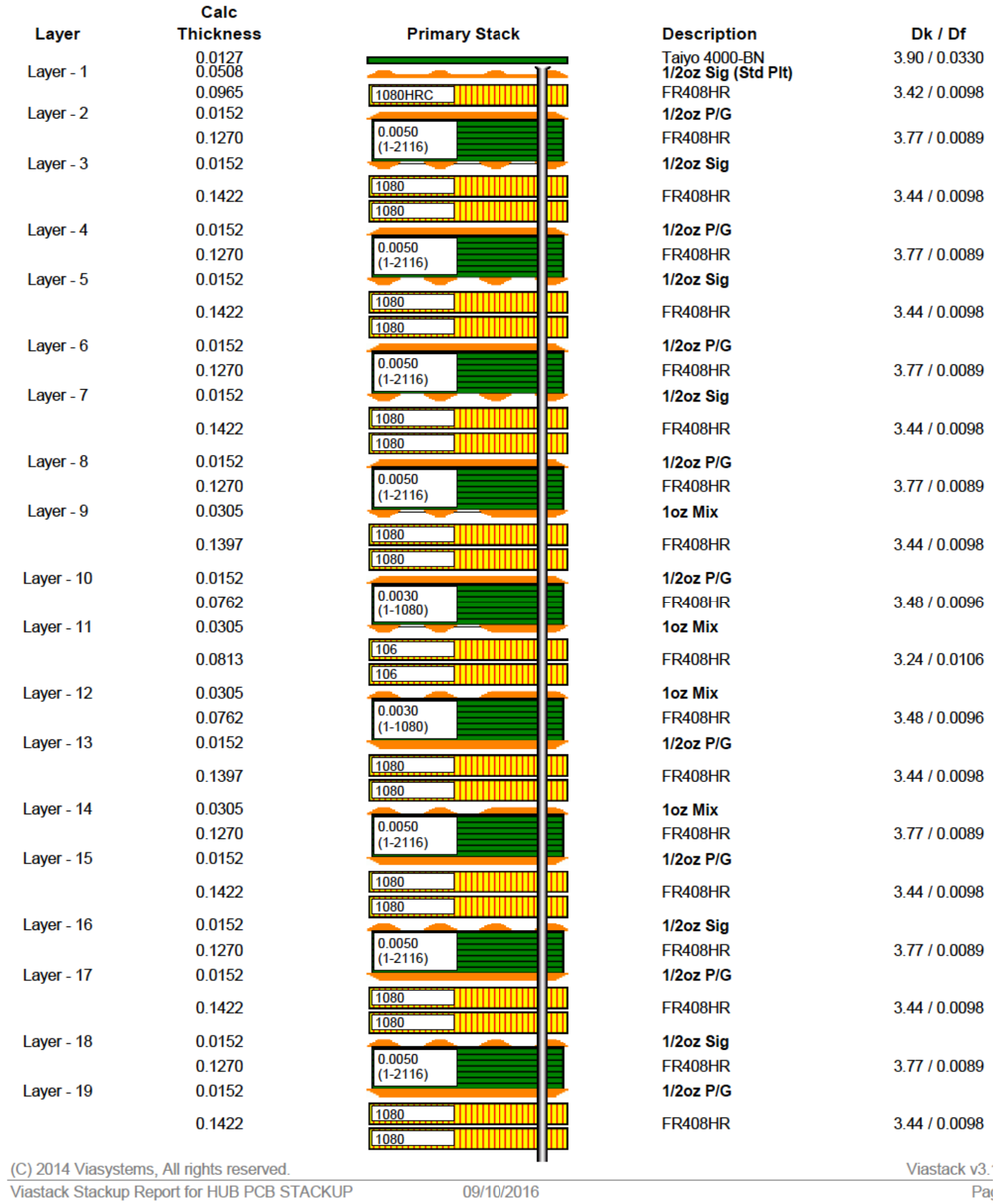
https://www.ttmtech.com/

Hub assembly was performed by Debron Electronics
- Same assembly company as CMX and HTM
- Excellent experience here and we plan to use them for production Hub cards.

http://www.debron-electronics.com/

TTM Technologies

Job Name : HUB PCB STACKUP
Customer : Debron Electronics
Part Num : HUB PCB STACKUP
Part Rev :
Engineer : Gus Trakas



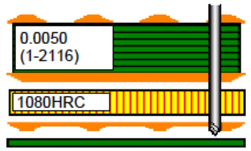
Layer	Calc Thickness	Description	Dk / Df
	0.0127	Taiyo 4000-BN	3.90 / 0.0330
Layer - 1	0.0508	1/2oz Sig (Std Plt)	
	0.0965	FR408HR	3.42 / 0.0098
Layer - 2	0.0152	1/2oz P/G	
	0.1270	FR408HR	3.77 / 0.0089
Layer - 3	0.0152	1/2oz Sig	
	0.1422	FR408HR	3.44 / 0.0098
Layer - 4	0.0152	1/2oz P/G	
	0.1270	FR408HR	3.77 / 0.0089
Layer - 5	0.0152	1/2oz Sig	
	0.1422	FR408HR	3.44 / 0.0098
Layer - 6	0.0152	1/2oz P/G	
	0.1270	FR408HR	3.77 / 0.0089
Layer - 7	0.0152	1/2oz Sig	
	0.1422	FR408HR	3.44 / 0.0098
Layer - 8	0.0152	1/2oz P/G	
	0.1270	FR408HR	3.77 / 0.0089
Layer - 9	0.0305	1oz Mix	
	0.1397	FR408HR	3.44 / 0.0098
Layer - 10	0.0152	1/2oz P/G	
	0.0762	FR408HR	3.48 / 0.0096
Layer - 11	0.0305	1oz Mix	
	0.0813	FR408HR	3.24 / 0.0106
Layer - 12	0.0305	1oz Mix	
	0.0762	FR408HR	3.48 / 0.0096
Layer - 13	0.0152	1/2oz P/G	
	0.1397	FR408HR	3.44 / 0.0098
Layer - 14	0.0305	1oz Mix	
	0.1270	FR408HR	3.77 / 0.0089
Layer - 15	0.0152	1/2oz P/G	
	0.1422	FR408HR	3.44 / 0.0098
Layer - 16	0.0152	1/2oz Sig	
	0.1270	FR408HR	3.77 / 0.0089
Layer - 17	0.0152	1/2oz P/G	
	0.1422	FR408HR	3.44 / 0.0098
Layer - 18	0.0152	1/2oz Sig	
	0.1270	FR408HR	3.77 / 0.0089
Layer - 19	0.0152	1/2oz P/G	
	0.1422	FR408HR	3.44 / 0.0098

Viastack v3.
Viastack Stackup Report for HUB PCB STACKUP 09/10/2016 Pa

TTM Technologies

Layer	Calc Thickness
Layer - 20	0.0152
	0.1270
Layer - 21	0.0152
	0.0965
Layer - 22	0.0508
	0.0127

Primary Stack



Description	Dk / Df
1/2oz Sig	
FR408HR	3.77 / 0.0089
1/2oz P/G	
FR408HR	3.42 / 0.0098
1/2oz Sig (Std Plt)	
Taiyo 4000-BN	3.90 / 0.0330

|| Through

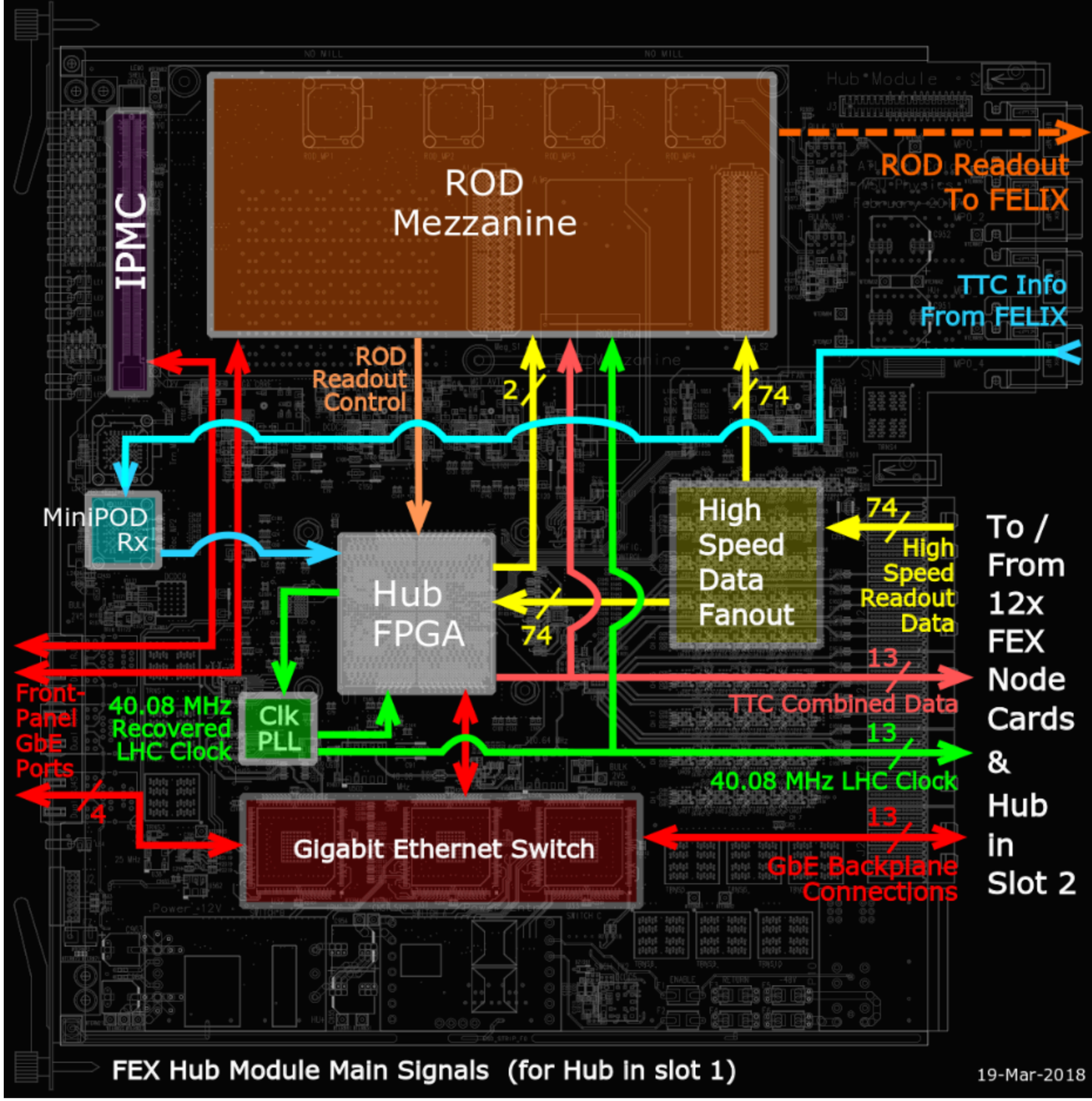
Materials: Isola FR408HR High Speed High-Tg FR4

Requirement	Req. Thickness	Tol +	Tol -	Calc Thick
Incl. Plating & Mask	3.0505	0.3048	0.3048	3.0683
Incl. Mask over Laminate	2.9489	0.2946	0.2946	2.9667
Incl. Plating	3.0251	0.3023	0.3023	3.0429
After Lamination	2.9540	0.1473	0.1473	2.9718
Over Laminate	2.9235	0.2921	0.2921	2.9413

Impedance Type	Layer	Design	Actual	Pitch	Plane	tpd ps Atten	Rdc Rac	L ph C pf	Target	Tol (ohms)	Predict
1 EC Microstrip	L1	0.14000	0.14500	0.40000	-	141.7	0.062	7660	100	10.0	99.88
	-	0.14000	0.14500	-	L2	0.34	-	2.6			
2 EC Stripline	L3	0.14000	0.13000	0.40000	L2	159.5	0.232	8145	100	10.0	100.34
	-	0.14000	0.13000	-	L4	0.37	-	3.1			
3 EC Stripline	L5	0.14000	0.13000	0.40000	L4	159.5	0.232	8145	100	10.0	100.34
	-	0.14000	0.13000	-	L6	0.37	-	3.1			
4 EC Stripline	L7	0.14000	0.13000	0.40000	L6	159.5	0.232	8145	100	10.0	100.34
	-	0.14000	0.13000	-	L8	0.37	-	3.1			
5 EC Stripline	L9	0.14000	0.12500	0.40000	L8	158.4	0.128	8052	100	10.0	99.70
	-	0.14000	0.12500	-	L10	0.36	-	3.1			
6 EC Stripline	L14	0.14000	0.12500	0.40000	L13	158.4	0.128	8052	100	10.0	99.70
	-	0.14000	0.12500	-	L15	0.36	-	3.1			
7 EC Stripline	L16	0.14000	0.13000	0.40000	L15	159.5	0.232	8145	100	10.0	100.34
	-	0.14000	0.13000	-	L17	0.37	-	3.1			
8 EC Stripline	L18	0.14000	0.13000	0.40000	L17	159.5	0.232	8145	100	10.0	100.34
	-	0.14000	0.13000	-	L19	0.37	-	3.1			
9 EC Stripline	L20	0.14000	0.13000	0.40000	L19	159.5	0.232	8145	100	10.0	100.34
	-	0.14000	0.13000	-	L21	0.37	-	3.1			
10 EC Microstrip	L22	0.14000	0.14500	0.40000	L21	141.7	0.062	7660	100	10.0	99.88
	-	0.14000	0.14500	-	-	0.35	-	2.6			

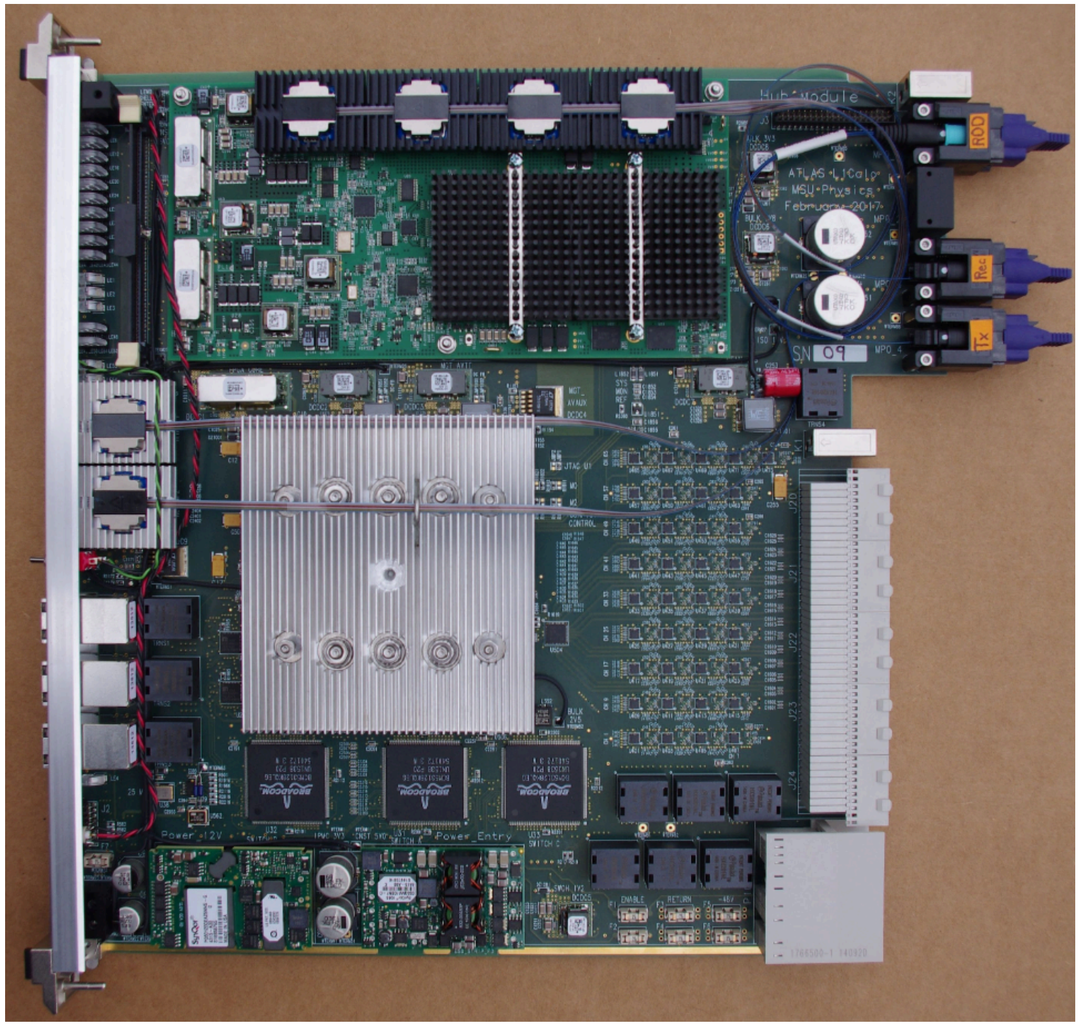
Board Layout

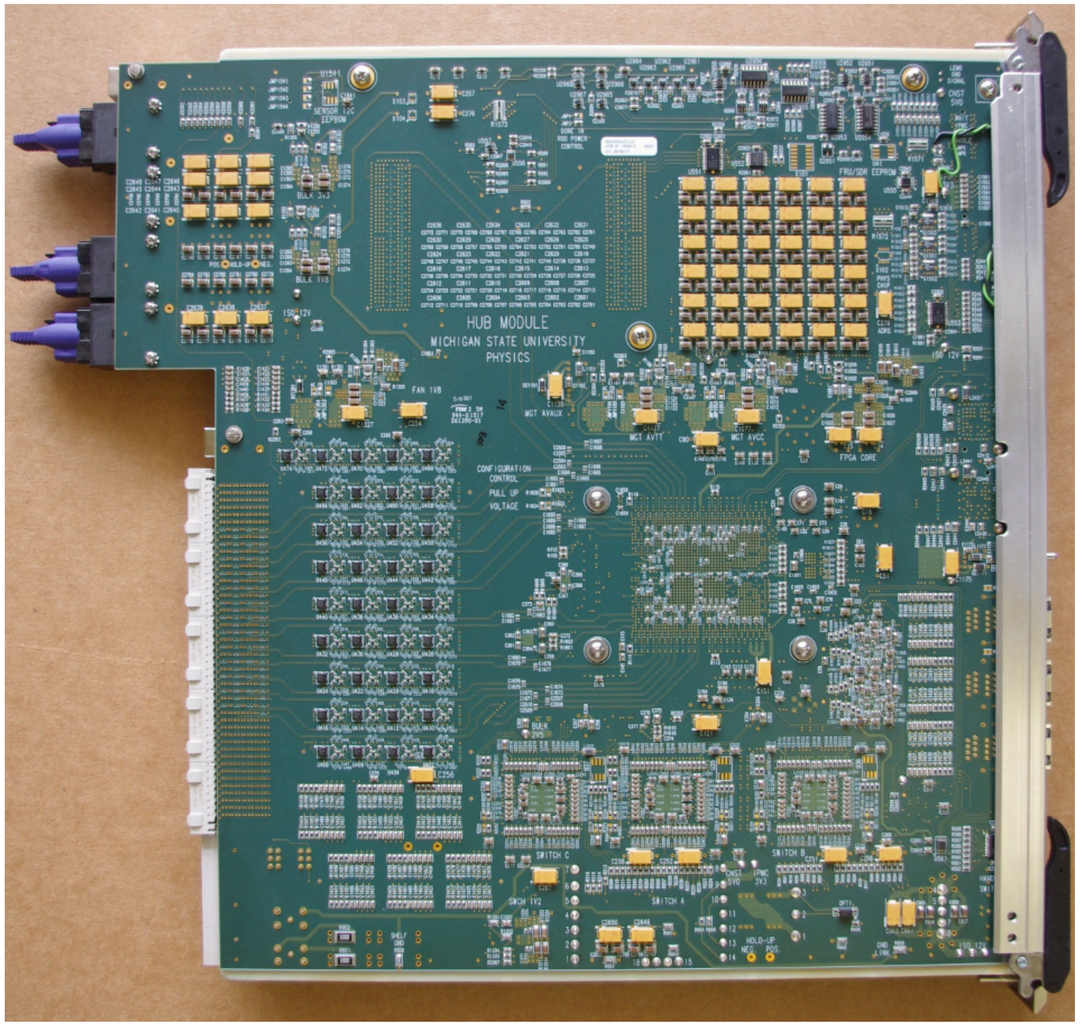
- Core functions of the Hub hardware
  1) Host the ROD Mezzanine
  2) Receives Zone-2 FEX readout data and provide to the ROD
  3) Distribute LHC master clock to FEX, Hub and ROD modules
  4) Distribute TTC and ROD control data to FEX, Hub and ROD modules
  5) Provide Ethernet switch for the ATCA shelf via the Base Interface



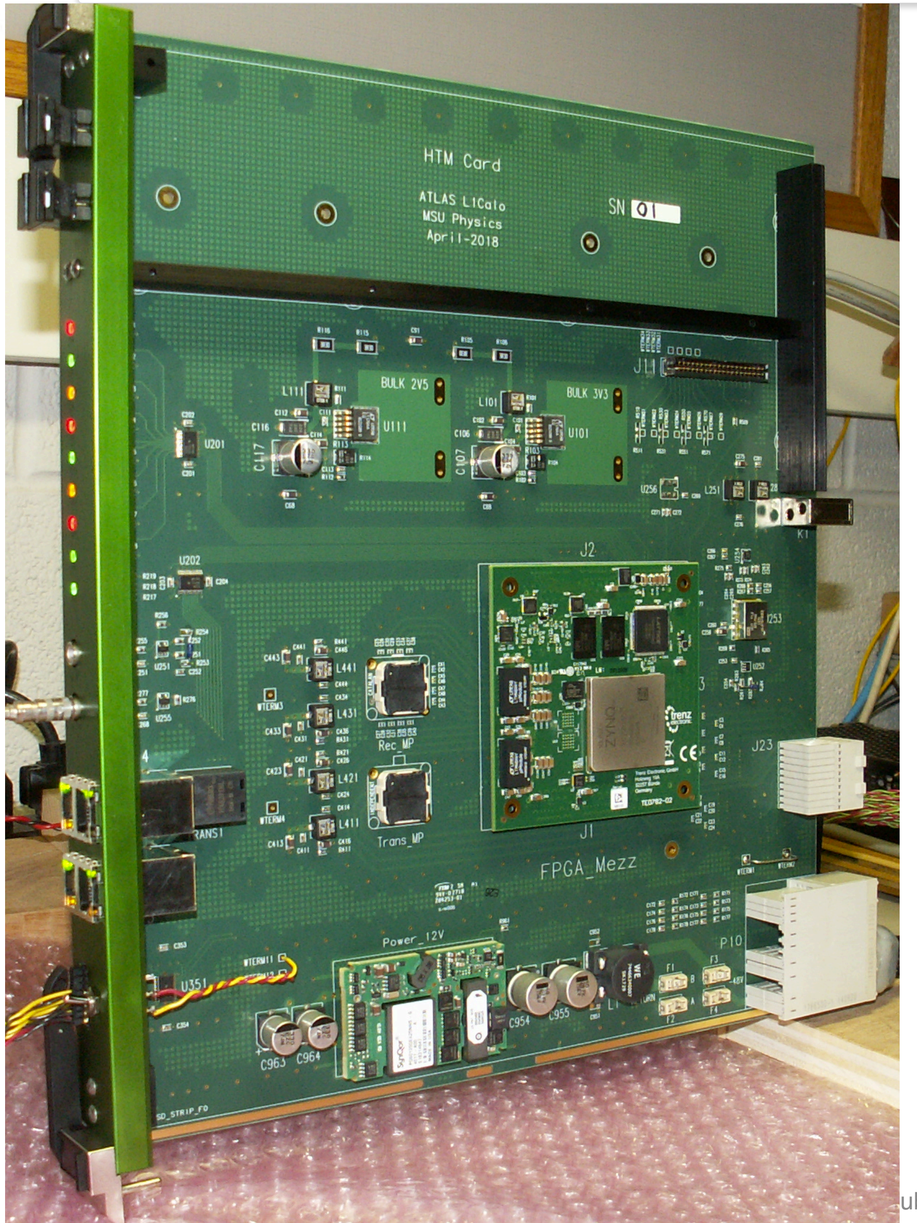
Prototype Hub Modules

- 9 Hub prototypes were build (8 with FPGAs)
  - Here: Hub S/N 09 with ROD and optical cabling included to illustrate final installation assembly.





Hub Test Module



- Hub Test Module (HTM) designed to allow full system tests far in advance of a full shelf of FEX/FTM cards
  - Developed at MSU. 20 cards delivered July 2018.
- HTM design specifics
  - ATCA form factor, 10 layer board
  - Hosts a commercial mezzanine card with a 7-series Zynq
  - Receives Hub TTC & clock via Zone-2
  - Sources 6 lanes of “FEX” data to each Hub slot, up to 10.26 Gbps
  - Optional MiniPods to emulate all Hub/ROD optical interfaces
  - Connections to both Hub GbE networks

TTM Technologies

Viasystems Technologies Corp. LLC
8150 Sheppard Ave E
Toronto, ON, M1B 5K2

Job Name : 181875
Customer : DEBRON INDUSTRIAL ELECTRONICS
Part Num : 40-00643-00LF
Part Rev : -
Engineer : Yogi Perin

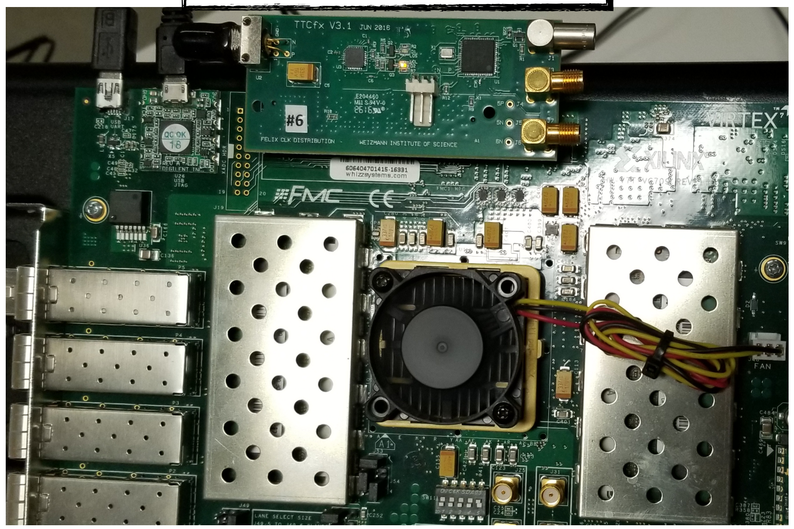
Layer	Cust Thickness	Calc Thickness	Primary Stack	Description	Dk / Df
		0.0005		Taiyo 4000-HFX DI	3.50 / 0.0190
Layer - 1		0.0020		**1/2oz Mix (Std Plt)**	
		0.0038	1080 - 71%	FR408HR	3.42 / 0.0098
Layer - 2		0.0006		**1/2oz P/G**	
		0.0100	0.0100 (2-2116)	FR408HR	3.69 / 0.0089
Layer - 3		0.0006		**1/2oz Sig**	
		0.0040	3313 - 63%	FR408HR	3.48 / 0.0096
Layer - 4		0.0006		**1/2oz P/G**	
		0.0210	0.0210 (2-2116/2-1652)	FR408HR	3.79 / 0.0086
Layer - 5		0.0012		**1oz Mix**	
		0.0034	3313 - 63%	FR408HR	3.48 / 0.0096
Layer - 6		0.0012		**1oz Mix**	
		0.0210	0.0210 (2-2116/2-1652)	FR408HR	3.79 / 0.0086
Layer - 7		0.0006		**1/2oz P/G**	
		0.0040	3313 - 63%	FR408HR	3.48 / 0.0096
Layer - 8		0.0006		**1/2oz Sig**	
		0.0100	0.0100 (2-2116)	FR408HR	3.69 / 0.0089
Layer - 9		0.0006		**1/2oz P/G**	
		0.0038	1080 - 71%	FR408HR	3.42 / 0.0098
Layer - 10		0.0020		**1/2oz Mix (Std Plt)**	
		0.0005		Taiyo 4000-HFX DI	3.50 / 0.0190

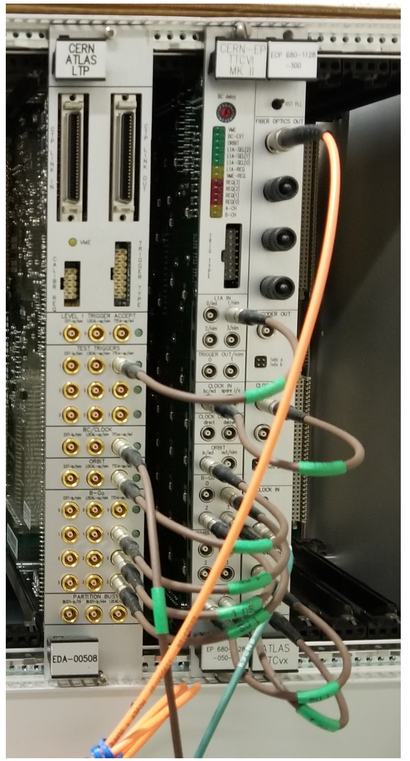
Materials: Isola FR408HR High Speed High-Tg FR4

MSU Test Stands

- MSU has two Hub/HTM test stands available for system tests
  - 14 slot ATCA shelf (40G qualified), primarily used for bandwidth tests. Shown here with 12 HTM cards.
  - 6 slot ATCA shelf (40G qualified), primarily used for firmware development.
- System test capabilities
  - VME TTC system providing 40.08 MHz master clock, L1A, ECR, BCR, etc.
  - FELIX functions via TTCfx v3.1 mezzanine on VC709 Xilinx dev board.
  - Optical connections between HTMs and Hub/ROD cards
  - Full backplane link population with 8 lanes to/from each slot
  - 16 PCs to source & sink GbE throughput tests

TTCfx v3.1 + VC709





TTCvi
TTCvx
***Modified to deliver 40.08 MHz clock**

Hub Testing Status

- MSU has fully assembled 8 Hub modules. Delivered 24 May 2017, ready for testing 16 June 2017.
  - All modules were fully tested on the bench and with all available HW here at MSU
    - This includes RODs, FTM, HTMs. The availability of each varied over time.
  - 2 modules were sent to Cambridge before we had ROD or FTM (S/N 02, 03). Used in ROD/FTM/eFEX tests since then.
  - 1 module was sent to CERN (S/N 09), mated with ROD (S/N 04), fully tested with FTM.
  - 5 modules at MSU, all tested with full shelf of HTMs since August 2017.

- Between 14-slot and 6-slot shelves we now have 4 months straight rotating 5 Hubs in operation here at MSU (ignoring the 3 modules in EU)
  - No ROD or Hub MGT link errors observed that were not associated with known HTM issues.
  - GbE switch has been thoroughly tested for throughput, packet loss, errors

- FYI: Hub sent to CERN was damaged when someone dropped it.
  - Front-panel alignment pin was broken off.
  - Hub S/N 09 now back at MSU and is going through retesting (all looks great so far)
  - These are potentially expensive mistakes.

Hub Test Overview

Example text from Hub Test Plan.
Full test scope posted on agenda.

Detailed list of acceptance tests:

Category: MGT Link Tests

1. Verify that the 13 Equalization Group Enable Signals are all working OK and routed to the correct sets of MGT Fanout Chips.
2. Verify that the 4 MiniPOD Receiver MGT channels and the 8 MiniPOD Transmitter MGT channels are all working OK.
3. Verify that the Hub FPGA can receive 6 lanes of MGT data from all 12 of the FEX slots.
4. Verify that the Hub can receiver 6 lanes of MGT data from all 12 of the FEX slots and correctly pass this data to the ROD.
5. Verify that the Hub FPGA can send out Combined Data to the 12 FEX slots, to the ROD on This Hub, and to the Other Hub.
6. Verify that This Hub can Receive Combined Data that was sent out by the Other Hub.
7. Verify that This Hub can Receive the Readout Control data that was sent out by the ROD on This Hub.
8. Verify that This Hub can send out two lanes of Readout data to the Other Hub.
9. Verify that This Hub can Receive two lanes of Readout data from the Other Hub.
10. Verify that This Hub can Receive and correctly pass to its ROD one lane of readout data from the Other Hub.
11. Verify that the FPGA on This Hub can send one lane of its readout data to the ROD on This Hub

Category: Power Supplies and Hub Component Cooling Tests

1. During MSU Final Assembly and Bench Testing

Power and Cooling Tests

Power Supplies & Component Cooling

✔ 1. During MSU Final Assembly and Bench Testing
   a. Verify (measure) 11 power supply output voltages and 7 power supply output currents while the FPGA is configured with test firmware.
   b. The 7 DCDC Converters on each Hub are tested and setup for: Vin_On, Vin_Off, Vout_Margin_High, Vout_Margin_Low, and Vout_Scale_Loop.

✔ 2. Verify that the I2C PMBus monitoring of the 7 DCDC Converter output voltages and currents is working OK by reading them from the Front Panel I2C Bus connector. The intent is to verify that the IPMC has access to this data.

✔ 3. Verify that the FPGA's System Monitor reads out correct data for the Si Temperature, 1V8 Aux power, and 0V95 Core power.

✔ 4. Verify the sequencing and ramp rate for at least two of the power supply voltages, e.g. DC/DC-1 FPGA_Core, DC/DC-5 SWCH_1V2, and DC/DC-8 Bulk_3V3.

✔ 5. Verify that the board power enable circuit, the board start-up reset circuit and the two front panel board power status LEDs are all working correctly.

✔ 6. Verify the expected Hub FPGA Si Temperature with the Hub running in the Shelf with standard air flow rate and the highest wattage FPGA firmware that we have available (currently about 38 Watts).

✔ 7. Verify that the expected operating temperature is readout from the two MiniPODs via their control/monitoring serial bus connection to the Hub FPGA.

✔ Done on all cards ✔ Done on 1-7 cards

Power & Resource Estimates

Load firmware designed to push DCDC supplies close to operating conditions.

- All available MGTs operating IBERT IP core and also IPbus firmware
  - Power consumption estimated at 38W.
  - Note: this version requires less than ~25% of FPGA fabric resources, which is useful for a simple extrapolation on the next pages

Utilization Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	195922	716160	27.36
LUTRAM	6361	154560	4.12
FF	347658	1432320	24.27
BRAM	431.50	2520	17.12
DSP	160	1200	13.33
IO	127	416	30.53
GT	80	80	100.00
BUFG	420	1200	35.00
MMCM	4	20	20.00

Power **Summary** | On-Chip

Total On-Chip Power:	**37.608 W**
Junction Temperature:	**55.2 °C**
Thermal Margin:	44.8 °C (52.3 W)
Effective θJA:	0.8 °C/W
Power supplied to off-chip devices:	0.002 W
Confidence level:	Low

Implemented Power Report

Power Consumption & Cooling

Power consumption is well within design capacity

- Total power consumption for maximum usage is 71W (FPGA:38W, GbE/Fanout:25.1W, MiniPOD/Clk:8.2W)
  - We could be pushing the switch harder in these tests, but it cannot dissipate more than a few Watts.
- Hub supply capacity is 300W
  - 100W reserved for ROD, 200W reserved for Hub

Cooling design is adequate

- Hub FPGA silicon temps are at ~45C for the full IBERT FW load.
- ROD FPGA silicon temps are at ~54C for the full IBERT FW load.
- Shelf fan speed set at ~40% of maximum

FPGA silicon temperatures measured with a full 14-slot shelf of 12 HTMs, 2 Hub modules and 1 ROD.

FPGA temperature ---------------->	Hub2		ROD2	
V------------ Configuration Stage	temp C		temp C	
---	---	---	---	---
Hub2 power up with safe foundation	26		--	
Hub2 Config with ibert+ipbus V1.2	46	+20	--	
ROD2 power ON	46		26.5	
Hub2 Turn OFF unused TX	43.5	-2.5	26.5	
Hub2 Define links (DFE ON)	43.5		26.5	
Hub2 Turn DFE OFF all links	42.5	-1	26.5	
ROD2 Config FPGA with Ed's ibert	42.5		54.3	+28
ROD2 Define links (DFE ON)	42.5		54	
ROD2 Turn OFF all TX except RO Ctrl	42.5		52	-2
ROD2 Turn DFE OFF all links	42.5		49.5	-2.5

Power Consumption & Cooling

DCDC supplies all have acceptable margin

- Hub FPGA consumes ~38W with IBERT FW design (*prediction was 38W*)
- **Core 0.95V supply** draws 8A using ~25% of fabric resources. Final Hub FW design anticipated to use <50% of fabric resources, so margin is good (>50% margin).
- **MGT rail supply** margins are adequate (36% margin for AVTT). Note, this is all the MGTs we *can* use, so it cannot increase substantially.
- **Fanout chips** consume 21.8W (~40% margin).

Converter	FPGA_ CORE	MGT_ AVCC	MGT_ AVTT	SWCH _1V2	BULK _1V8	FAN_ 1V8	BULK_ 3V3
Voltage	0.95 V	1.00 V	1.20 V	1.20 V	1.80 V	1.80 V	3.3 V
Draw	8.04 A	9.38 A	12.7 A	1.94 A	0.62 A	12.1 A	2.25 A
Capacity	40 A	20 A	20 A	12 A	12 A	20 A	12 A

MiniPOD Temperatures

- Hub MiniPOD temps are read via IPbus/AXI interface to I2C
  - Temps are quite low, typically around 30C. The Tx MiniPOD is in the Rx MiniPOD shadow, so a bit warmer.
  - NB: Hub and ROD MiniPODs are not on the sensor I2C bus that the IPMC sees. Rather, they are on an isolated I2C bus accessed via their FPGAs.
    - Thus, while we can read the ROD DCDC supplies, we do not see the ROD MiniPODs directly.

Example read of Hub miniPOD transmitter

```
MiniPod type verified to be: trans_mpod
Minipod internal temperature is 32.22 C
The voltage on the 2.5 Vcc power supply is 2.4657 V
The voltage on the 3.3 Vcc power supply is 3.2596 V
The serial number of the current device: trans_mpod is : A17285016
The operating time is 3038.0 hours or 126.583333333 days
Optical power for channel number trans_mpod is: 0.14646524684 dBm or 1034.3 µW
Optical power for channel number trans_mpod is: 0.911039440903 dBm or 1233.4 µW
Optical power for channel number trans_mpod is: -0.00130307891732 dBm or 999.7 µW
Optical power for channel number trans_mpod is: 1.06496870139 dBm or 1277.9 µW
Optical power for channel number trans_mpod is: 0.137217780511 dBm or 1032.1 µW
Optical power for channel number trans_mpod is: 1.09646031091 dBm or 1287.2 µW
Optical power for channel number trans_mpod is: 0.152759066819 dBm or 1035.8 µW
Optical power for channel number trans_mpod is: 1.0510124455 dBm or 1273.8 µW
Optical power for channel number trans_mpod is: -0.220935723629 dBm or 950.4 µW
Optical power for channel number trans_mpod is: 1.3165073809 dBm or 1354.1 µW
Optical power for channel number trans_mpod is: 0.262471814778 dBm or 1062.3 µW
Optical power for channel number trans_mpod is: 1.20080134129 dBm or 1318.5 µW
The nominal wavelenght for device trans_mpod is 845.0 nm ( ± 15.015  nm)
```

Example read of Hub miniPOD receiver

```
MiniPod type verified to be: recvr_mpod
Minipod internal temperature is 28.45 C
The voltage on the 2.5 Vcc power supply is 2.4807 V
The voltage on the 3.3 Vcc power supply is 3.2876 V
The serial number of the current device: recvr_mpod is : A1719407F
The operating time is 3052.0 hours or 127.166666667 days
Optical power for channel number recvr_mpod is: 0 dBm or 0 µW, is module connected?
Optical power for channel number recvr_mpod is: 0 dBm or 0 µW, is module connected?
Optical power for channel number recvr_mpod is: 0 dBm or 0 µW, is module connected?
Optical power for channel number recvr_mpod is: 0 dBm or 0 µW, is module connected?
Optical power for channel number recvr_mpod is: 0 dBm or 0 µW, is module connected?
Optical power for channel number recvr_mpod is: 0 dBm or 0 µW, is module connected?
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Optical power for channel number recvr_mpod is: 0 dBm or 0 µW, is module connected?
```
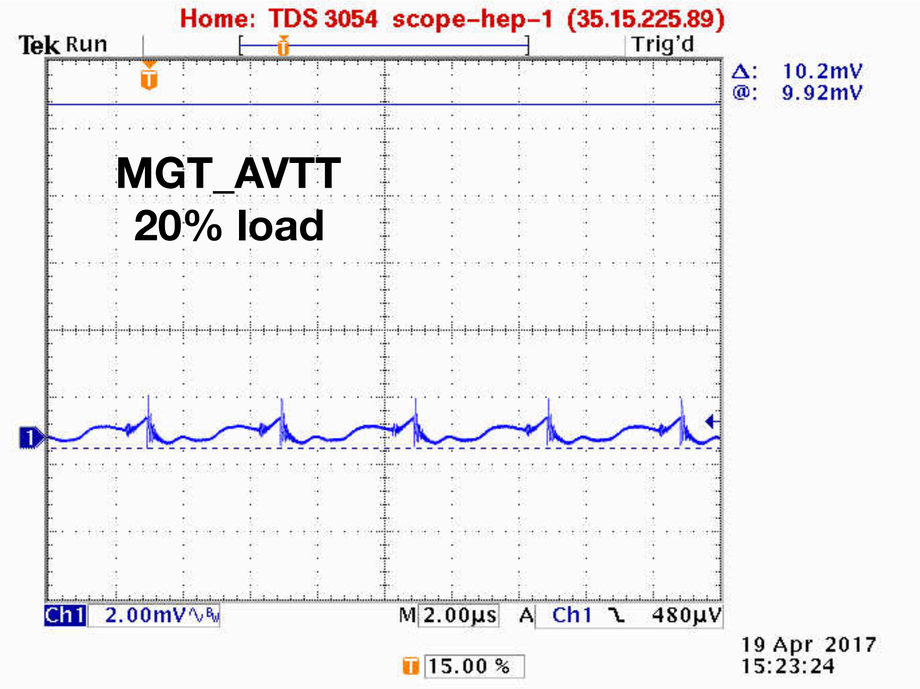
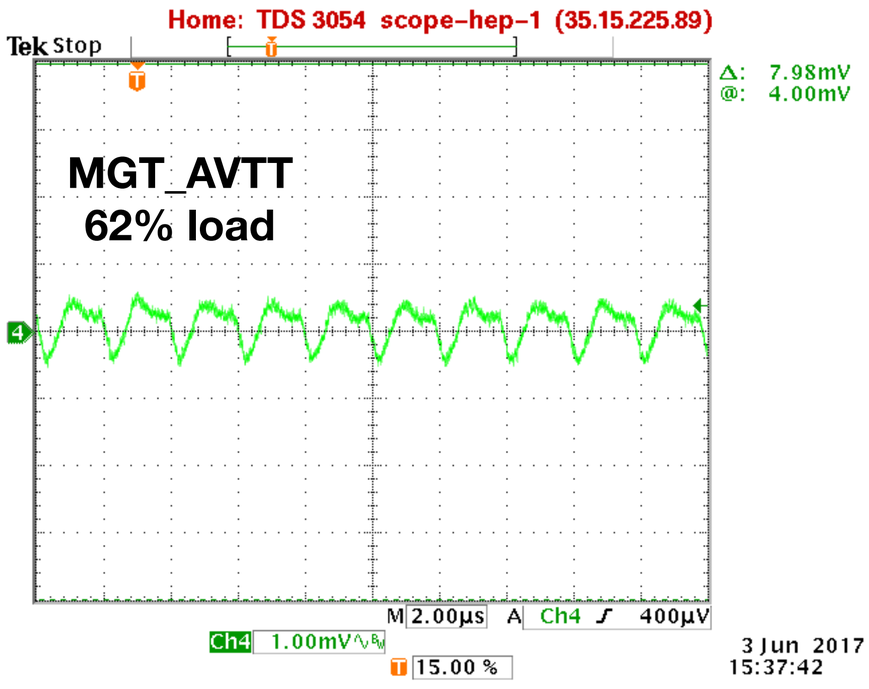

Power Supply Stability

- Hub power supplies are trimmed and checked for accuracy at final assembly on the bench.
  - Critical Ultrascale supplies have a 3% voltage tolerance, and MGT supplies specify noise < 10 mV pk-pk.
  - The DCDC converters have required very little voltage trimming.
  - Multiple ceramic, low ESR tantalum and polymer capacitors are used to ensure stiff supply structures over a wide bandwidth.
  - The MGT_AVTT/AVCC and FAN_1V8 DCDC supplies also include external LC output filters.
  - +12V power feed to the ROD includes a large bank of filter bypass capacitors to minimize input power noise.





Clock Tests

Clock Tests

✔ 1. Verify that the 25.0 MHz and 40.0787 MHz oscillators are running at the correct frequency and are stable.

✔ 2. Verify the 40.0787 and 320.6296 MHz PLLs have the correct LHC frequency tracking range.

✔ 3. Verify both sides of the First 40 MHz Fanout to the: Hub FPGA, ROD, 320 MHz PLL, and Second 40 MHz Fanout.

✔ 4. Verify both sides of the 13 outputs from the Second 40 MHz Fanout: 12 to the FEXs and 1 to Other Hub.

✔ 5. Verify both sides of the outputs from the 320 MHz Fanout: 8 connections to MGT Reference Inputs and 1 Logic Clock to the Hub FPGA.

✔ 6. Verify that when operated as the Other Hub (i.e. the Hub that does not directly receive an optical TTC signal from FELIX), that the Hub card can correctly receive its LHC Reference Clock from the backplane.

✔ 7. Verify that the Hub handles a frequency/phase shift in a manner that allows the recipients of the distributed clock (FEX and ROD) to remain locked and smoothly transition during the clock-change process.

✔ Done on all cards ✔ Done on 1-7 cards

Clock Bench Tests

Two primary tests:

- Verify all Hub clocks are at the correct frequency, clean and arrive at their destinations

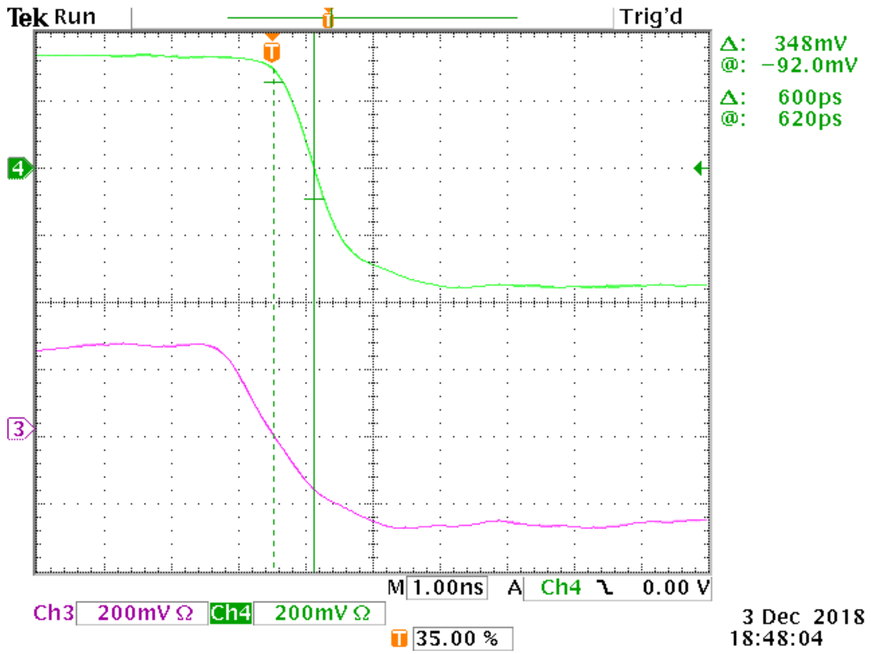
- Verify that the Hub clock circuit is stable during the known frequency sweep of the input master LHC clock.
  - The fastest frequency sweep in the LHC RF system is 22 Hz/sec
  - The Hub PLL phase shift for a (up to) 22kHz/sec frequency sweep is 3 degrees, so LHC frequency sweep is ~ 1ps of phase shift.
  - The Hub PLL will “re-lock” following a discontinuous change in clock frequency or phase.
    - The Hub PLL will follow discontinuous changes smoothly and relic without FPGA logic or MGTs needing to take further action.

Clock Shelf Tests

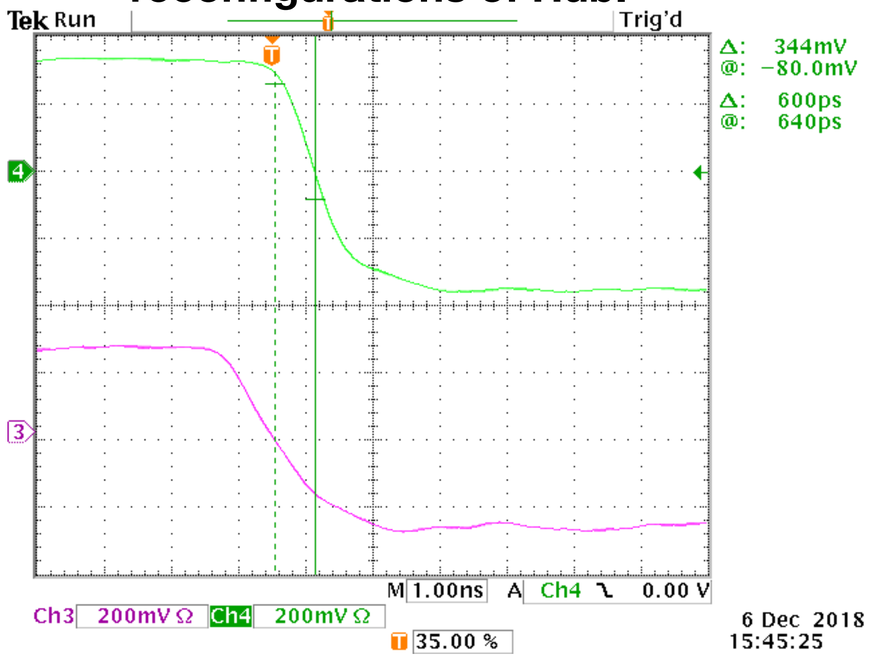
As described in previous presentation, we also carefully study the stability of the latency of the LHC master clock in the shelf.

- Full path from VME/TTC to HTM front panel.
  - Green: ECL clock from TTC crate
  - Magenta: CMOS clock from HTM front panel

Initial Reference



Test 3 days later after random resets, reconfigurations of Hub.



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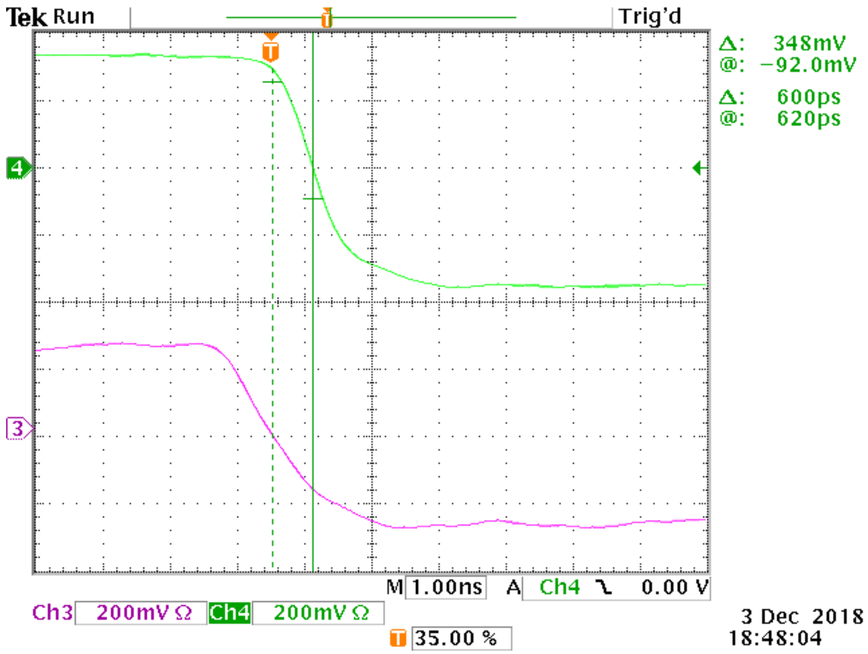

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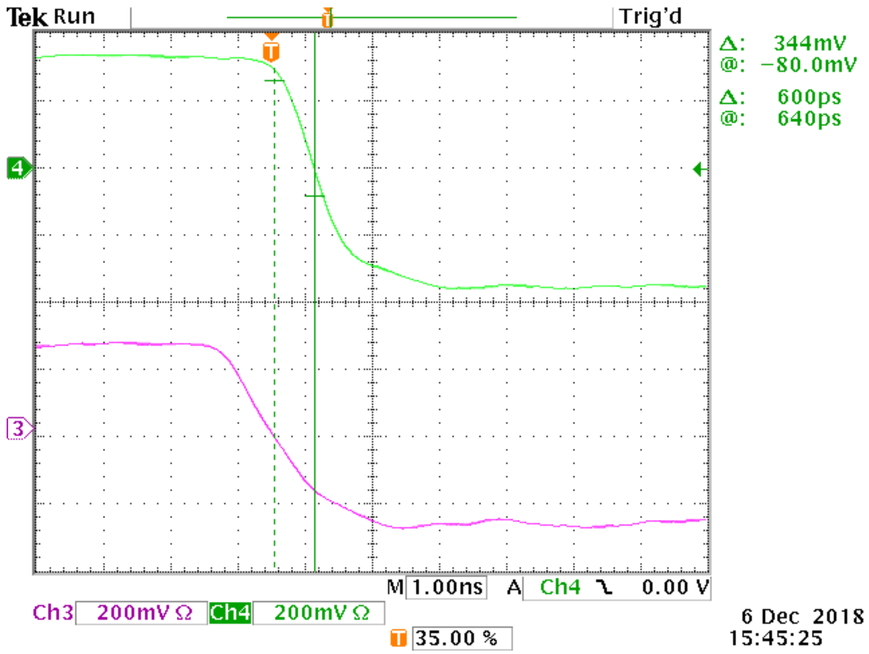


High Speed Link Tests

MGT Link Testing

✔ 1. Verify that the 13 Equalization Group Enable Signals are all working OK and routed to the correct sets of MGT Fanout Chips.

✔ 2. Verify that the 4 MiniPOD Receiver MGT channels and the 8 MiniPOD Transmitter MGT channels are all working OK.

✔ 3. Verify that the Hub FPGA can receive 6 lanes of MGT data from all 12 of the FEX slots.

✔ 4. Verify that the Hub can receiver 6 lanes of MGT data from all 12 of the FEX slots and correctly pass this data to the ROD.

✔ 5. Verify that the Hub FPGA can send out Combined Data to the 12 FEX slots, to the ROD on This Hub, and to the Other Hub.

✔ 6. Verify that This Hub can Receive Combined Data that was sent out by the Other Hub.

✔ 7. Verify that This Hub can Receive the Readout Control data that was sent out by the ROD on This Hub.

✔ 8. Verify that This Hub can send out two lanes of Readout data to the Other Hub.

✔ 9. Verify that This Hub can Receive two lanes of Readout data from the Other Hub.

✔ 10. Verify that This Hub can Receive and correctly pass to its ROD one lane of readout data from the Other Hub.

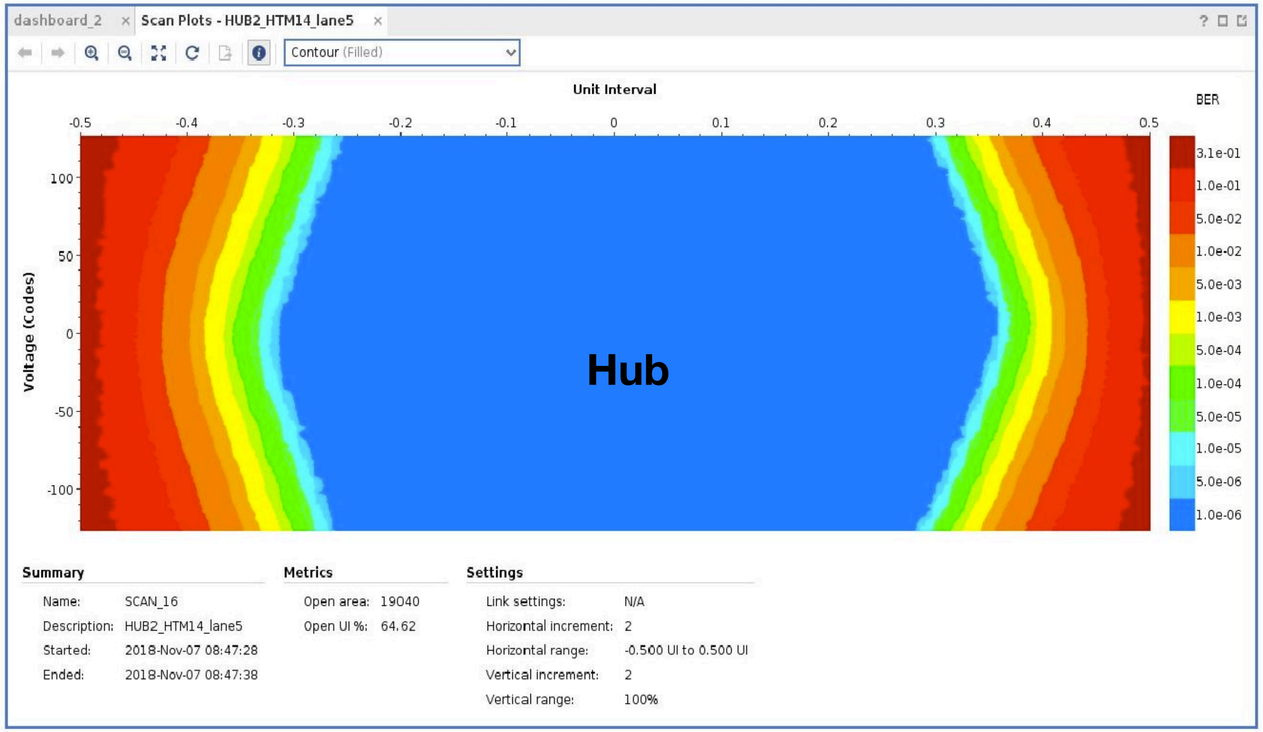
✔ 11. Verify that the FPGA on This Hub can send one lane of its readout data to the ROD on This Hub.

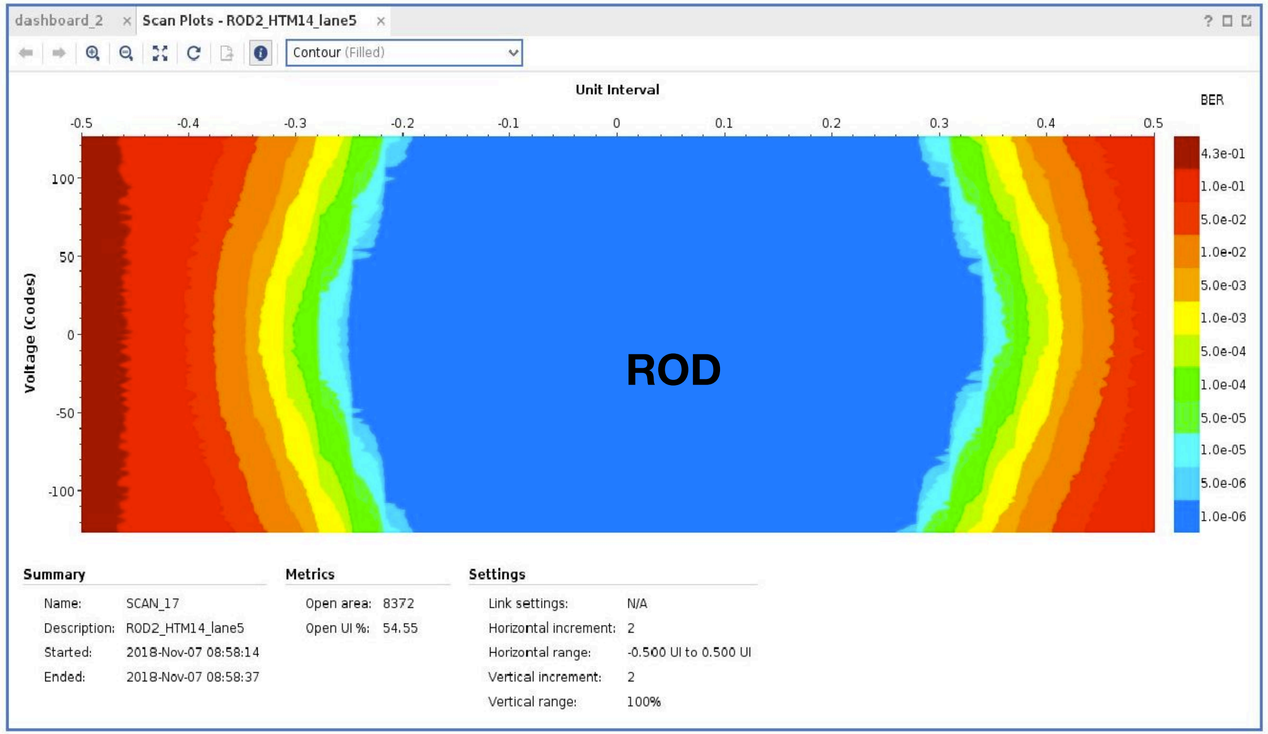
✔ Done on all cards ✔ Done on 1-7 cards

Hardware: Backplane Link Testing

- BER tests have been performed with Xilinx IBERT firmware at a line rate of 6.4 Gbps and using PRBS31
  - Two separate, long-duration runs have been performed and find the full system capable of **BER<6E-17**. No errors observed.
  - Eye diagrams have been produced for both Hub and ROD data links. <u>They all look very good.</u>

Hub Slot 2, HTM Module 14, Data Lane 5: DFE off, Fanout Eq on





A quick aside…

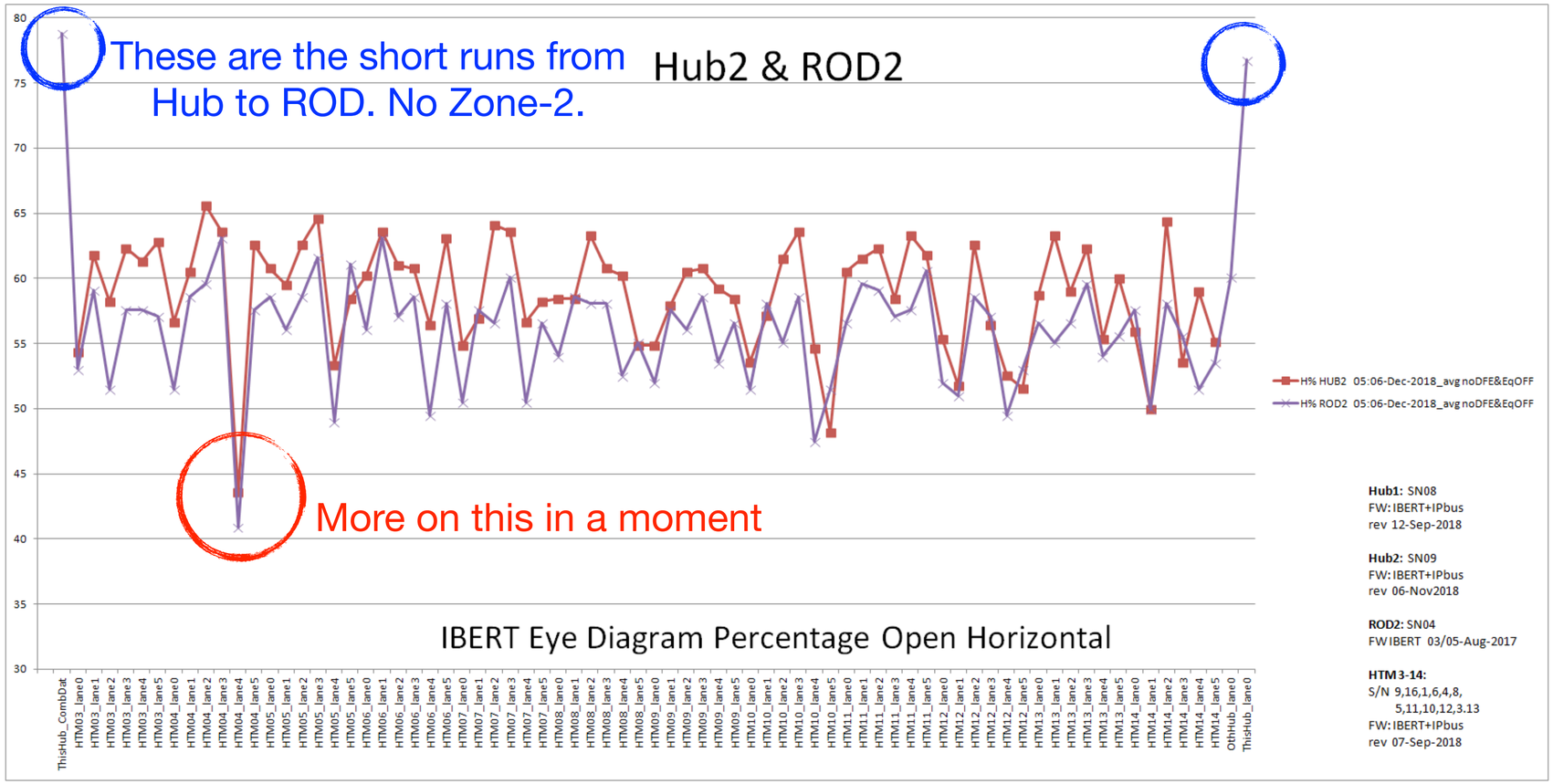
- During our MGT tests, we study the effects of equalization methods available on the Hub
  1) Decision Feedback Equalization (DFE), which is a feature of the Xilinx MGT receiver. This is the more power hungry of the options they provide. This appears to try to be a good general tool for many applications.

  2) Equalization in the Hub FEX data fanout buffers. This is designed to work well for copper signal paths, as we have on the Hub. This can be turned on or off for all lanes of data from a given FEX (HTM).

- While we do not need to rely upon these for good signal integrity, our goal has been to comprehensively understand the degrees of freedom in the problem.
  - Our effort here is not to gain margin, but rather to characterize the board.

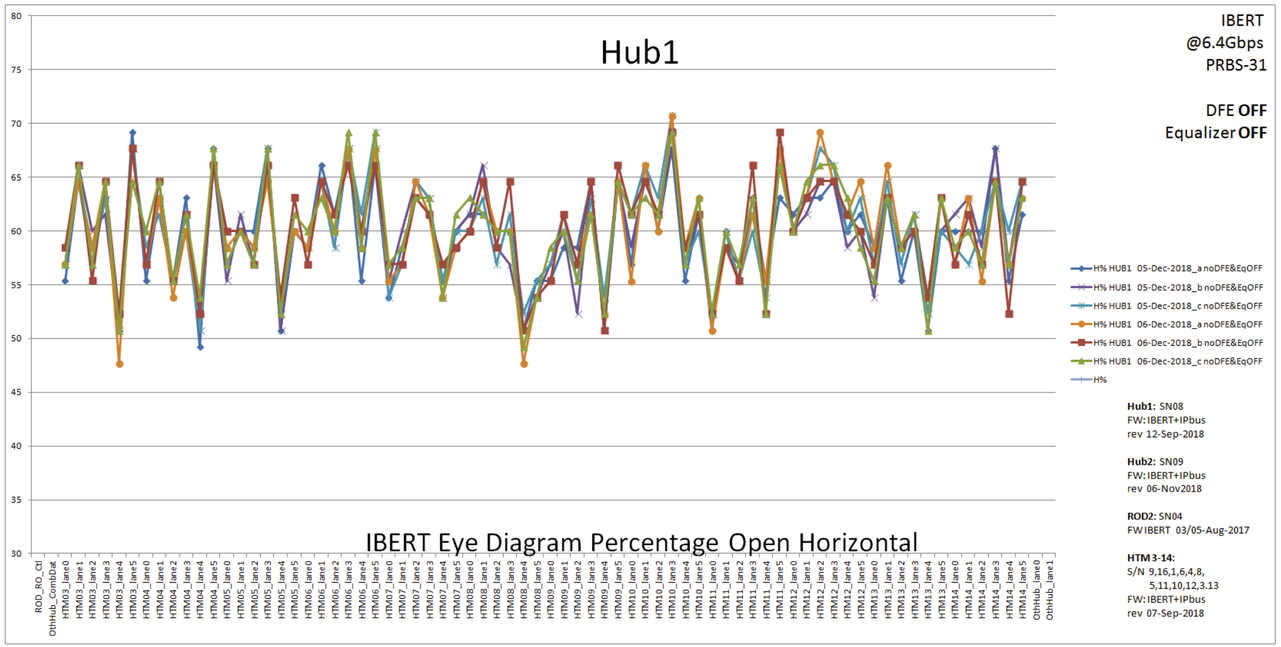
Hardware: Backplane Link Testing

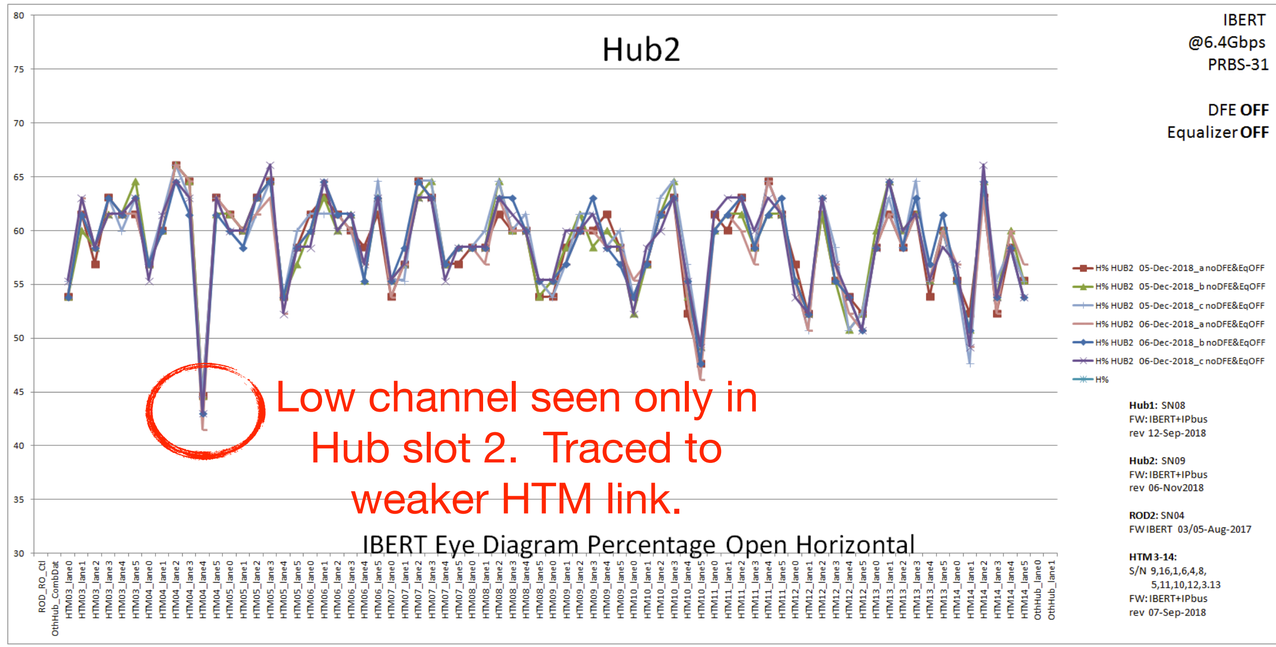
- BER tests have been performed with Xilinx IBERT firmware at a line rate of 6.4 Gbps and using PRBS31, including all FEX Zone-2 links for Hub and ROD.
  - Two separate, long-duration runs have been performed and find the full system capable of **BER<6E-17**. No errors observed.
  - Lots of interesting features, more on that in the following slides.



Hardware: Backplane Link Testing

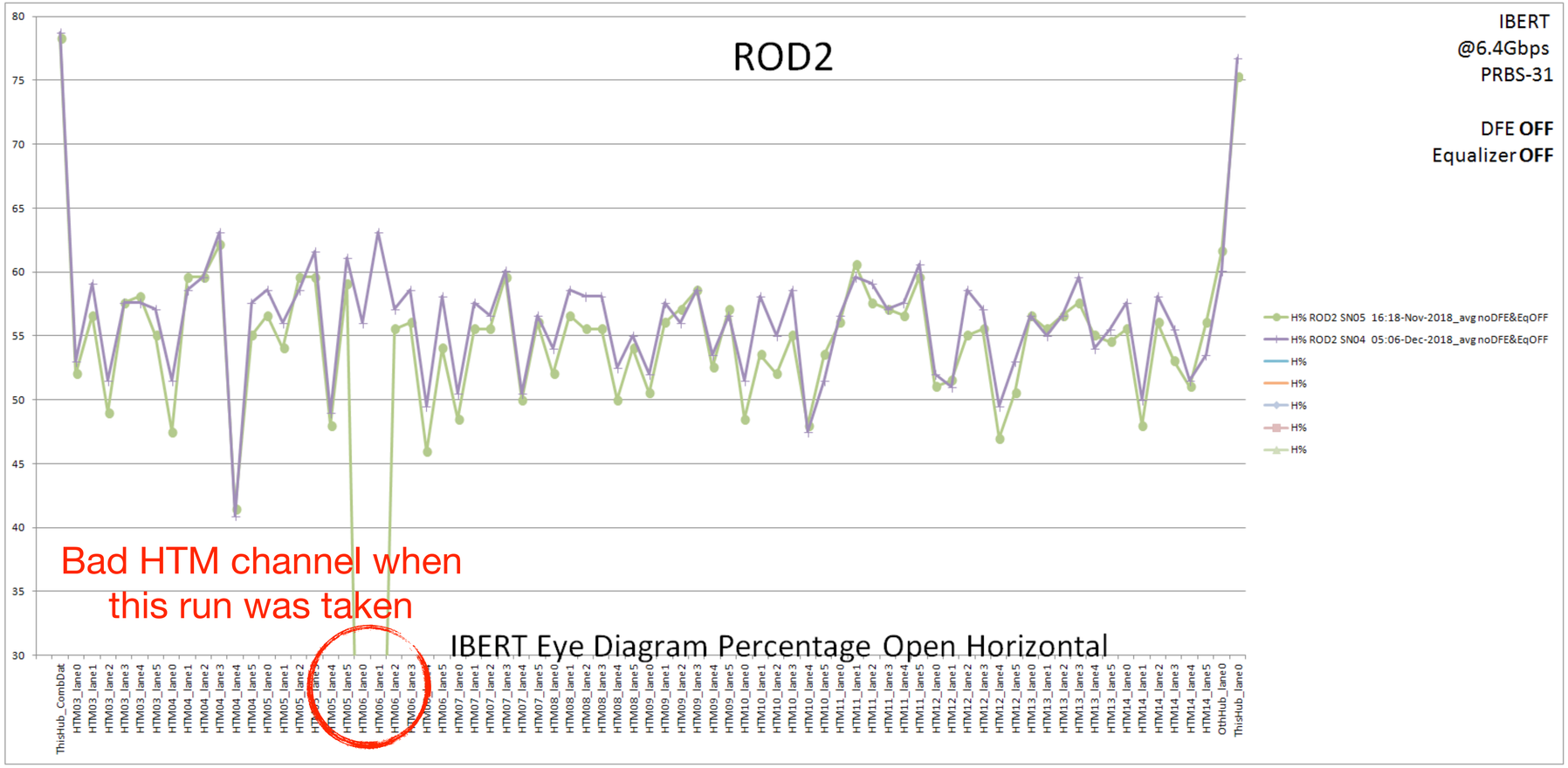
- Repeated tests of the Hub eye diagrams illustrate very high uniformity over Hub modules.
  - Repeated tests of the same card also show zero variation.
  - Quality and uniformity of the Hub PCB manufacturing and assembly processes is very high.
  - 6 Hubs shown here, 2 remaining in UK will be tested once we can swap them out.





Hardware: Backplane Link Testing

- Repeated tests of the ROD eye diagrams illustrate very high uniformity as well.
  - Each trace is a different Hub/ROD pair.
  - NB: green graph produced with a bad HTM, 2 links were dead.



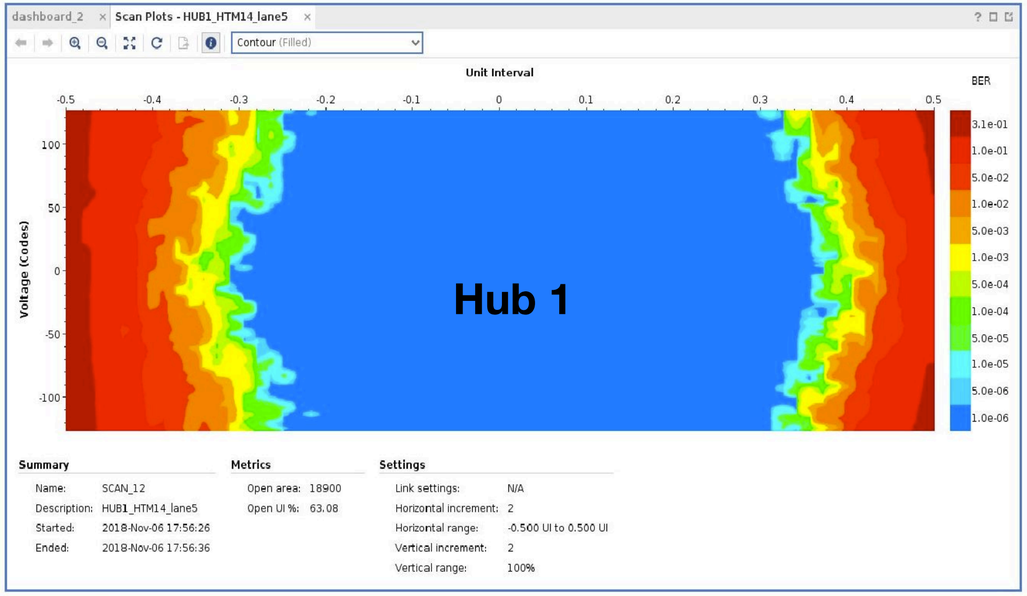
Hardware: Backplane Link Testing

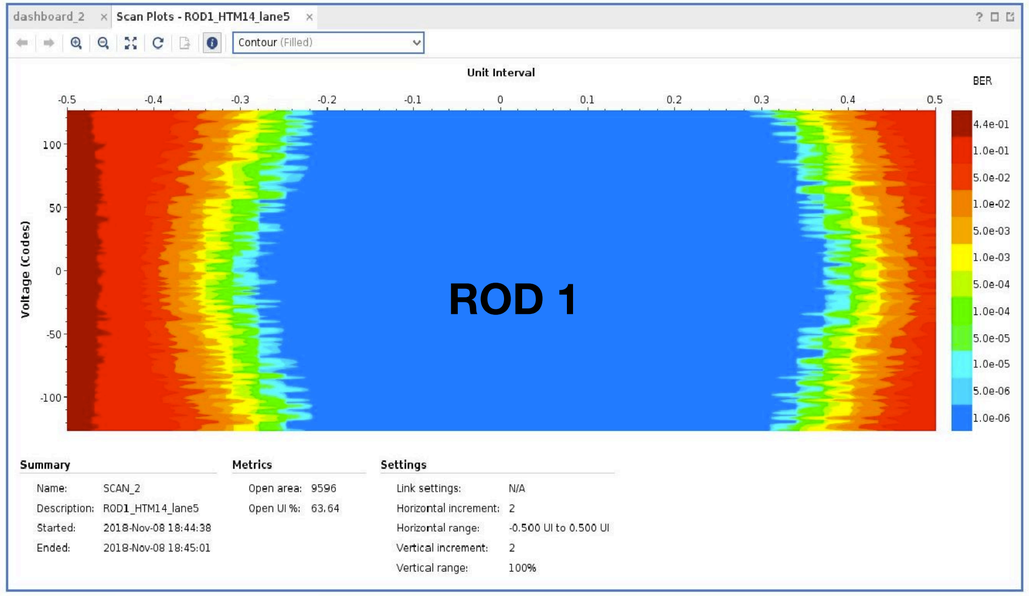
- Many interesting features in the backplane links to be explored. We've gone some way down the rabbit hole.
  1) Can we discern differences between GTY vs GTH transceivers? *Individual cases yes, on average no.*
  2) Does activity in the GbE switch reduce eye margin? *Nothing significant.*
  3) Do longer backplane traces have reduced margin? *Typically, yes. Though easier to see once HTM variation is accounted for.*
  4) Does the fanout equalizer improve margin? *Typically, yes.*
  5) Does the Xilinx MGT equalization (DFE) improve margin? *Typically, no.*
  6) Do intense random register tests reduce margin? *Typically, no.*
  7) Do we see significant margin loss due to cross talk? *Typically, no. But 3-5% variations are observed when using 1 HTM vs 12 HTMs.*

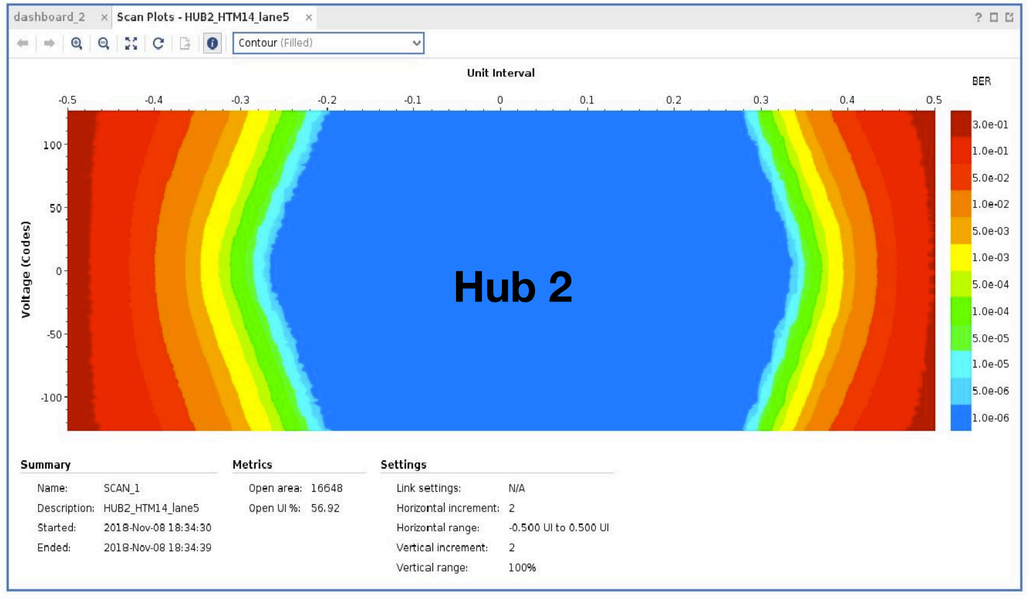
Random Register Tests: Random read/write register accesses in Hub FPGA via IPbus.

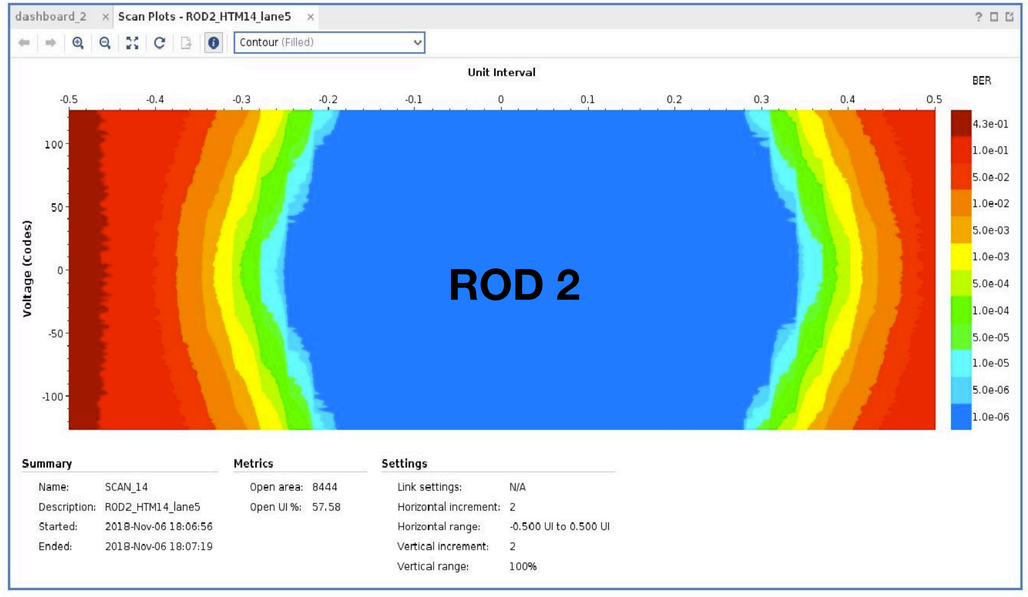
1	2	3	4	6	7	8
				All Sources 1-Oct	Single Lane 5:9-Oct	Single minus All
Comparison Emphasis	Hub#	HTM	Lane#	% Open Horiz	% Open Horiz	Delta % Open
Shorter from HTM	Hub2	HTM10	Lane3	58.46	60.00	+1.5
Longer from HTM	Hub2	HTM13	Lane2	63.08	63.08	0.0
Shorter from FanOut	Hub1	HTM09	Lane1	58.46	61.54	+3.1
Longer from FanOut	Hub1	HTM07	Lane0	56.92	56.92	0.0
GTH	Hub2	HTM08	Lane3	56.92	56.92	0.0
GTY	Hub2	HTM08	Lane4	61.54	61.54	0.0
Same Crate Side	Hub1	HTM09	Lane3	58.46	61.54	+3.1
Cross through Hub2	Hub1	HTM10	Lane0	63.08	60.00	-3.1
Out Of FanOut Array	Hub1	HTM14	Lane5	58.46	60.00	+1.5
No IPBus IO	Hub2	HTM03	Lane0	55.38	53.85	-1.5
While RandRegTest	Hub2	HTM03	Lane0	53.85	52.31	-1.5
Typical w/Equal OFF	Hub2	HTM09	Lane3	60.00	60.00	0.0
Typical w/Equal ON	Hub2	HTM09	Lane3	60.00	63.08	+3.1
Weaker Channel	Hub1	HTM03	Lane4	47.69	50.77	+3.1
Weaker Channel	Hub1	HTM05	Lane4	50.77	50.77	0.0
Weaker Channel	Hub1	HTM06	Lane4	43.08	46.15	+3.1
Weaker Channel	Hub1	HTM08	Lane4	41.54	47.69	+6.2
Weaker Channel	Hub2	HTM04	Lane4	46.15	50.77	+4.6
Weaker Channel	Hub2	HTM10	Lane5	50.77	53.85	+3.1
Weaker Channel	Hub2	HTM12	Lane1	46.15	47.69	+1.5
Weaker Channel	Hub2	HTM14	Lane0	50.77	50.77	0.0

DFE Performance: DFE Off, Fanout Eq Off

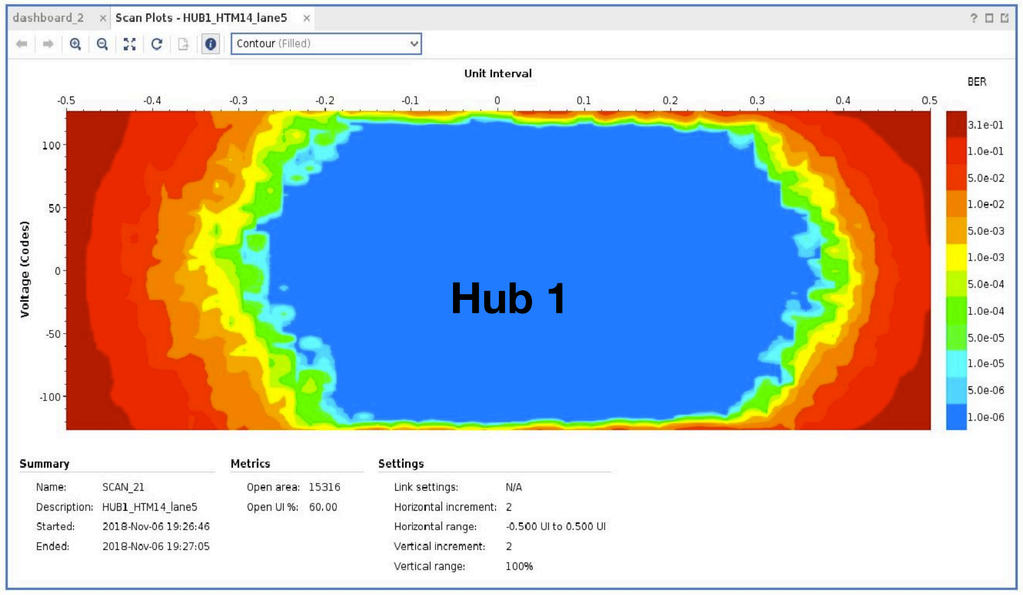


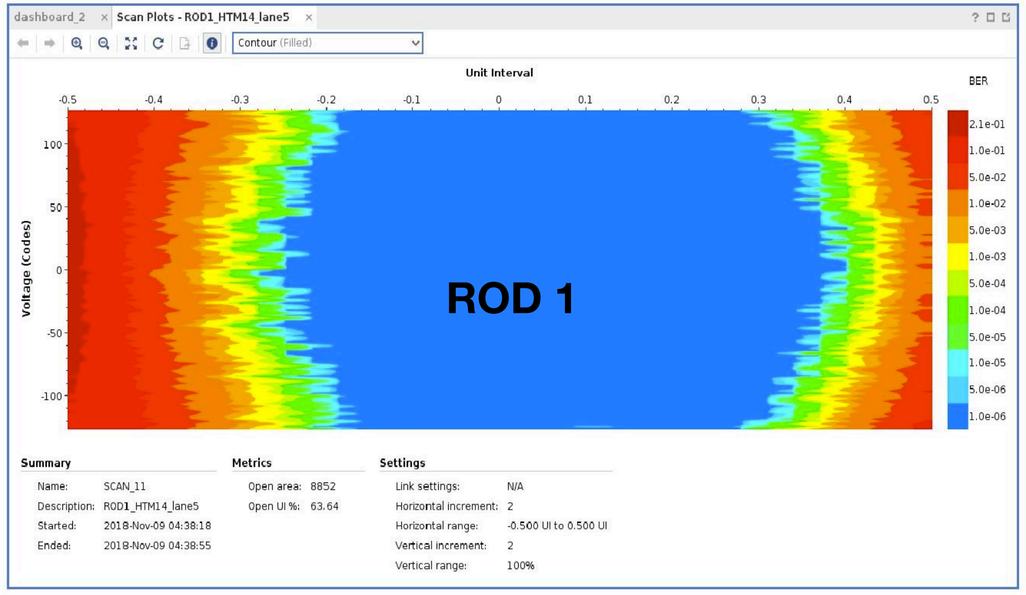


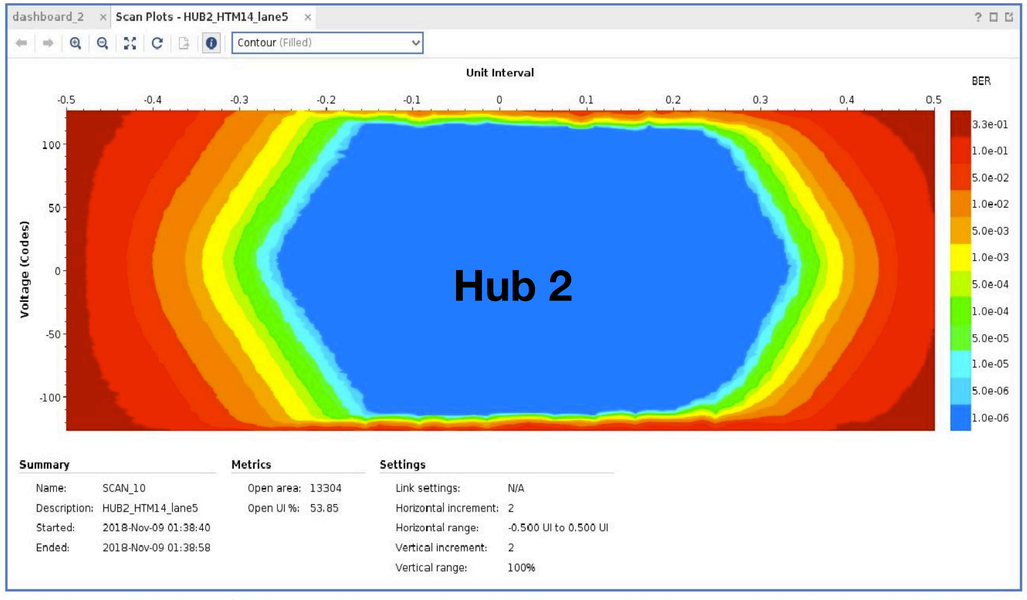


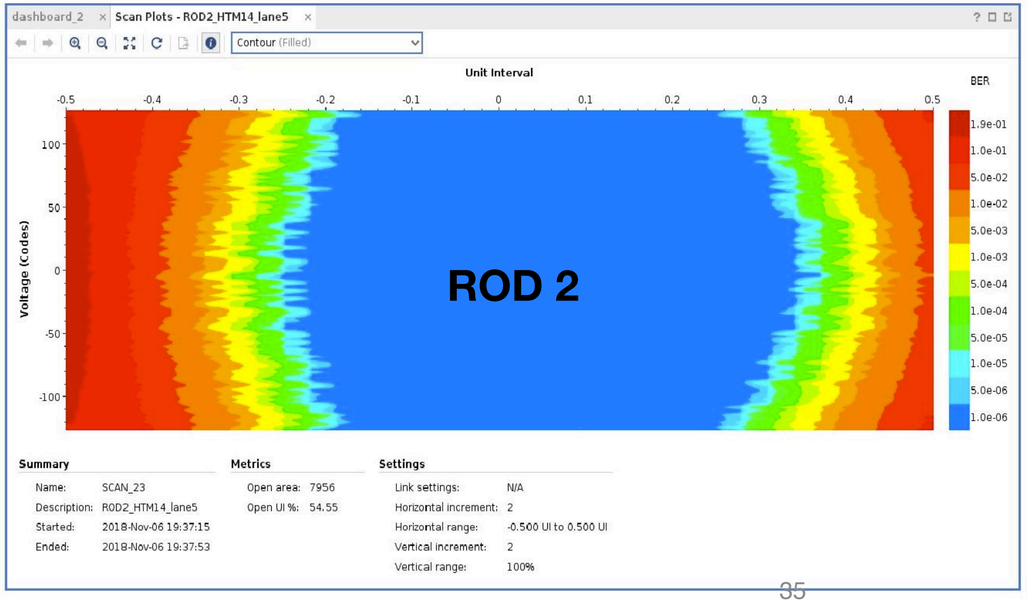


DFE Performance: DFE On, Fanout Eq Off

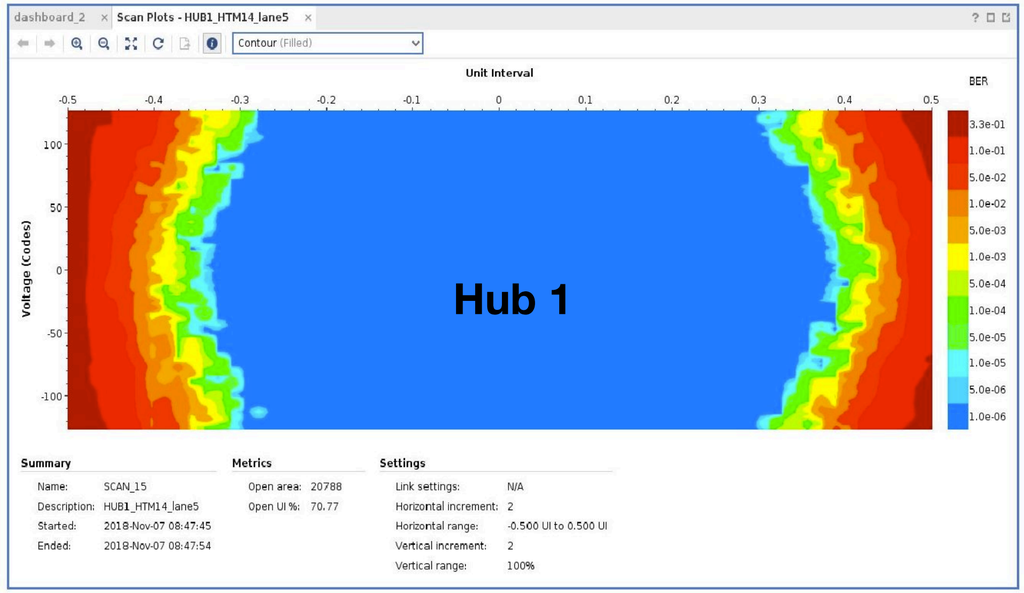


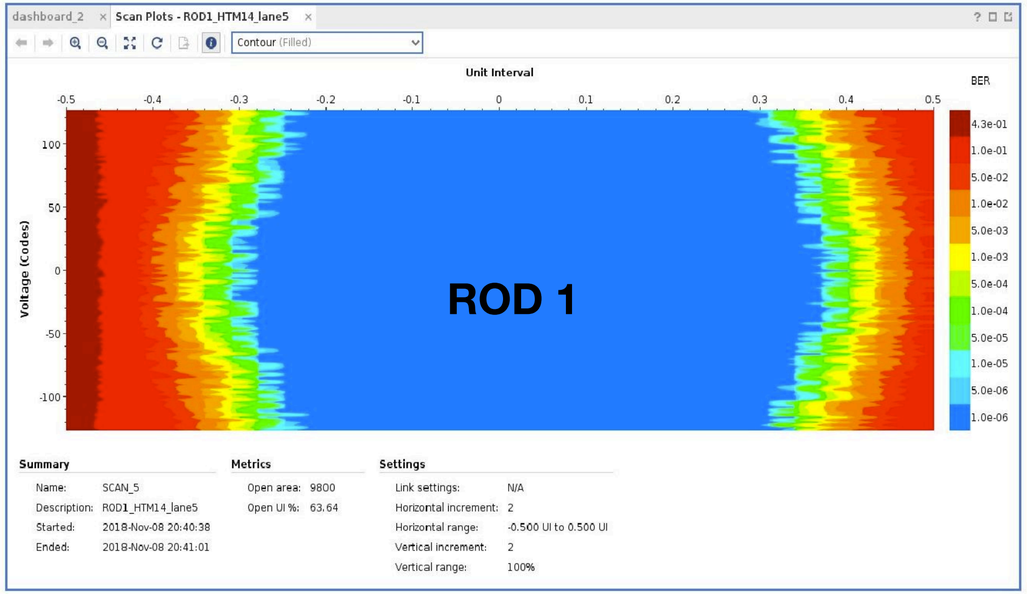


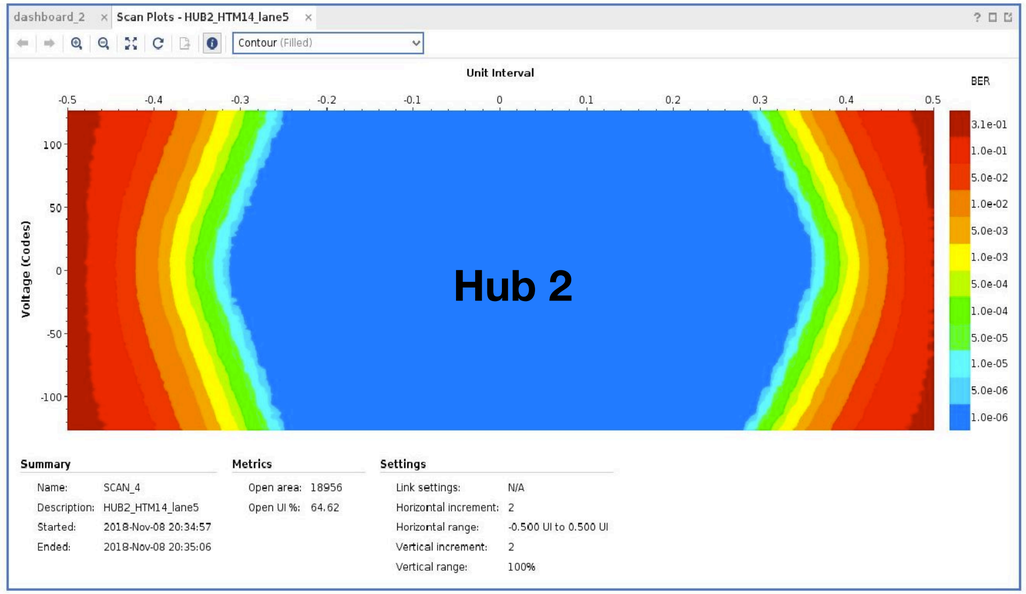


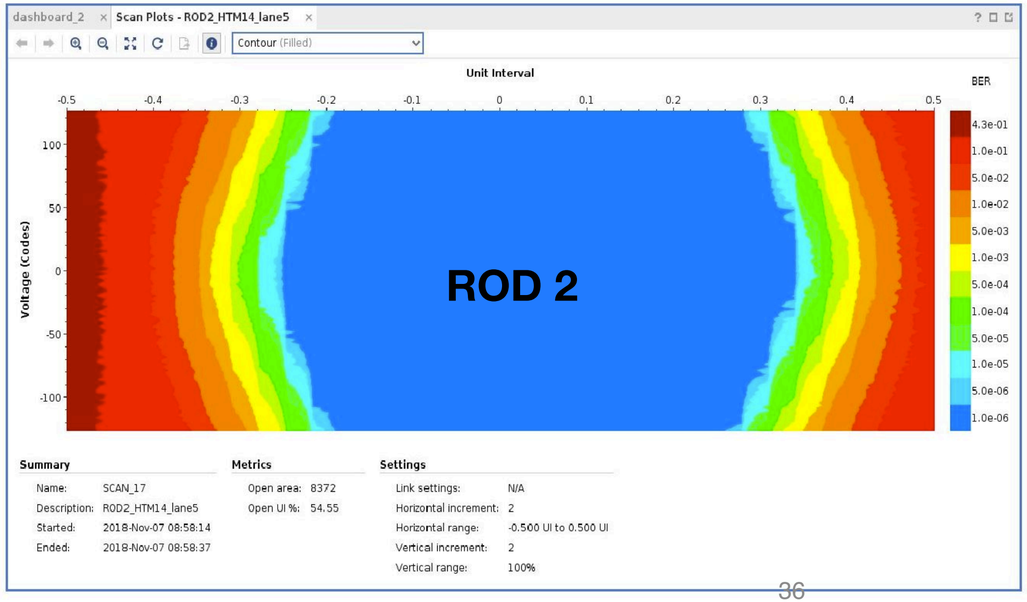


DFE Performance: DFE Off, Fanout Eq On

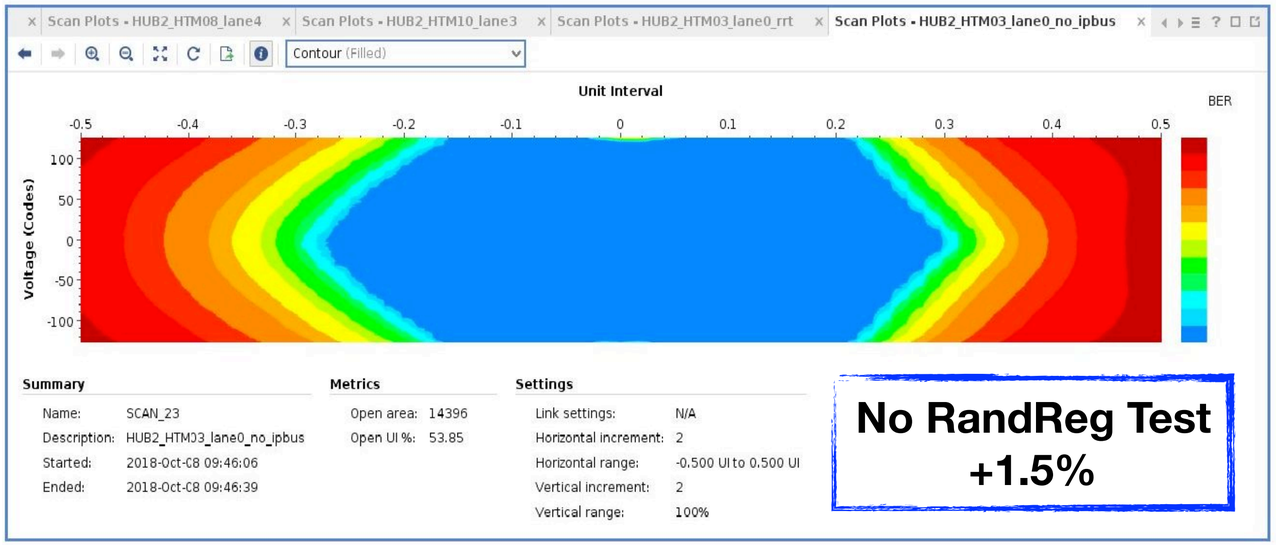


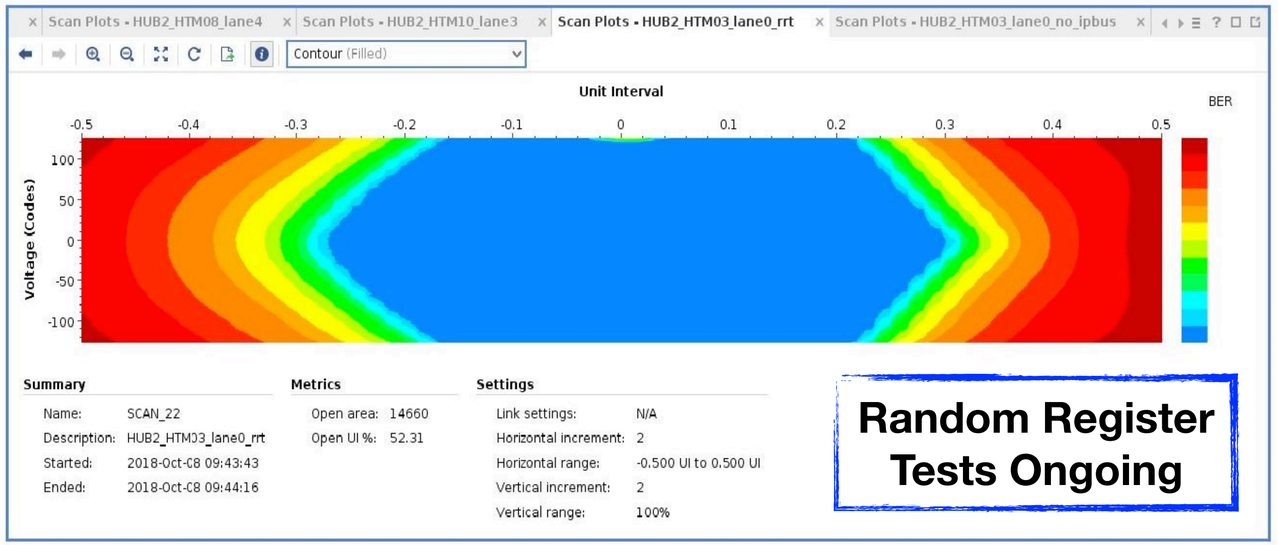


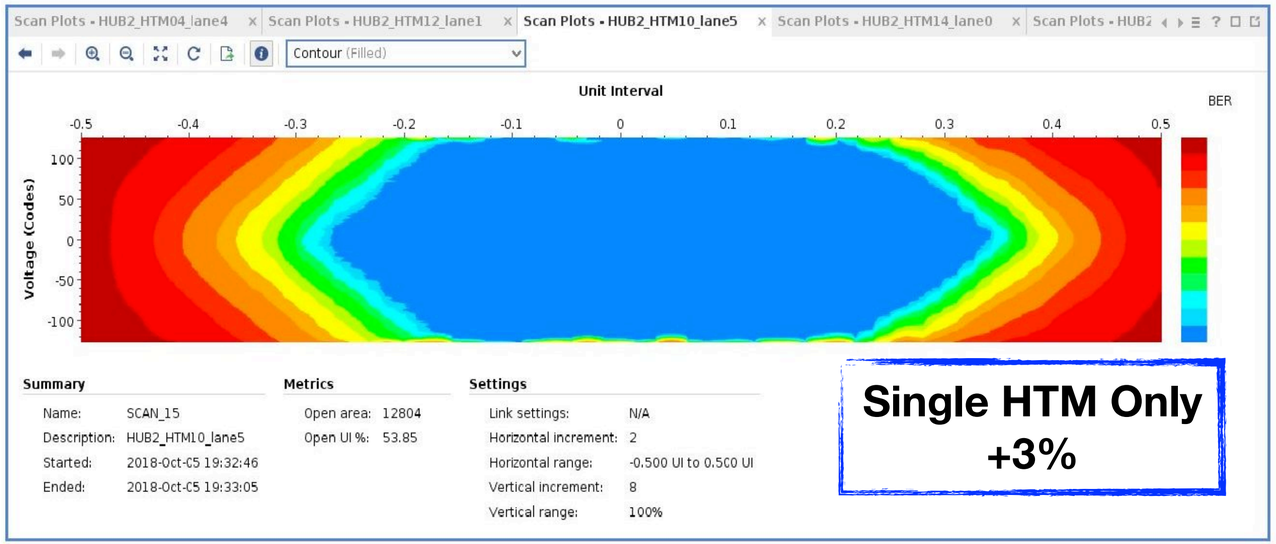


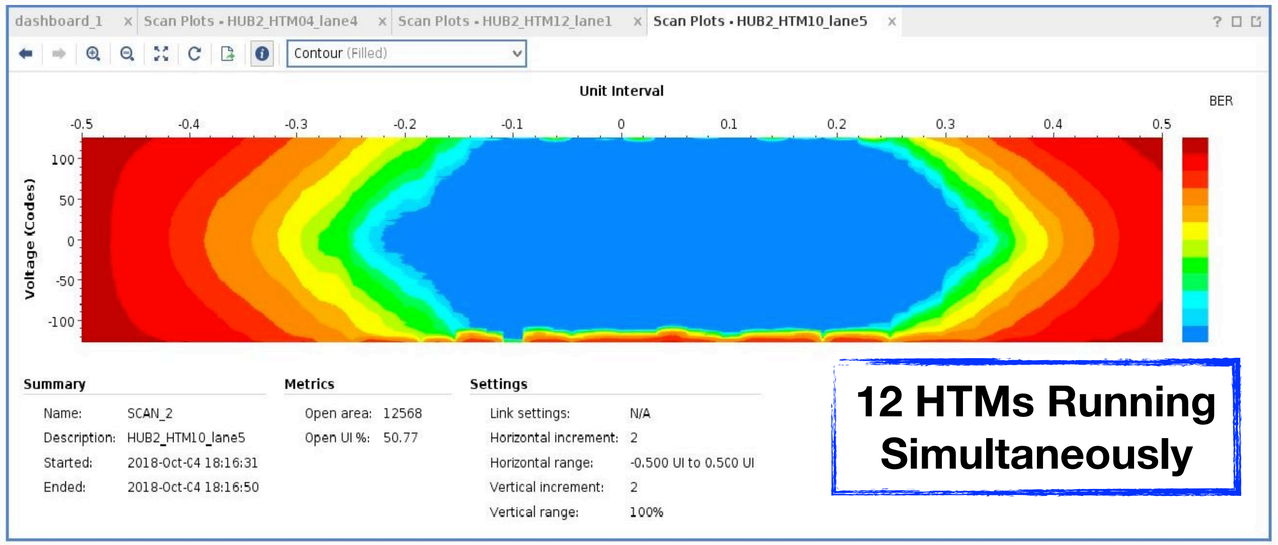


Other MGT Effects



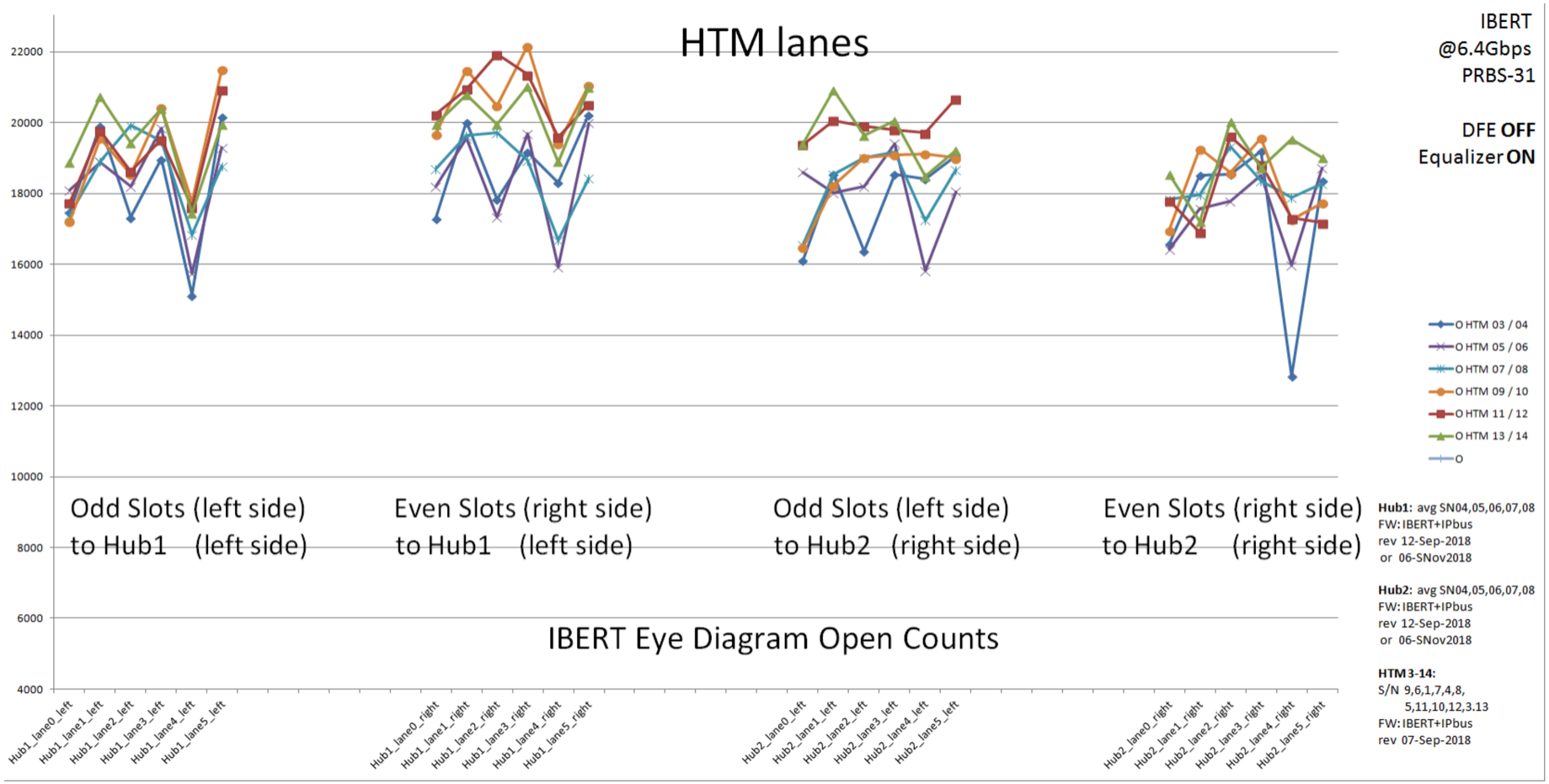






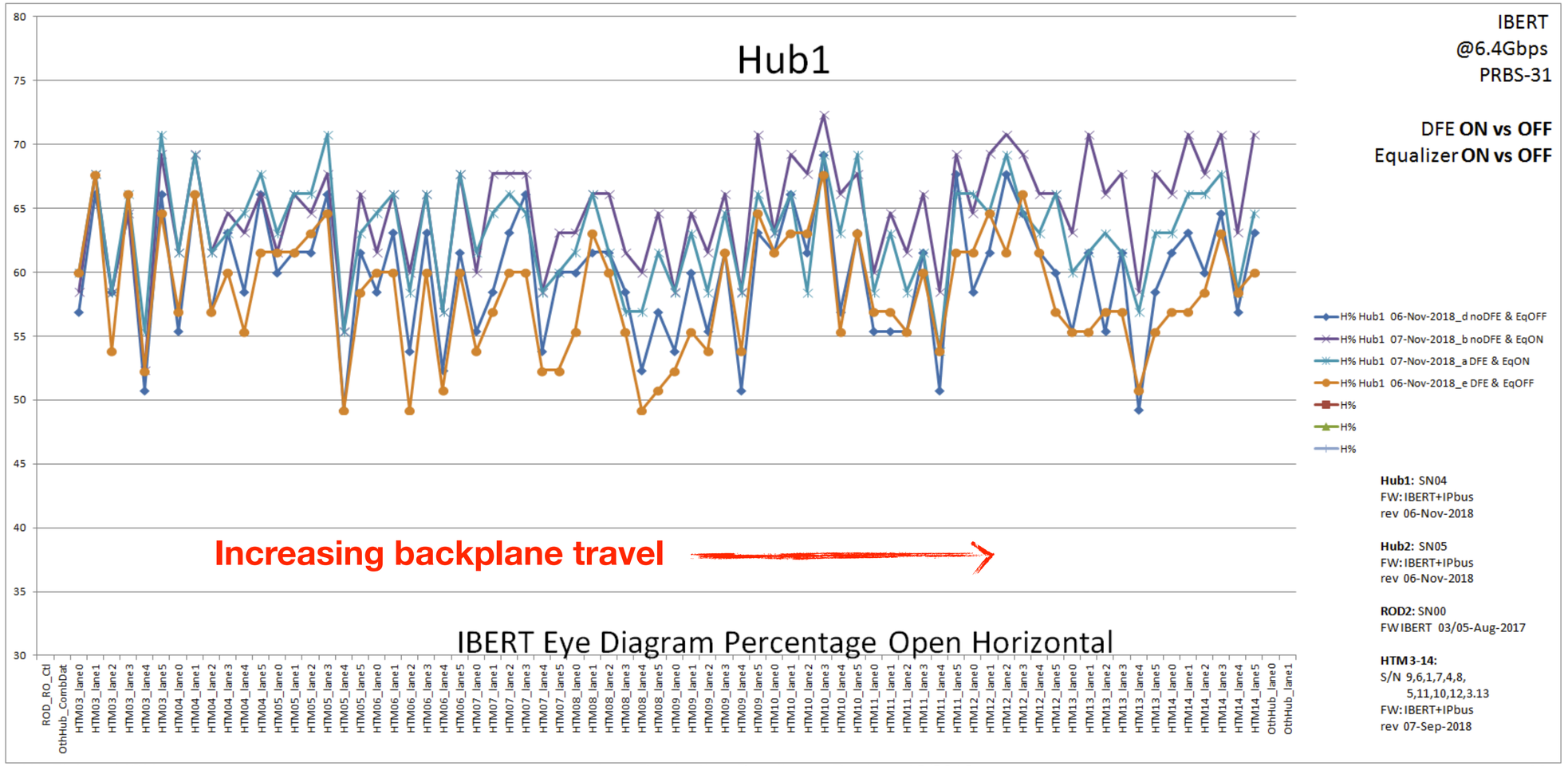
Hardware: Backplane Link Testing

- Structure in ROD/Hub eye diagrams correlates with HTM/backplane variations
  - HTM lane4 is systematically lower than lane5 (nb, Hub1 and Hub2 see different HTM MGTs)
  - Hub1 vs Hub2 backplane traces can also be discerned



Hardware: Backplane Link Testing

- Study of Hub fanout equalizers and MGT “Decision Feedback Equalization”
  - DFE is not always helpful and can add some noise, especially with longer backplane traces.
  - Equalization feature on Hub fanout uniformly improves MGT eye margin.



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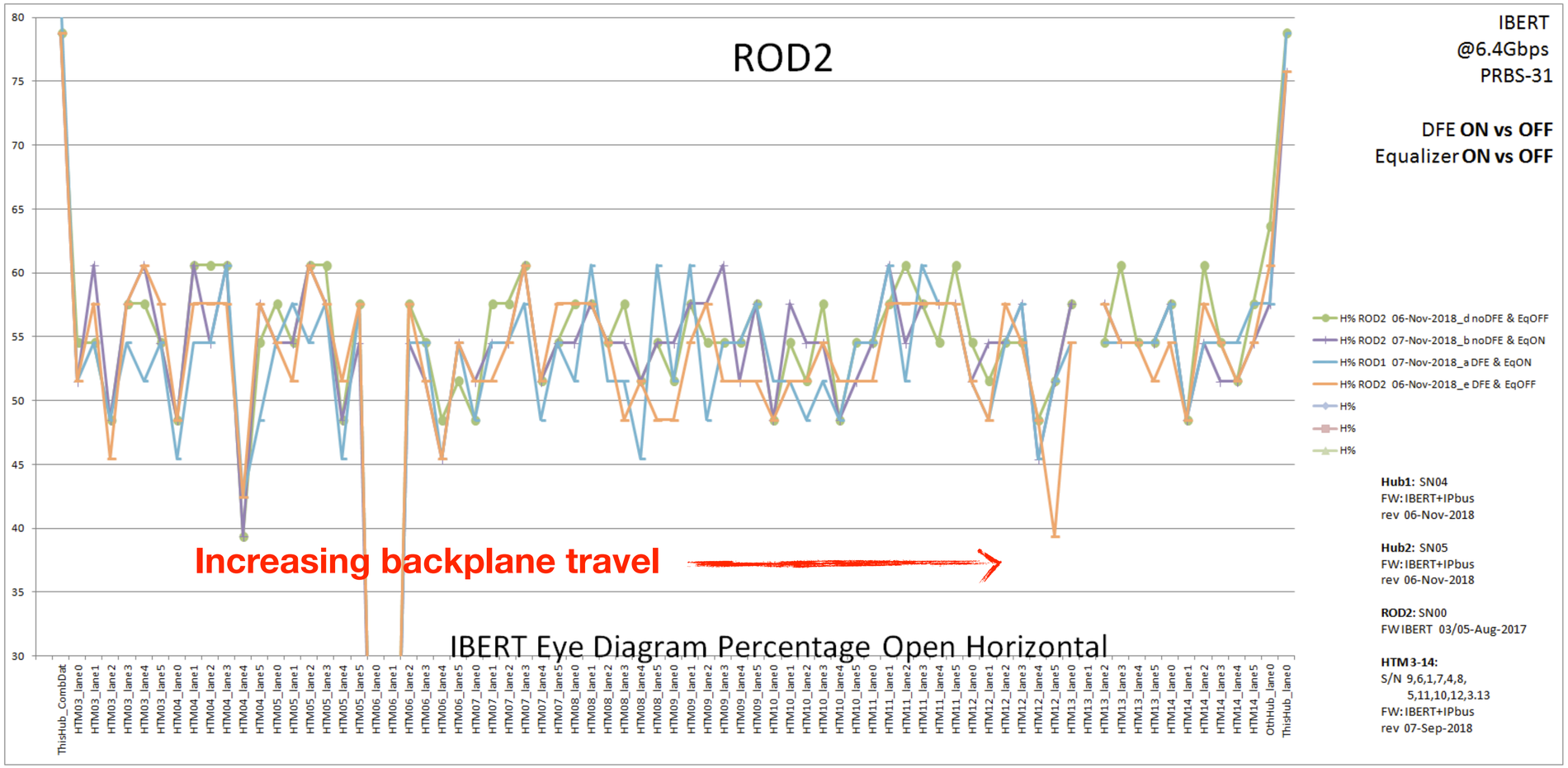


Hardware: Backplane Link Testing

- If you would like to look at more plots, there are many many more on the Hub and HTM websites:

https://web.pa.msu.edu/hep/atlas/l1calo/hub

https://web.pa.msu.edu/hep/atlas/l1calo/htm

Ethernet Switch Testing

GbE Switch Testing

✔ 1. Verify that both GbE links to the Hub's FPGA are working correctly (link to the GbE Switch on This Hub and link via the backplane Base Interface to the GbE Switch on the Other Hub).

✔ 2. Verify that all 22 GbE Switch Ports that are used on the Hub card carry GbE traffic OK.

✔ 3. Verify that the Hub's Front Panel GbE connection and GbE Magnetics for the ROD are all working OK.

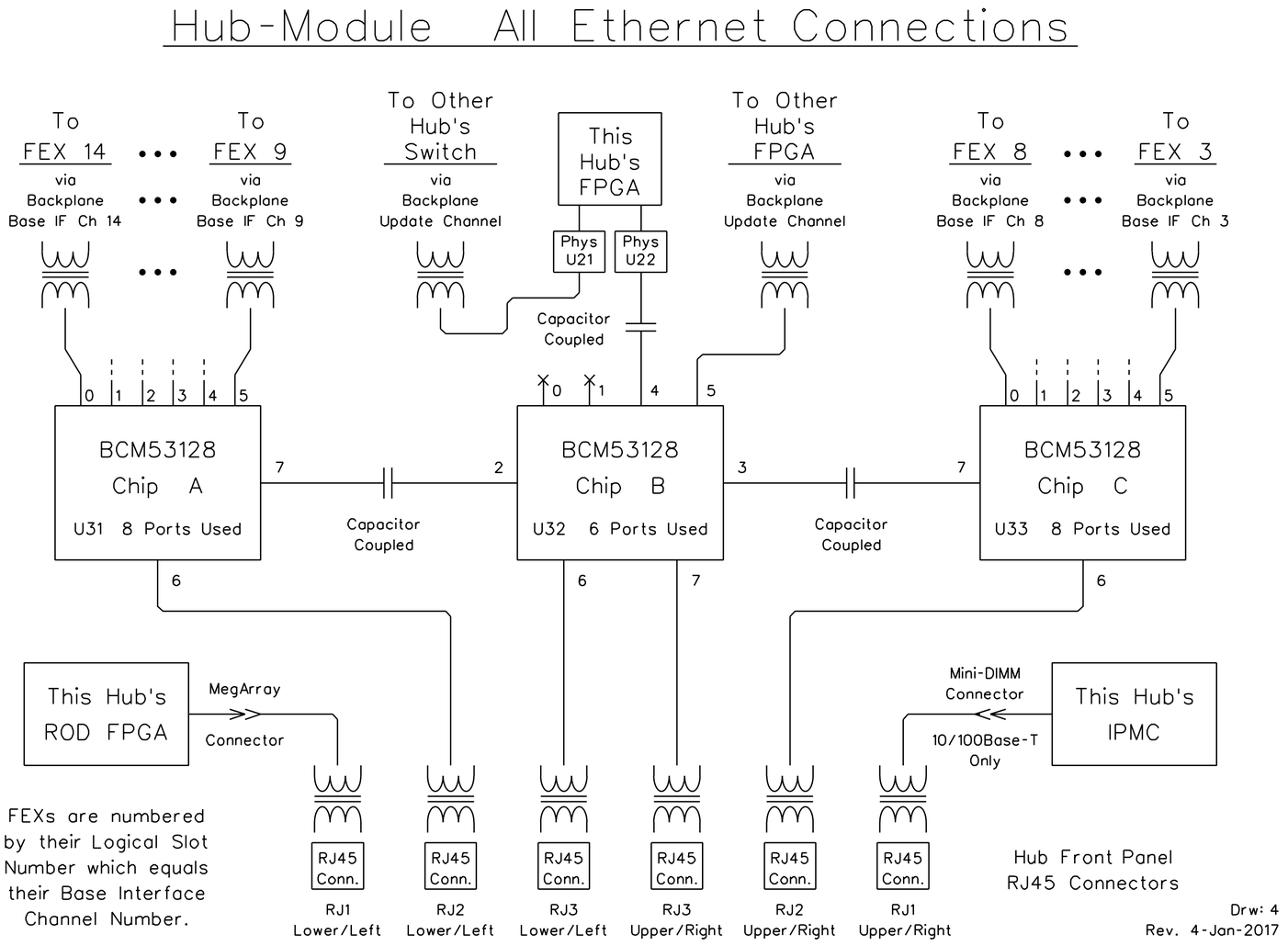
✔ 4. Verify that the Hub's Front Panel GbE connection and GbE Magnetics for the IPMC are all working OK.

✔ Done on all cards ✔ Done on 1-7 cards

GbE Switch Configuration

- Hub provides a 16-port GbE switch using three 8-port Broadcom BCM53128 chips
  - The chips can be interlinked to act as 1, 2 or 3 independent switches.
  - Our goal is to choose a single configuration that will satisfy all L1Calo use case needs, while minimizing the total number of external links to be maintained.
    - Maintaining shelf-specific or slot-specific Hub module spares is not a wise choice.

- Use case degrees of freedom
  - eFEX, jFEX, L1Topo shelves
  - DCS/Config and IPMC networks
  - Preferences tend towards higher bandwidth, thus 3-switch or 2-switch configurations.



GbE Switch Configuration

- Hub provides a 16-port GbE switch using three 8-port Broadcom BCM53128 chips
  - The chips can be interlinked to act as 1, 2 or 3 independent switches.
  - Our goal is to choose a single configuration that will satisfy all L1Calo use case needs, while minimizing the total number of external links to be maintained.
    - Maintaining shelf-specific or slot-specific Hub module spares is not a wise choice.

- Use case degrees of freedom
  - eFEX, jFEX, L1Topo shelves
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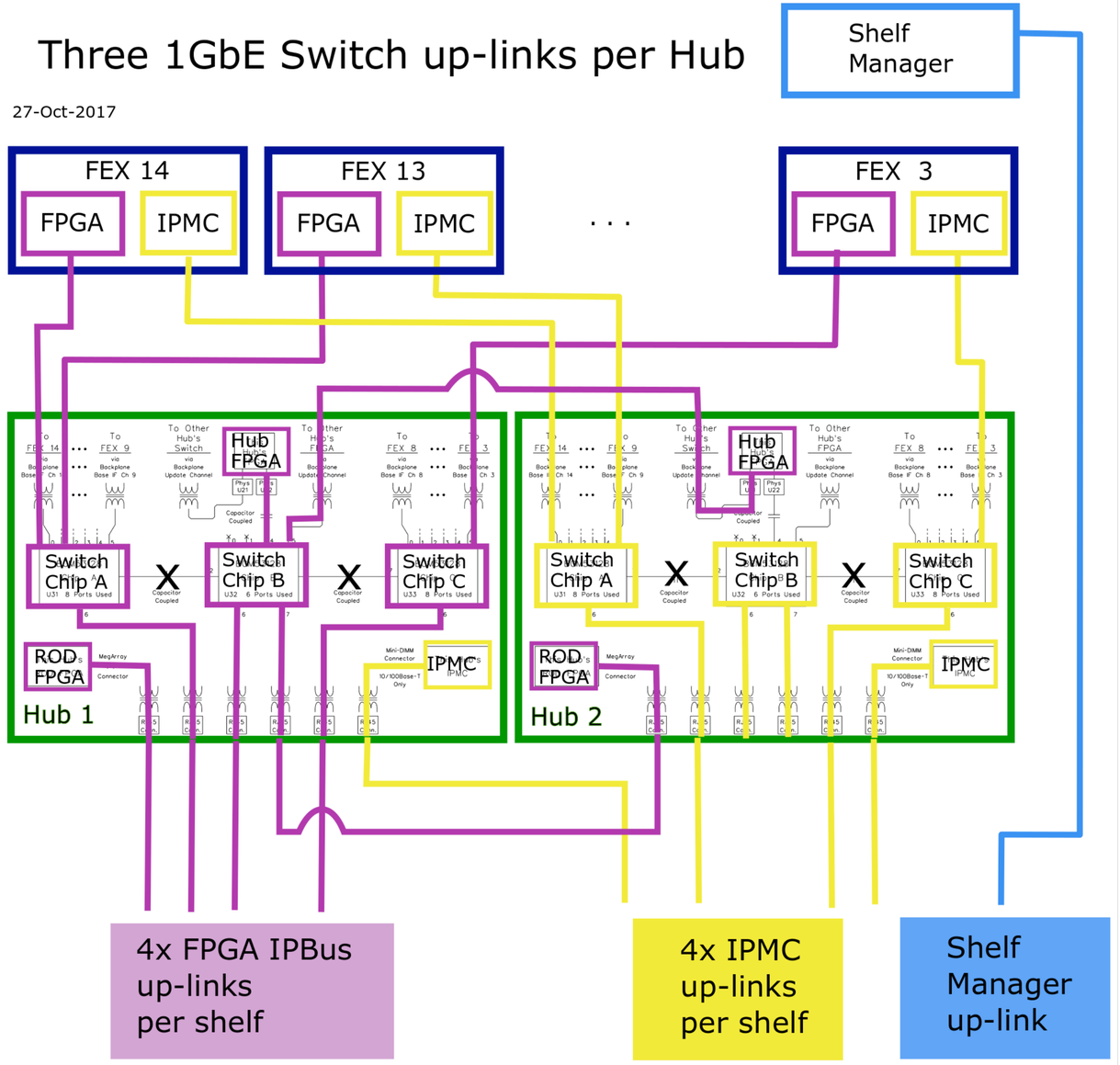

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- Use case degrees of freedom
  - eFEX, jFEX, L1Topo shelves
  - DCS/Config and IPMC networks
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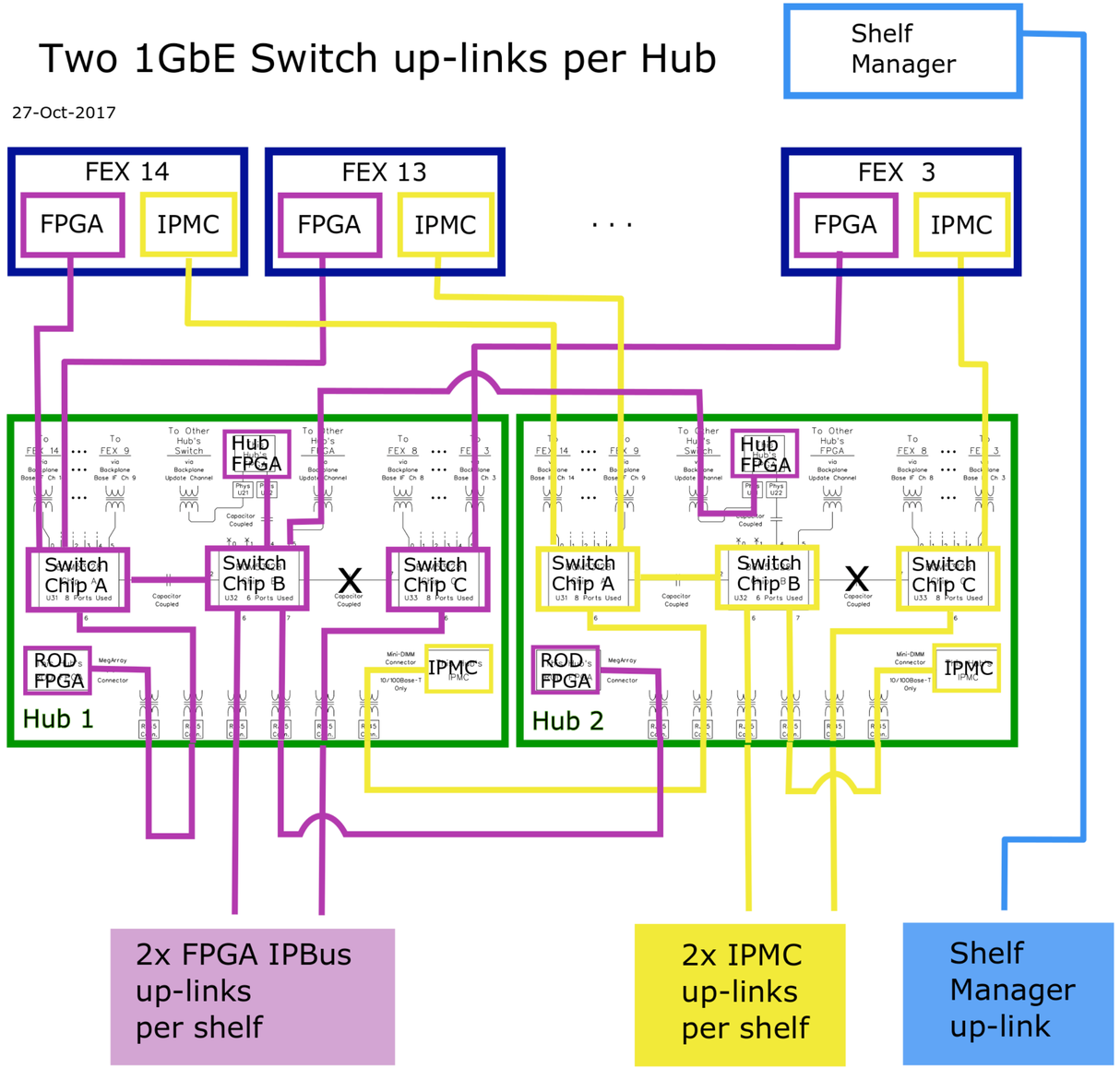
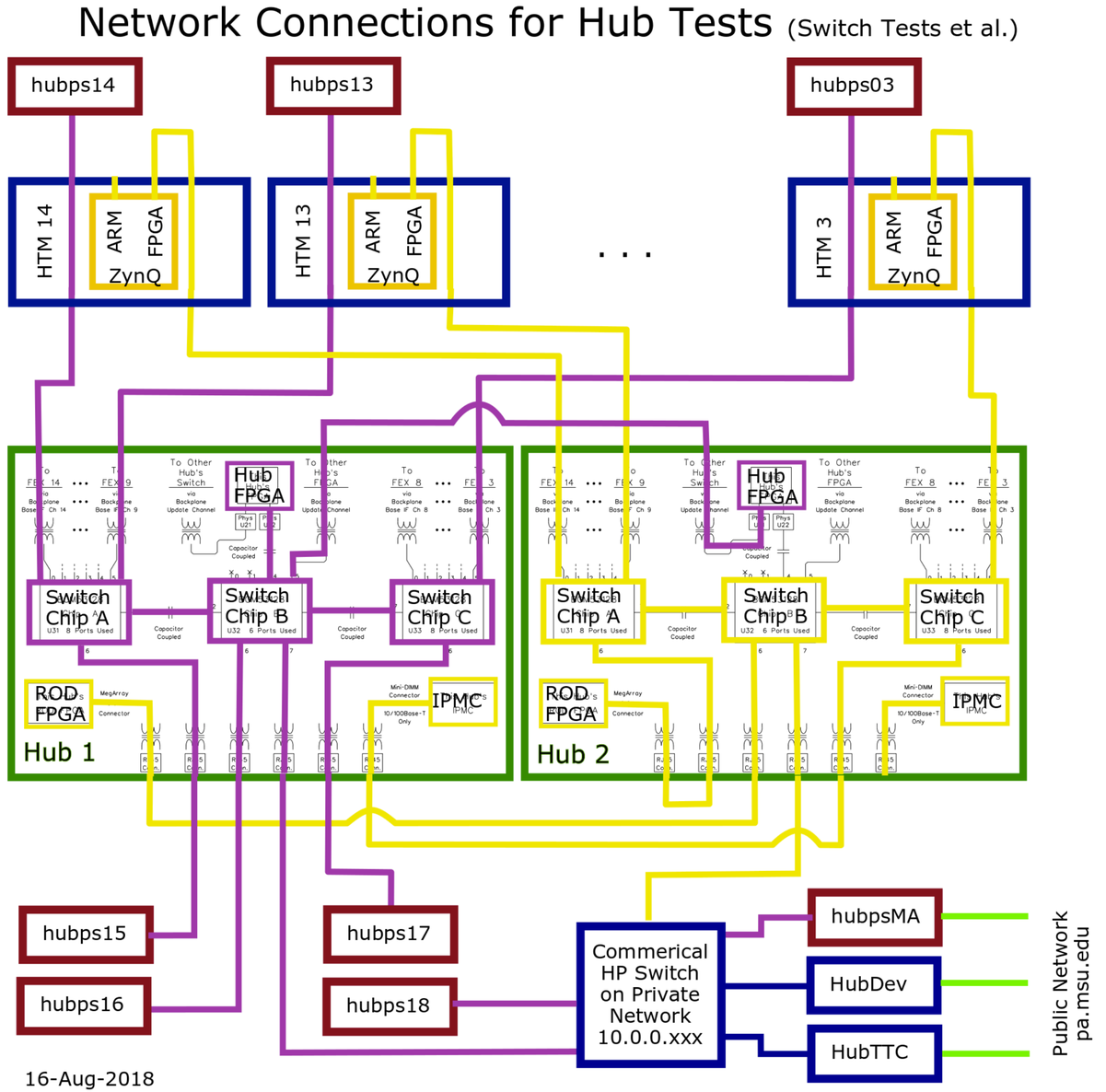
Configuration is flexible and can be decided once L1Calo plan is finalized.



GbE Switch Testing

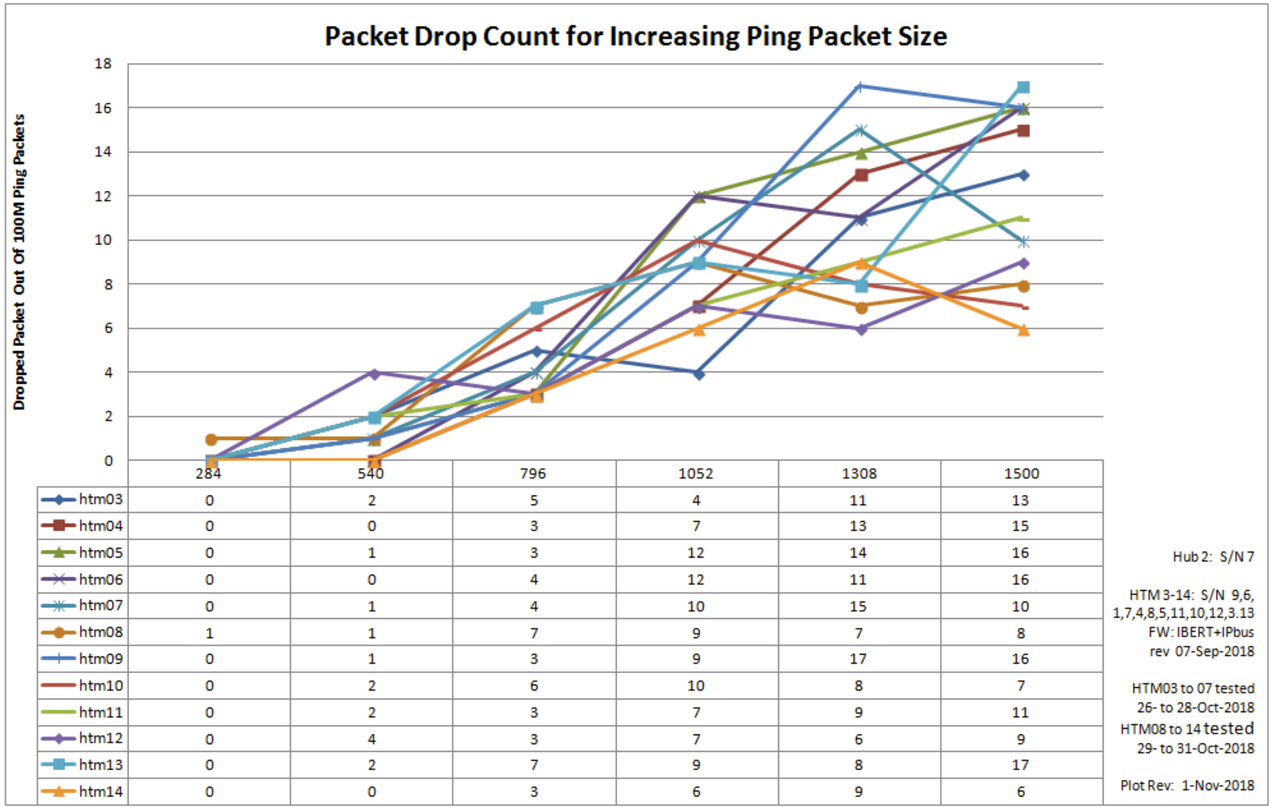
- We have leveraged our network diagnostic tools used for our US-ATLAS Tier-2/3 cluster here at MSU
  - In addition to standard ping-based test, include perfSONAR network tools
    - www.perfsonar.net
- Tests performed with 16 linux computers, 12 HTMs and 2 Hubs
  - Hub 1 switch backplane ports to linux running the perfSONAR toolkit
  - Hub 2 switch backplane ports to HTM Zynq 7000 with IPbus FW
- There are the primary categories of tests
  1) Single port packet drop tests using ping
  2) Single port throughput test using perf
  3) Concurrent full-mesh one-way ping



GbE Switch Testing

- Single port packet loss using adaptive ping
  - ping -A -q -c 10000000 -s 512 -I 4 <target>
  - Vary packet size to maximum MTU 1500 byte size
  - 100M packet test for each run
- Can compare linux nodes and FPGA/IPbus
  - Linux nodes never drop packets (this is a 540 byte test)
  - FPGA/IPbus packet loss is extremely small until you reach 1500 byte packets: 12/100M dropped on average
  - Hub switch is not in question, so we plan to investigate IPbus FW options to further characterize performance.

	to IPbus on HTM FPGA			to linux PS node	
Date-> / Hub ->	12-Oct Hub2 SN6	23-Oct Hub2 SN6	26:31-Oct Hub2 SN7	15-Oct Hub1 SN7	19-Oct Hub1 SN7
HTM Slot V	sent minus received	sent minus received	sent minus received	sent minus received	sent minus received
3	0	1	2	0	0
4	0	2	0	0	0
5	0	4	1	0	0
6	0	1	1	0	0
7	2	3	0	0	0
8	-	1	1	-	0
9	0	0	1	0	0
10	1	0	2	0	0
11	2	1	2	0	0
12	3	2	4	0	0
13	0	1	2	0	0
14	-	83	0	-	0



GbE Switch Testing

- In addition we test single port throughput using iperf tools
  - Use perfSONAR to run iperf3 and sequentially measure throughput between any two PS nodes
    - Tests both directions
  - Results on all switch ports are highly uniform and yield expected maximum throughput of >900 Mpbs

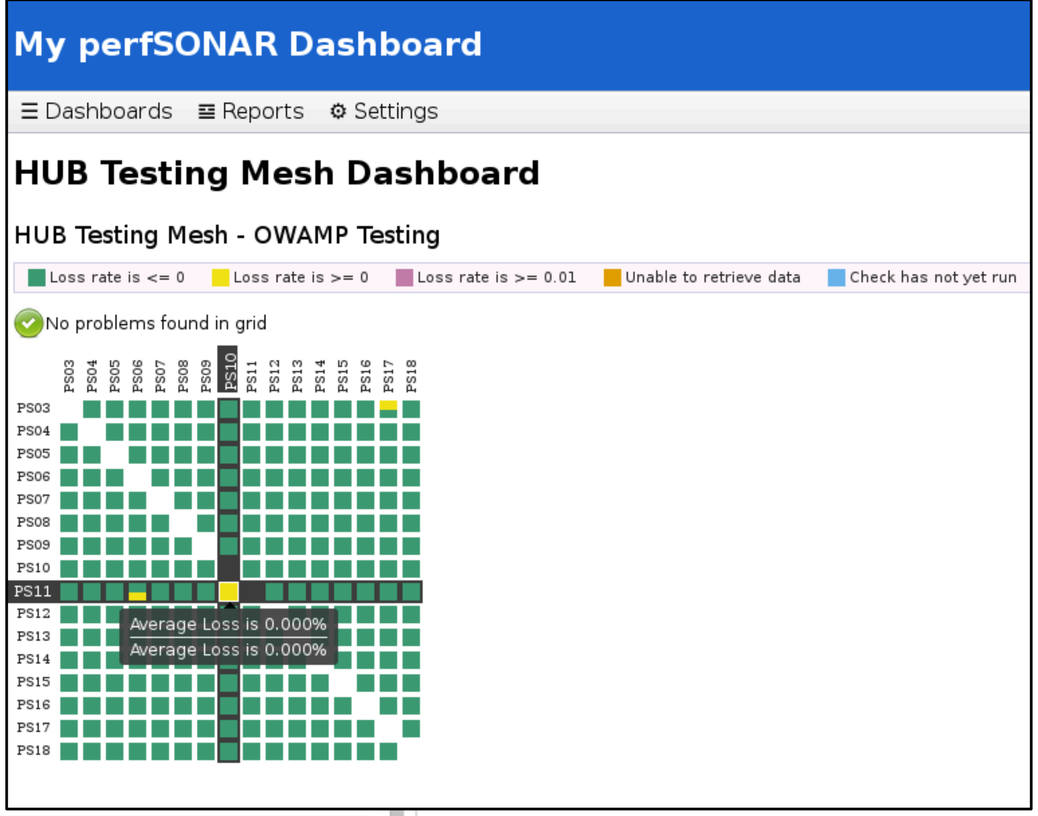
iperf Throughput Test Summary

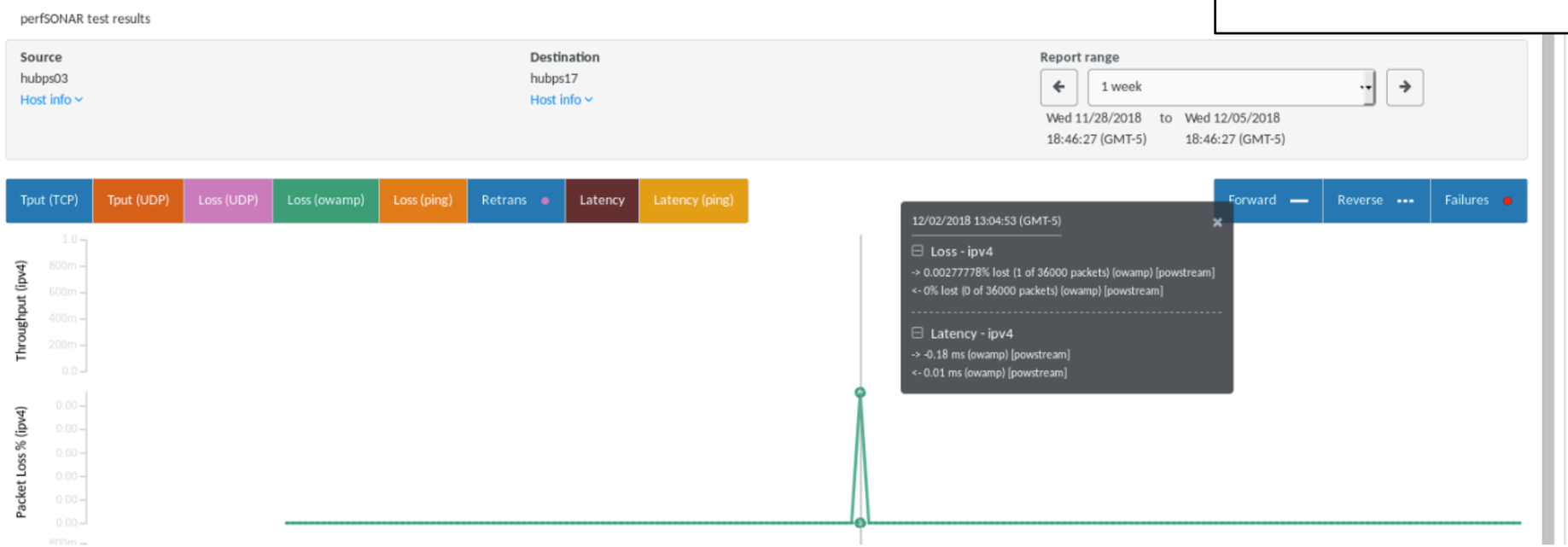
Test Date: Dec 5, 2018
Hub in Slot 1: SN08
each iperf3 transfers: 15 mn

from PS Node	to PS Node	Mbps Minimum	Mbps Maximum	Mbps Average
hubps03	hubps15	910.2	916.5	912.5
hubps04	hubps15	910.2	918.6	912.5
hubps05	hubps15	910.2	916.5	912.4
hubps06	hubps15	922.7	929.0	925.4
hubps07	hubps15	922.7	931.1	925.4
hubps08	hubps15	922.7	933.2	925.4
hubps09	hubps15	929.0	933.2	931.0
hubps10	hubps15	929.0	937.4	931.0
hubps11	hubps15	929.0	937.4	931.0
hubps12	hubps15	929.0	937.4	931.0
hubps13	hubps15	929.0	937.4	931.0
hubps14	hubps15	929.0	935.4	930.8
hubps16	hubps15	924.8	935.3	926.1
hubps17	hubps15	922.7	935.3	925.4
hubps18	hubps15	924.8	943.7	926.2
hubps15	hubps03	910.2	920.6	912.9
hubps15	hubps04	910.2	918.6	912.9
hubps15	hubps05	910.2	914.4	912.8
hubps15	hubps06	912.2	935.3	921.2
hubps15	hubps07	922.0	931.1	925.8
hubps15	hubps08	922.7	933.2	925.8
hubps15	hubps09	929.0	939.4	930.7
hubps15	hubps10	929.0	935.3	930.8
hubps15	hubps11	929.0	935.3	930.8
hubps15	hubps12	929.0	933.2	930.8
hubps15	hubps13	929.0	941.6	930.8
hubps15	hubps14	929.0	935.3	930.8
hubps15	hubps16	924.8	931.0	926.3
hubps15	hubps17	924.8	931.2	925.8
hubps15	hubps18	924.8	929.0	926.3

GbE Switch Testing

- Concurrent full-mesh one-way ping
  - Use OWAMP (One Way Active Measurement Protocol) to measure packet loss from one perfSONAR node to another
    - Setup concurrent/mesh tests on the 16 perfSONAR nodes
    - Plus one collector node with MaDDash collect tool
  - Each OWAMP test sends 10x 1450-byte (plus header) packets per second
    - Total ~55 Mbps sent and received on each on all Hub switch ports
    - Longest test ran for 5 days with a total of 3 packets dropped





Slow Control & Monitoring

IMPC, Slow Control

✔ 1. Verify that the three I2C buffers in the overall Sensor I2C Bus are working and be enabled or disabled via their control lines that run to the Hub's FPGA.

✔ 2. Verify that the Front Panel JTAG connector has access to the Hub's FPGA and that when the ROD is installed and powered up that the ROD's FPGA also appears in this JTAG string.

✔ 3. Verify that the two MiniPOD serial control & monitoring I/O buses are working and communicating with the Hub's FPGA.

✔ 4. Verify that the IPMC can negotiate via the IPMB Buses with the Shelf Manager and turn On or Off the Hub card appropriately.

✔ 5. Verify that the IPMC can detect the front panel handle switch position and correctly follow the protocol to turn the Hob module power On and Off.

✔ Done on all cards ✔ Done on 1-7 cards

I2C Monitoring & Multimastering

- The Hub I2C bus can be isolated from the IPMC I2C bus and we do not require I2C multimastering during “normal” L1Calo operations.
  - Outside debugging, commissioning and bench testing, only the IPMC will master the I2C bus.

- All Hub & ROD components on the I2C bus are able to be accessed & monitored
  - DCDC converters, FPGA sysmon are primary targets.

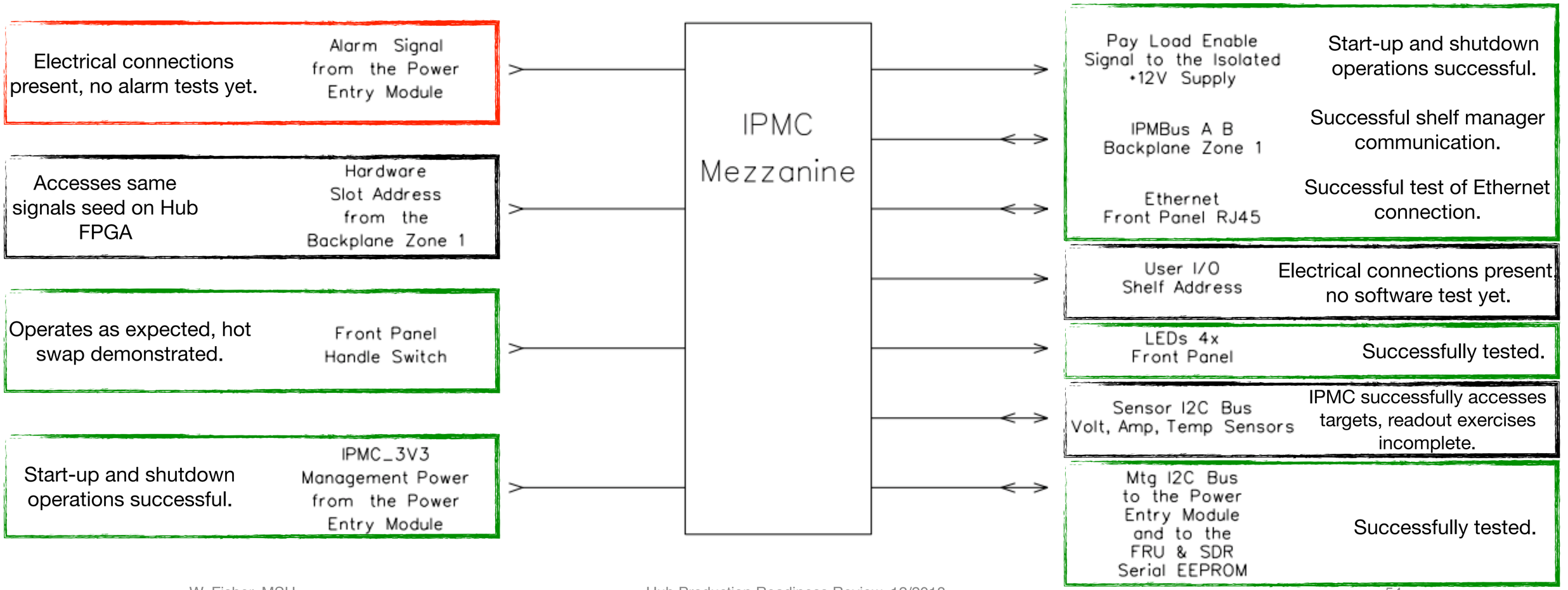
- We have tested our ability to perform I2C arbitration with the IPMC
  - Successfully able to detect bus busy and data FIFO status on the I2C bus.
  - Hub IPbus/I2C software reliably detects IPMC cycles, with a state machine designed to wait for successful I2C mastering arbitration.
  - O(300k) cycles executed without I2C error in a long test run.

Example read of Hub miniPOD transmitter

```
MiniPod type verified to be: trans_mpod
 Minipod internal temperature is 32.22 C
 The voltage on the 2.5 Vcc power supply is 2.4657 V
 The voltage on the 3.3 Vcc power supply is 3.2596 V
 The serial number of the current device: trans_mpod is : A17285016
 The operating time is 3038.0 hours or 126.583333333 days
 Optical power for channel number trans_mpod is: 0.14646524684 dBm or 1034.3 µW
 Optical power for channel number trans_mpod is: 0.911039440903 dBm or 1233.4 µW
 Optical power for channel number trans_mpod is: -0.00130307891732 dBm or 999.7 µW
 Optical power for channel number trans_mpod is: 1.06496870139 dBm or 1277.9 µW
 Optical power for channel number trans_mpod is: 0.137217780511 dBm or 1032.1 µW
 Optical power for channel number trans_mpod is: 1.09646031091 dBm or 1287.2 µW
 Optical power for channel number trans_mpod is: 0.152759066819 dBm or 1035.8 µW
 Optical power for channel number trans_mpod is: 1.0510124455 dBm or 1273.8 µW
 Optical power for channel number trans_mpod is: -0.220935723629 dBm or 950.4 µW
 Optical power for channel number trans_mpod is: 1.3165073809 dBm or 1354.1 µW
 Optical power for channel number trans_mpod is: 0.262471814778 dBm or 1062.3 µW
 Optical power for channel number trans_mpod is: 1.20080134129 dBm or 1318.5 µW
 The nominal wavelenght for device trans_mpod is 845.0 nm ( ± 15.015  nm)
```

Hardware: IPMC

- We have successfully tested all relevant electrical connections to/from the IMPC, and verified their proper operation.
  - Due to limitations in obtaining IPMC software, however, this area has not been fully explored.
  - L1Calo uncertainty in IPMC choice has not helped clarify how to proceed in this area.
  - We are working with both LAPP and CERN IPMCs, possess sufficient LAPP IPMCs for the production run.



Other Hardware Aspects

Miscellaneous / Other

✔ 1. Verify that all 66 Front Panel LEDs are working and are of the correct color.

✔ 2. Verify the Physical aspects of this Hub card:

a. Dimensions look correct (e.g. none of the brackets are in backwards).

b. The board's corners are in good shape.

c. The Insertion and Extraction forces feel correct and are smooth.

d. The Front Panel Labels are clear and not scratched.

e. All of the backplane connectors line up in a straight row and are fully inserted.

f. Nothing is loose or likely to vibrate in the air flow (e.g. the discrete power wires or fiber optic ribbons, or power supply LC filter comps).

g. MiniPOD and FPGA heat sinks are correctly installed.

h. The MiniPODs are fully seated and screwed down.

i. The MiniPOD Fiber Optic Ribbon Cables are correctly routed and not blocking air flow.

✔ 3. Verify that all 9 ESD ground points are correctly connected so that the card is safe to handle.

✔ 4. Verify that the card auto-configures its FPGA from its Flash memory at power up

✔ 5. Verify that the ROD can control the open collector output signals from the Hub's Front Panel LEMO Connector.

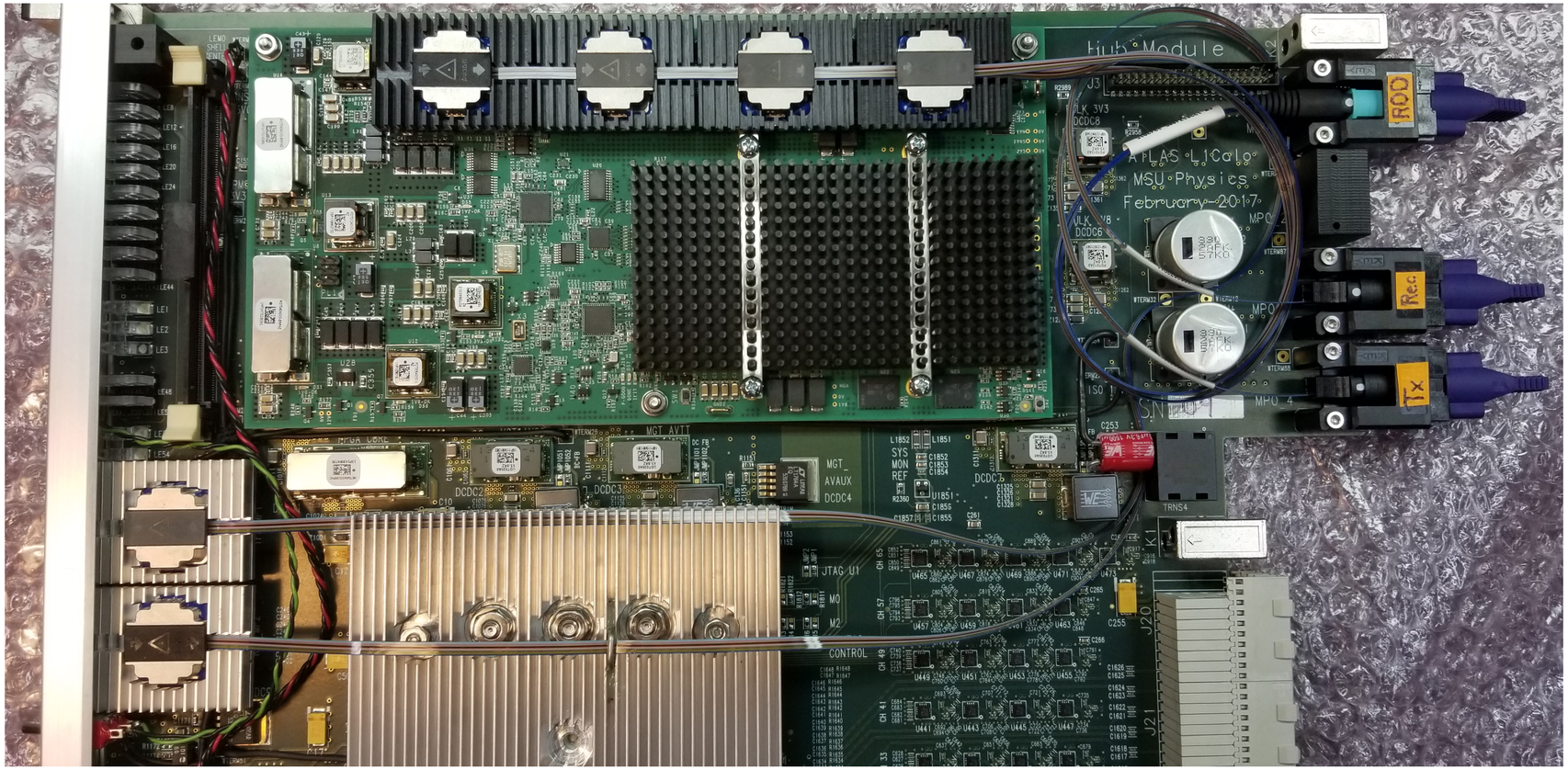
✔ 6. Verify the correct operation of the 4 Power Control signals and the 8 Spare TBD signals between the Hub and ROD cards.

✔ 7. Verify the correct fuses are installed.

✔ 8. Verify that both Front Panel FPGA output Access Signals are working OK.

Fiber Management

- The Hub/ROD routes fibers for six MiniPODs through Zone-3
  - The four ROD MiniPOD fiber ribbons cleverly bundle to one MPO, as seen in the picture.
  - The two Hub fiber ribbons are kept separate to simplify cabling in USA15.
    - Rx signals are required. External Tx link can be added in RTM in the future if required without disturbing the Rx optical fibers that bring the TTC signal.



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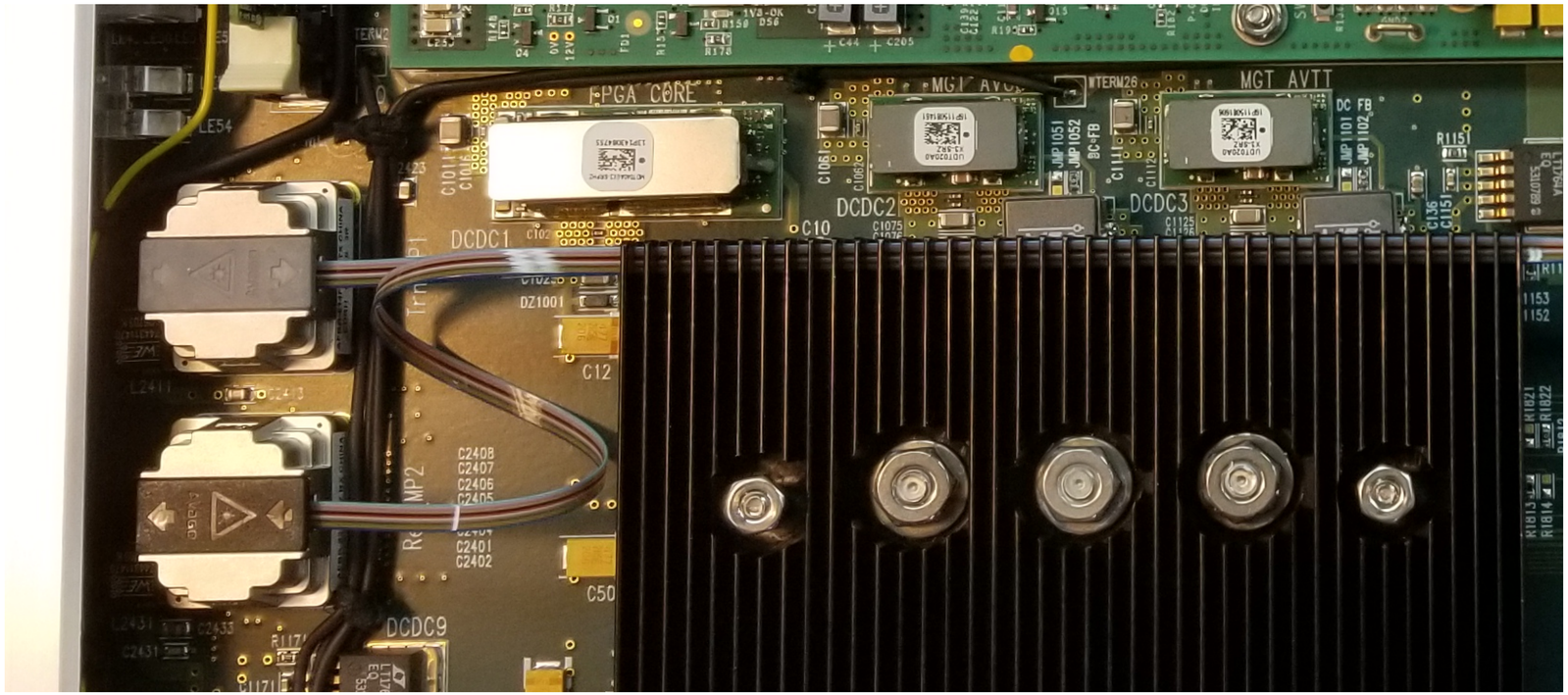
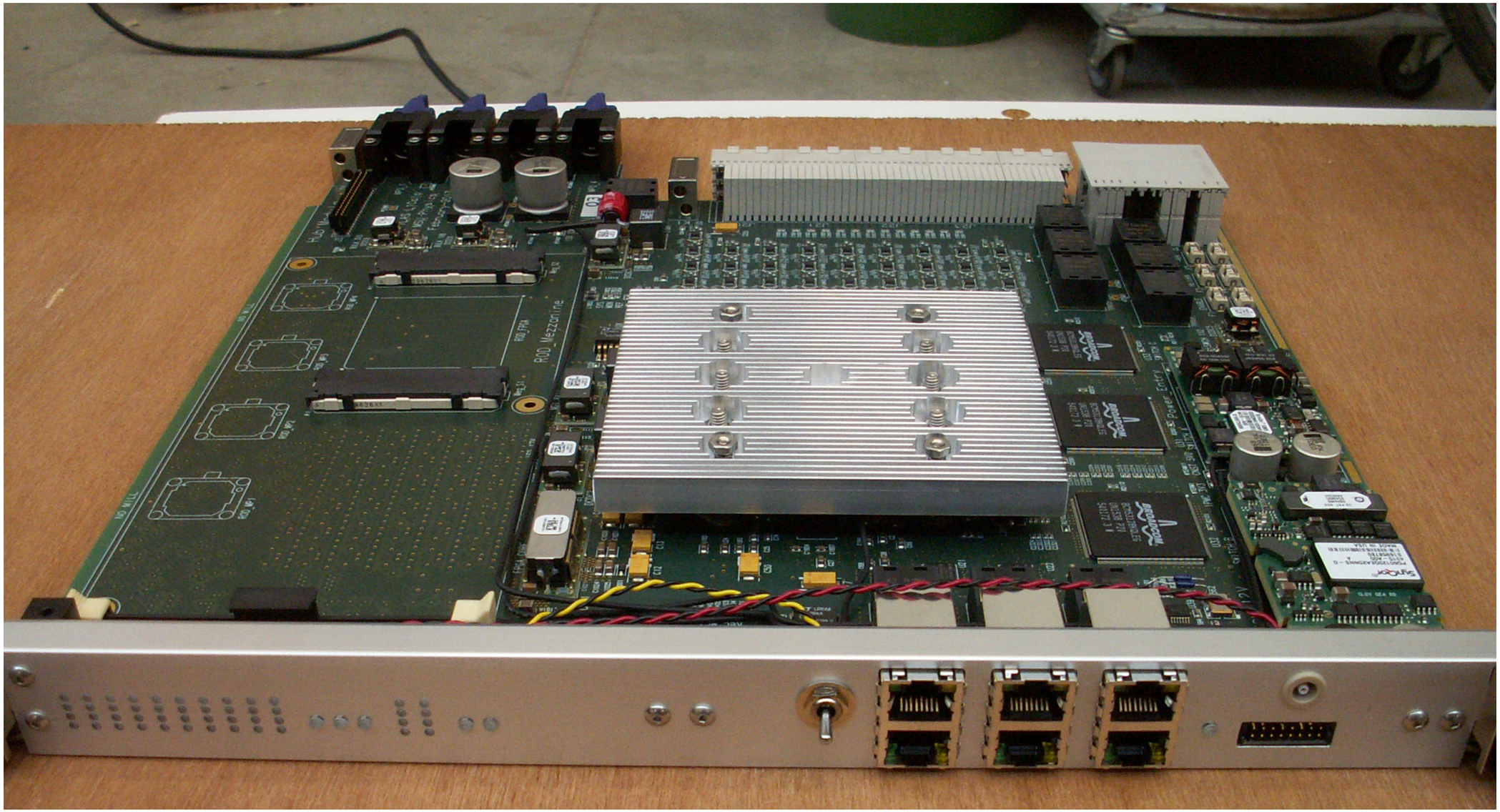


Front Panel



Front Panel

LEDs for each GbE connection: Each FEX slot, both connections on each Hub, connections between switch chips.

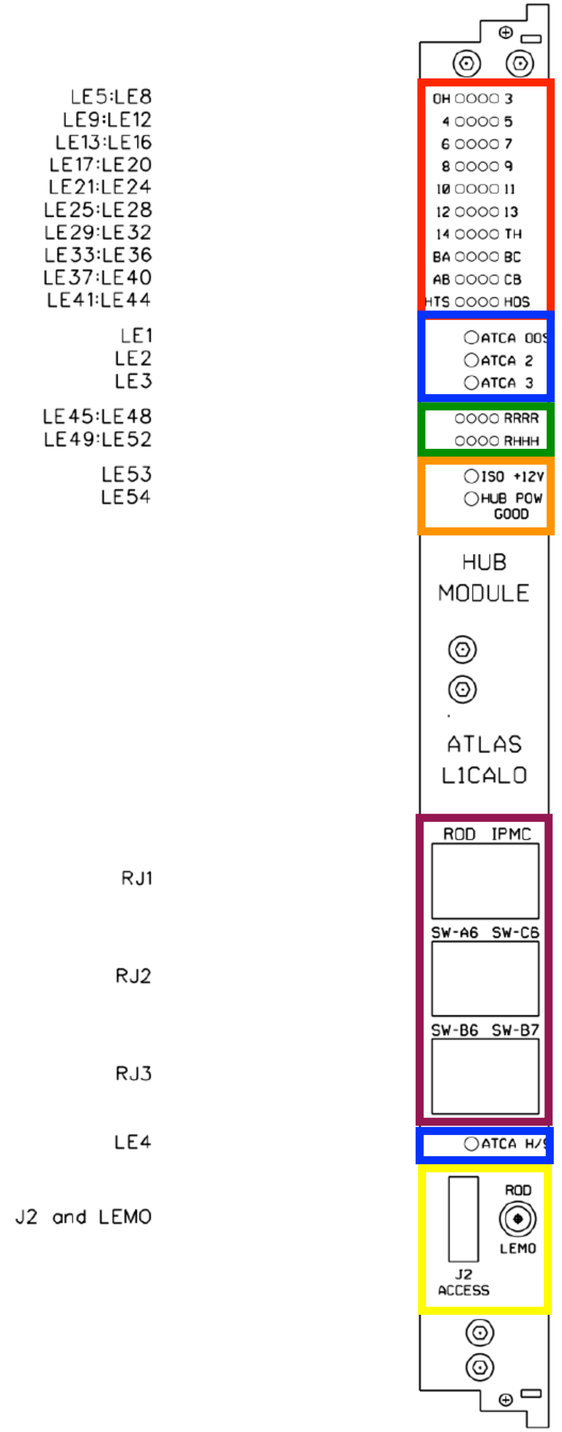
ATCA-required LEDs for IPMC

5 ROD-defined LEDs, 3 Hub “spare” LEDs

Hub power indicators

RJ45 protrusions

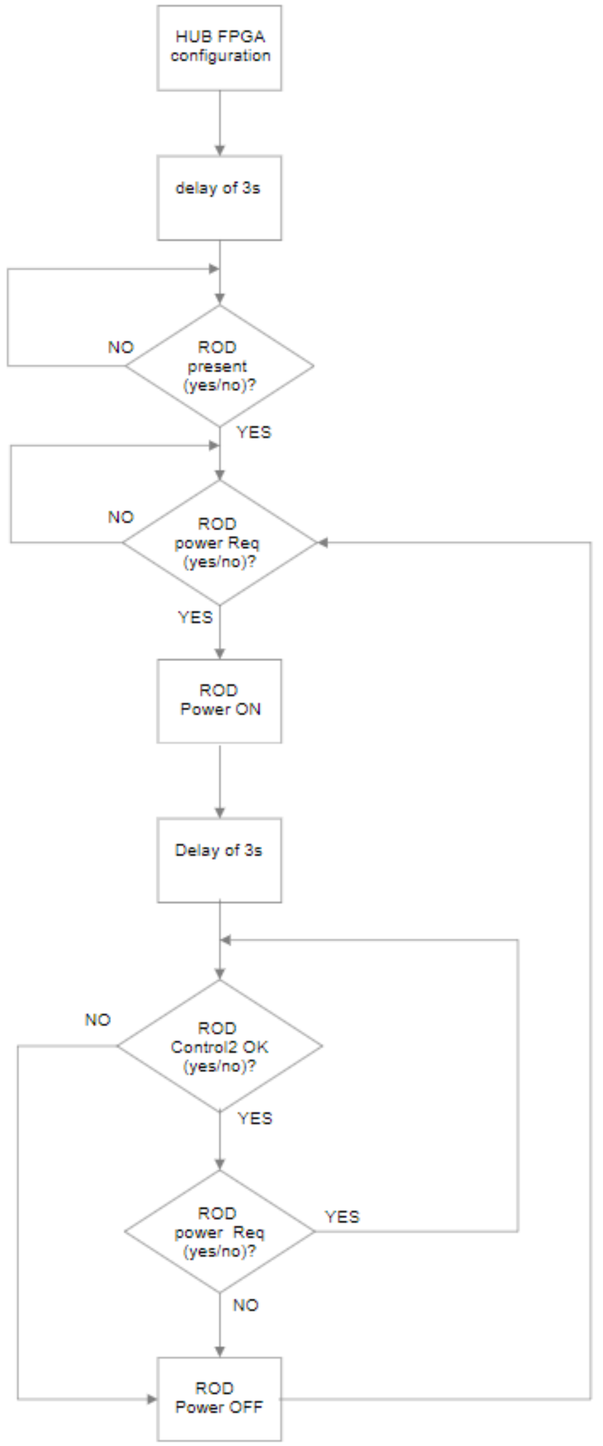
LEMO and JTAG/I2C protrusions



Core Firmware Aspects

ROD Power Up

- Hub controls ROD power up sequence using a state machine
  - There are currently three states considered
    - ROD Present (pull-down resistor on the ROD)
    - ROD Power Ctrl2 (ROD controlled power status)
    - ROD Power Request (IPbus register option)
      - NB: this is used for Hub testing and can be removed for final FW if desired.
  - There are currently two additional states that can be included as needed
    - ROD Power Ctrl3 (ROD configuration ready)
    - ROD SMB Alert (ROD power supply error)



1. Signals that are being used by the power up engine

1.a ROD_PRESENT_B_TO_FPGA

This signal is a pull-down resistor on the ROD. When the ROD is NOT present this signal goes HI on the Hub.

1.b ROD_Power_Control_2_FPGA

This is an input to the Hub's FPGA. When HI this signal indicates that all power supplies on the ROD are operating correctly.

ROD_Power_Enable
ROD_Power_Enable_B

These two signal are outputs from the Hub FPGA that through some hardwired logic on the Hub tell the ROD when it may turn ON its power supplies.

1.c ROD power request is controlled by the IPbus register

2. Signals that are not being used by the power up engine

2.a ROD_Power_Control_3_FPGA

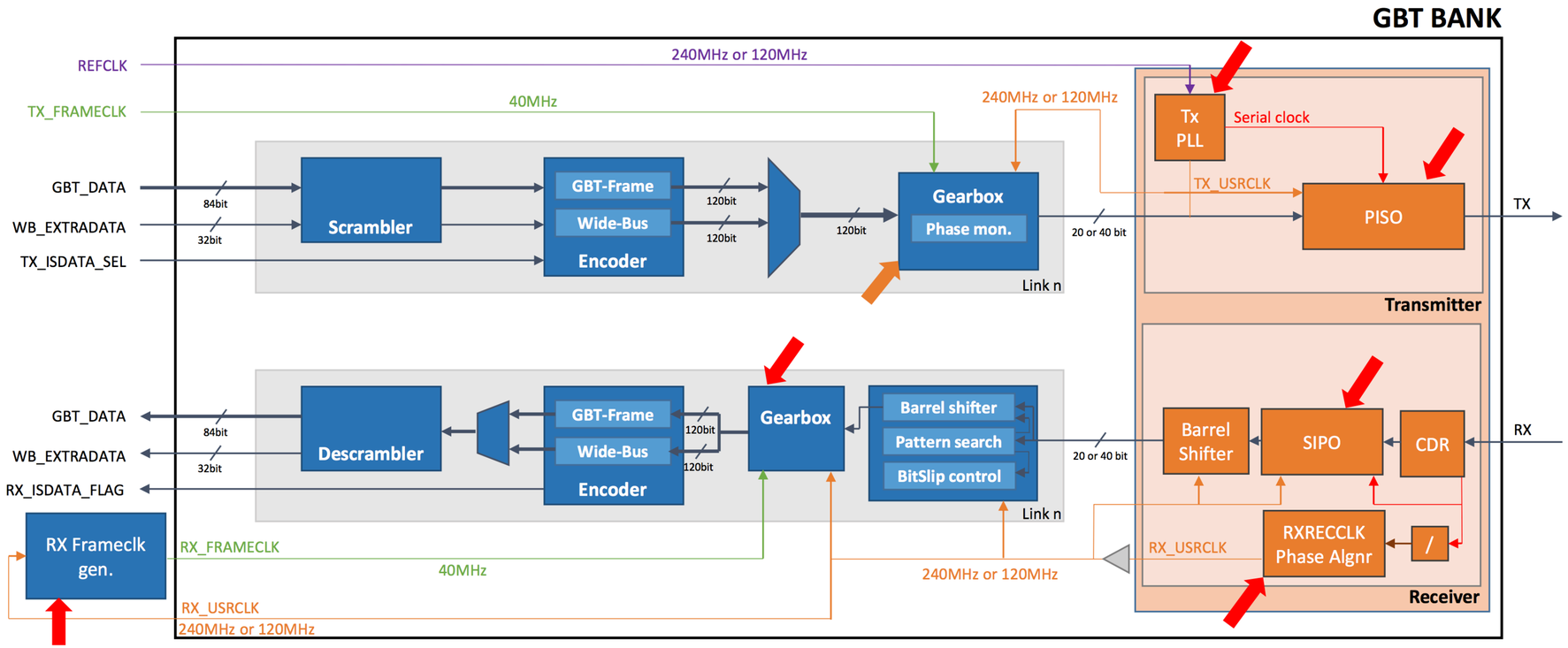
This is an input to the Hub's FPGA. When HI this signal indicates that the ROD is Configured and fully ready for normal L1Calo operation.

2.b FPGA_RODs_SMBALERT_B

This is an input to the Hub's FPGA that when LOW indicates a power supply problem on the ROD. During normal operation this signal should always be HI.

GBT/TTC Clock Recovery

- As stated previously, the LHC clock is recovered from the TTC signal provided via FELIX and decoded via the GBT firmware.
  - 120 MHz reference clock generated at MGT quad QPLL
  - All features of the firmware behave as expected
    - Stable, deterministic latency clock recovered and fanned out.



https://indico.cern.ch/event/489996/contributions/2291863/attachments/1345764/2028939/GBTTutorial_-_TWEPP2016.pdf

TTC/Combined Data Fanout

- To define the phase of the arrival of the TTC/Combined data, we use the LHC master clock as the reference. This minimizes the variation across the system and provides an easily-to-verify, stable reference.
  - 128 bits of control data are received from the ROD at a 6.4 Gbps line rate
    - This data is translated and merged with TTC data in the Hub (L1A, ECR, BCR)
  - 128 bits of TTC/Combined data are transmitted from the Hub at a 6.4 Gbps line rate
    - At the receiver, the data is transferred into a parallel register
  - The 128 bits of the TTC/Combined data are provided to the users at the output of a 128 bit wide D register.
    - The D register is updated on the positive edge of the FPGA's 40.08 MHz clock that is locked to the LHC backplane reference clock.
    - These 128 bits are stable at all times except during the update.

- Receiver FPGA requirements
  - MGT reference clock to receive the 6.4 Gbps link
  - 40.08 MHz clock locked to the LHC backplane reference clock

** The Readout Control and Combined TTC Specification (v0.5) is linked to the indico page.

Summary

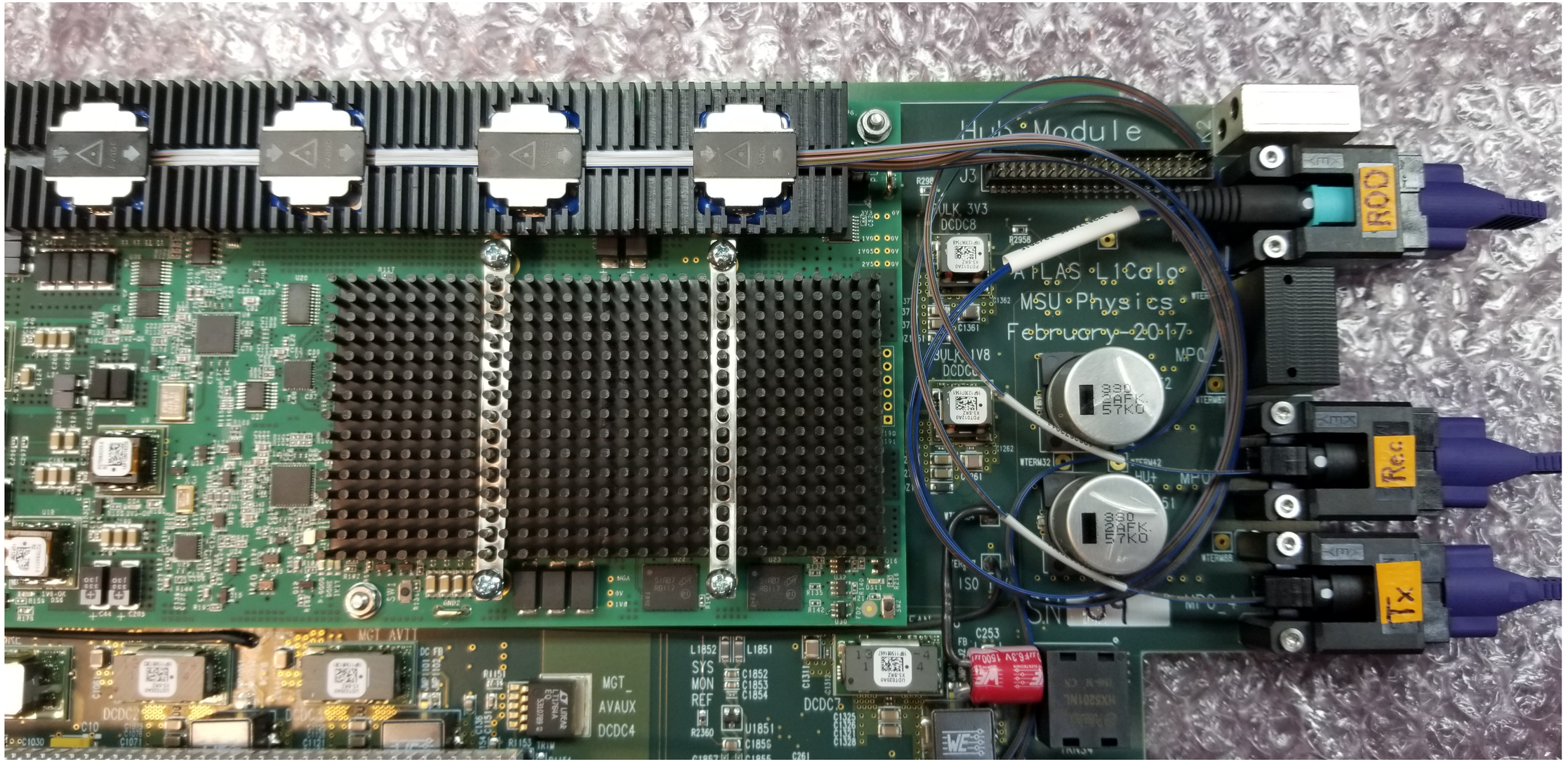
- Extended tests of the Hub PCB have been presented
  - Focus here on core functions of the Hub in the L1Calo system, as related to the hardware design
    - Additional test results are available for those interested.
      - https://web.pa.msu.edu/hep/atlas/l1calo/hub/
      - https://web.pa.msu.edu/hep/atlas/l1calo/htm/

- Eight Hub modules have been produced (+1 without an FPGA)
  - Six Hub modules have been tested in a full shelf with HTMs, and we plan to characterize the remaining 2 boards currently in the UK when possible.
    - Very high level of uniformity over the prototype run.
    - No residual issues identified in tests thus far.
    - No MGT errors of any kind observed on Hub or ROD.

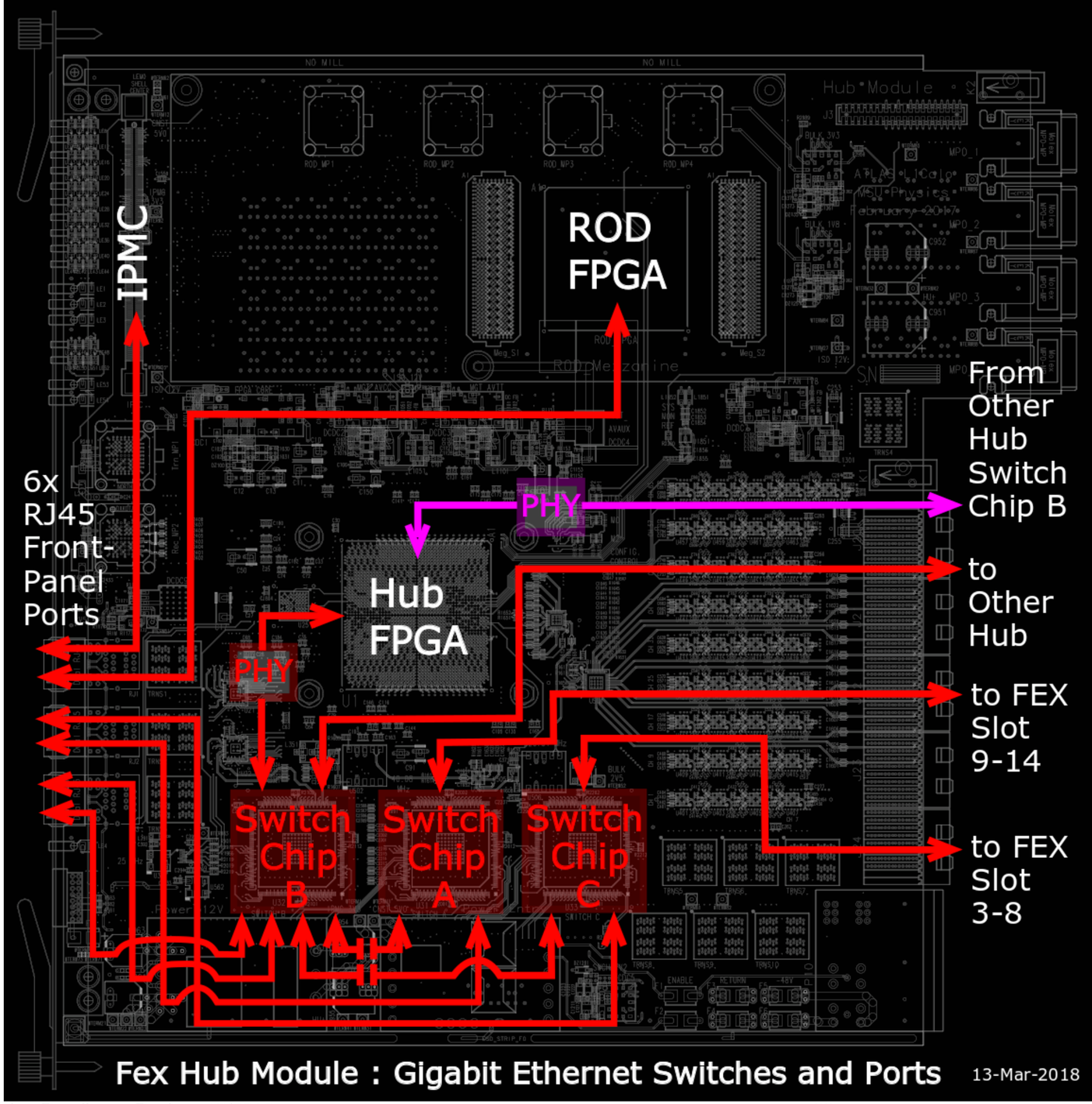
- Next presentation will cover the schedule goals for the Hub build.

Backup Slides

Fiber Management



Hub GbE Switch Layout



Hub Readout Path