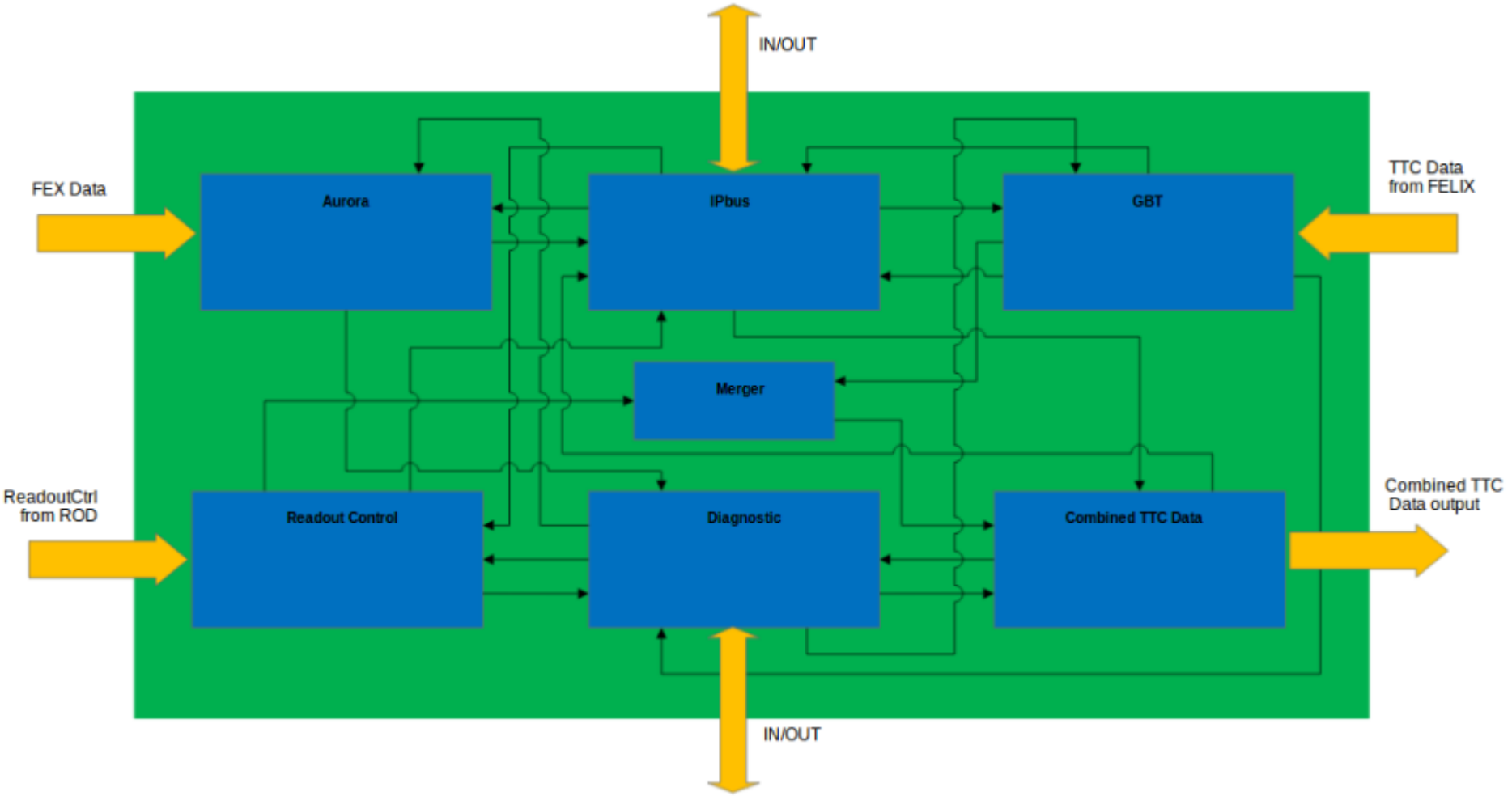
HUB FW overview

- HUB FW development process - split into several separate stages.
- IPbus → implemented and tested (passed)
- Readout Control (@6.4Gbps) → implemented and tested (passed)
- Combined TTC/Data (@6.4Gbps) → implemented and tested (passed)
- GBT (@4.8Gbps) → implemented and tested (passed)
- Aurora8b/10b (6.4 Gbps) → initially implemented and tested on the VU095
  Internal loopback tests on the HUB module
- Final step → merging process to provide the production firmware (HUB1 and HUB2)
- Slice Tests in Cambridge and MSU good occasion to validate the firmware
- Very comprehensive HUB diagnostic firmware includes several stages:
- (majority of these configurations are provided):
- - config 1: IBERT (all Quads) @ 6.4 Gbps
- - config 2: IBERT (all Quads) @10.24 Gbps
- - config 3: IBERT (all Quads) @ 6.4 Gbps; integrated with the IPbus
- - config 4: IBERT (all Quads - Quad224) @ 6.4 Gbps; integrated with the IPbus and GBT
- - config 5: IBERT (all Quads) @ 6.4 Gbps; integrated with the IPbus and GBT
- - config 6: IBERT (all Quads) @10.24 Gbps; integrated with the IPbus and GBT
- - config 7: IBERT (all Quads) @ 6.4 Gbps; integrated with the GBT, IBERT controlled by IPbus
- - config 8: IBERT (all Quads) @10.24 Gbps; integrated with the GBT, IBERT controlled by IPbus

HUB FW diagram



GBT, Combined_TTC/DATA overview

- HUB module is obliged to distribute TTC information throughout the shelf.
- The combined_TTC/DATA bits are defined to provide TTC information as well
- as initialization functions (Aurora).The link is set to run at 6.4Gbps raw rate
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- The HUB uses MiniPOD optical receiver to receive TTC signals (GBT) from the FELIX system
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- Receive the Reset signal (Aurora Initialization) from the Readout_CTRL stream,
- then merging with the TTC info and distribute it to the appropriate shelf slot
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- Several Combined_TTC links within the shelf; each FEX slot (3-14); one between
- each HUB and ROD; links between two HUBs
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- Combined_TTC/DATA links on the HUB FPGA is implemented with use of several
- components, including the MGT transceivers (GTH and GTY), control and diagnostic logic

Combined_TTC/DATA Physical Implementation

- The Combined_TTC/Data link on the HUB FPGA is implemented with the use of several components,
- including the MGT transceivers (GTH and GTY), control and the diagnostic logic.
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- The Combined_TTC/DATA link is designed to operate at 6.4 Gbps.
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- The physical implementation of the Combined_TTC/DATA stream assumes that there are 4 Control Registers on the Hub TX side, and Shadow Registers on the Rx side (Receiver: FEX, ROD and other HUB).
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- The transmitter side generates the 128 bit message from 4 Control registers: Word_0, Word_1,
- Word_2, and Word_3. The transmitter side logic is in charge to write control information into these
- Control Registers. The contents of these registers are continuously transmitted to the modules
- (within the shelf) which receives the data into a duplicate set of 4 registers referred to as shadow registers. Anything written into a Control Register at the transmitter side will appear in the corresponding Shadow register at the receiving side within the following LHC clock.
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- The least significant byte of Word_0 is reserved for the 8b10b Comma character K28.5.
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Combined_TTC/DATA Bit definition

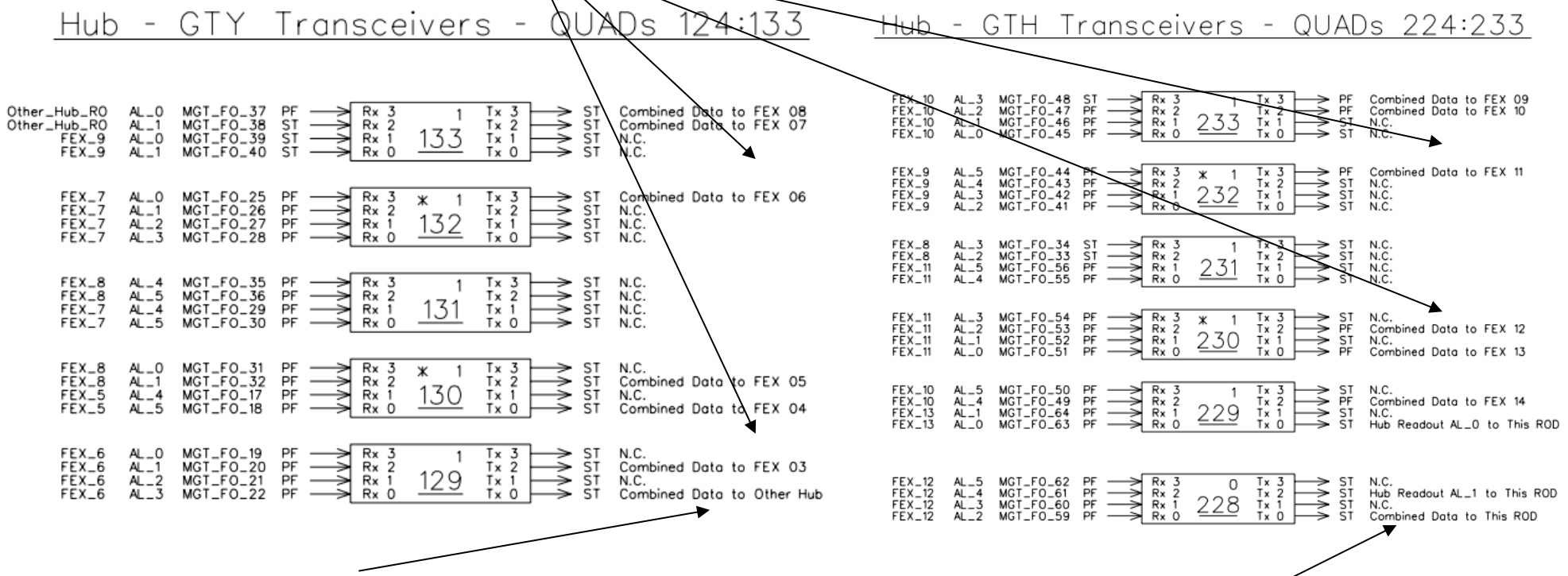
Combined_TTC/DATA bit definitions:
The least significant byte of Word_0 is reserved for the 8b10b Comma Character K28.5

word 0			word 1			word 2			word 3	
bit	0XBC = K28.5		bit			bit			bit	
0	0		0	L1ID(0)		0	control channel		0	Link_reset(0)
1	0		1	L1ID		1	control channel		1	Link_reset(1)
2	1		2	L1ID		2	control channel		2	Link_reset(2)
3	1		3	L1ID		3	control channel		3	Link_reset 3
4	1		4	L1ID		4	control channel		4	Link_up(0)
5	1		5	L1ID		5	control channel		5	Link_up(1)
6	0		6	L1ID		6	control channel		6	Link_up(2)
7	1		7	L1ID		7	control channel		7	Link_up(3)
8	version(0)		8	L1ID		8	control channel		8	Link Enable(0)
9	version(1)		9	L1ID		9	control channel		9	Link Enable(1)
10	version(2)		10	L1ID		10	control channel		10	Link Enable(2)
11	version(3)		11	L1ID		11	control channel		11	Link Enable(3)
12			12	L1ID		12	control channel		12	ROD XOFF
13			13	L1ID		13	control channel		13	0 (ROD reserved)
14			14	L1ID		14	control channel		14	0 (ROD reserved)
15	reserved		15	L1ID		15	control channel		15	0 (ROD reserved)
16	L1A		16	L1ID		16	control channel		16	0 (ROD reserved)
17	BCR		17	L1ID		17	control channel		17	0 (ROD reserved)
18	ECR		18	L1ID		18	control channel		18	0 (ROD reserved)
19	Privileged Readout		19	L1ID		19	control channel		19	shelf(0)
20	felix_backpressure(0)		20	L1ID		20	control channel		20	shelf(1)
21	felix_backpressure(1)		21	L1ID		21	control channel		21	shelf (2)
22	felix_backpressure(2)		22	L1ID		22	control channel		22	shelf(3)
23	felix_backpressure(3)		23	L1ID(23)		23	control channel		23	CRC (9-bit)
24	felix_backpressure(4)		24	ECRID(0)		24	control channel		24	CRC (9-bit)
25	felix_backpressure(5)		25	ECRID(1)		25	control channel		25	CRC (9-bit)
26	felix_backpressure(6)		26	ECRID(2)		26	control channel		26	CRC (9-bit)
27	felix_backpressure(7)		27	ECRID(3)		27	control channel		27	CRC (9-bit)
28	felix_backpressure(8)		28	ECRID(4)		28	control channel		28	CRC (9-bit)
29	felix_backpressure(9)		29	ECRID(5)		29	control channel		29	CRC (9-bit)
30	felix_backpressure(10)		30	ECRID(6)		30	control channel		30	CRC (9-bit)
31	felix_backpressure(11)		31	ECRID(7)		31	control channel		31	CRC (9-bit)

Specification for Readout Control & Combined TTC Serial links in L1Calo (ver.0.5)

Combined_TTC/DATA Link placement

Links between each FEX slot and HUB



Link between two HUBs

Link between the ROD and HUB

Readout_Control overview

- The HUB module is obliged to receive the Readout Control (Readout_CTRL) information from the ROD via serial link named Readout_CTRL. The HUB module is the only one module within the shelf which gets the Readout Control data from the ROD
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- That information is used by the Hub, also fanned out to the rest of the system. The main purpose is to provide resets to all of the data links (Aurora) between the Fex's and the ROD plus HUB module
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Readout_Control
Physical Implementation

- The Readout_Ctrl link on the HUB module is implemented with the use of MGT Transceiver GTH, control and diagnostic logic
- The Readout_Ctrl link is designed to operate at 6.4 Gbps.
- In order to to control message transmission within a single LHC clock period, the length of the message is limited to 128 bits
- The HUB Readout Control FW features one receiver (RX). In order to debug the design, the standard Xilinx diagnostic components are being used to monitor the data flow (as for example like the ILA and VIO).
- The physical layer is configured with the use of GT wizard
- The physical implementation of the Readout_CTRL links assumes that there are Control Registers on the Tx ROD side, and Shadow Registers on the Rx HUB side. The transmitter side generates the 128 bit message from 4 Control registers: Word_0, Word_1, Word_2, and Word_3. The transmitter side logic is in charge to write control information into these registers for transmission to the modules within the shelf. These registers are continuously transmitted to the HUB which receives the data into a duplicate set of 4 registers referred to as Shadow Registers. Anything written into a Control Register at the transmitter side will appear in the corresponding Shadow register at the receiving side within the following LHC clock.

Control and Shadow Register

There are Control Registers on the TX side and Shadow Register on the RX side

Figure 1: Control and Shadow Registers

Readout_Control
Bit definition

- The bits within the Readout Control words are primarily defined to provide initialization functions for
- all of the FEX data links
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word 0		word 1		word 2		word 3	
bit	OXBC = K28.5	bit		bit		bit	
0	0	0	slot 3 link reset	0	slot 3 channel up	0	slot 3 Link Enable
1	0	1	slot 4 link reset (0)	1	slot 4 channel up (0)	1	slot 4 Link Enable
2	1	2	slot 5 link reset (0)	2	slot 5 channel up (0)	2	slot 5 Link Enable
3	1	3	slot 6 link reset	3	slot 6 channel up	3	slot 6 Link Enable
4	1	4	slot 7 link reset	4	slot 7 channel up	4	slot 7 Link Enable
5	1	5	slot 8 link reset (0)	5	slot 8 channel up (0)	5	slot 8 Link Enable
6	0	6	slot 9 link reset (0)	6	slot 9 channel up (0)	6	slot 9 Link Enable
7	1	7	slot 10 link reset	7	slot 10 channel up	7	slot 10 Link Enable
8	version 0	8	slot 11 link reset	8	slot 11 channel up	8	slot 11 Link Enable
9	version 1	9	slot 12 link reset (0)	9	slot 12 channel up (0)	9	slot 12 Link Enable
10	version 2	10	slot 13 link reset (0)	10	slot 13 channel up (0)	10	slot 13 Link Enable
11	version 3	11	slot 14 link reset	11	slot 14 channel up	11	slot 14 Link Enable
12	0	12	0	12	0	12	0
13	0	13	slot 4 link reset (1)	13	slot 4 channel up (1)	13	0
14	ROD XOFF (to all slots)	14	slot 4 link reset (2)	14	slot 4 channel up (2)	14	0
15	Global Link Reset	15	slot 4 link reset (3)	15	slot 4 channel up (3)	15	0
16	0	16	slot 5 link reset (1)	16	slot 5 channel up (1)	16	0
17	0	17	slot 5 link reset (2)	17	slot 5 channel up (2)	17	0
18	0	18	slot 5 link reset (3)	18	slot 5 channel up (3)	18	0
19	0	19	slot 8 link reset (1)	19	slot 8 channel up (1)	19	shelf (0)
20	0	20	slot 8 link reset (2)	20	slot 8 channel up (2)	20	shelf (1)
21	0	21	slot 8 link reset (3)	21	slot 8 channel up (3)	21	shelf (2)
22	0	22	slot 9 link reset (1)	22	slot 9 channel up (1)	22	shelf (3)
23	0	23	slot 9 link reset (2)	23	slot 9 channel up (2)	23	CRC (9- bit)
24	0	24	slot 9 link reset (3)	24	slot 9 channel up (3)	24	CRC (9- bit)
25	0	25	slot 12 link reset (1)	25	slot 12 channel up (1)	25	CRC (9- bit)
26	0	26	slot 12 link reset (2)	26	slot 12 channel up (2)	26	CRC (9- bit)
27	0	27	slot 12 link reset (3)	27	slot 12 channel up (3)	27	CRC (9- bit)
28	0	28	slot 13 link reset (1)	28	slot 13 channel up (1)	28	CRC (9- bit)
29	0	29	slot 13 link reset (2)	29	slot 13 channel up (2)	29	CRC (9- bit)
30	0	30	slot 13 link reset (3)	30	slot 13 channel up (3)	30	CRC (9- bit)
31	0	31	0	31	0	31	CRC (9- bit)

Specification for Readout Control & Combined TTC Serial links in L1Calo (ver.0.5)