Specification for
Readout Control & **Combined TTC/Data**
Serial links in L1Calo

Version 0.5

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History

0.0 EF: Original

0.1 EF: Added ‘channel up’ signals to Readout Control link and added ‘Privileged Readout’, ‘ECRID’, and ‘ROD N Channel Up’ to the Combined TTC/Data link

0.2 EF:

0.3 EF: Added Felix Backpressure to Combined TTC WORD(0) bits(20-31)

0.4 EF: Separated general information off into “General Architecture” section

EF: Added clarification regarding information sent from Hub-1 versus Hub-2

EF: Combined TTC expanded to include four “Link_up” bits and four “Link_enable” bits in order to accommodate the four Aurora channels on each jFEX board.

EF: Readout Control expanded to include four “Channel_up” bits per slot for slots 3-8. These are to provide status for each of the four Aurora links on the jFEX (6 slots for the 6 modules). The original bits have changed position from WORD 0 to WORD 2.

0.5 EF: Readout_control bit definition:
Re-arranged link resets and channel-up flags to separate the three additional jFEX links per board. This allows the possibility for future jFEX changes without affecting the eFEx bit definitions.
EF: Combined_TTC: Updated description of Felix Backpressure
EF: Combined_TTC; removed “reset(3:0)” bits from word_0(15:12) There were no Readout_CTRL bits to map to these CTTC bits.
EF: updated paragraph numbering
EF: added comments regarding link reliability

1 General Architecture

The *Readout Control* link is broadcast by the ROD to the Hub. It contains status and control information regarding the Aurora and other backplane information. The Hub takes this information and distributes it to all of the Node Modules, along with the Atlas TTC information via the *Combined TTC* link.

1.1 ROD-1/Hub-1 versus Rod-2/Hub-2

ROD-1 transmits the Readout_Control link to Hub-1. Hub-1 then uses information from this link, combined with the incoming Atlas TTC information to form the Hub-1 Combined_TTC Link. This Hub-1 Combined_TTC information is then broadcast to all of the Node modules as well as ROD-1. The TTC information is also sent to Hub-2.

ROD-2 transmits its Readout_Control link to Hub-2. Hub-2 then uses information from this link, combined with the incoming Atlas TTC information to form the Hub-2 Combined_TTC Link. This Hub-2 Combined_TTC information is then transmitted to the ROD-2. Hub-2 also broadcasts some subset of this information to all of the Node modules over the Hub-2 Combined_TTC link. The information in this link contains all of the necessary information from the ROD-2 Readout Control, but may not contain any of the TTC related information.

Node Modules should sample any required TTC information from the Hub-1 Link. Node Modules should sample Link Control and Status information as appropriate from each of the Hub-1 and Hub-2 Combined TTC links.

1.2 Physical Implementation

Both the Combined_TTC and Readout_Ctrl links are implemented with MGT Transceivers, control logic, and the four main data registers. It is set to run at 6.4Gbps raw rate. When 8b/10b overhead is accounted for, the effective rate is reduced to 6.4 * 0.8 = 5.12Gbps. In order to fit control message transmission within a single LHC clock period, the length of the message is limited to 128 bits.

$$(1/(6.4\text{Gbps} * 0.8)) * 128 \text{ bits} = 25\text{nS} = 1/40\text{MHz}$$

1.3 Control and Shadow Registers

The transmitter side generates the 128 bit message from 4 Control registers: Word_0, Word_1, Word_2, and Word_3. The transmitter writes control information into these registers for transmission to the receiver. These registers are repeatedly/continuously transmitted over the link. In the receiver, the data is placed into a duplicate set of 4 registers referred to as shadow registers. Anything written into a transmitter Control Register will appear in the corresponding receiver Shadow register within the following LHC clock. (note: latency may be greater depending upon synchronisation)

The least significant byte of Word_0 is reserved for the 8b10b Comma character K28.5.

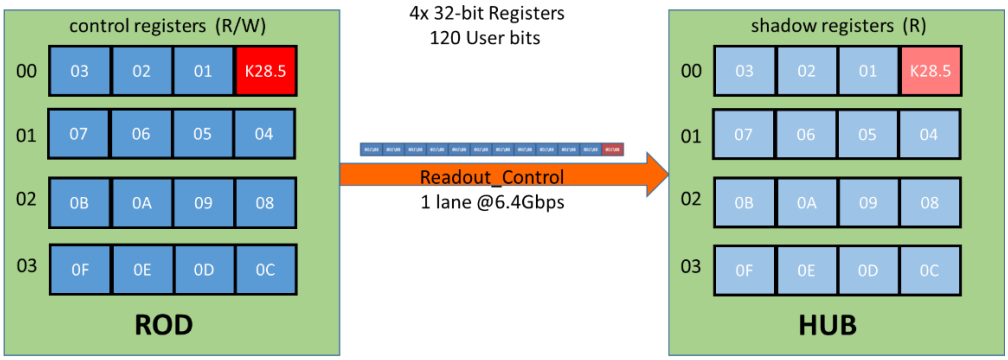

Figure 1: Control and Shadow Register

1.4 Link Reliability

Both the Readout_CTRL and Combined_TTC contain CRC fields to help ensure reliability. If the receiver detects a CRC error, it must assume that all four broadcast words are corrupted and must be rejected.

Any bits that the transmitter may activate for only a single cycle are at risk of being lost if a crc error occurs. Control bits should therefore be driven valid for multiple cycles where possible. However, in some cases, this is not possible. See individual bit definitions for how these are handled.

If a Readout_CTRL or Combined_TTC link goes down, the receiver will see multiple, consecutive CRC errors.

If the ROD receives multiple consecutive CRC errors, it will reset the Hub and ROD Readout_CTRL and Combined_TTC links.

If the Hub receives multiple consecutive CRC errors from the ROD, it should…….. (Action to be defined) (Probably reset itself, and the rod if we can define a signal)

If a Node receives multiple consecutive CRC errors from the HUB, it should…….. (Action to be defined) (Probably reset its receiver. Perhaps it could send a UFC message to the ROD and/or Hub?)

2 Readout Control (Readout_Ctrl)

The Readout Control serial link, named Readout_CTRL in the design, is transmitted from the ROD to the Hub only. It contains control information that is used by the Hub, and is also fanned out to the rest of the system. The main purpose is to provide resets to all of the data links (Aurora) between the Fex's and the ROD.

2.1 Control Bit Definition

The bits within the Readout Control words are primarily defined to provide initialisation functions for all of the Node data links.

Readout_CTRL register bit definitions									
word 0		**word 1**		**word 2**		**word 3**	
bit	0XBC = K28.5	**bit**		**bit**		**bit**	
0	0	0	slot 3 link reset	0	slot3 channel up	0	slot 3 Link Enable
1	0	1	slot 4 link reset (0)	1	slot4 channel up(0)	1	slot 4 Link Enable
2	1	2	slot 5 link reset (0)	2	slot5 channel up(0)	2	slot 5 Link Enable
3	1	3	slot 6 link reset	3	slot6 channel up	3	slot 6 Link Enable
4	1	4	slot 7 link reset	4	slot7 channel up	4	slot 7 Link Enable
5	1	5	slot 8 link reset (0)	5	slot8 channel up(0)	5	slot 8 Link Enable
6	0	6	slot 9 link reset (0)	6	slot9 channel up(0)	6	slot 9 Link Enable
7	1	7	slot 10 link reset	7	slot10 channel up	7	slot 10 Link Enable
8	version 0	8	slot 11 link reset	8	slot11 channel up	8	slot 11 Link Enable
9	version 1	9	slot 12 link reset (0)	9	slot12 channel up(0)	9	slot 12 Link Enable
10	version 2	10	slot 13 link reset (0)	10	slot13 channel up(0)	10	slot 13 Link Enable
11	version 3	11	slot 14 link reset	11	slot14 channel up	11	slot 14 Link Enable
12	0	12	0	12	0	12	0
13	0	13	slot 4 link reset (1)	13	slot4 channel up (1)	13	0
14	ROD_XOFF (to all slots)	14	slot 4 link reset (2)	14	slot4 channel up (2)	14	0
15	Global_Link_Reset	15	slot 4 link reset (3)	15	slot4 channel up (3)	15	0
16	0	16	slot 5 link reset (1)	16	slot5 channel up (1)	16	0
17	0	17	slot 5 link reset (2)	17	slot5 channel up (2)	17	0
18	0	18	slot 5 link reset (3)	18	slot5 channel up (3)	18	0
19	0	19	slot 8 link reset (1)	19	slot8 channel up (1)	19	shelf(0)
20	0	20	slot 8 link reset (2)	20	slot8 channel up (2)	20	shelf(1)
21	0	21	slot 8 link reset (3)	21	slot8 channel up (3)	21	shelf (2)
22	0	22	slot 9 link reset (1)	22	slot9 channel up (1)	22	shelf(3)
23	0	23	slot 9 link reset (2)	23	slot9 channel up (2)	23	CRC (9-bit)
24	0	24	slot 9 link reset (3)	24	slot9 channel up (3)	24	CRC (9-bit)
25	0	25	slot 12 link reset (1)	25	slot12 channel up (1)	25	CRC (9-bit)
26	0	26	slot 12 link reset (2)	26	slot12 channel up (2)	26	CRC (9-bit)
27	0	27	slot 12 link reset (3)	27	slot12 channel up (3)	27	CRC (9-bit)
28	0	28	slot 13 link reset (1)	28	slot13 channel up (1)	28	CRC (9-bit)
29	0	29	slot 13 link reset (2)	29	slot13 channel up (2)	29	CRC (9-bit)
30	0	30	slot 13 link reset (3)	30	slot13 channel up (3)	30	CRC (9-bit)
31	0	31	0	31	0	31	CRC (9-bit)

Table 1: Readout_Ctrl bit assignments

2.1.1 Comma Character

Bits 7 to 0 of Word_0 contain the Comma character that maintains alignment of the 4 shadow registers with their corresponding Control registers. The chosen character is K28.5 = 0xBC.

2.1.2 Version

The 4-bit value contains the version number of this overall bit assignment. It will be held at “0000” through the initial debug phases, where many changes may occur.

2.1.3 ROD_XOFF

When active, this signal indicates that the ROD cannot currently accept further data from Fex sources. This signal is fanned-out to the shelf FEX’s by the Hub via the Combined_TTC link. This control halts data from ALL FEX’ s as a group. There is no mechanism for halting individual FEX’s.

This bit remains active for the duration of the time that data should be paused.

2.1.4 Global_Link_Reset

This single bit is used to reset **ALL** of the data (Aurora) links within the shelf. The primary use is in the first initialisation after power-up. The ROD can hold this reset active for an indefinite amount of time. On the trailing edge (deactivation), the eFex’s should provide additional timing control for the

GTReset and Reset signals on the Aurora interface. This signal is fanned-out to the shelf FEX's by the Hub via the Combined_TTC link.

2.1.5 Slot_N_link_reset_M

These signals allow the ROD to reset **individual** links providing data to it. It is asserted when the ROD is attempting to bring up a link which has gone down for some reason.

The appropriate bits (as defined by logical slot) are placed into the Combined_TTC link to each node by the Hub. Within the Combined_TTC link, they are referred to as Link_Reset[3:0].

The node module (FEX) should use the signal to reset its Aurora interface plus any additional logic required to resume normal data transmission.

The active time of these bits is indeterminate, and may be only a few broadcast cycles. On the trailing edge (deactivation), the nodes should provide additional timing control for the GTReset and Reset signals on the Aurora interface.

The jFEX modules will electrically connect to logical slots 04, 05, 08, 09, 12, and 13. Each jFEX module has four independent Aurora data links which can be controlled separately. Four independent Link Resets are therefore provided for these logical slots.

In slots where multiple resets are provided, eFEX modules, having only one Aurora interface, should use only the M=0 reset bits.

2.1.6 Slot N Channel Up M

These bits report on whether each slot's Aurora Channel is 'UP' or 'Down'. The information is rebroadcast to each FEX slot in the so that the Aurora transmitter knows if the receiver side of the channel (the ROD) is up. If a channel goes down, the ROD shall attempt to reset both Rx and Tx ends of the link.

Slots 3-8 have four channel up status bits each. This is to cover the case of jFex where each of four processors has its own data link to the ROD. It is expected that eFex boards in these slots will only use the M=0 Channel Up bit.

2.1.7 Slot N Link Enable

The ROD may disable the links from some boards within the shelf. This would happen in the case where a link reset had been applied, however the link still does not come up. It can also be used during commissioning to eliminate processing of selected slots. Note that in the case of jFEX, all four aurora links should be disabled if the slot enable is not present ('1')

2.1.8 Shelf Number

These bits are currently reserved. There is a possibility to derive the Shelf Number from a rotary switch on the ROD. Use of this option is still TBD

2.1.9 CRC (9-bit)

CRC is included to provide additional robustness on this link. Erroneous resets could cause loss of data. Choice of polynomial is from https://users.ece.cmu.edu/~koopman/crc/index.html

The chosen polynomial is 0x17d in Koopman format of 0x2fb in explicit+1 format.

The CRC is calculated over all four words of each transmission. When a CRC error occurs, all four of the associated words must therefore be ignored.

All bits within the four-word broadcast will be held active for at least two four-word broadcast periods in order to reduce the probability of missing an active signal due to CRC error.

3 Combined TTC/Data (Combined_TTC)

There are several Combined_TTC links within the shelf; one between each Node (Fex) slot (slots 3-14) and each Hub. There is also one between each Hub and ROD pair. These links distribute TTC information throughout the shelf. In addition, they incorporate the appropriate Link Reset information from the Readout_Ctrl link and distribute it to the appropriate shelf slot.

3.1 Physical Implementation

The physical implementation of the Combined_TTC links is similar to that of the Readout_Ctrl link. There are control registers on the Tx (Hub) side, and Shadow registers on the Rx side.

3.2 Control Bit Definition

The bits within the Combined_TTC control words are primarily defined to provide TTC information as well as initialisation functions for all of the Node data links (Aurora). The TTC information is sourced from a dedicated TTC interface on the Hub. The initialisation information is sourced from the ROD via the Readout_Ctrl link.

word 0			word 1			word 2			word 3	
bit	0XBC = K28.5		bit			bit			bit	
0	0		0	L1ID(0)		0	control channel		0	Link_reset(0)
1	0		1	L1ID		1	control channel		1	Link_reset(1)
2	1		2	L1ID		2	control channel		2	Link_reset(2)
3	1		3	L1ID		3	control channel		3	Link_reset 3
4	1		4	L1ID		4	control channel		4	Link_up(0)
5	1		5	L1ID		5	control channel		5	Link_up(1)
6	0		6	L1ID		6	control channel		6	Link_up(2)
7	1		7	L1ID		7	control channel		7	Link_up(3)
8	version(0)		8	L1ID		8	control channel		8	Link Enable(0)
9	version(1)		9	L1ID		9	control channel		9	Link Enable(1)
10	version(2)		10	L1ID		10	control channel		10	Link Enable(2)
11	version(3)		11	L1ID		11	control channel		11	Link Enable(3)
12			12	L1ID		12	control channel		12	ROD XOFF
13			13	L1ID		13	control channel		13	0 (ROD reserved)
14			14	L1ID		14	control channel		14	0 (ROD reserved)
15	reserved		15	L1ID		15	control channel		15	0 (ROD reserved)
16	L1A		16	L1ID		16	control channel		16	0 (ROD reserved)
17	BCR		17	L1ID		17	control channel		17	0 (ROD reserved)
18	ECR		18	L1ID		18	control channel		18	0 (ROD reserved)
19	Privileged Readout		19	L1ID		19	control channel		19	shelf(0)
20	felix_backpressure(0)		20	L1ID		20	control channel		20	shelf(1)
21	felix_backpressure(1)		21	L1ID		21	control channel		21	shelf (2)
22	felix_backpressure(2)		22	L1ID		22	control channel		22	shelf(3)
23	felix_backpressure(3)		23	L1ID(23)		23	control channel		23	CRC (9-bit)
24	felix_backpressure(4)		24	ECRID(0)		24	control channel		24	CRC (9-bit)
25	felix_backpressure(5)		25	ECRID(1)		25	control channel		25	CRC (9-bit)
26	felix_backpressure(6)		26	ECRID(2)		26	control channel		26	CRC (9-bit)
27	felix_backpressure(7)		27	ECRID(3)		27	control channel		27	CRC (9-bit)
28	felix_backpressure(8)		28	ECRID(4)		28	control channel		28	CRC (9-bit)
29	felix_backpressure(9)		29	ECRID(5)		29	control channel		29	CRC (9-bit)
30	felix_backpressure(10)		30	ECRID(6)		30	control channel		30	CRC (9-bit)
31	felix_backpressure(11)		31	ECRID(7)		31	control channel		31	CRC (9-bit)

Table 2: Combined TTC/Data bit definitions

3.2.1 Comma Character

Bits 7 to 0 of Word_0 contain the Comma character that maintains alignment of the 4 shadow registers with their corresponding Control registers. The chosen character is K28.5 = 0xBC.

3.2.2 Version

The 4-bit value contains the version number of this overall bit assignment. It will be held at “0000” through the initial debug phases, where many changes may occur.

3.2.3 Level 1 Accept (L1A)

L1 Accept is used to indicate when an event has been accepted by the Central Trigger Processor. The L1ID will be valid during the same broadcast cycle where L1A is active.

L1A is only active for a single broadcast cycle, and so there is the possibility of a Node or ROD missing it in the case of a crc error. If a node module drops an L1A, it would likely fail to produce data, headers, and trailers for that event. This will result in a timeout error occurrence in the ROD.

If the ROD misses the L1A, it will receive unexpected readout packets from any Nodes which have successfully received the L1A. The ROD will place these unexpected packets into a debug stream.

3.2.4 Bunch Counter Reset (BCR)

Entities within the shelf may keep local bunch counters. These are kept in sync using the BCR.

The Bunch Counter is a local 12-bit counter that increments each LHC clock. It counts to a value of 3563 and then rolls over to 0.

The first bunch after that in which BCR is asserted is bunch 0.

BCR is only active for a single broadcast cycle, and so there is the possibility of missing it in the case of a crc error. However, it is possible to design the counter in such a way as to provide further protection. The counter should be reset on (value = 3563) OR (BCR ='1'). If a BCR is missed, the counter should still remain in sync.

3.2.5 Event Counter Reset (ECR)

Entities within the shelf may keep local event counters. These are kept in sync using the ECR.

The Event counter is a local 24-bit counter that increments each L1A. It is reset to '-1' on ECR. The first event after ECR is number 0.

ECR is only active for a single broadcast cycle, and so there is the possibility of missing it in the case of a crc error. However, given that the ECRID is broadcast directly, the needs for a local counter is diminished.

3.2.6 Privileged Readout

This bit indicates that a full data readout has been requested.

On each 40 MHz cycle, the delayed L1A, ECR, and BCR are read from the pipeline. If the L1A bit is set, the Privileged Readout FIFO is inspected. If the FIFO is not empty (this is the expected condition), the Privileged Readout 0 or 1 value is read and asserted on the backplane at the same time as the L1A, ECR, and BCR.

3.2.7 Felix Backpressure

These bits are used to convey the backpressure status as passed to the Hub from the Felix Backpressure GBT link. The 12 bits are each carried on individual eLinks within the GBT. The Hub receives the GBT link and inserts the individual backpressure bits into the Combined_TTC stream.

These bits are only used by the ROD. They are used to stop ROD data on any of the (up to) 12 individual Full Mode links going to Felix.

These bits should remain asserted for the duration of the time that Felix is asserting backpressure.

3.2.8 L1ID

The L1ID should match the value in a local Event Counter. However, it is broadcast explicitly over this link to enhance channel reliability.

If a CRC error is detected in a message, then all four words must be discarded. In this case, the L1A may be completely missed, thus putting the local entity out of sync with the rest of the system. The L1ID however, may be correctly read in the next message that doesn't contain a crc error.

Other bits within the four-word broadcast will be held active for at least two four-word broadcast periods in order to reduce the probability of missing an active signal due to CRC error.

3.2.9 ECRID

These bits are an extension of the L1ID. In the past, this has been generated on each board independently. Now the L1ID and ECRID bits are combined into a single 32-bit counter and broadcast from the Hub to all other boards.

3.2.10 Control Channel

These bits are reserved for a possible future implementation of a message channel

3.2.11 Link Reset

As the Aurora Receiver, the ROD must control all of the Aurora Data Link initialisation. The Link Reset signal is therefore derived from the Readout_Ctrl link. The Hub should connect to the appropriate Readout_Ctrl Link Reset for the slot to which the Combined_TTC is connected. Each endpoint also has a local reset timer to control Aurora link establishment.

There are four Link Reset bits to allow each of the four jFEX Aurora links (per Hub) to be reset individually. The eFEX should listen to Link Reset 0.

Below is an example of routing from Hub to a Slot-3 Fex

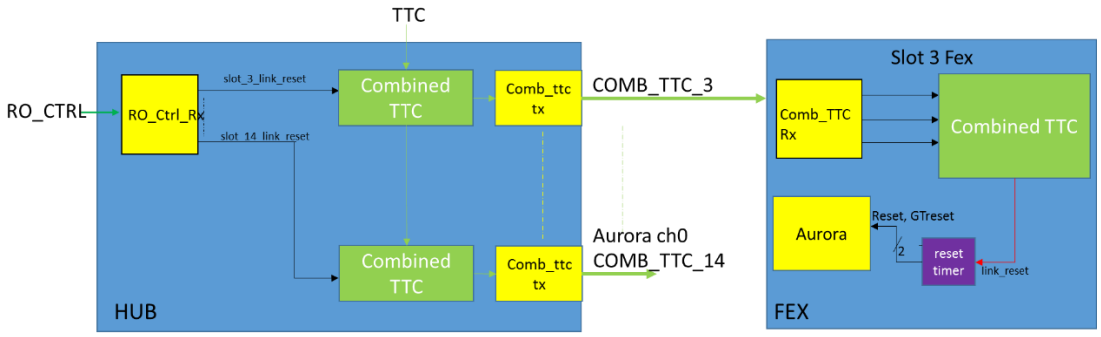

Figure 2: Example of Link Reset Routing

3.2.12 ROD XOFF

When active, this signal indicates that the ROD cannot currently accept further data from Fex sources. This signal is taken from the Readout_Ctrl and is fanned-out to the shelf FEX's over each slot's Combined_TTC link.

When active, the FEX should pause transmission immediately.

3.2.13 Link_Up (3:0)

These signals indicate to each FEX whether or not the corresponding ROD Rx Aurora channel is "Up". The eFEX should use only Link_Up(0)

3.2.14 ROD Reserved

These bits are reserved for future ROD functionality to be defined

3.2.15 Shelf Number

The Hub provides the shelf number to all Combined_TTC targets via these bits.

3.2.16 CRC (9-bit)

CRC is included to provide additional robustness on this link. Erroneous resets could cause loss of data. Choice of polynomial is from https://users.ece.cmu.edu/~koopman/crc/index.html

The chosen polynomial is 0x17d in Koopman format of 0x2fb in explicit+1 format.

The CRC is calculated over all four words of each transmission. When a CRC error occurs, all four of the associated words must therefore be ignored. Because of this, local counters for L1ID and ECRID should not be used. If a reset is missed due to a crc error, then these values would not be updated. L1ID and ECRID should be taken directly from the Combined_TTC link.