

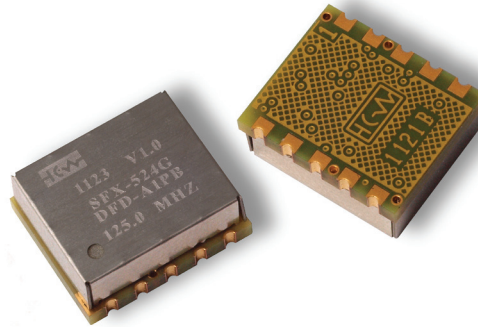
# SFX-524G Synchronous Clock Generators

**CONNOR  
WINFIELD**



PLL

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## Applications

SONET / SDH / ATM  
DWDM / FDM  
FEC (Forward Error Correction)

## Features

- 3.3V High Precision PLL
- Jitter Generation OC-192 Compliant
- Surface Mount
- Inputs Compatible with LVCMOS, LVPECL to 300 MHz
- Frequency Translation up to 800 MHz
- Alarm detection for Loss of Lock/ Loss of Reference condition
- Space-Saving 12x14mm Leadless Package
- ROHS Compliant



Bulletin **SG186**  
Revision **08**  
Date **16 Nov 2016**

## General Description

The SFX-524G is a high precision frequency translator that translates an input between 8 kHz to 300MHz, to output frequencies between 8 MHz and 800 MHz. The SFX-524G supports all major FEC rates such as 15/14, 255/237 etc.

SFX-524G is well suited for use in line cards, service termination cards and similar functions to provide reliable reference, phase locked, synchronization for TDM, PDH, SONET

and SDH network equipment. The SFX-524G provides a jitter filtered, wander following output signal synchronized to a superior Stratum or peer input reference signal.

The SFX-524G includes a lock detect alarm output.

Parts are assembled using high temperature solder to withstand surface mount reflow process. This product is compliant with all required ROHS specifications.

## Absolute Maximum Rating

Table 1

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V <sub>CC</sub>	Power Supply Voltage	-0.3	-	4.0	Volts	
V <sub>I</sub>	Input Voltage	-0.2	-	V <sub>CC</sub> +0.3V	Volts	
T <sub>S</sub>	Storage Temperature (OptionF)	-55	-	125	°C	

## Specifications

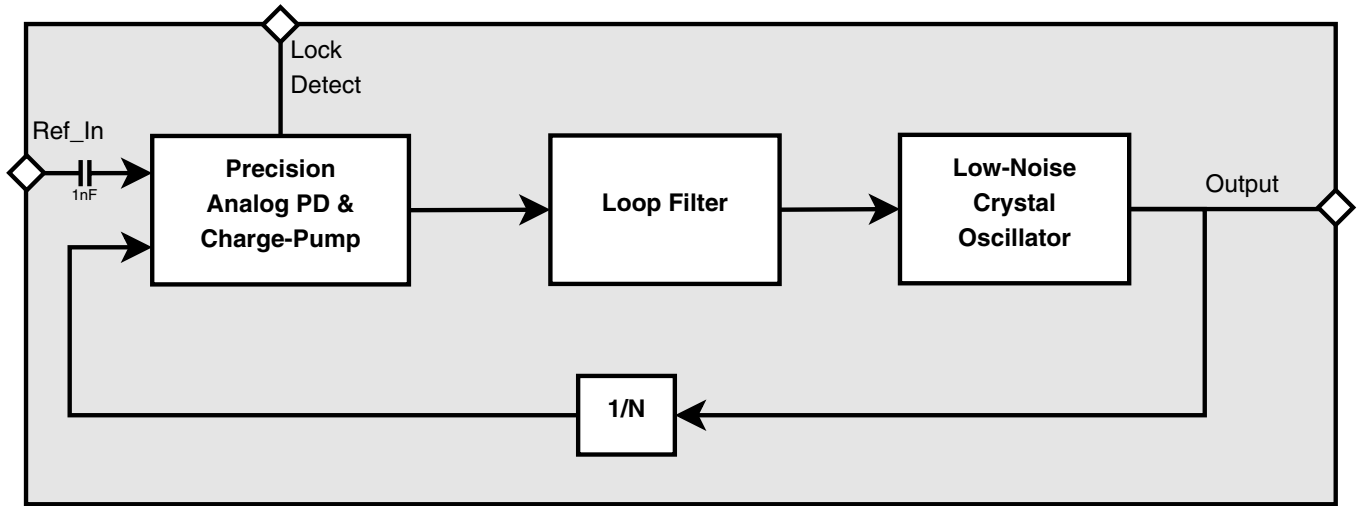
Table 2

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
f <sub>IN</sub>	Input Frequencies	8 k	-	300 M	Hz	
f <sub>OUT</sub>	Output Frequencies (LVPECL)	19.44 M	-	800 M	Hz	
	Output Frequencies (LVCMOS)	8 M	-	130 M	Hz	
V <sub>CC</sub>	Supply Voltage (3.3 V <sub>DC</sub> )	3.13	3.3	3.46	Volts	
I <sub>CC</sub>	Supply Current	-	65	-	mA	
F <sub>IN</sub> Input Characteristics						
V <sub>FIN</sub>	Input Voltage	0.6	-	3.3	V <sub>pp</sub>	1.0
F <sub>OUT</sub>	LVCMOS OUTPUT (Option A)	TYP. 3.3V LVCMOS				
F <sub>OUT</sub>	LVPECL OUTPUT (Option F)					
V <sub>FOUT</sub>	Differential Output Voltage	-	0.65	-	Volts	2.0, 3.0
T <sub>R</sub> /T <sub>F</sub>	Rise/Fall Time @20% to 80%	-	0.6	1.5	ns	
SYM	Output Symmetry	45		55	%	
J <sub>GEN2</sub>	Jitter Generation RMS (12 kHz - 20 MHz)		0.20	-	ps	4.0
J <sub>TRAN</sub>	Jitter Transfer Function	-	-	0.1	dB	5.0
TF	Input Frequency Tracking	±40	-		ppm	
T <sub>OP</sub>	Operating Temperature	<b>C</b> = 0 <b>D</b> = 0 <b>F</b> = -40	-	70 85 85	°C	
SSB Phase Noise (for SFX-524G-DFF-A10Z only)						6.0
	at 10Hz offset	-	-57	-45	dBc/Hz	
	at 100Hz offset	-	-92	-80	dBc/Hz	
	at 1kHz offset	-	-120	-110	dBc/Hz	
	at 10kHz offset	-	-138	-135	dBc/Hz	
	at 100kHz offset	-	-150	-145	dBc/Hz	
	at 1MHz offset	-	-157	-147	dBc/Hz	
	at 10MHz offset	-	-160	-150	dBc/Hz	
∅ <sub>OFF</sub>	Phase Offset	-	5	15	ns	6.0
∅ <sub>DYN</sub>	Dynamic Phase Offset	-	-	1	ns	7.0

- NOTES:
- 1.0: F<sub>IN</sub> is internally AC-coupled. Slew rate must be >500V/μs (<2 ns/V), Contact factory for sinewave input.
  - 2.0: Internally biased. External AC-coupling capacitor recommended. Please see Figure 2 for recommended connection diagram.
  - 3.0 V<sub>FOUT</sub> is the voltage difference between F<sub>OUT</sub> and CF<sub>OUT</sub>
  - 4.0 156.25 MHz.
  - 5.0: GR-253-CORE, Sec. 5.6.2.1.2
  - 6.0: ∅<sub>OFF</sub> must be <15ns for >3 consecutive cycles for Lock Detect to be set high. One high, any cycle with ∅<sub>OFF</sub> >25ns will reset Lock Detect.
  - 7.0: Change in phase offset over temperature, relative to 25°C

## Functional Block Diagram

Figure 1



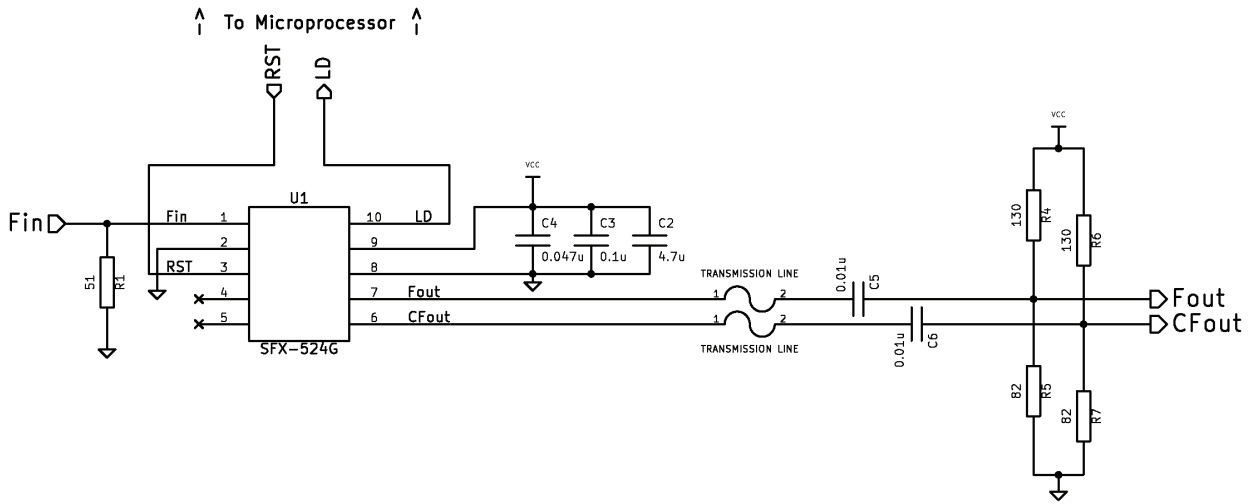
## Pin Description

Table 3

PIN #	SYMBOL	I/O	Level	Function
1	FIN	I	LVPECL or LVCMOS	Input Frequency Note: Input is AC coupled for handling either LVCMOS or LVPECL input signals
2	GND	GND	Supply	Ground
3	RST	I	LVCMOS	Active Low Reset
4		N/C	N/A	Do Not Connect
5		N/C	N/A	Do Not Connect
6	FOUT	O	LVPECL or LVCMOS	Frequency Output
7	CFOUT	O	LVPECL or GND	Complementary Frequency Output Note: For the LVCMOS Option, this connection is tied to GND
8	GND	GND	Supply	Ground
9	VCC	VCC	Supply	Power Supply Voltage (3.3V ±5%)
10	LD	O	LVCMOS	Lock Detect Locked = Logic 1 Loss of Signal = Logic 0

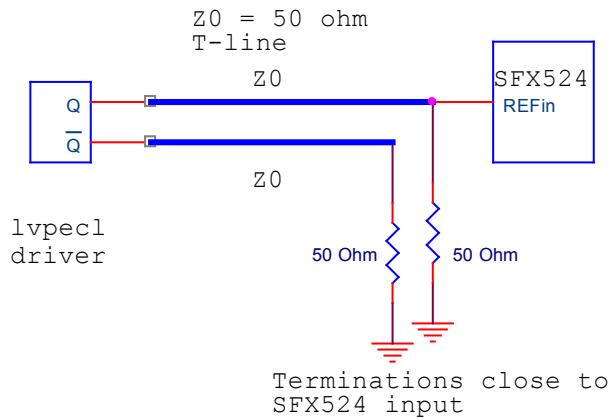
## Output Load and Power Supply Filtering Recommendations

Figure 2



## LVPECL Input Termination

Figure 3

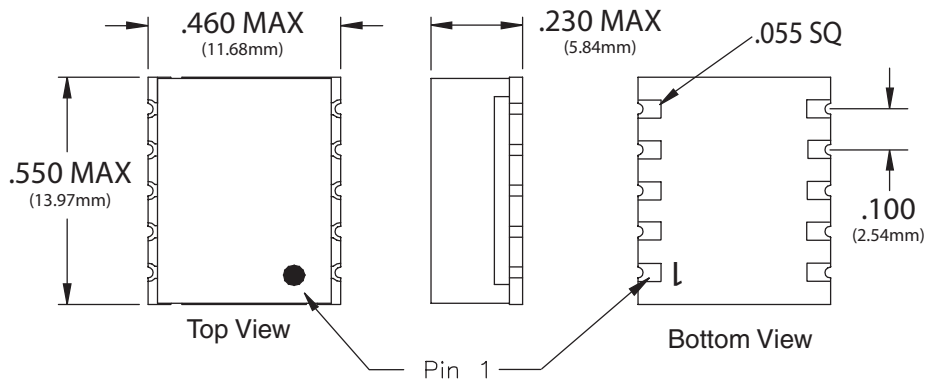


## SFX524 LVPECL Input termination scheme

Note: Continuous ground plane under 50 ohm lines. With very short traces you can use up to 150 ohms

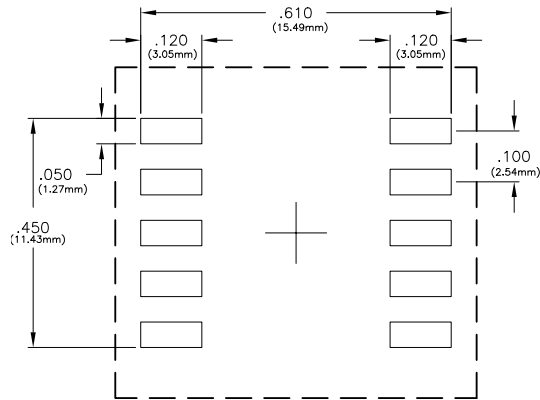
## Package Dimensions

Figure 4



## Recommended Footprint Dimensions

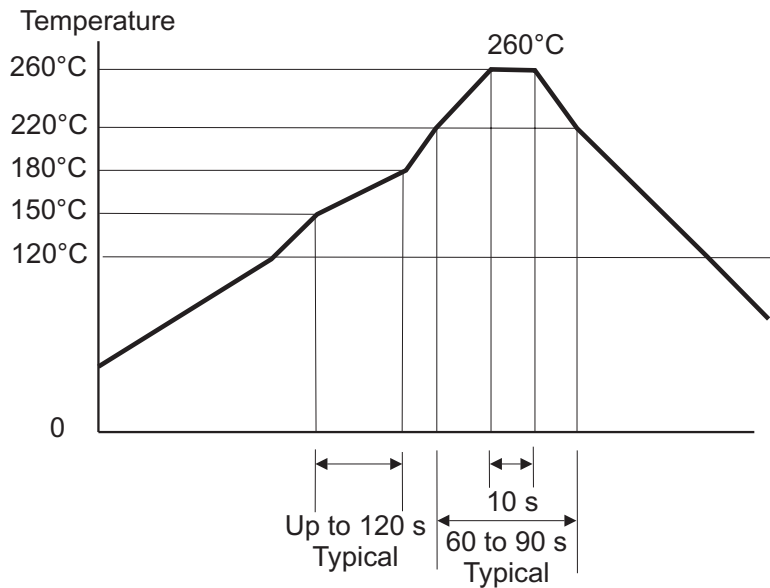
Figure 5



DASH LINES ARE KEEP OUT AREA  
AND SOLDER MASK FILLED EXCEPT PADS

## Solder Profile

Figure 6



Meets IPC/JEDEC J-STD-020C

## Standard Frequencies

Table 4

156.25 MHz	A	Output Freq not listed	S
125.00 MHz	B	26.00 MHz	T
8 kHz	C	32.768 MHz	W
16 kHz	D	38.880 MHz	X
64 kHz	E	49.152 MHz	Y
1.024 MHz	F	204.80 MHz	Z
161.1328125 MHz	G		
1.544 MHz	H	51.84 MHz	0
2.048 MHz	J	61.44 MHz	1
4.096 MHz	K	77.76 MHz	2
8.192 MHz	L	82.944 MHz	3
10.00 MHz	M	100.00 MHz	4
16.384 MHz	N	139.2640 MHz	5
10.24 MHz	O	155.520 MHz	6
19.440 MHz	P	166.6286 MHz	7
20.480 MHz	R	622.080 MHz	8
Input Freq not listed	S	666.5143 MHz	9

### Ordering Information

**SFX-524G- [X][X][X] - [X][X][X][X]**

**Supply Voltage**  
D = 3.3 V<sub>DC</sub> ±5%

**Output Logic**  
A = LVCMOS  
F = Comp. LVPECL

**Temperature Range**  
C = 0°C to 70°C  
D = 0°C to 85°C  
F = -40°C to 85°C

**Input Logic**  
A = LVCMOS/LVPECL  
(See Table 2)

**Number of Input Frequencies**  
1: 1 Input Frequency

**Output Frequency (See Table 2)**  
See standard frequencies chart above.  
\* If the desired frequency is not listed,  
Please Consult a sales representative  
for availability of additional frequencies.

**Input Frequency (See Table 2)**  
See standard frequencies chart above.  
\* If the desired frequency is not listed, Please Consult  
a sales representative for availability of additional  
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Revision	Date	Note
00	04/11/11	Released to public
01	05/05/11	Block Diagram Update
02	05/09/11	Output Frequency Update, added Phase Offset & New Package Dwgs
03	05/23/11	Add Phase Noise to Specs & DYN Information
04	06/15/11	Specification edits and new Figure 2
05	01/24/13	Added 161.1328125 to Table as G; Increased Input Frequency to 300 MHz
06	01/29/13	Clarified LVPECL input terminations, amplitude and slew rate; updated typical jitter and added Figure 3.
07	09/02/14	Standard Frequencies Updates
08	11/16/16	Updated Recommended Footprint Dimensions