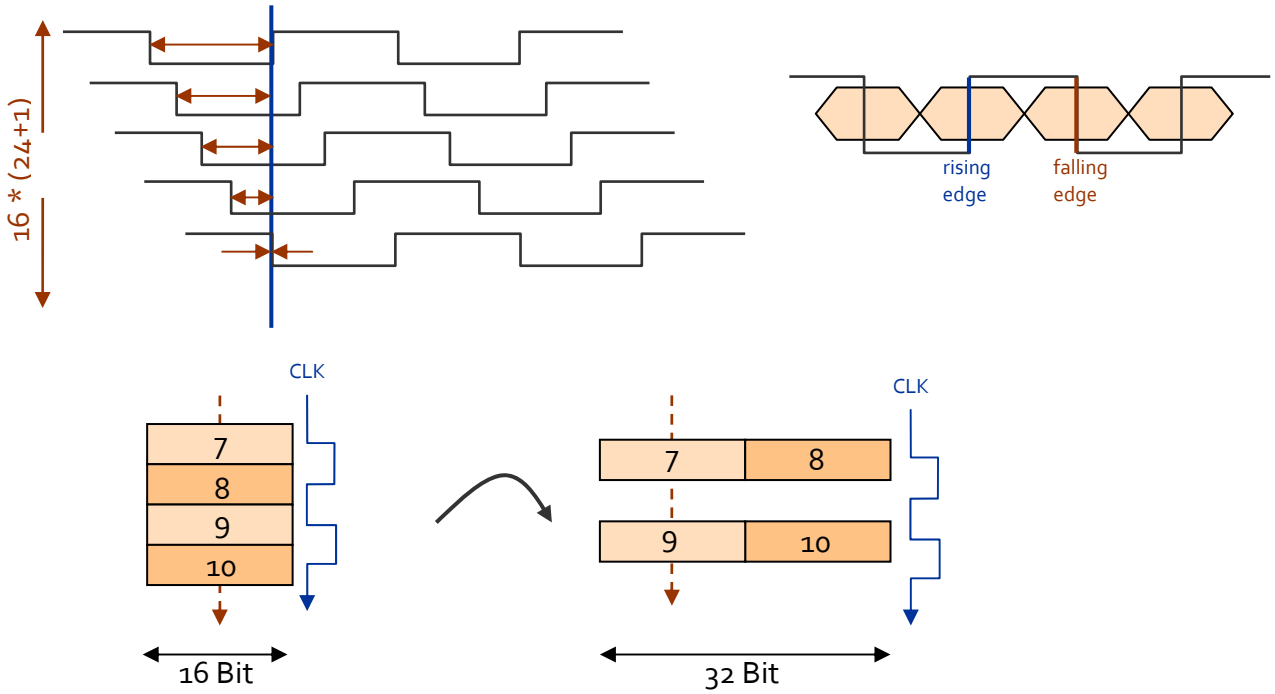
Backplanetester Firmware Specifications

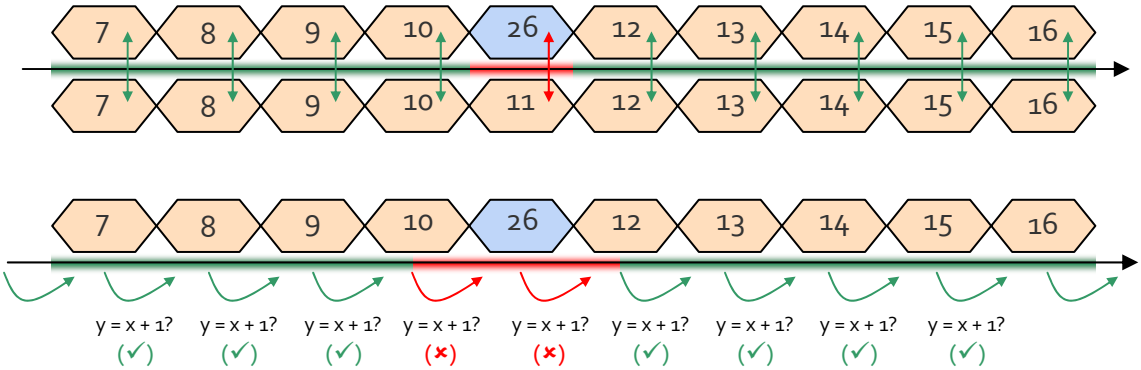
ATLAS
-Mainz-

Functionality:

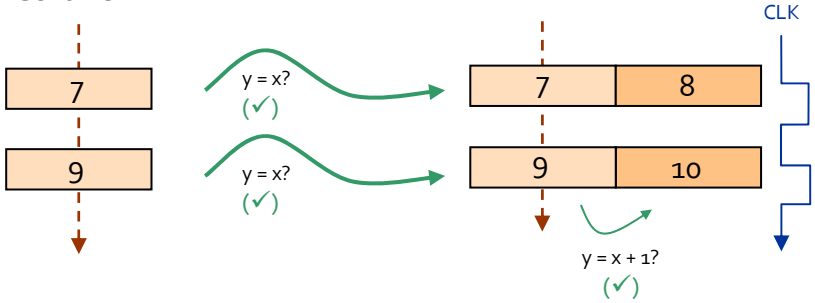
- Shift timing delays of single sub channels that could raise from different lengths of cables, 16 * (24+1) sub channels, with Double Data Rate (DDR)



- Send patterns through the backplane (first: simple counter patterns and count transmission errors for 16 * (24+1) sub channels



- Counting mechanism:



- count errors, put them readable via VME in error registers (16 channels)

Communication via VME to the PC:

- Addresses only in the VME-Part
- Registers in program as Std-Logic-Vector (VME, 16 Bit)
- Registers: control register, status register, pulse register, 16 error registers, 4 * 16 delay registers, possibly also 4 (8) * 16 * (24+1) input register suitable for reading the delayed data

Addresses of the VME part short form			
Address hex.	Function	No. of Registers	Name in VHDL-Code
0x0000	Version register	1	versionreg
0x0002	Status register	1	statusreg
0x0004	Control register	1	controlreg
0x0006	Pulse register	1	pulsereg
0x0100 – 0x011E	error counter [0 .. 15]	16	errorcount[0..15]
0x0200 – 0x027E	Delay register ([A..D][0..15])	64 (16 * 4)	delayreg_[A..D][0..15]
0x0400 – 0x043E	Readback register ([A..B][0..15])	32(16 * 2)	readbackreg_[A..B][0..15]

Use of the VME Registers			
Register (16 Bit)	Bit No.	Function	Logic
versionreg	[0..15]	read 16-Bit Version No.	0x0000 = Version 0, not finished
	[0..15]	read 16-Bit Version No.	0x0001 = Version 1, first testing version for hardware
statusreg	0	validity of REFCLK (200 MHz)	1 = active, 0 = inactive
	1	counting phase active	1 = active, 0 = inactive
controlreg	0	global reset (resets all counters and clocks)	1 = active, 0 = inactive
	1	counter reset (resets all counters)	1 = active, 0 = inactive
	2	activate counting phase (activates counting of bit errors)	1 = active, 0 = inactive
	3	stop counting phase (deactivates counting of bit errors)	1 = active, 0 = inactive
pulsereg			
delayreg_A [0..15]	[0..11]	increases IDELAY (="Bit Up") [12..24]	1 = active, 0 = inactive
delayreg_B [0..15]	[0..11]	increases IDELAY (="Bit Up") [0..11]	1 = active, 0 = inactive
delayreg_C [0..15]	[0..11]	decreases IDELAY (="Bit Down") [12..24]	1 = active, 0 = inactive
delayreg_D [0..15]	[0..11]	decreases IDELAY (="Bit Down") [0..11]	1 = active, 0 = inactive
readbackreg_A [0..15]	[0..11]	data behind IODELAY [0..11]	
readbackreg_B [0..15]	[0..11]	data behind IODELAY [12..24]	

Addresses of the VME part long form			
Address hex.	Function	Size	Name in VHDL-Code
0x0000	version register	16 Bit (15..0)	versionreg
0x0002	status register	16 Bit (15..0)	statusreg
0x0004	control register	16 Bit (15..0)	controlreg
0x0006	pulse register	16 Bit (15..0)	pulsereg
0x0100	error counter (0)	16 Bit (15..0)	errorcounto
0x0102	error counter (1)	16 Bit (15..0)	errorcount1
0x0104	error counter (2)	16 Bit (15..0)	errorcount2
0x0106	error counter (3)	16 Bit (15..0)	errorcount3
0x0108	error counter (4)	16 Bit (15..0)	errorcount4
0x010A	error counter (5)	16 Bit (15..0)	errorcount5
0x010C	error counter (6)	16 Bit (15..0)	errorcount6
0x010E	error counter (7)	16 Bit (15..0)	errorcount7
0x0110	error counter (8)	16 Bit (15..0)	errorcount8
0x0112	error counter (9)	16 Bit (15..0)	errorcount9
0x0114	error counter (10)	16 Bit (15..0)	errorcount10
0x0116	error counter (11)	16 Bit (15..0)	errorcount11
0x0118	error counter (12)	16 Bit (15..0)	errorcount12
0x011A	error counter (13)	16 Bit (15..0)	errorcount13
0x011C	error counter (14)	16 Bit (15..0)	errorcount14
0x01F0	error counter (15)	16 Bit (15..0)	errorcount15
0x0200	delay register (A0)	16 Bit (15..0)	delayreg_A0
0x0202	delay register (B0)	16 Bit (15..0)	delayreg_B0
0x0204	delay register (C0)	16 Bit (15..0)	delayreg_C0
0x0206	delay register (D0)	16 Bit (15..0)	delayreg_D0
0x0208	delay register (A1)	16 Bit (15..0)	delayreg_A1
0x020A	delay register (B1)	16 Bit (15..0)	delayreg_B1

0x020C	delay register (C1)	16 Bit (15..0)	delayreg_C1
0x020E	delay register (D1)	16 Bit (15..0)	delayreg_D1
0x0210	delay register (A2)	16 Bit (15..0)	delayreg_A2
0x0212	delay register (B2)	16 Bit (15..0)	delayreg_B2
0x0214	delay register (C2)	16 Bit (15..0)	delayreg_C2
0x0216	delay register (D2)	16 Bit (15..0)	delayreg_D2
0x0218	delay register (A3)	16 Bit (15..0)	delayreg_A3
0x021A	delay register (B3)	16 Bit (15..0)	delayreg_B3
0x021C	delay register (C3)	16 Bit (15..0)	delayreg_C3
0x021E	delay register (D3)	16 Bit (15..0)	delayreg_D3
0x0220	delay register (A4)	16 Bit (15..0)	delayreg_A4
0x0222	delay register (B4)	16 Bit (15..0)	delayreg_B4
0x0224	delay register (C4)	16 Bit (15..0)	delayreg_C4
0x0226	delay register (D4)	16 Bit (15..0)	delayreg_D4
0x0228	delay register (A5)	16 Bit (15..0)	delayreg_A5
0x022A	delay register (B5)	16 Bit (15..0)	delayreg_B5
0x022C	delay register (C5)	16 Bit (15..0)	delayreg_C5
0x022E	delay register (D5)	16 Bit (15..0)	delayreg_D5
0x0230	delay register (A6)	16 Bit (15..0)	delayreg_A6
0x0232	delay register (B6)	16 Bit (15..0)	delayreg_B6
0x0234	delay register (C6)	16 Bit (15..0)	delayreg_C6
0x0236	delay register (D6)	16 Bit (15..0)	delayreg_D6
0x0238	delay register (A7)	16 Bit (15..0)	delayreg_A7
0x023A	delay register (B7)	16 Bit (15..0)	delayreg_B7
0x023C	delay register (C7)	16 Bit (15..0)	delayreg_C7
0x023E	delay register (D7)	16 Bit (15..0)	delayreg_D7
0x0240	delay register (A8)	16 Bit (15..0)	delayreg_A8
0x0242	delay register (B8)	16 Bit (15..0)	delayreg_B8
0x0244	delay register (C8)	16 Bit (15..0)	delayreg_C8

0x0246	delay register (D8)	16 Bit (15..0)	delayreg_D8
0x0248	delay register (A9)	16 Bit (15..0)	delayreg_A9
0x024A	delay register (B9)	16 Bit (15..0)	delayreg_B9
0x024C	delay register (C9)	16 Bit (15..0)	delayreg_C9
0x024E	delay register (D9)	16 Bit (15..0)	delayreg_D9
0x0250	delay register (A10)	16 Bit (15..0)	delayreg_A10
0x0252	delay register (B10)	16 Bit (15..0)	delayreg_B10
0x0254	delay register (C10)	16 Bit (15..0)	delayreg_C10
0x0256	delay register (D10)	16 Bit (15..0)	delayreg_D10
0x0258	delay register (A11)	16 Bit (15..0)	delayreg_A11
0x025A	delay register (B11)	16 Bit (15..0)	delayreg_B11
0x025C	delay register (C11)	16 Bit (15..0)	delayreg_C11
0x025E	delay register (D11)	16 Bit (15..0)	delayreg_D11
0x0260	delay register (A12)	16 Bit (15..0)	delayreg_A12
0x0262	delay register (B12)	16 Bit (15..0)	delayreg_B12
0x0264	delay register (C12)	16 Bit (15..0)	delayreg_C12
0x0266	delay register (D12)	16 Bit (15..0)	delayreg_D12
0x0268	delay register (A13)	16 Bit (15..0)	delayreg_A13
0x026A	delay register (B13)	16 Bit (15..0)	delayreg_B13
0x026C	delay register (C13)	16 Bit (15..0)	delayreg_C13
0x026E	delay register (D13)	16 Bit (15..0)	delayreg_D13
0x0270	delay register (A14)	16 Bit (15..0)	delayreg_A14
0x0272	delay register (B14)	16 Bit (15..0)	delayreg_B14
0x0274	delay register (C14)	16 Bit (15..0)	delayreg_C14
0x0276	delay register (D14)	16 Bit (15..0)	delayreg_D14
0x0278	delay register (A15)	16 Bit (15..0)	delayreg_A15
0x027A	delay register (B15)	16 Bit (15..0)	delayreg_B15
0x027C	delay register (C15)	16 Bit (15..0)	delayreg_C15
0x027E	delay register (D15)	16 Bit (15..0)	delayreg_D15