PPM modifications for a FINAL prototype

"Interim Design Review" for the final pre-series of PPMs (16 PPMs in a PPr Crate)

The ATLAS group at KIP Heidelberg

Nov.2005, P.Hanke

Introduction.

The first prototypes of PPMs came into operation in spring 2004. FOUR printed circuit boards were produced. A first one was equipped in-house with components and, finally, with daughter-boards (ANINs, MCMs, LCDs, TTCdec) to make up a functional Pre-Processor Module.

The other three PCBs were equipped at a company to establish the out-sourced procedure for full production of 160 PPMs later on. Also, these PPMs came into operation during the second half of 2004. A decisive test took place at the "last" period of CERN test-beam in summer 2004. Important conclusions could be drawn from this "slice-test", which involved the whole chain from detector-sources all the way to Data-Acquisition.

Many periods of detailed testing in laboratories followed, to clear up performance issues. Several modifications on details of implementation were done on the prototypes including a complete "re-design" of an important daughter-board (the LCD). The prototypes in their present form fulfill all the requirements. This has been shown in the latest test-sessions (e.g. tests on readout at RAL, real-time signal recording from TileCal at ATLAS-USA15).

All conclusions drawn must be worked into a re-design of the Pre-Processor Module. To summarize and to check the completeness of the "updates/modifications" is the purpose of this review.

See also: Talk of K.Mahboubi given at the Joint Meeting on the ATLAS Level-1 Calorimeter Trigger at CERN in Nov.2005.

The first PPM design.

The first PCB has been used in system-tests at KIP, RAL and at the CERN testbeam from summer 2004 onwards. Some insufficiencies were identified. Solutions were worked out and have been implemented. Hence, currently four identically updated and fully working PPMs (4 * 64 channels) are available for test-work with the signal-sources (the ATLAS calorimeters) at CERN.

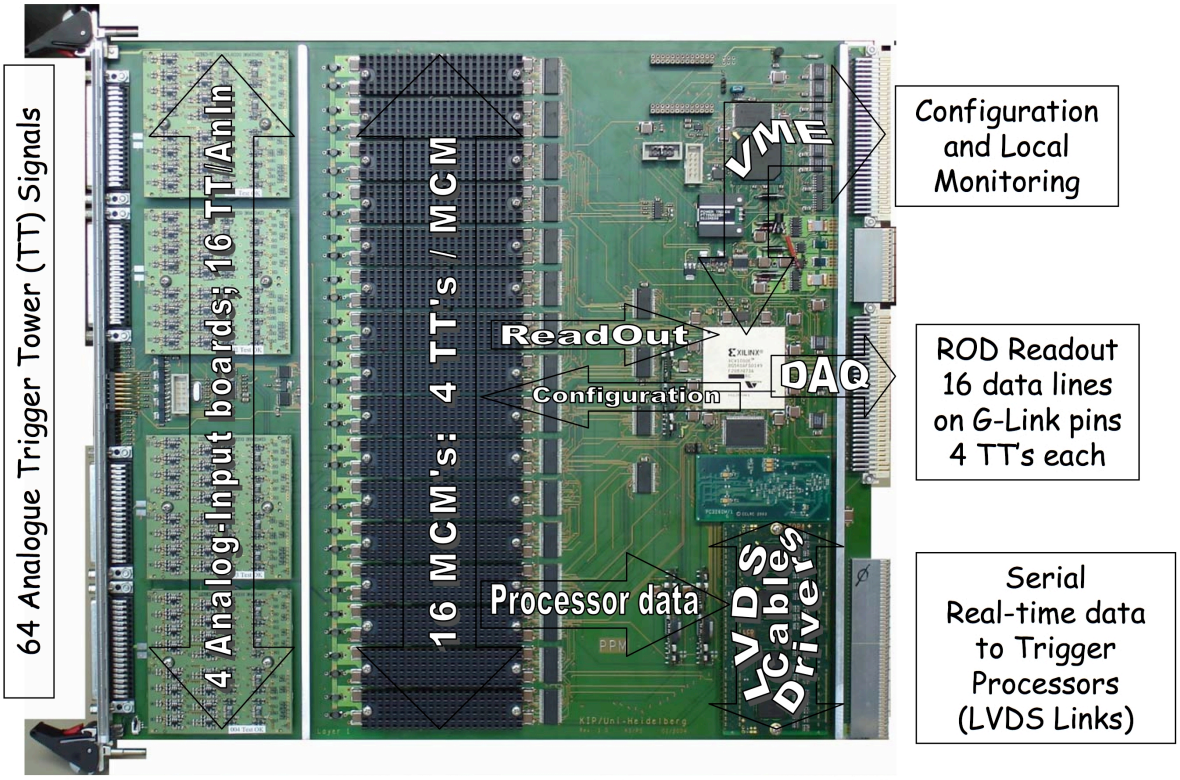


Figure 1 : The PPM and its periphery.

The list of problems and their solutions.

The following sections list all the items of concern. To impose structure on the list, we choose to group the issues according to functionality. The primary issue in the trigger system is the decision-making real-time data path.

Since a complex, highly integrated system as ours does not permit checks by diagnostic tools (oscilloscopes...), an equally important area is the readout data path.

Finally, issues related to the module as a whole are treated in the last section dealing with the PPM's infrastructure etc.

The Real-time Signal Path

- Cross talk on ANIN.

First design: In very early check-out work with "realistic" pulses, replayed from test-beam recordings, a certain cross-talk percentage was observed on specific pairs of channels on the

ANIN daughterboard. The quantitative analysis showed cross-talk around the 4-5 % level, i.e. at 2.5 Volt input signal-amplitude (corresp. to Et = 250 GeV) we observed appr. 100 mV of a coupled fake-signal in a neighbour-channel. ATLAS had defined an UPPER limit of 1% (i.e. 2.5 GeV of Et) for cross-talk anywhere in the analog signal-chain. We considered it unacceptable, that one single point on the ANIN daughterboard should exceed this limit.

Current implementation: The reason for cross-talk was localised at a quad line-receiver OpAmp., where other PCB routing ran parallel to the input of channel#4 for some millimeters. The solution involved re-routing. To avoid similar problems in a new layout, we decided to use single OpAmps for each analog signal arriving. The second and final ANIN shows no observable cross-talk.

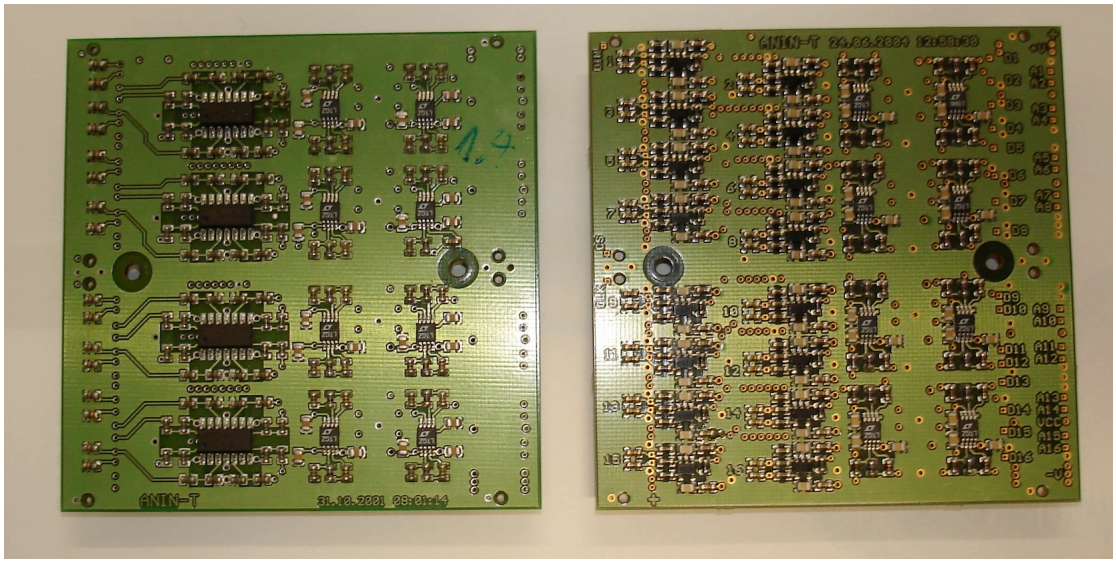


Figure 2 : ANIN (left: quad OpAmps, right: NEW design with single OpAmps)

- ANIN changes on DAC-ranges for signal-offset.

First design: The signal-conditioning is determined by the dimensioning of passive components around the crucial Op.-Amplifier in each channel (see LT1813 in the schematics of the AnIn).

Current implementation: The re-layout contains some passive components, whose values are slightly changed. This was done to make sure, that all signal-offsets can be adjusted with some safety-margin left for eventualities.

Gain of Op-Amplifier to map the signal into the FADC window: The feed-back is set to give Gain=0.48 on the signal (a measurement says: Gain=0.475). This maps 0 to 2.5V full range onto the 0-1.0 Volt FADC-window. Caveat: There is additional, small signal-attenuation present from the "filter-resistor" on the MCM-"balcony" (default-filter-RC = 47 Ohm, 150 pF). ---> The resulting, final gain needs to be re-measured with DC from the FP-connector (0 to +- 1.25V) to the FADC in terms of FADC-counts.

DC-Offset to shift the signal to the FADC window: The FADC reference-voltage is 2.5 Volt (a measurement says: V-center=2.49V). This is the center-voltage around which the FADC digitises. The FADC starts to digitise at a Voltage of 1.92V seen at the AnIn-output.

DAC-range to shift a bipolar signal: Absent analog input-signal and DAC=0 yields 1.65V at the AnIn-output. One DAC-step corresponds to 2.06 FADC-counts (measured). DAC=255 (full range) would yield 2.25V at the AnIn-output (calculated; to be verified by measuring at

the FADC). Hence, an analog signal-input can be shifted by 220 FADC-counts “downwards” and by 305 FADC-counts “upwards”.

- Changes around the MCM.

There were absolutely **no changes** to this specific “daughter-board”. Most of our effort went with highest priority into the test and design-verification of this essential module. The device was “PRRed” in January 2005. Production is well advanced meanwhile (>50% done).

1. Distribution of TTC clock on the PPM for “real-time” pipelining.

First design: The first PPM was plaqued with unwanted distortions on LHC clock-signals (40.08 MHz) being fanned out from buffers to the MCMs. Some part of the layout in the “digital” PPM area was left to an “auto-router” including the clock-lines.

Current implementation:

The LHC Clock distribution cannot be left to an “automatism”, unless the “auto-router” is properly tought what the priorities are. The problems were largely cured by a “series termination” at the source (i.e. buffers). This removes “reflections” and/or “under-/over-shoots”.

But, the main conclusion is, to route the “clock-tree” manually and carefully.

2. I2C clock for serial data.

First design: On the PPM board, the serial clock of the I2C bus was implemented following the “standard” (bi-directional lines, open drain/collector with pull-up). Reliable setting of Phos4-parameters required improvement of the I2C clock-signal distributed to the MCMs (rise-time of clock; reflections).

Current implementation:

- Higher drive strength (better rise-time) is achieved by a “push-pull” driver from the ReM_FPGA. This is possible, because the bus is used in “write-direction” only (to the Phos4).
- Series resistors on the clock-distribution from the ReM_FPGA dampens the reflections. It works also as moderate “pull-up” (see Figure below). A 3k “pull-up” sits inside the Phos4 chip (see Figure below).

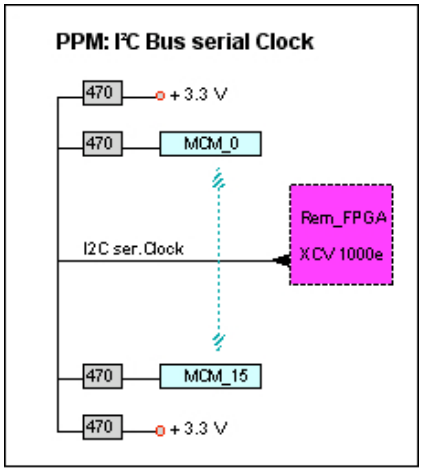


Figure 3 : Termination for I2C clock.

3. Phos4 initialisation.

First design: Occasionally, the Phos4 chips could not be accessed after "power -ON". This was tracked to some residual voltage (>0.7 V) before the 3.3V supply was ramped up by the "Hot-Swap" controller. This prevented I2C-access to the Phos4.

Current implementation: Insertion of an active "pull-down" (transistor) gives clean initilisation of the Phos4s on all MCMs.

- Pre-compensation on PPM for "MCM to LCD" signal transfer.

First design: The PPM has high-speed serial LVDS links across the printed-circuit board, which run at 480 MBaud over "strip-lines". The track-length can be as long as 30 cm. Investigations showed, that the differential LVDS-signal streams suffer from attenuation. This leads to reduced "opening of the data-eye". Another problem was identified as "shift of the zero-line", when the data-content is unbalanced (highly un-equal number of "0" and "1" in the serial bit-stream).

Current implementation: The problems are cured by the introduction of "pre-emphasis" on the board directly behind the LVDS-sources on the MCMs. Furthermore, a "pull-up" on the negative signal-branch keeps the data-eye well centered at zero.

- Re-design of LCD.

First design: Similar problems as described above were present after the "LVDS repeater" driving the long (12 to 15 m) cable-lines. In fact, some effects observed on the board were "magnified" after the cables. LVDS cross-talk was also observed due to non-optimal positioning of the "pre-emphasis" components. The two FPGAs implemented were found to be "over-loaded" driving the number of outputs. These findings led to a complete re-design of the fanout and cable-driving daughterboard called "Lvds Cable Driver" (LCD).

Current implementation: A new LCD board was developed with **four** FPGAs and modified usage of FPGA-internal banks of LVDS buffers. The passive RC-network for Pre-Emphasis of each signal was placed in the PCB layout as close as possible to LVDS-drivers on the FPGAs. All this resulted in very good transmission quality for these 480 MBaud data. Bit-Error Rates (BER) were measured to be so small, that safe operation of the Trigger is achieved, i.e. BER ≤ 1/10**15 guarantees a sufficiently small contribution of "fake triggers" in ATLAS.

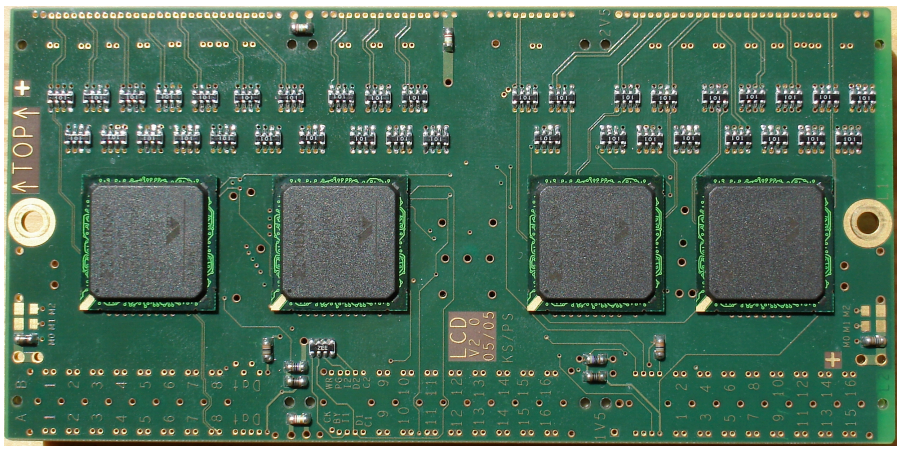


Figure 4 : LCD(top) with 4 FPGAs and Pre-Emphasis circuits (Rs) at outputs.

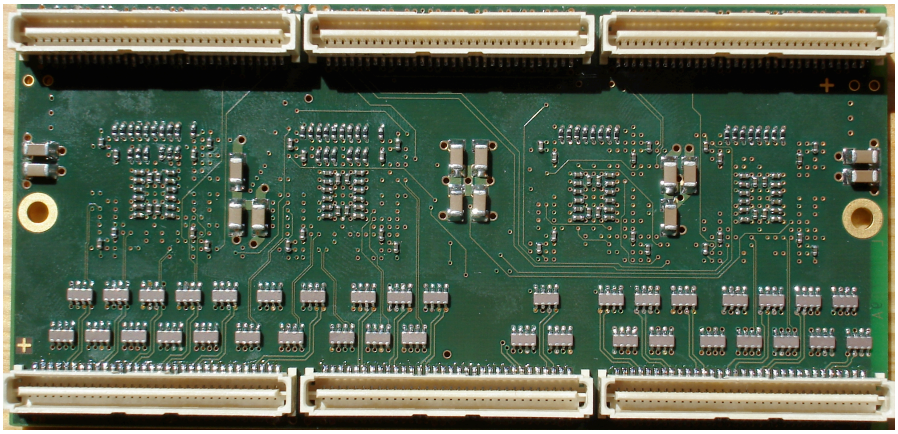


Figure 5 : LCD (bot) with Pre-Emphasis circuits (Cs) at outputs.

The combined improvements are shown in the following figure comparing the first design-approach to the current implementation.

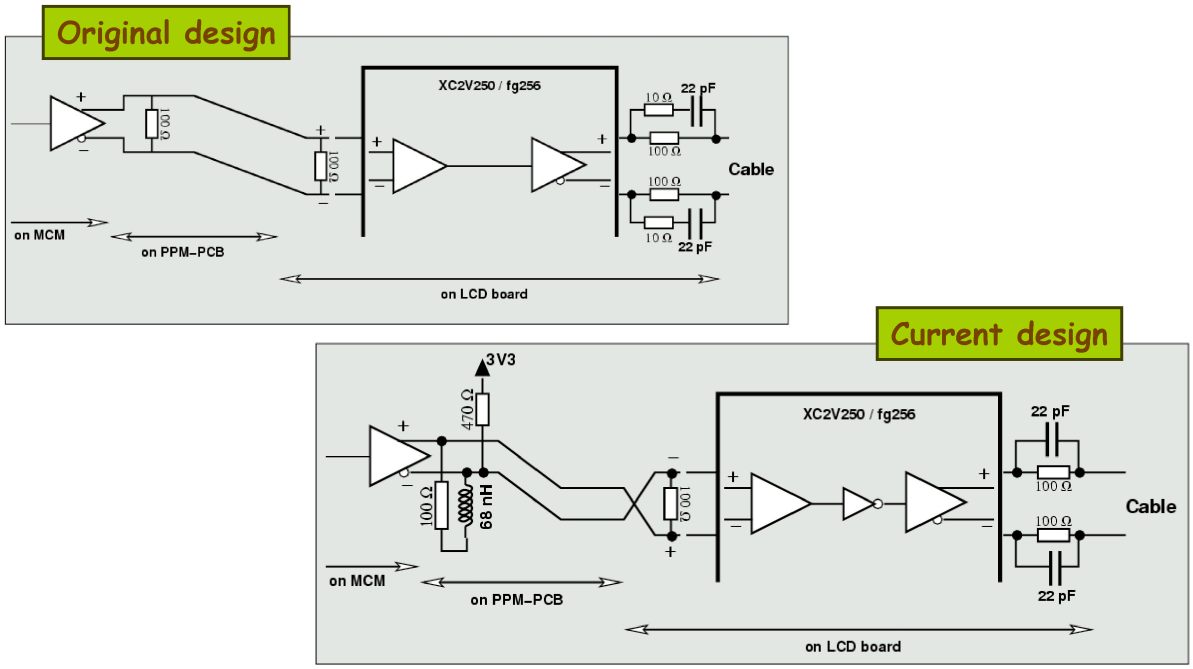


Figure 6 : The entire "pre-emphasis chain" on the PPM.

Note the LC pre-emphasis directly after the LVDS-serialiser on the MCM, the "pull-up" and the "inversion", which is re-inverted in the driving FPGA. The "inversion" improves the data-eye by using the sharper high-low transition in chips.

The Readout Path.

- Firmware (i.e. loading of bit-files to devices on PPM).

First design: The CPLD, handling VME traffic, has very limited resources left over to serve the Flash-RAM loader. Demands have increased due to the LCD update (4 FPGAs). The VME protocolling, however, is well tested, hence shall not be changed in future versions of the PPM.

Current implementation:

The new approach involves a SECOND CPLD to handle Flash-RAM loading. This leaves the VME CPLD literally untouched. The new, "widened" scheme is shown in the first figure of the **Appendix**.

The Flash-RAM in consideration has a capacity of 4 MBytes, which can be allocated as bit-file store in the following way.

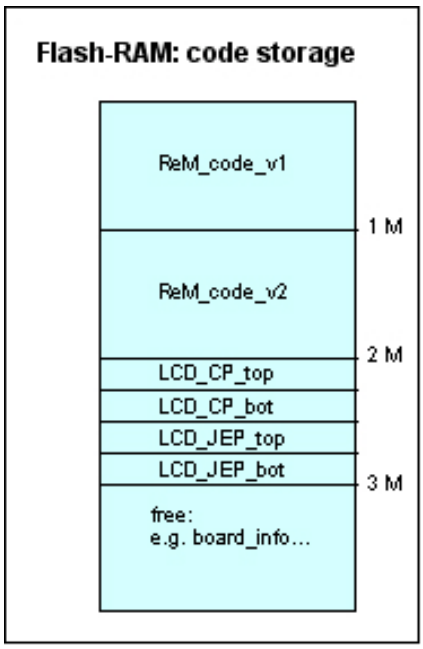


Figure 7 : Space allocation for "firmware" in Flash-RAM.

- Firmware-code

is not subject in this review, but has been developed much further during tests. The firmware-code has now reached a status of "stability". NOTE, that there are no limitations due to availability of resources on the implemented XCV_1000E. Readout at full speed and specified max. data-volume has been verified.

- SRAM usage outside Rem FPGA

First design: The PPM holds a Static RAM for fast data-storage at the "disposal" of the ReM_FPGA. Its size is 1 MByte (256k * 32 bits).

Current implementation:

The same component is available on the market with larger capacity. The pin-compatible version providing 4 MBytes will be implemented. Storage of "hardware" information like "unbiased rate/ cell" or "unbiased energy-histogram /cell" will be possible without restriction.

- Optical Glink (RAL board in the rear of the PPr Crate).

First design: A "electrical" G-Link connection was used to transmit event readout data to the 6U RODs.

Current implementation: It is decided to use the GLink in 16 bit mode only. Also a new version of the RGTM (Rear G-Link Transmission Module) with an optical link is "standard" from now on. POWER and CLOCK come from the PPM board by pin-through. Hence,

switching ON/OFF goes along with the PPM in the same slot. Also, the G-Link status is available on the PPM board for evaluation.

The PPM's infrastructure, VME, TTC etc.

- On Hardware : "status LEDs" to front-panel.

First design: The PPM has some LEDs activated. Some more could be implemented to make visual status-control easier.

Current implementation: The proposal for the final PPM is shown in the figure below. Experience from tests has initiated this LED-allocation, which hopefully follows the "colour-convention" once established (NG).

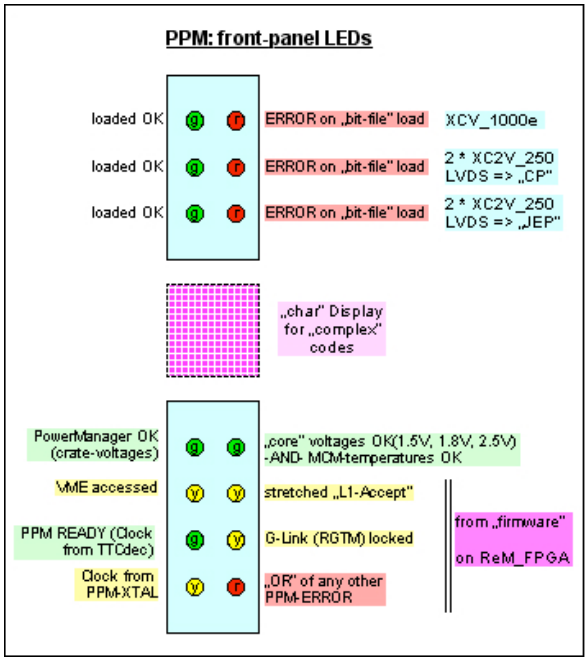


Figure 8 : The "illuminated" PPM front-panel (LEDs), if visible.

- VME-CPLD (closely coupled to "firmware loading).

First design: As described above, the CPLD code is well debugged on the existing PPMs, hence shall remain "untouched" in its functionality.

Current implementation: A second device assumes the task of "Flash-RAM administration (see above).

- TTCdec daughterboard.

First design: The currently implemented PLL is leads to a deteriorated rise-time on the LHC-clock to be distributed across the PPM (see figure below).

Current implementation:

1. Meanwhile, a new configurable TTCdec card has been designed, which can be used anywhere in the Level-1 Calo. Trigger system, i.e. a jumper-field allows either to include a PLL in the clock-output or to use the clock-output straight forward.

2. Mounting holes on the new TTCdec-daughterboard are NOT correctly placed compared to the prototype-version. The new PPM layout adapts to the mirrored hole-positions to have proper mechanical fixation also for the new TTCdec board.

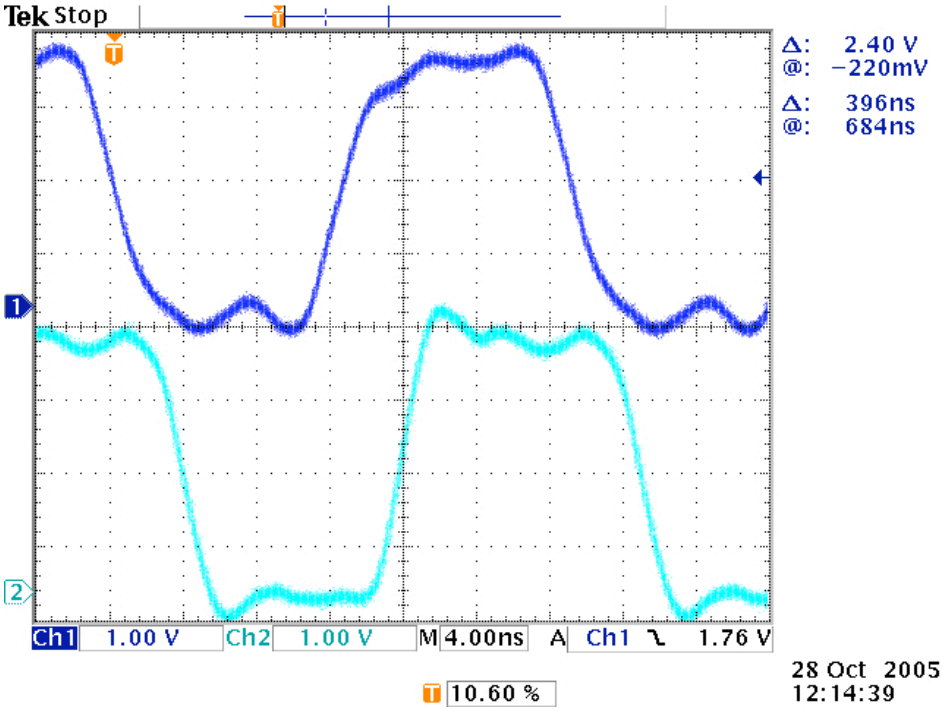


Figure 9 : TTCdec clock – with PLL (upper trace) – wihtout PLL (lower trace)

- CAN-Controller.

First design: The Level-1 community has agreed on a certain micro-controller to be used on all modules. The CAN MicroMod of the early PPMs is replaced.

Current implementation: A newly developed daughterboard holds the Fujitsu MB90F594. The schematics and the physical layout of the daughterboard on the PPM is shown in the second figure of the **Appendix**.

The CAN controller should be accessible from VME for local testing (e.g. MCM temperatures). A "minimal" interface consisting of 8-bit data (read) and 4 control-lines (write) to/from the VME-side will be sufficient.

- "Hot-Swap" controller.

First design: "Live-insertion" of a second PPM into a crate showed an undesired effect. When the "hot-swap" controller ramps up the inserted PPM, an in-rush of current results in a "dip" followed by a "spike" on the 3.3V of the crate. The amplitude of the "dip/spike" is only some hundred milli-Volt, but sufficiently big to trigger the controller of the first PPM into switching off.

Current implementation:

The controller's sensitivity is +- 10%, i.e. +- 300mV and "fast" reacting. It can been decreased by "flattening" the spike (passive filter on the sense-line). Then, the current-surge on the 3.3V does not lead anymore to "switching-off" a neighbour-PPM in the crate.

- Use of "Hot-Swap".

First design: The originally intended use of "hot-swap" implied only, that power at the PPM-board is switched-off for exchange of the module. It does NOT ascertain quiescent VME-bus traffic. Consequently, a reboot of a crate-controller or other non-intended actions can take place.

Current implementation:

The problem has been eliminated by powering the bus-defining CPLD from a source which goes OFF last (5V instead of 3.3V). This prevents "undefined states" on VME bus-lines, which may lead to undesired actions in the crate.

- Miscellaneous: PCB, assembly....

TTC-distribution: The PPMs in the VME-crate shall receive a TTC clock with equal delay from the distribution point, the TCM in slot 21.

Technically, this means to develop hardware (flex PCB?) to distribute the electrical TTC-PECL signals with the same propagation delay (equal "route-length" on PCB) to the slot#5 up to slot#20. The physical place is the rear of connector P0 on the VME backplane.

Assembling connectors: The assembling company must watch the alignment of "Mezzanine" connectors holding the daughterboards. Those connectors have, unfortunately, no mechanical alignment pins. Hence, alignment must be controlled by automatic placement onto the solder-pads. We (KIP) must emphasise this point before production starts – or else, have a lot of re-work to do.

Summary, Schedule, Production Testing.

Summary:

KIP proceeds to build the PPM with all the improvements included as listed above with the clear aim to obtain a FINAL version. Validity of the modifications has been proven in detailed tests: @ Laboratories in KIP and RAL and @ ATLAS in CERN.

Time-Planning:

We go for a "pre-series" of 16 (+2 = 18) FINAL PPMs. They make up one full PP-Crate as it will be configured in ATLAS-USA15. Tests of full crate-operation shall show the viability of the system for operation in the experiment over the many years of ATLAS-DAQ to come.

Layouting, starting from the reviewed schematics, will be done with outmost care and, probably, to a very large extent "by hand". The PCB-part, where most work will go in, is the "rear part" of the PPM, i.e. the "digital" side behind the MCMs. Experience gained with the first design will definitely be used. No new tooling will be tried out at this stage.

The time foreseen for layouting is Jan./Feb. 2006 (6 weeks). PCB manufacturing brings the PPM project to mid-March 2006. In-house assembly and thorough testing of the first PPM lasts another month till mid-April 2006.

Assembly of the remaining PCBs (16 or 17) takes 4 weeks till mid-May 2006. It must be noted, that 72 ANIN boards and 18 LCD boards have to be produced in parallel during Feb.-Apr.2006. The necessary MCMs (>288 pieces) will be available.

A full Pre-Processor Crate (16 PPMs) for CERN-USA15 could be available at the end of May 2006.

"Full Production"planning (for another 142 PPMs).:

Production of PPMs (142), ANINs (568+spares), LCDs (142+spares) will have to take place in the second half of 2006.

"Full Production" Testing:

KIP has infrastructure for production-testing of fully equipped PPMs. A VME-crate serving as "test-rig" is available at our laboratory. The crate's power is (will be) equipped with an added 48Volt power-brick to run a 9U ROD in the test-environment as well.

Hence, the test-rig consists of:

- 9U VME-crate with CPU (set-up, control, spy readout).
- TCM for TTC-distribution.
- 6U VME-crate for TTC generation.
- 64-fold analog Input to feed a PPM.
- Multiplexer to check 4 LVDS channels into LVDS receiver in 6U VME.
- 9U ROD to check G-Link output.

The running of the test-rig requires software-overhead, which must be completed. Many software blocks are already put togther into a package similar to the MCM test-package.

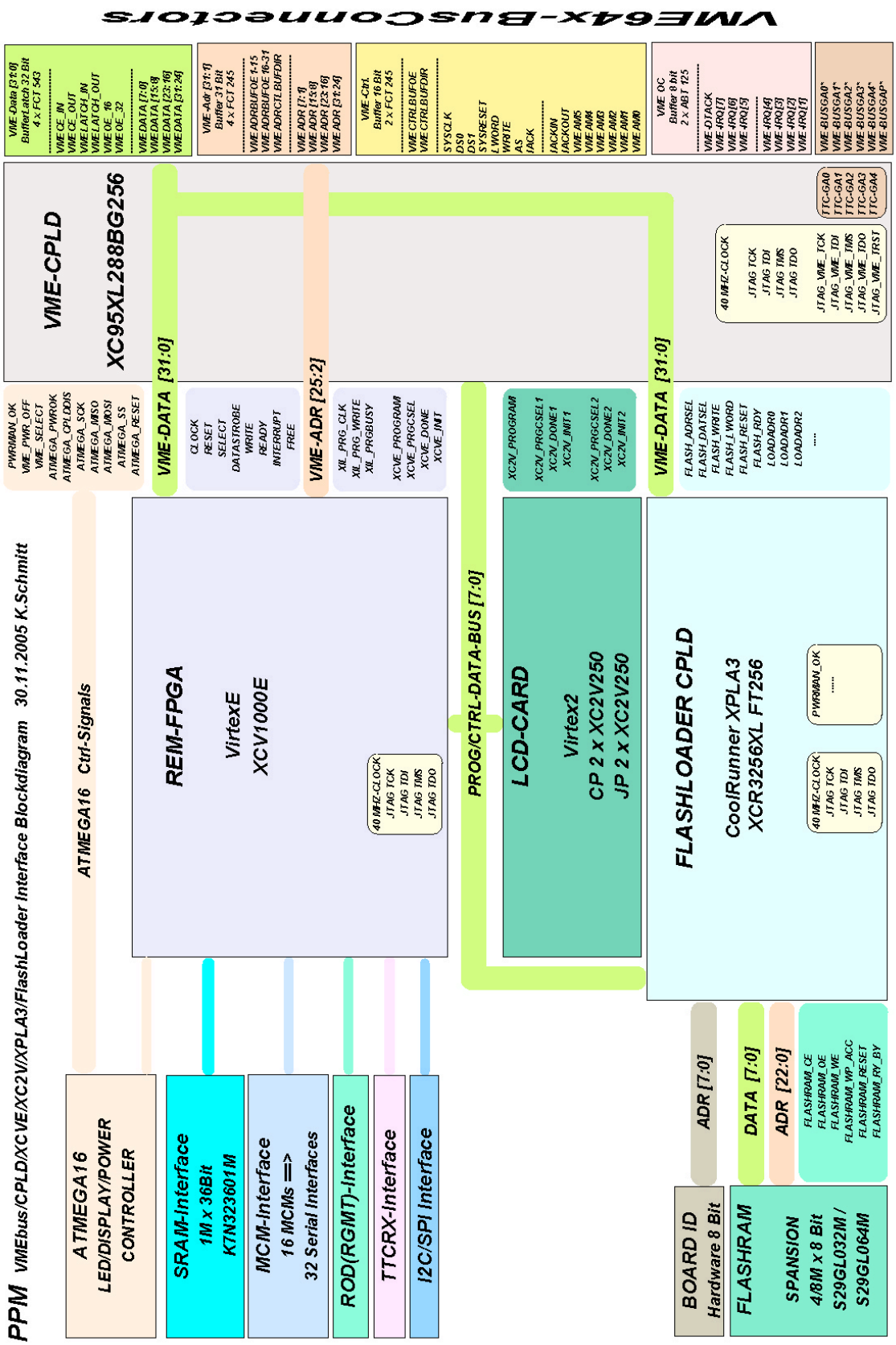
ATLAS Check-out:

The "updated" FOUR existing PPM-prototypes do the "job" properly. They cover the needs for calorimeter signal check-out during 2006.

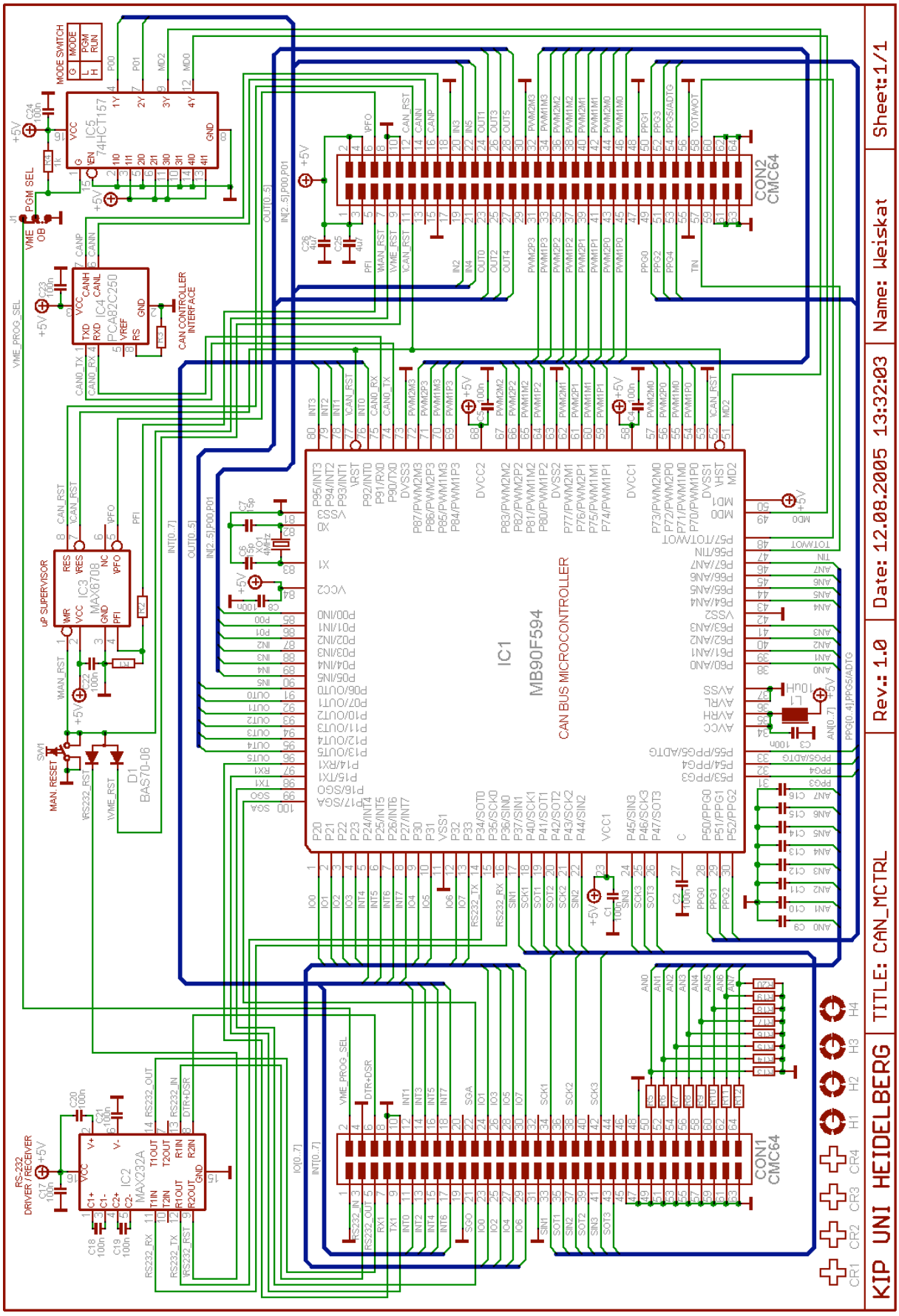
CONTENT

Appendix (PPM-VME, CAN, Technical Listings)

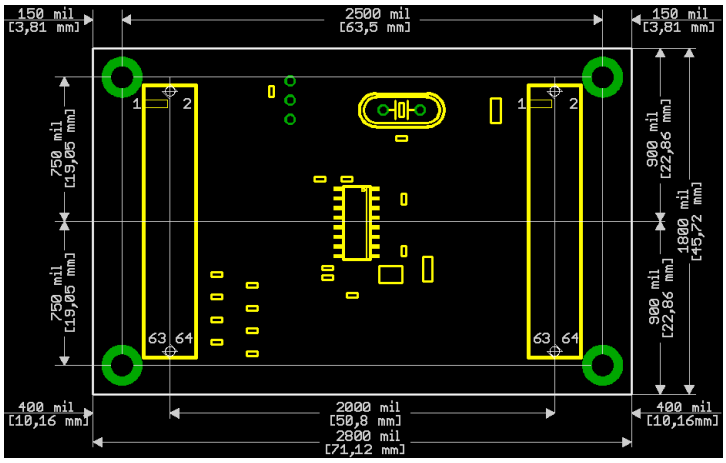
- PPM-VME block-diagram



- Schematics of CAN-Controller.



- Dimensions of CAN-Controller.



- List of “technical” modifications, which resulted from the points listed in this document.

PPM Änderungs Liste 26.10.2005

F.-Nr.	Korrektur in	Kennwort/Bauteil	Text	S
1	Lib	VMEHOTSWAP	kein Lötstop auf bottom am Schalter-Stecker	9
2	Lib	RM 4720	Pad zu enge aneinander (ca. + 0.6 mm)	9
3	Lib	RM2716	Pad zu enge aneinander (ca. + 0.4 mm)	9
4	Lib	PPM_TTC_RX	SteckerPins zu enge aneinander (ca. + 0.6 mm)	60
5	Rou	PPM_TTC_RX	Keine VIA im Stecker (Lib Via keep_out)	60
6	Lib	TO220SR	Pin 1 + Pin 3 vertauscht	9
7	Lib	XV3	Pin 1 Marke	13
8	Lib	2x5A_56_40_W	Pin 1 Marke (2x7, 2x8, ... genauso)	13
9	Lib	SOT89	Pad zu klein	19
10	Lib	TO92 T6	Replace to SMD	18
11	Lib	PCAN	Pin 1 Marke	18
12	Lib	9U_FIX	Rout keep out zu klein	
13	Scm	HotSwap	Vorlast an PWR-Eingängen (Plan-Seite)	9
14	Scm	U15	Pullup an FlashRAM BY#	14
15	Scm	R98	Pullup an XCVE_VME_RDY / XCVE_VME_INT -> 3k3	
16	Lib	RES4DIL_1206	Pin 1 Marke	
17	Rou	CPCI.....	Massebrücken zu dünn	47
18	Mech	9U_FIX	Kanten runden	
19	Scm	ATMEGA16	Pullup an CPLDDIS -> 2k2 Ohm	19
20	Rou	LSND3B5	Sense-Leitung zu dünn	9
21	Lib		Bohrloch Mezzanin zu klein	
22	Lib	K7M803625M	Pad zu schmal	52
23	Scm		Serien-R rück GLINK (alles nach J2)	10
24	Scm/Lib	-	Testpin 12V, 5V, 3.3V, -12V, Gnd als Block	9
25	Scm	HotSwap	3v3 über FET nach 0V (Transistor&FET)	9
26	Scm		Tiefpass am G -12V PWRFET	
27	Scm	R148, R149, R152	Done-Sig PullDown R , 33k	
28	Scm	TTCrx	Verzugslage R!! -> 1kOhm	60
29	Mech/Lib	ANIN, MCM	2,5 mmFertigmaß f. Haltelöcher	
30	Mech/Lib	LCD	2,5 mmFertigmaß f. Haltelöcher	
31	Mech/Lib	TTCrx	2,5 mmFertigmaß f. Haltelöcher	
32	Scm		PWRon von CAN -> PWRon after SYSFAILE	18
33	Scm	VME-P2	PWRout VCC, Pin D13 / D14 / D15 / D16 nach Rear Gling BOA	10
34	Scm	R2_0, R3_0	2mOhm PWR-Sense	9
35	Scm	R4_0	100mOhm PWR-Sense	9
36	Scm	U17-U20	Serien-R in alle von MCM	
37	Scm	U17-U20	CLK Verteilung und Termin. zu MCM	
38	Scm	U13 CPLD	Serien-Termin XIL_PRG_CCLK Pin J4 = 47 Ohm	13
39	Scm	R18_(1-16)	100 Ohm	
40	Scm	R2_(1-16)	1 kOhm	
41	Scm	R4_(1-16)	470 Ohm	
42	Scm	R20_(1-16)	kein Widerstand, Leiterbahn auf Top, A-GND D-GND	
43	Scm	R42, R45	470 Ohm I2C-Bus	
44	Scm	R43, R44	1 kOhm I2C-Bus	
45	Scm	R67, R68	10 Ohm TTC-RX ???	
46	Scm	R65, R66	100 Ohm TTC-RX	
47	Scm	S21P1 LCD	Xilinx select 2x neu (4Chip)	
48	Scm	S23	CAN-Micromodul neu!!! (VME / RS232 connect)	18
49	Scm	>RGTM<	RearG-Link Modul optic neu!!!	
50	Scm	P22	Pulldown f. JTag ext.	17
51	Scm	R13x, 14x, 15x	R-L Terminierung an MCM lvds out	24ff
52	Scm	"	Symmetrier-R an MCM lvds out	
53	Scm	X3	Ausgang gebuffert auf RearG-Link Modul	44
54	Scm	-LED-	Freie LED's zuordnen	44
55	Rou		Anitstatic-Strip lang, nur Lötseite (LPmax =2.0mm)	
56	Scm		CAN-Bus Signalpin`s , wo hin???	10
57	Rou	Frontpl.	Brk. GND - Erde zu duenn	
58	Scm	TTCrx	Testpin CLK-dist	
59				

PPM Änderungs Liste 26.10.2005

F.-Nr.	Korrektur in	Kennwort/Bauteil	Text	S
60				
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67			PWR-up 3,3V PWRFet == schneller !?!?!	
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91	Bestueck	Mezzanine-Stecker	Ausrichtung fuer DaughterPCBs !	
92	Mech	TTCdec	Loecher fuer Befest.-Schrauben ?	
93	PCB	LEDs	Front-Panel: Clk=vorh.; L1-Accept? VME-Access?	
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