Project Specification

Project Name: ATLAS Level-1 Calorimeter Trigger – TTC Decoder Card (TTCDec)

W. Qian

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Distribution for all updates:

Project Manager:	**V. J. O. Perera**
Customer:	**C. N. P. Gee**
Group Leader responsible for Project:	**R. N. J. Halsall**
Project Managers of related projects:	**R. Staley, S. Silverstein, U. Schaefer**
Account Manager:	**S. P.H. Quinton**
Level-1 Trigger Project Manager:	**E. Eisenhandler**

Contents

Document History

Version 1.0	(September 2003)	First release
Version 1.1	(November 2005)	Routed Clock40Des1 before PLL to original Clock40 pin Added drawings of mounting holes Added production test plan

1 Scope

This document describes the specification for the production TTC Decoder (TTCDec) card, which will be used in the ATLAS level-1 calorimeter trigger system.

The LHC Timing, Trigger and Control (TTC) signals are encoded together and distributed over a hierarchy of passive optical fiber tree couplers. Within the ATLAS level-1 calorimeter trigger system, one TTC optical fiber is brought to each individual processor crate, where a TCM module converts the optical TTC signal into electrical TTC signal and then distributes the electrical TTC signal to all other processor modules within the same crate. On each processor module, a TTC Decoder card is used to decode the incoming electrical TTC signal and provide synchronous timing, level-1 trigger and broadcast and individually-addressed controls.

2 Related projects and documents

2.1 TTC web at http://ttc.web.cern.ch/TTC/intro.html
2.2 TTCrx manual at http://ttc.web.cern.ch/TTC/TTCrx_manual3.10.pdf
2.3 TTCFanout module at http://hepwww.rl.ac.uk/Atlas-L1/Modules/TTC/TTCFanout_Version1.0.pdf
2.4 ATLAS TDR at http://atlasinfo.cern.ch/Atlas/GROUPS/DAQTRIG/TDR/tdr.html

3 Requirement and specifications

The TTCDec card is implemented as a plug-on daughter-card. In the center of this daughter-card is a TTCrx ASIC chip developed by CERN RD12. The main tasks of the TTCDec card are:

- Provides suitable powers to TTCrx ASIC and other onboard logic
- Provides buffering for input electrical TTC signal
- Routes signals between TTCrx ASIC and TTCDec connectors
- Provides LED indication for TTCrx locking status
- Provides power-up reset function
- Provides terminations for differential TTC signal input and I2C bus
- Provides on-board crystal clock and clock selection function
- Provides PLLs for zero-delay clock distributions
- Sets the initial TTC address of TTCrx ASIC

3.1 Block diagram

The block diagram of TTCDec card is shown in Figure 1. Apart from TTC input, reset and clock signals, all other signal pins on TTCrx ASIC are directly routed to the connectors of the TTCDec card.

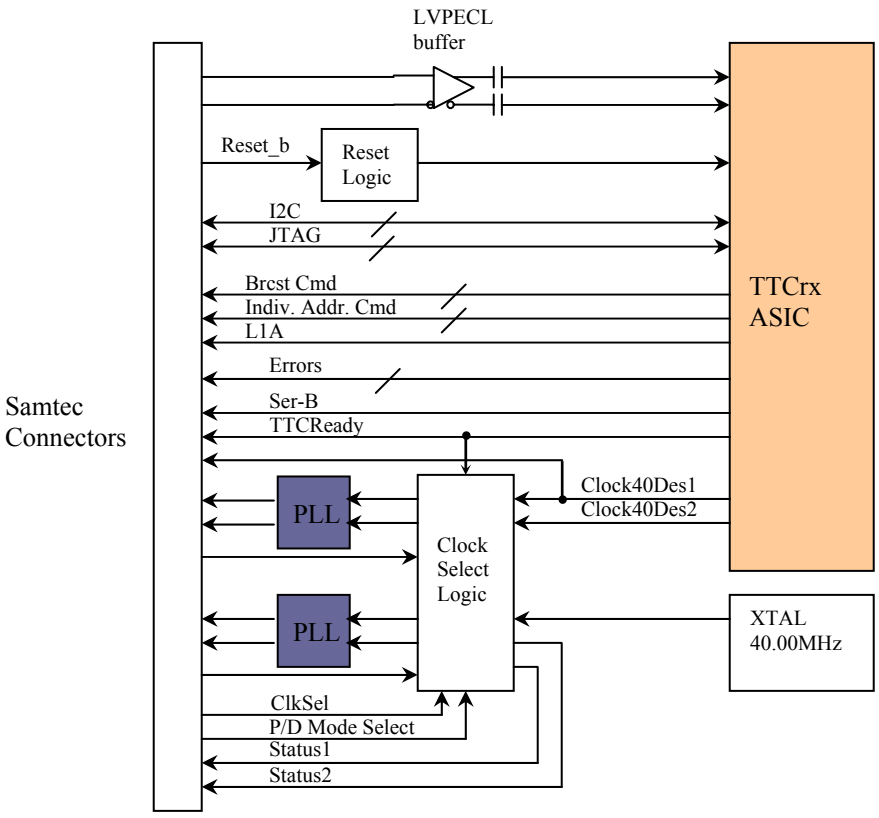


Figure 1: TTCrx Block diagram

3.2 Power supply

The TTCDec operates with only +3.3V. Onboard filter generates quiet supply for the analog part of the TTCrx ASIC and PLLs.

3.3 TTC signal buffering

The TTCDec only accepts +3.3V LVPECL differential TTC signal input. A LVPECL line receiver (MAX9321) is used on the TTCDec to buffer the TTC signal input.

3.4 Reset

The TTCDec provides on-board power-up reset function, which resets the TTCrx ASIC upon power-up. The TTCrx ASIC can also be reset by an external reset pulse (Reset_b), which, according to TTCrx manual, should have a width of 50us at least.

3.5 Clocks and PLLs

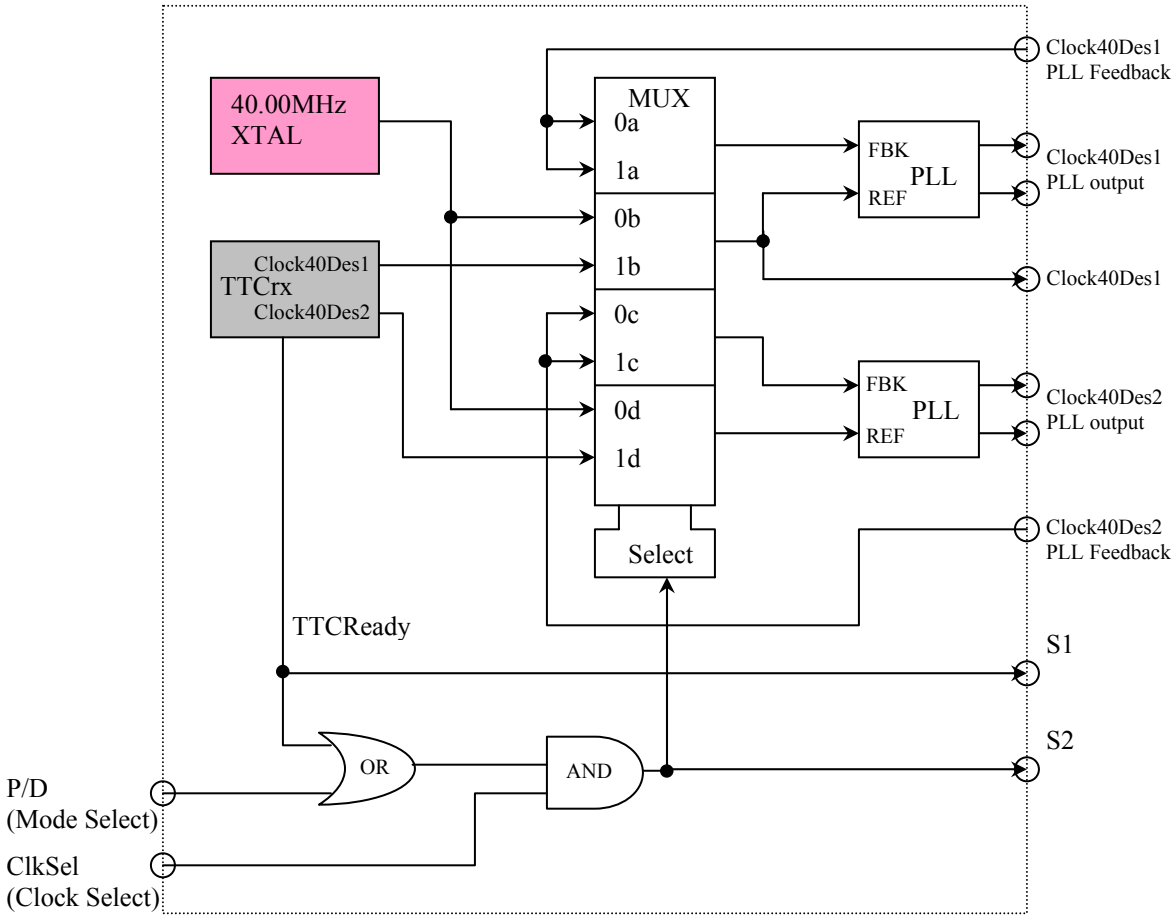


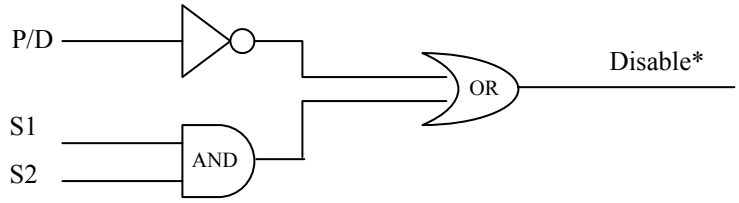
Figure 2: Clock selection scheme on TTCDec

The clock selection scheme on the TTCDec is shown in Figure 2. There are two input control bits (P/D Mode select and ClkSel clock select) and two output status bits (S1 and S2). The two deskewed clocks from TTCrx, Clock40Des1 and Clock40Des2, are selected or deselected simultaneously. The detailed function is as below.

- P/D = 1: Protected Mode (Normal Running Mode)
  - ClkSel = 1: Select TTCrx as clock source, S1=TTCReady, S2 =1
  - ClkSel = 0: Select XTAL as clock source, S1=TTCReady, S2 =0
- P/D = 0: Debug Mode
  - ClkSel = 1: Clock source automatic changeover
    - TTCReady = 1: Select TTCrx as clock source, S1 =1, S2 = 1
    - TTCReady = 0: Select XTAL as clock source, S1 =0, S2 = 0
  - ClkSel = 0: Select XTAL as clock source, S1=TTCReady, S2=0

In Protected Mode (P/D = 1), the control bit ClkSel should be set according to the status bit S1 (TTCReady). Whenever S1 = 0 or S2 = 0, which means TTCrx lock loss or XTAL selected as clock source, the corresponding motherboard **MUST** disable data being sent

on the external interfaces (one example of active low Disable* logic is shown below). When S1=0 and S2=1, which means TTCrx is the clock source and TTCrx is not ready, the output clock is the TTCrx free-running clock, so the output clock frequency is UNKNOW.



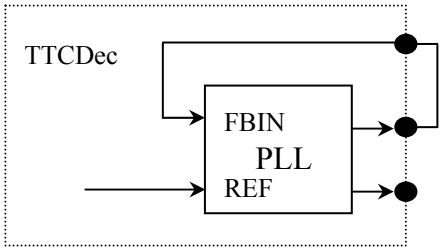
In Debug Mode (P/D = 0), motherboard can either select XTAL as clock source or change clock source automatically according to the TTCReady of TTCrx.

The MUX is inserted into the PLL feedback path as well to compensate the propagation delay through the MUX in the reference path.

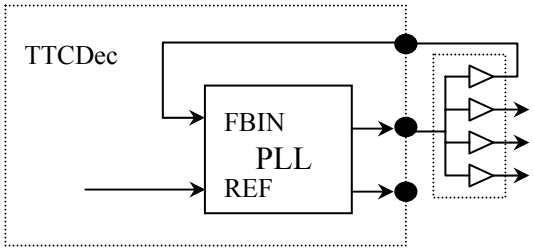
It is recommended that each motherboard put 2 LEDs on its front panel for the two status bits S1 and S2 from the TTCDec, so that it is easy to find out the lock status of the TTCDec and which clock source is used.

The Clock40Des1 before the PLL is also routed to the TTCDec connector. This Clock40Des1 may be used by PPM to drive the LVDS link.

The feedback input pins of PLLs are routed to the TTCDec connector as well, allowing for zero-delay clock fanout distribution to be constructed on motherboards as shown below.



PLL configuration without fanout



PLL configuration with external fanout

3.6 Signal timing

All signal tracks are of minimum length. The time skew due to the signal track length difference is negligible (no more than 0.1ns).

3.7 Indicators

One LED for TTCReady on the top side of the TTCDec.

3.8 Grounding

The internal ground planes in the middle of the Samtec Q-Strip connectors H1 and H2 should be connected to the PCB ground at various points to improve electrical performance.

For high-speed signals (especially the clocks), ground pins should also be assigned near the signal pins within the connectors.

3.9 Termination

The differential TTC signal input is parallel terminated with a 100 Ω resistor.
The I2C bus is pulled-up to +3.3V by 2.2 KΩ resistors.

3.10 Configuration

No EPROM is needed. EnProm/PromReset pin is connected to GND via a 100k resistor.

SubAddr<7:6> are connected to GND via 100k resistors.

I2C_ID and Chip_ID addresses are set initially by resistors on SubAddr<5:0> and Dout<7:0> upon reset. Dout<5:0> are connected to GND via 100k resistors, Dout<7:6> and SubAddr<5:0> are connected to VCC via 100k resistors. So the initial I2C address is 00h, and the initial TTC chip address is 3FC0h.

The TTCrx can be configured through I2C interface. Two pull-up resistors on the TTCDec connect SCL and SDA to VCC for correct operation.

If JTAG signals are not used, the JTGATCK, JTAGTDI, JTAGTMS and JTAGTRST_b signals (CMOS inputs) should be fixed to logic 0 on the 9U motherboards. A solder link is also provided for JTAGTRST_b signal on the TTCDec to fix it to ground if needed.

3.11 Testpoints

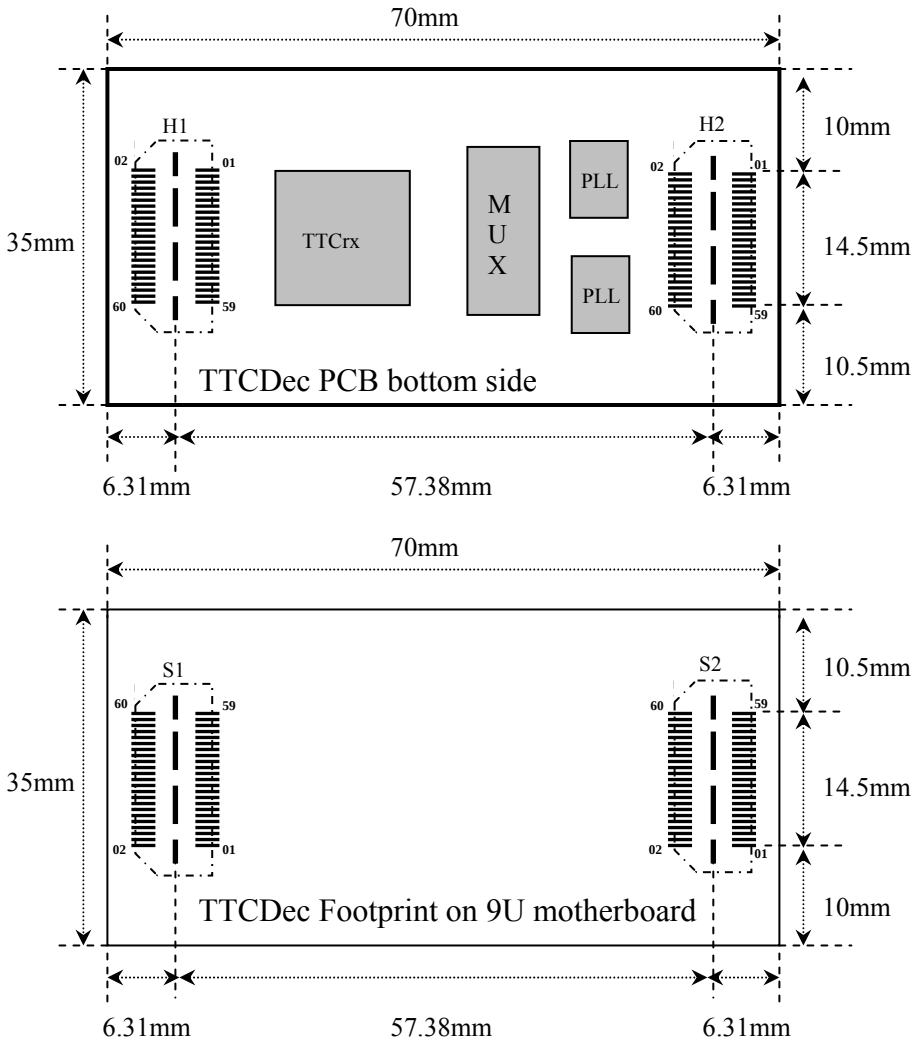
Testpoints should be provided for TTC input, TTCReady, Reset, Clock40, L1A, VCC and GND on the top side of the TTCDec.

4 Implementation

4.1 Physical dimensions

In order to minimize the dimensions of this daughtercard, active components may be placed on both sides of PCB board. On 9U motherboard, no components should be placed underneath the TTCDec except for the two sockets S1 and S2.

The following figures give a rough idea of the possible PCB layout. The final dimensions may change and subject to the real layout design. Datasheet of Samtec QStrip Mezzanine connectors should be referred to when making the footprints for the headers and sockets. The alignment pins of the connectors should be placed within the footprints for assembly. Attention should be paid to the different numbering of pin assignment for header footprint and socket footprint.



4.2 Connector type and Pin Assignments

The connectors chosen for the TTCDec are Samtec Q-Strip Mezzanine Connectors:

- QSH-030-01-L-D-A (socket on motherboard)
- QTH-030-01-L-D-A (header on TTCDec)
- Pin pitch: 0.5mm, Stack height: 5mm
- Pin number: 60 (30 per row, dual rows)

The pin assignment of connectors H1 and H2 on the TTCDec card is shown in Table 1 and Table 2.

Pin No.	***Pin Name***	***Pin No.***	***Pin Name***
1	DoutStr	2	GND
3	DQ0	4	DQ1
5	DQ2	6	DQ3
7	GND	8	GND
9	SubAddr0	10	SubAddr1
11	SubAddr2	12	SubAddr3
13	SubAddr4	14	SubAddr5
15	SubAddr6	16	SubAddr7
17	GND	18	GND
19	Dout0	20	Dout1
21	Dout2	22	Dout3
23	Dout4	24	Dout5
25	Dout6	26	Dout7
27	GND	28	GND
29	Reset_b	30	Status1
31	GND	32	Status2
33	GND	34	GND
35	In	36	GND
37	In_b	38	GND
39	GND	40	GND
41	GND	42	P/D
43	SCL	44	ClkSel
45	SDA	46	VCC
47	GND	48	VCC
49	JTAGTDI	50	VCC
51	JTAGTMS	52	VCC
53	JTAGTDO	54	VCC
55	JTAGTCK	56	VCC
57	JTAGTRST_b	58	VCC
59	GND	60	VCC

Table 1: H1 Header Pin Assignment

Pin No.	*Pin Name*	*Pin No.*	*Pin Name*
1	SinErrStr	2	DbErrStr
3	GND	4	GND
5	Clock40Des1	6	Clock40L1A
7	GND	8	GND
9	Clock40Des2_FBIN	10	GND
11	GND	12	Clock40Des1_FBIN
13	Clock40Des2_PLL1	14	GND
15	GND	16	Clock40Des1_PLL1
17	Clock40Des2_PLL2	18	GND
19	GND	20	Clock40Des1_PLL2
21	GND	22	GND
23	GND	24	GND
25	BrcstStr1	26	Brcst2
27	Brcst3	28	Brcst4
29	Brcst5	30	BrcstStr2
31	Brcst7	32	Brcst6
33	BCntRes	34	EvCntRes
35	GND	36	GND
37	EvCntHStr	38	L1Accept
39	BCntStr	40	EvCntLStr
41	GND	42	GND
43	BCnt1	44	BCnt0
45	BCnt3	46	BCnt2
47	BCnt5	48	BCnt4
49	GND	50	GND
51	BCnt7	52	BCnt6
53	BCnt9	54	BCnt8
55	BCnt11	56	BCnt10
57	GND	58	GND
59	GND	60	Ser_B_Ch

Table 2: H2 Header Pin Assignment

5 Testing

The tests for the production TTCDec cards include the following:

- Connectivity test
  - Signal connections between TTCrx ASIC and TTCDec connectors
- Function tests
  - Reset (power-up reset and external reset)
  - TTC input buffer
  - TTCReady (LED)
  - Clock selection
  - Clock jitter
  - Chip basic address setting

These tests will be performed in two steps.

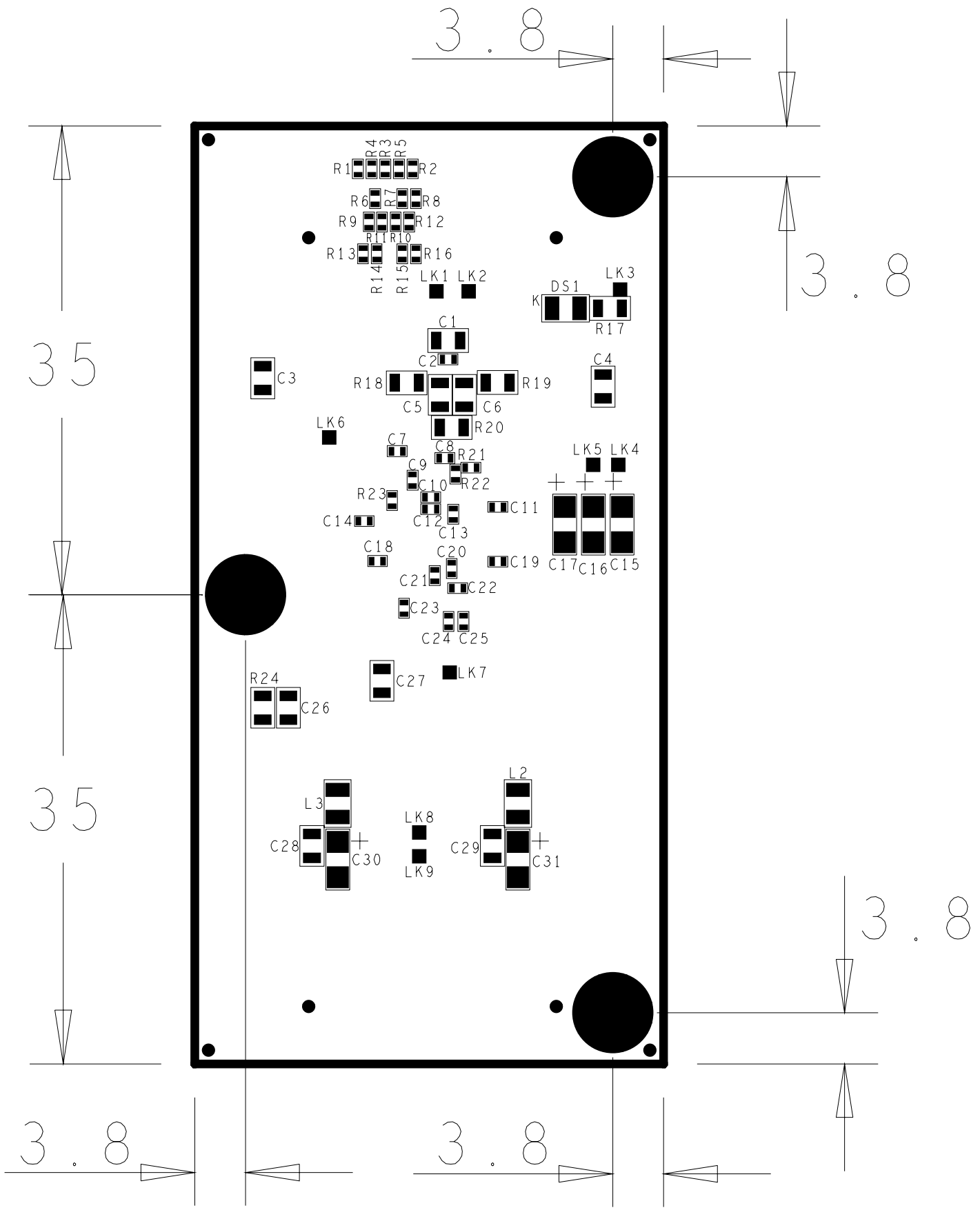
First, a TTCFanout module and an oscilloscope will be used to do the function tests of the TTCDec. In this step, functions such as Reset, TTC input buffer, TTCReady, Clock selection and Clock jitter will be tested.

After a TTCDec card passes the first step test, it will then be integrated with motherboards for the chip basic address setting test and connectivity test. So the second step test of the TTCDec card is an integral part of motherboard production test. The chip basic address setting of the TTCDec can be easily tested via I2C interface. The connectivity of the TTCDec card can be tested via JTAG by including the TTCDec into the motherboard JTAG chain. Alternatively, it can be tested by TTC commands.

ATLAS TTC DECODER CARD PC3260M/2

FIXING HOLE DIMENSIONS

BOARD VIEWED ON 'A' FACE (TOP)



ATLAS TTC DECODER CARD PC3260M/2

PHYSICAL DIMENSIONS

BOARD VIEWED ON 'F' FACE (UNDERSIDE)