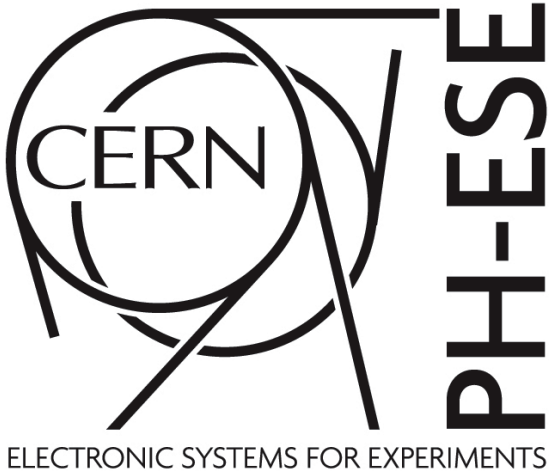

CERN
PH-ESE
ELECTRONIC SYSTEMS FOR EXPERIMENTS

The TTC system and Jitter in LHC experiments

PH-ESE seminar

18 December 2012

Sophie Baron

OUTLINE

- Bunch Clock Origin
  - From the Radio Frequency to the Bunch Clock
  - The TTC system
- What is a good Bunch Clock?
  - Vocabulary – jitter, phase noise etc..
  - Who is sensitive to what?
  - A good Bunch Clock in two words
- Measuring the clock quality
  - Bunch Clock measurement for the detectors
  - Bunch Clock measurement for the sub-systems
- Conclusion
  - Lessons learned

The Radio Frequency (RF)

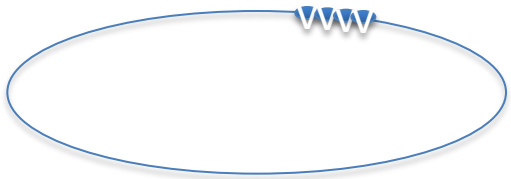
From Radio Frequency to Bunch Clock

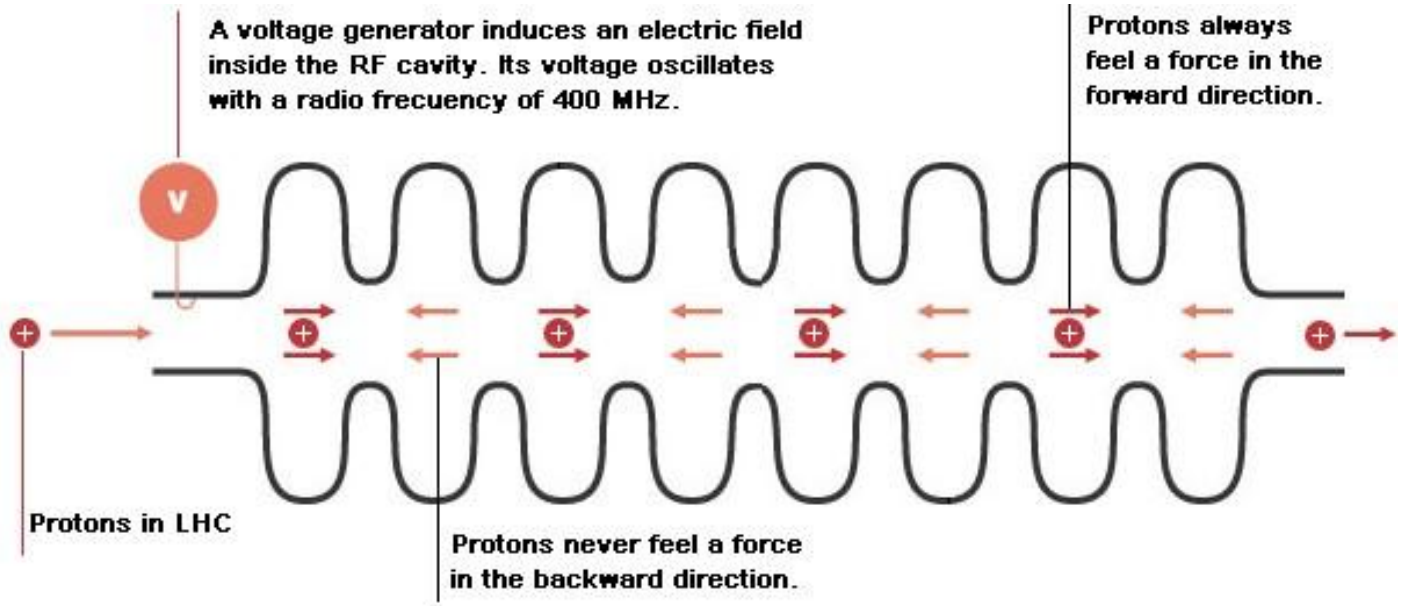
The Bunch Clock Clients

The TTC system

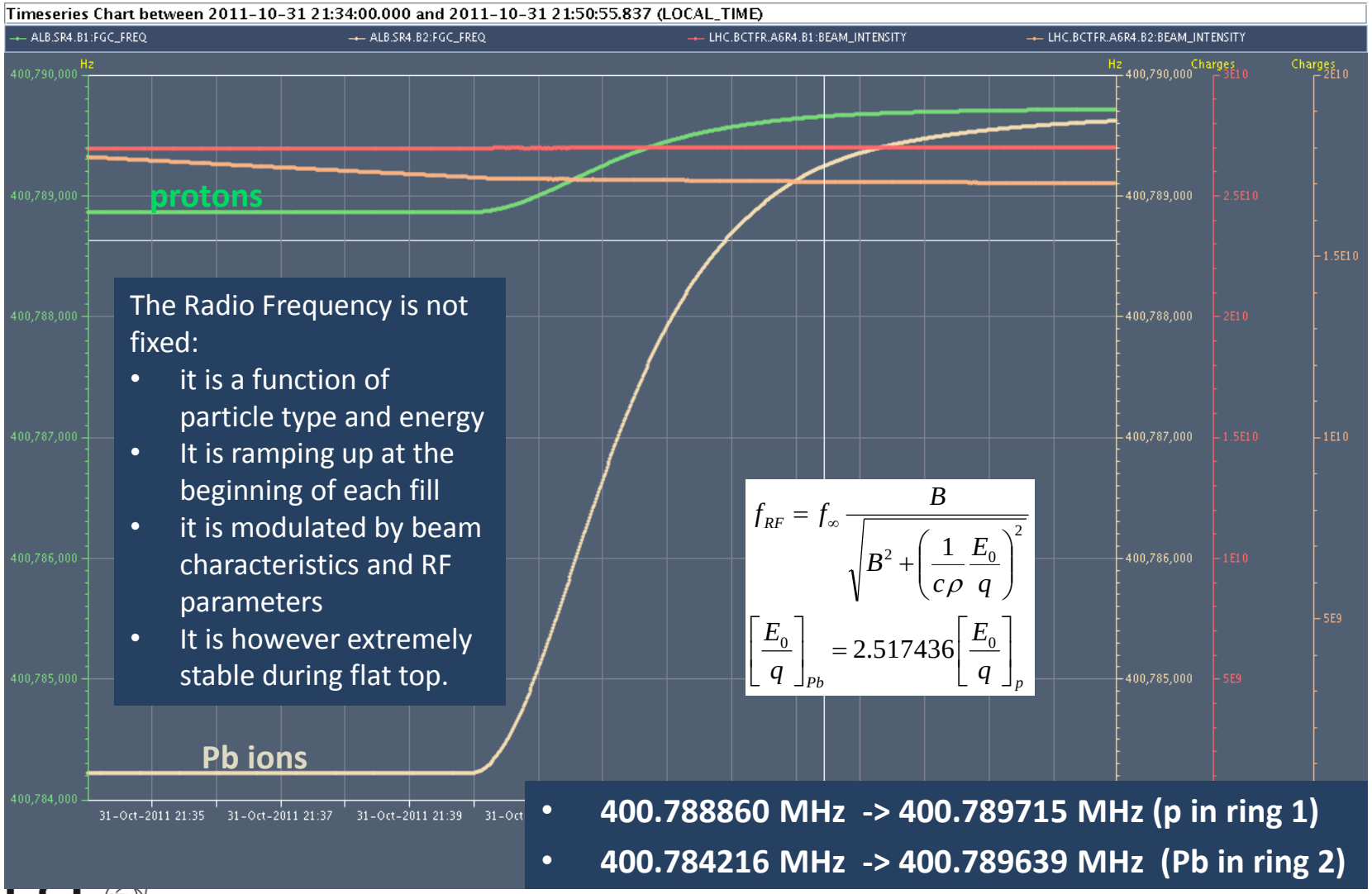
BUNCH CLOCK ORIGIN

RF cavities in LHC
(4 modules@point4, Echenevex)





The Radio Frequency is not always the same



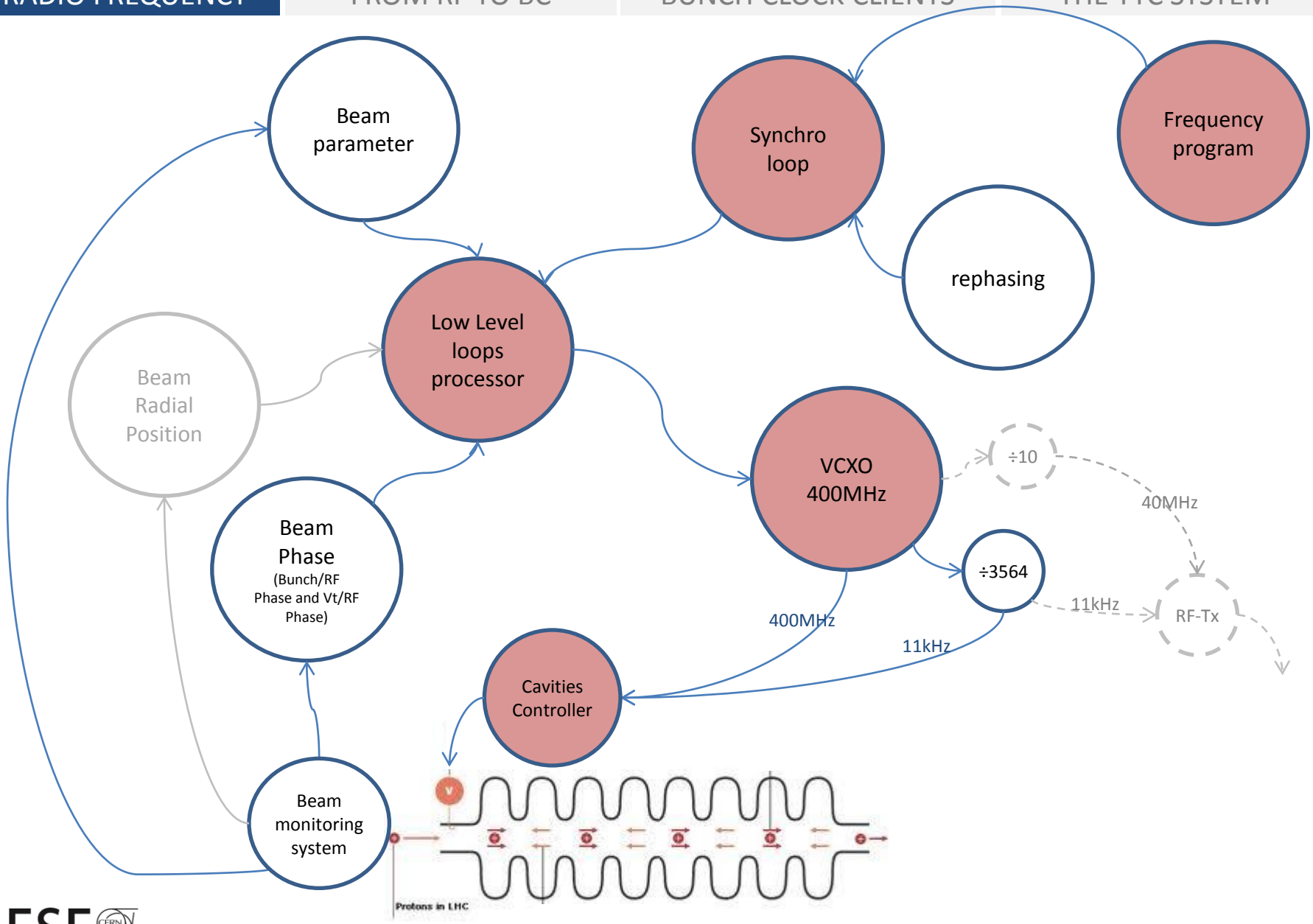
The Radio Frequency is not fixed:

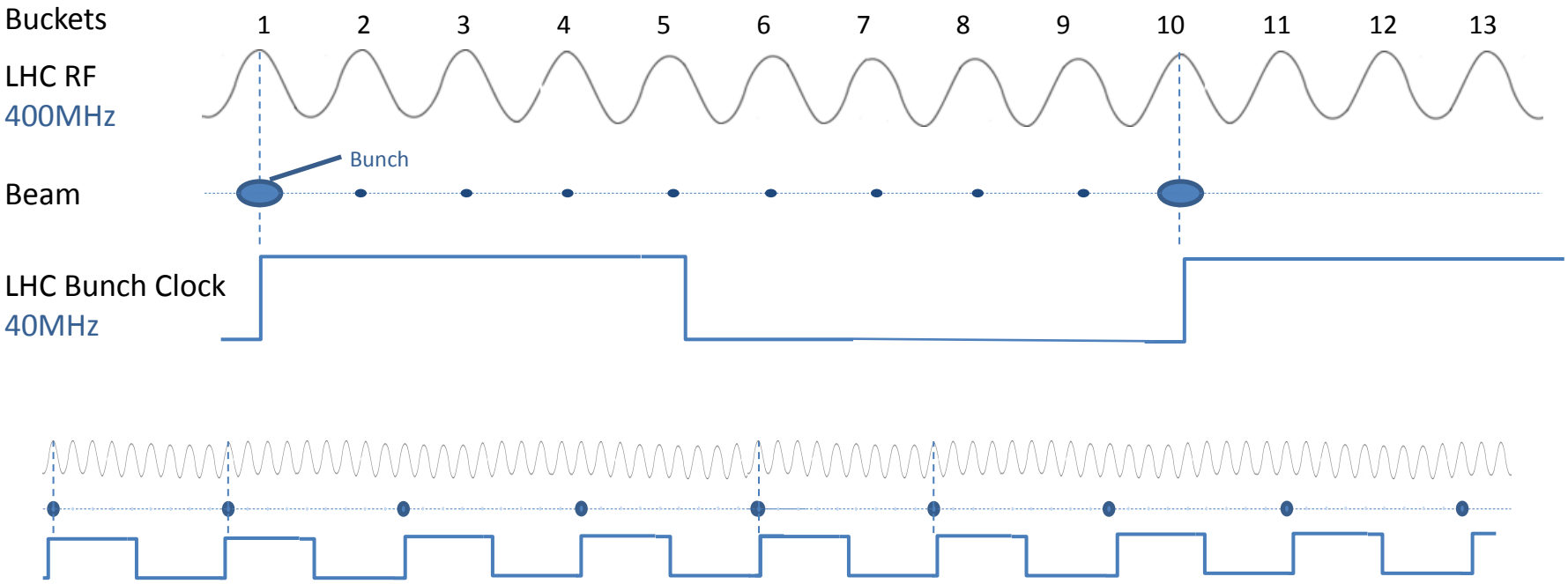
- it is a function of particle type and energy
- It is ramping up at the beginning of each fill
- it is modulated by beam characteristics and RF parameters
- It is however extremely stable during flat top.

$$f_{RF} = f_{\infty} \frac{B}{\sqrt{B^2 + \left(\frac{1}{c\rho}\frac{E_0}{q}\right)^2}}$$

$$\left[\frac{E_0}{q}\right]_{Pb} = 2.517436\left[\frac{E_0}{q}\right]_{p}$$

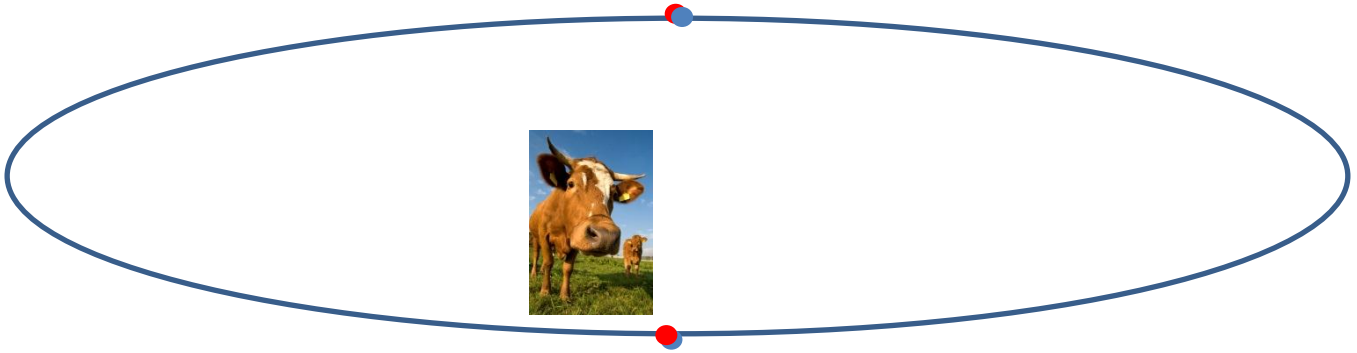
- **400.788860 MHz -> 400.789715 MHz (p in ring 1)**
- **400.784216 MHz -> 400.789639 MHz (Pb in ring 2)**


Beam parameter
Synchro loop
Frequency program
rephasing
Low Level loops processor
Beam Radial Position
VCXO 400MHz
÷10
40MHz
÷3564
11kHz
RF-Tx
Beam Phase (Bunch/RF Phase and Vt/RF Phase)
400MHz
11kHz
Cavities Controller
Beam monitoring system
Protons in LHC

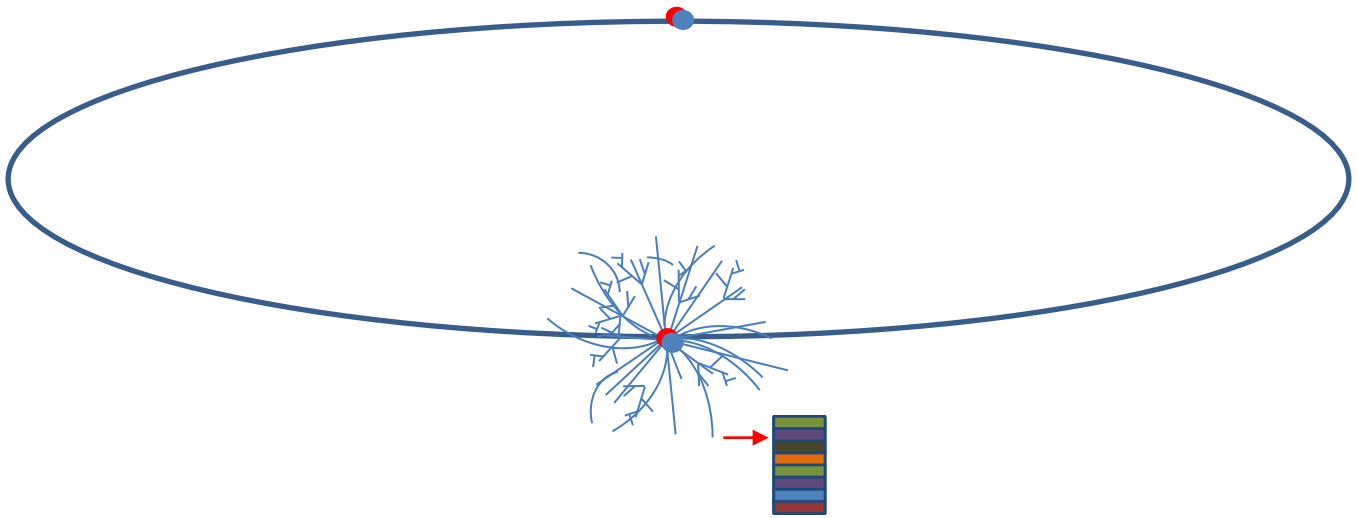


The Bunch Clock is the frequency at which an observer sitting close to the ring could 'see' particles passing

- Simplistic case: 2 bunches, 2 beams, 1 observer



- Simplistic case: 2 bunches, 2 beams, 1 experiment, 1 fifo



In detectors, everything is happening synchronously to the Bunch Clock:

- Collisions
- Signal sampling for Analogue to Digital conversion
- Time measurement
- Trigger transmission
- Data storage
- Data reduction
- Data transmission

=> The Bunch Clock has to be delivered EVERYWHERE, ANYTIME, and with a excellent QUALITY

=> This is one of the mandates of the TTC, and this is on what we will focus today

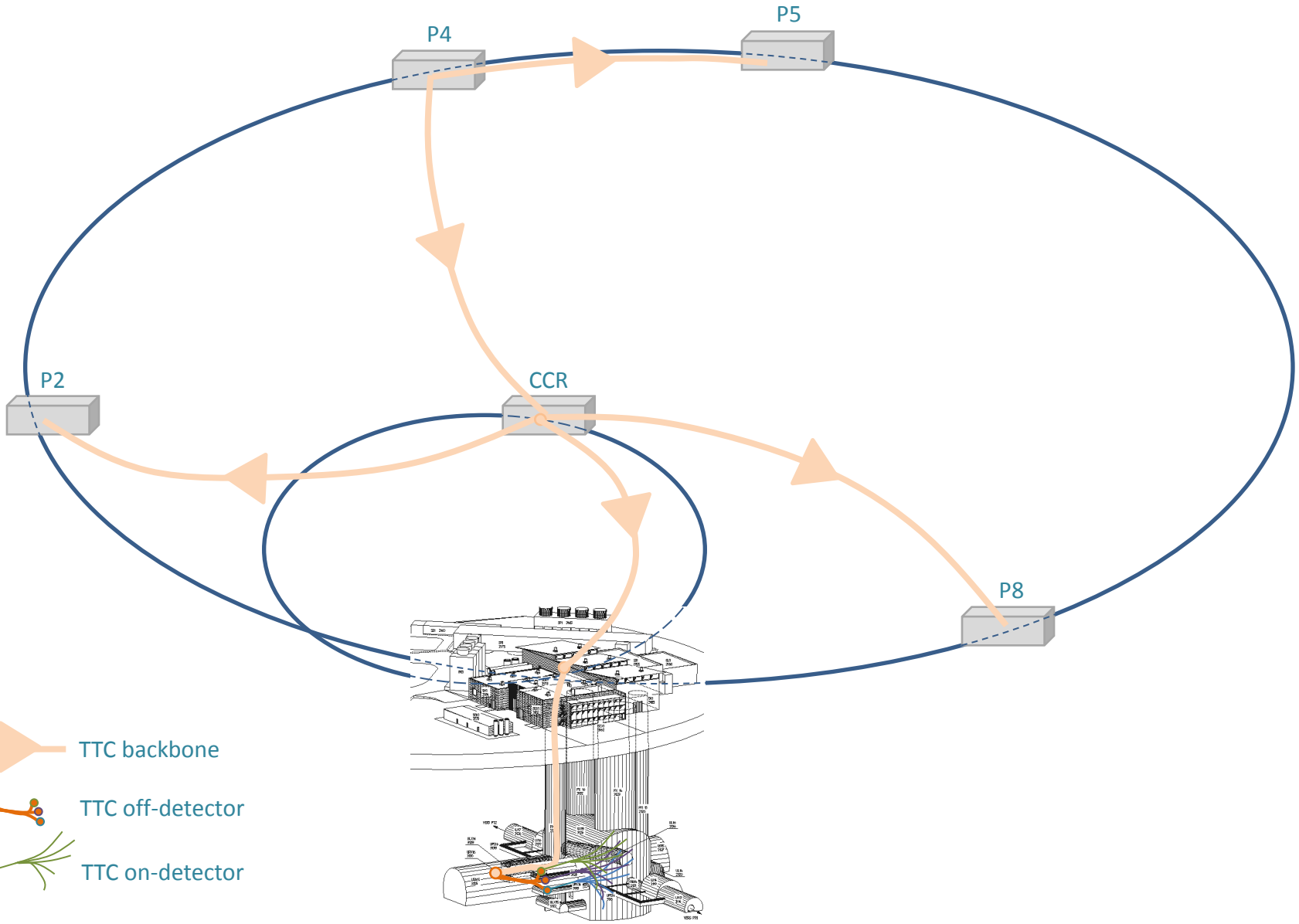
The Radio Frequency (RF)

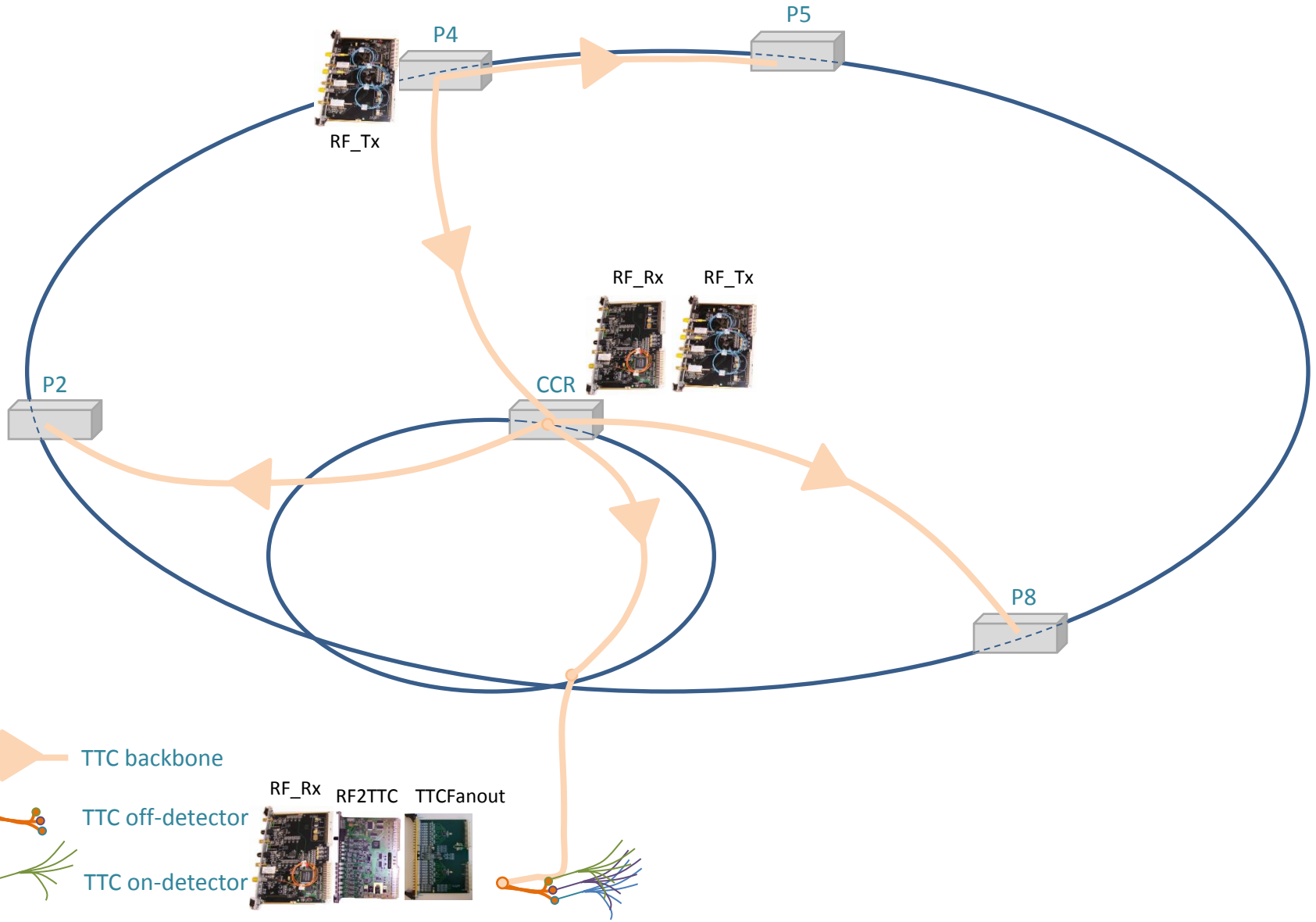
From the Radio Frequency to the Bunch Clock

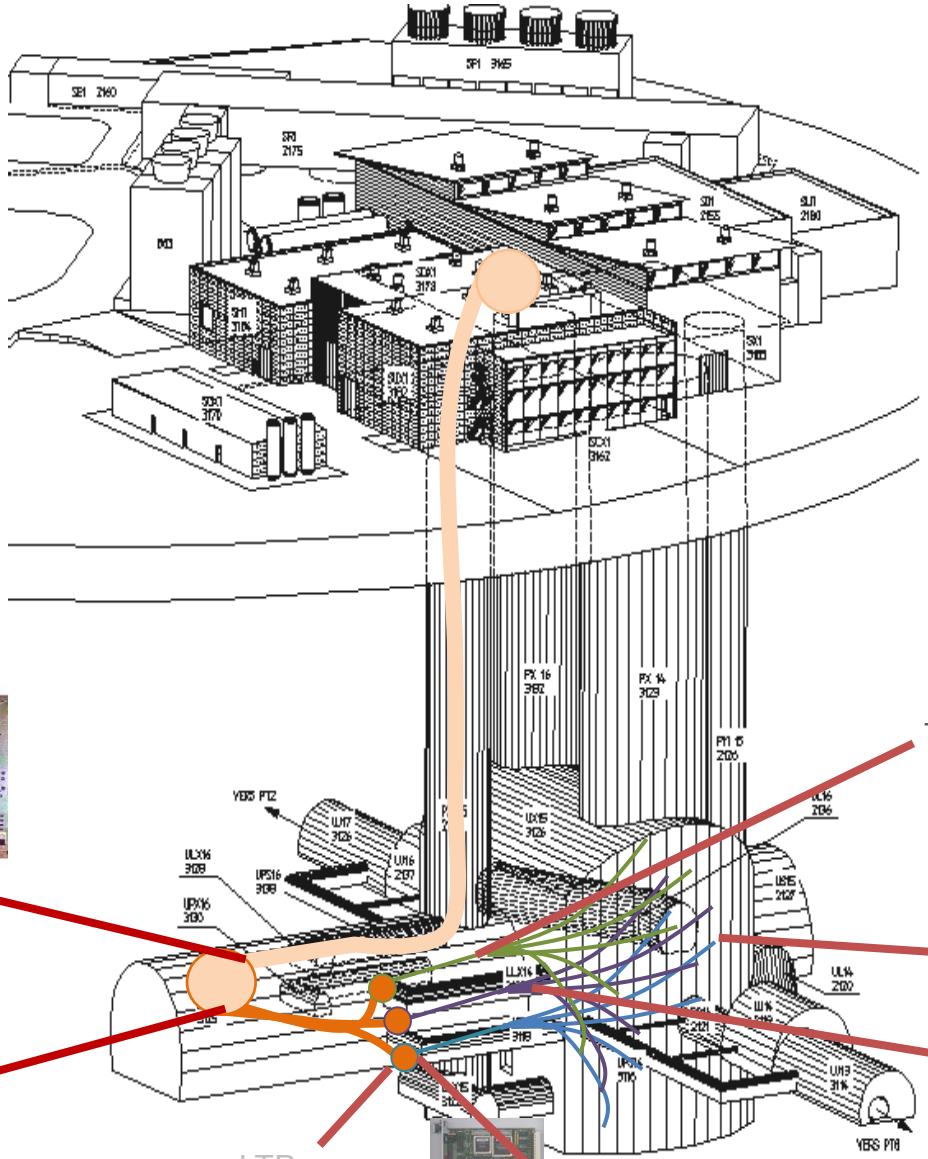
The Bunch Clock Clients

The TTC system

BUNCH CLOCK ORIGIN


P4
P5
P2
CCR
P8
TTC backbone
TTC off-detector
TTC on-detector


P4
P5
RF_Tx
RF_Rx
RF_Tx
P2
CCR
P8
TTC backbone
TTC off-detector
TTC on-detector
RF_Rx
RF2TTC
TTCFanout


RF_Rx
RF2TTC
TTC
Fanout
CTP
LTP
TTCvi
TTCex
TTCrx
TTCrq
QPLL
TTCoc

Vocabulary: Jitter & Co

Who is sensitive to what?

A good clock in 2 words

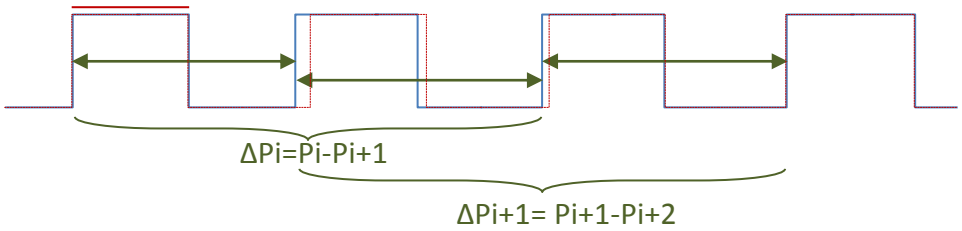
WHAT IS A GOOD BUNCH CLOCK SIGNAL?

- Time Domain measurements
  - Jitter types
    - Cycle to cycle jitter (cy2cy)
    - Period jitter
    - Time Interval Error jitter
    - Skew jitter
  - Representation
- Frequency Domain representation
  - Spectrum
  - Phase noise
- Time and Frequency domain relationships
- Jitter decomposition

Time Domain measurements

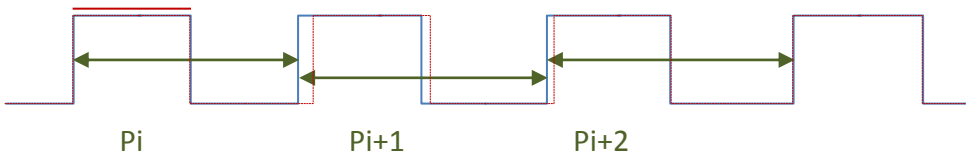
Cycle-to-cycle jitter:

Short term variation in the clock period between adjacent clock cycles.
Contains the highest frequency components of jitter.



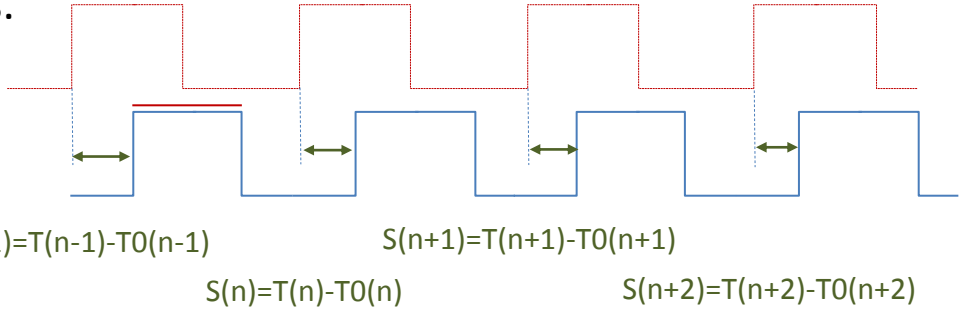
Period jitter:

- Short term variation in the clock period over all measured clock cycles, compared to the average clock period.
- Contains relatively high frequency components of jitter.
- *Do not mix with **Periodic** jitter*



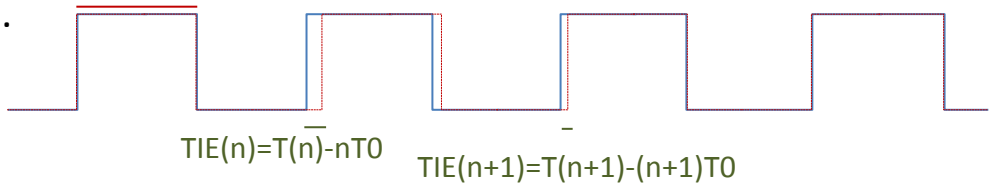
Time Domain measurements

Skew jitter: Phase error between the reference clock and the measured clock over all clock periods.

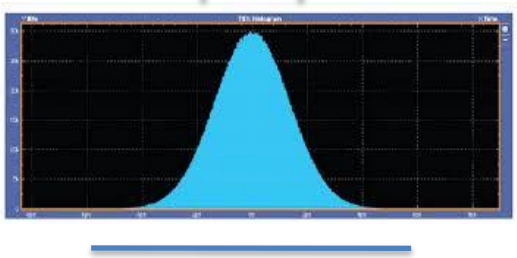
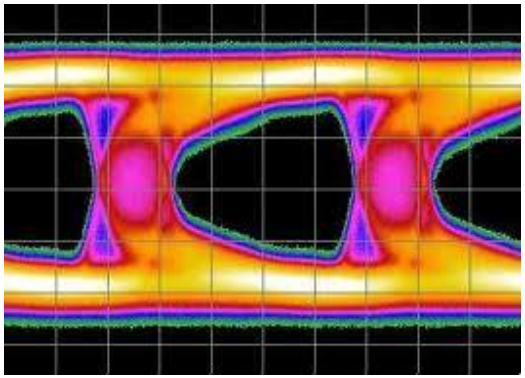
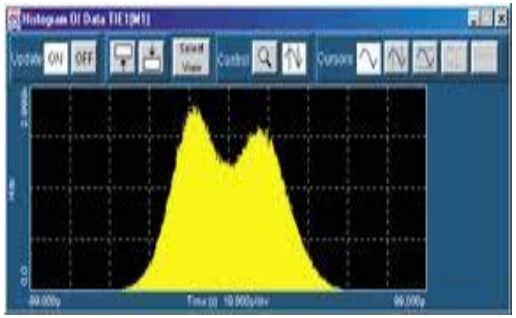


TIE jitter (Time Interval Error or accumulated/phase Jitter):

- Actual deviation from the ideal clock period over all clock periods.
- Includes jitter at all modulation frequencies.
- Analysis of its Probability Density Function (PDF) gives substantial information on the jitter sources.



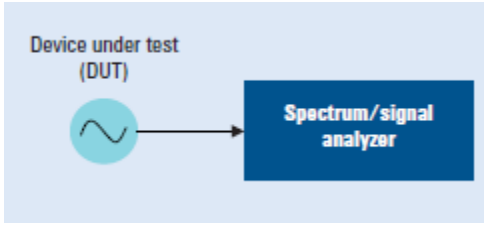
Wander: very slow variations < 10Hz.

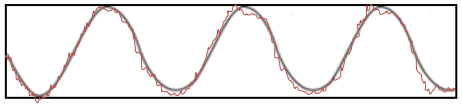
Time Domain (oscilloscope or SDA traditional views)	Probability Density Function (PDF)
	σ= std deviation = rms jitter  pkpk jitter
	

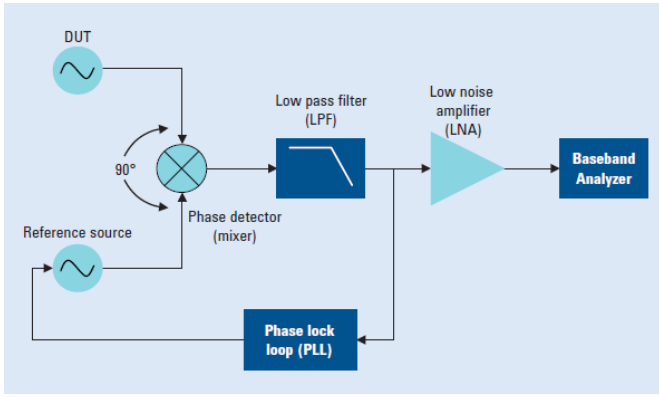
Frequency domain: Spectrum and Phase Noise

Ideal Oscillator : videal $(t) = v0 \sin 2\pi\, fct$

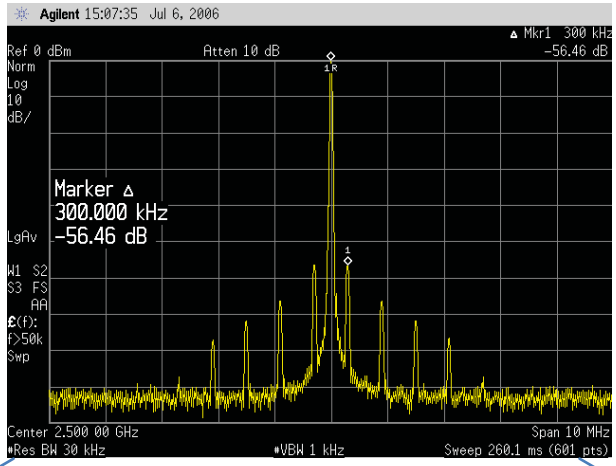
Real Oscillator : $vreal(t) = (v0 + \Delta v(t)) \sin(2\pi\, fct + \varphi(t))$







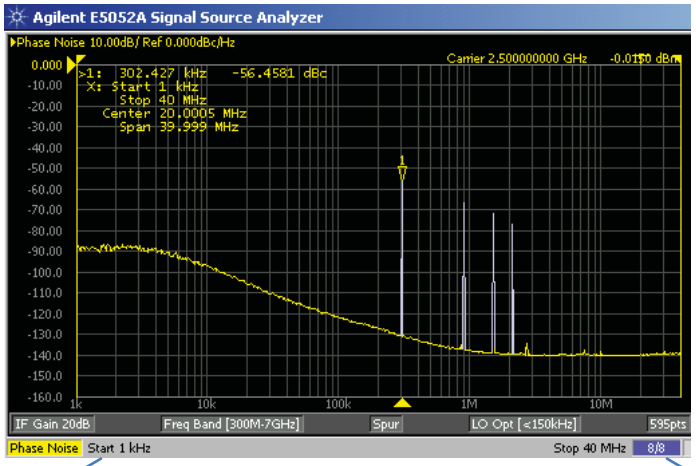
Spectrum=frequency spectral density



Frequency domain of the signal

$$S(f) = |F[vreal(t)]|^2$$
$$= |F[(v0 + \Delta v(t))\sin(2\pi ft + \varphi(t))]|^2$$

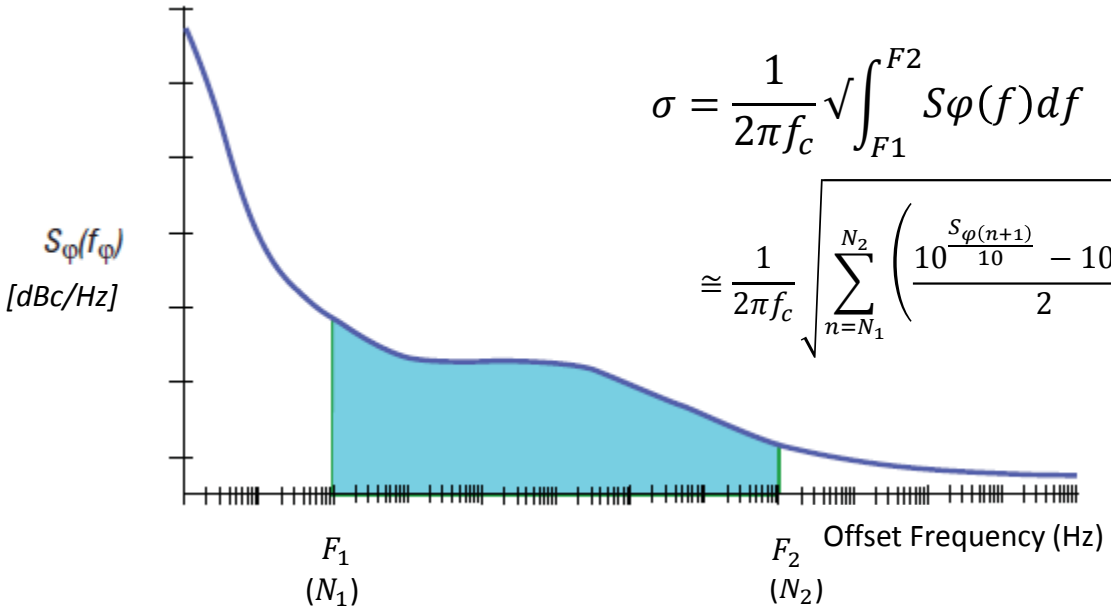
Phase Noise=phase spectral density



Frequency domain of the phase noise

$$S\varphi(f\varphi) = |F[\varphi(t)]|^2 = |\varphi(f\varphi \sim)|^2$$

- Time and Frequency Domain relationships
  - Getting RMS jitter out of phase noise plot (very close to TIE)



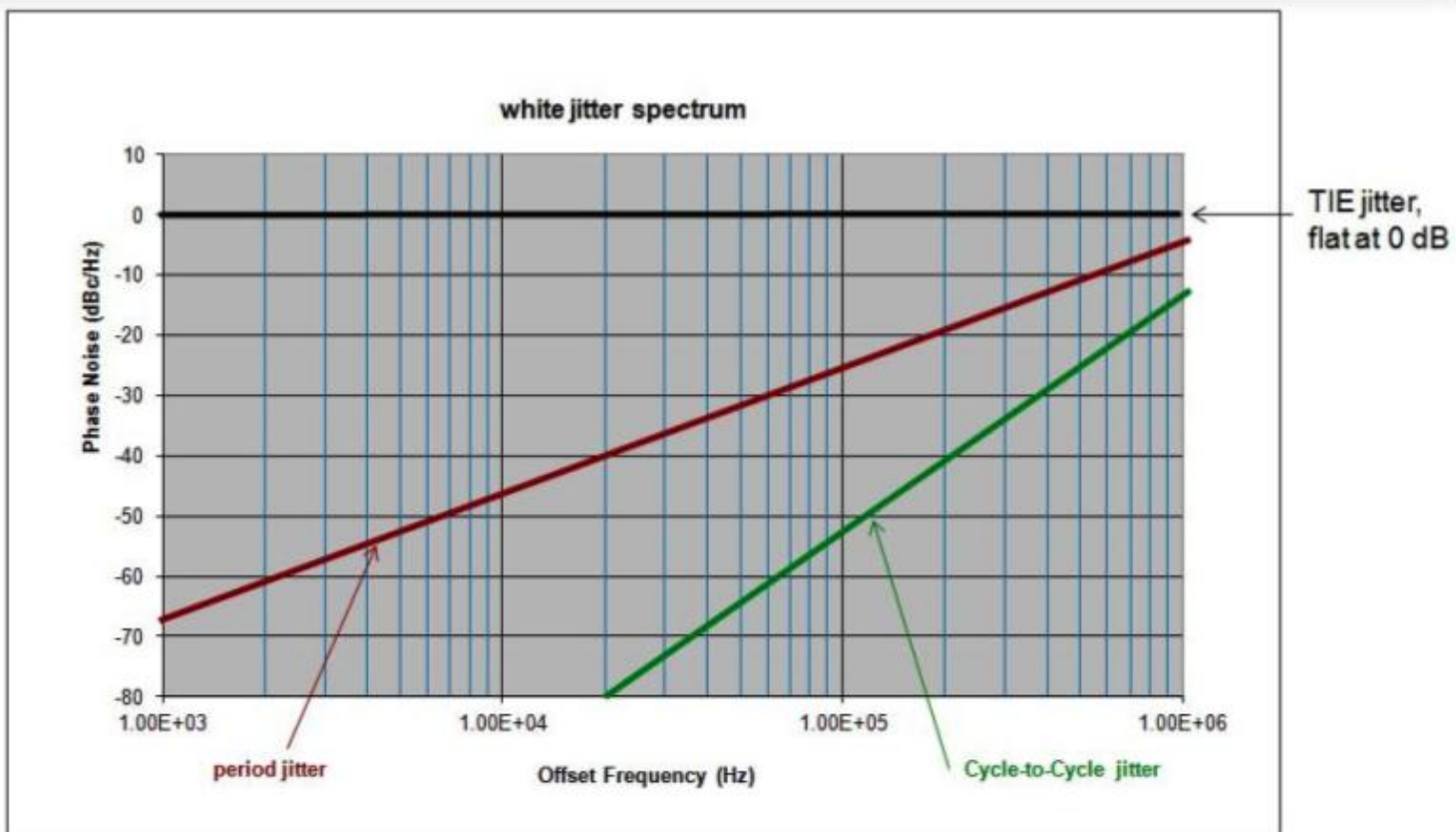
$$\sigma = \frac{1}{2\pi f_c}\sqrt{\int_{F1}^{F2} S\varphi(f)df}$$

$$\cong \frac{1}{2\pi f_c}\sqrt{\sum_{n=N_1}^{N_2}\left(\frac{10^{\frac{S_{\varphi(n+1)}}{10}} - 10^{\frac{S_{\varphi(n)}}{10}}}{2} * (f_{n+1} - f_n)\right)}$$

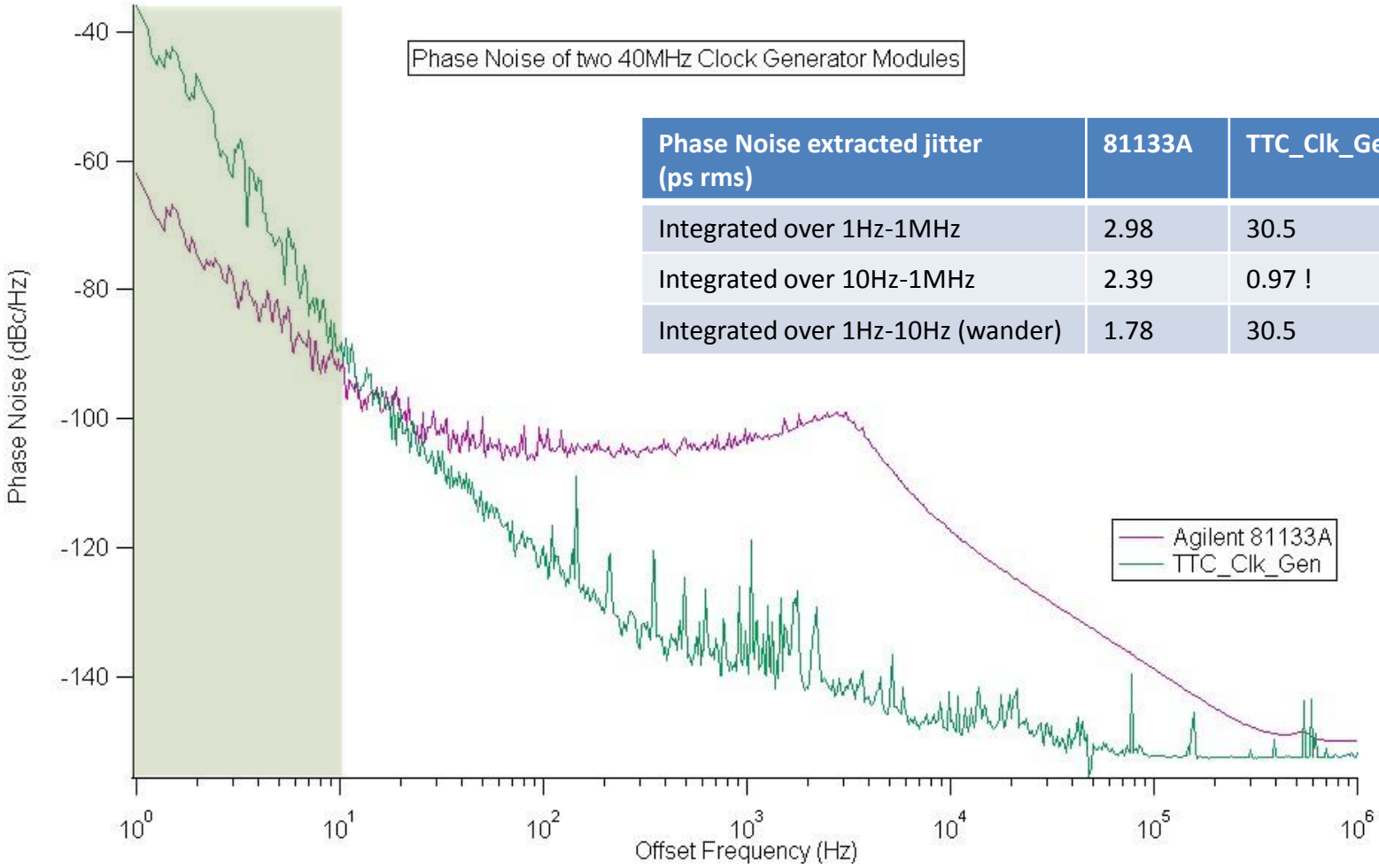
Phase Noise plot - discrete

Point	Offset freq (Hz)	Phase noise (dBc/Hz)
n	f_n	$S_{\varphi(n)}$
0	1	-61.99
1	1.018	-62.46
2	1.036	-62.93
..	..	..

- Cycle to Cycle, Period and TIE jitter in frequency domain



○ Wander: easy to visualize in frequency domain



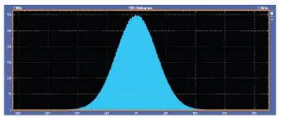
Phase Noise extracted jitter (ps rms)	81133A	TTC_Clk_Gen
Integrated over 1Hz-1MHz	2.98	30.5
Integrated over 10Hz-1MHz	2.39	0.97 !
Integrated over 1Hz-10Hz (wander)	1.78	30.5

JITTER

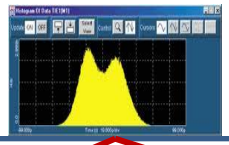
Gaussian and **unbounded** PDF, quantity is often « rms »

Usually periodic or narrowband, the PDF is bounded, quantity is often « pkpk »

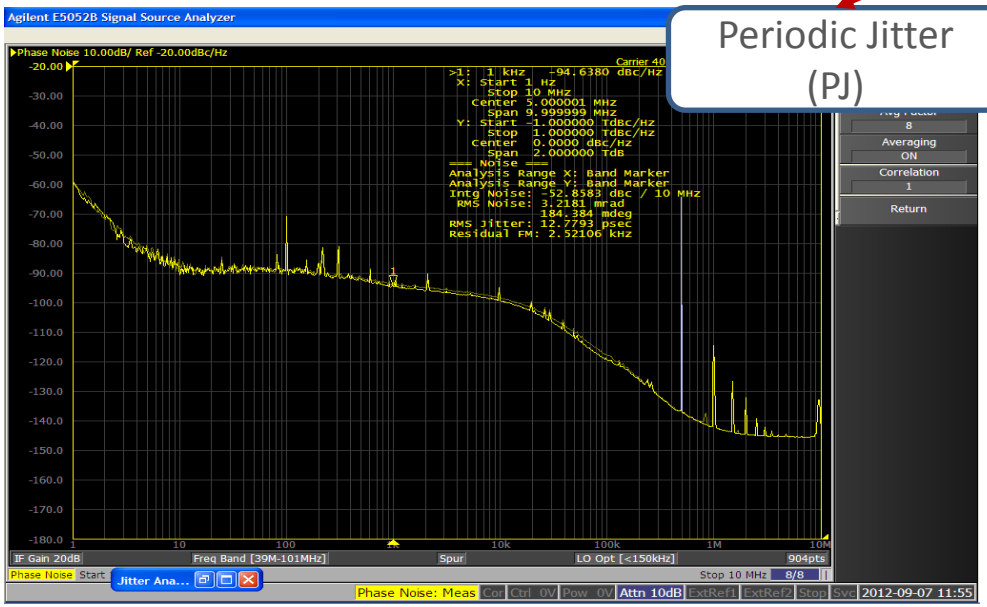
Random Jitter (RJ)



Deterministic Jitter (DJ)



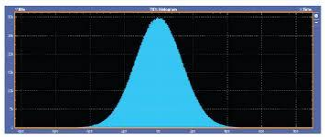
Periodic Jitter (PJ)



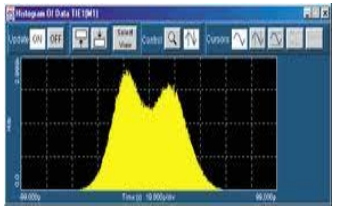
Data Dependent Jitter (DDJ)

Not discussed in this talk - Impossible to detect on a simple clock signal. (Only valid for clock recovery out of a serial data link. Only detected by time domain analysis)

- Random jitter sources
  - Caused by accumulation of a huge number of uncorrelated processes that have small magnitude
  - Random noise phenomena
    - Thermal noise, Shot noise, Pink noise, etc…
    - Occur in all semiconductors and components (PLLs, Oscillators, Tx, Rx etc…)
  - Typical representation of induced jitter: Gaussian & unbounded PDF
  - Quantified by the Standard Deviation (rms)



- Deterministic jitter sources
  - Caused by a comparatively small number of processes that can be correlated and may have large amplitudes,
  - System & Data Dependent phenomena
    - Crosstalk, dispersion, impedance mismatch
    - Inter Symbol Interference (ISI), Duty-Cycle Distortion (DCD), Bit sequence periodicity
  - Typically detected as deviation of the PDF from Gaussian shape
  - Quantified by the pkpk value, as they induce a bounded phase deviation



Vocabulary: Jitter & Co

Who is sensitive to what?

A good clock in 2 words

WHAT IS A GOOD BUNCH CLOCK SIGNAL?

- Digital Systems:
  - Very sensitive to setup and hold time
  - ⇒ basically related to PKPK CY2CY AND PERIOD JITTER.

- PLLs:
  - Track the slow variations of the clocks, and filter out the high frequency components.
  - Can not deal with sudden jumps which may unlock them.
  - ⇒ PKPK CY2CY JITTER
  - ⇒ WANDER can also be a problem when it means frequency drifting out of the locking range.

- ADCs:
  - Very sensitive to timing errors as jitter is directly converted into amplitude sampling errors, and SNR.
  - Unregularly sampling edges can distort of the shape of digitized pulses.
  - ⇒ This is thus more about PKPK CY2CY AND PERIOD JITTER than about TIE.

- Serial Data Links:
  - Need to combine low Bit Error Rate (BER) and good Clock Recovery
    - BER is related to the quality of the clock
      - Transmitter is very sensitive to ANY CLOCK JITTER (because of clock multiplication).
      - On the channel, data jitter is correlated to DUTY CYCLE DISTORTION of the clock (DCD)
      - Receiver and CDR are highly sensitive to HIGH FREQUENCY JITTER
    - Quality of the Clock Recovery is a trade off between low BER (requires high bandwidth PLL) and noise rejection (requires narrow bandwidth PLL)
    - Serial Data Links understanding requires TIE decomposition and often frequency domain analysis

- Detectors - Event reconstruction over a huge system

  - 1000s of Bunch Clock destinations spread all over the detectors
    - Low SKEW JITTER between all clock signals (from every branches of the distribution tree) to guaranty channel-to-channel consistency

  - Stable phase between Bunch Clock and Beam
    - Low SKEW JITTER between Bunch Clock and Bunches over a fill
    - limited WANDER during broadcast, in particular on long-haul transmission (between point4 and experiments)
    - Deterministic Static Phase between branches and top of the clock tree from fill to fill and between power cycles

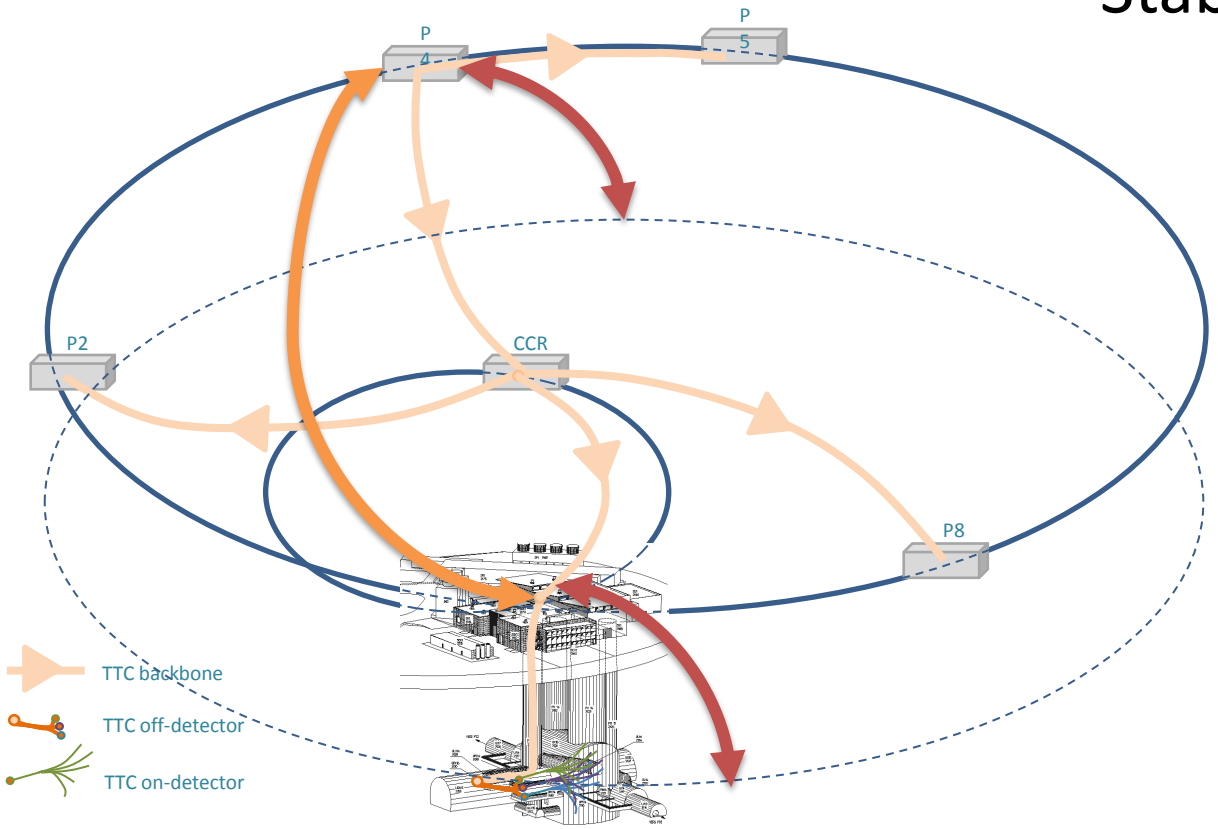
Vocabulary: Jitter & Co

Who is sensitive to what?

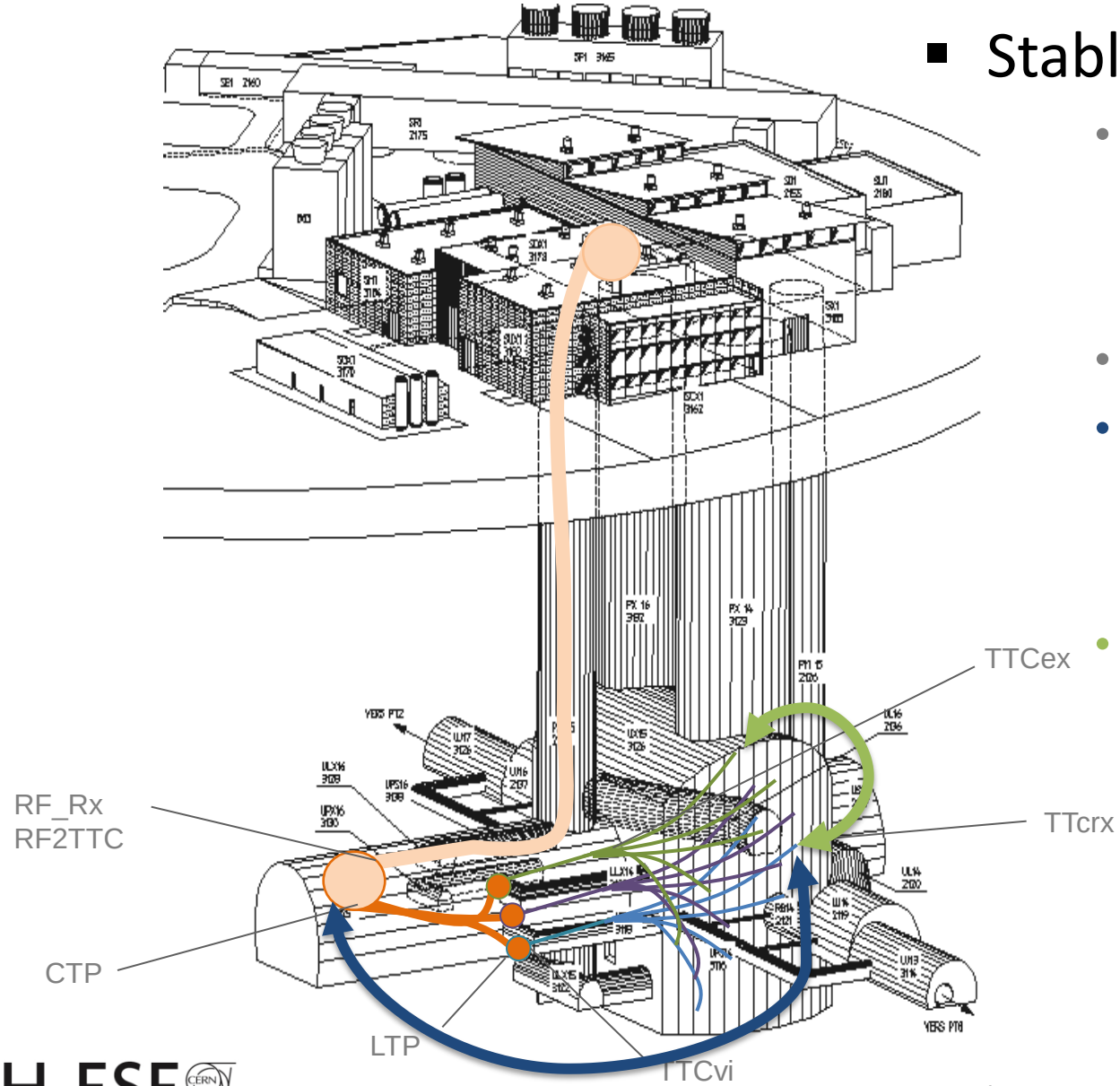
A good clock in 2 words

WHAT IS A GOOD BUNCH CLOCK SIGNAL?

- **Detector** cares about **Stable Phase** (slow variations or skew jitter versus reference)
- **Sub-systems** care about **Low Jitter** (of Bunch Clock as such)



- Stable Phase
  - Beam Jitter:
    - Beam vs RF
    - Beam at experiments versus BC
  - Temperature drift



- Stable Phase
  - Beam Jitter:
    - Beam vs RF
    - Beam at experiments versus BC
  - Temperature drift
  - Determinism
    - BC at Front End Boards versus BC at Central Trigger
  - Channel skew jitter
    - BC at Front End Board X versus BC at Front End Board Y (channel to channel skew jitter)

- Low Jitter
  - Cycle to cycle jitter
  - Period jitter
  - Overall jitter
    - Time Interval Error jitter
    - Phase Noise jitter

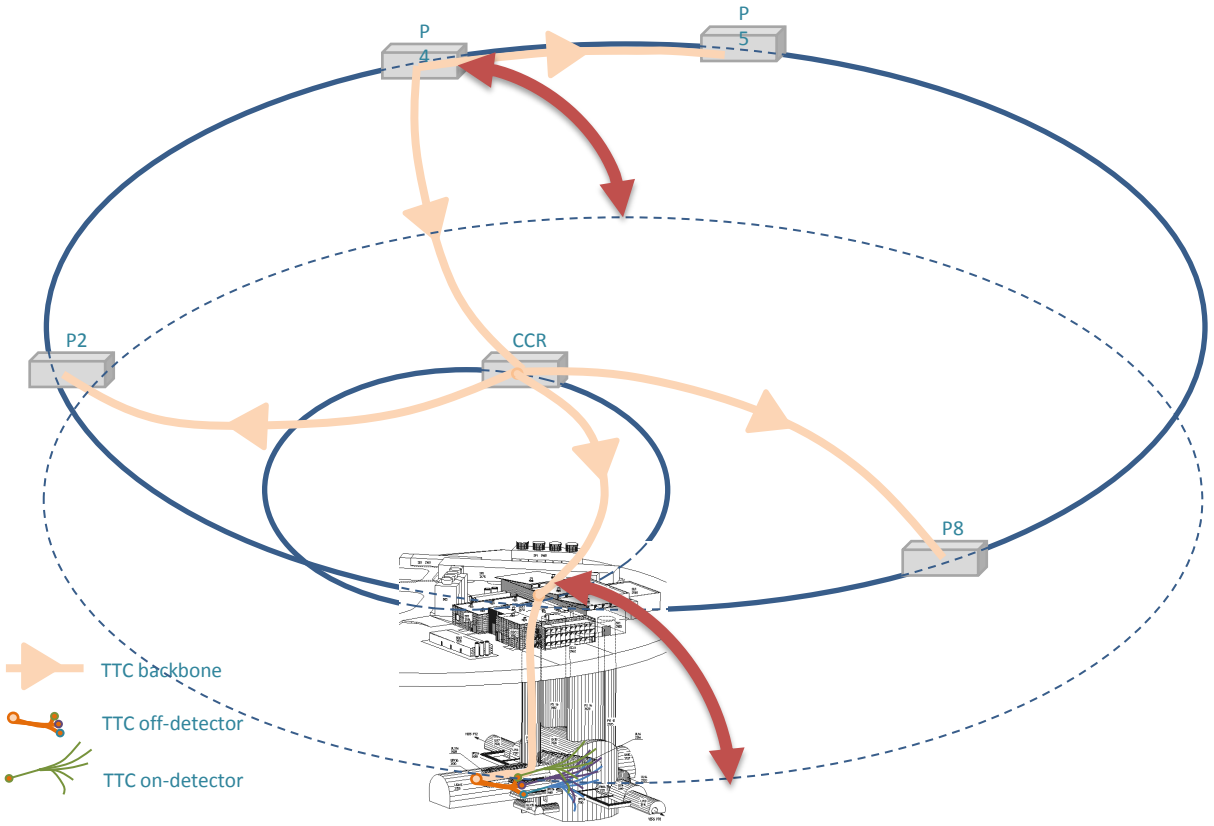
Phase

- Beam Jitter
- Temperature Drift
- Determinism
- Channel Skew Jitter

Jitter

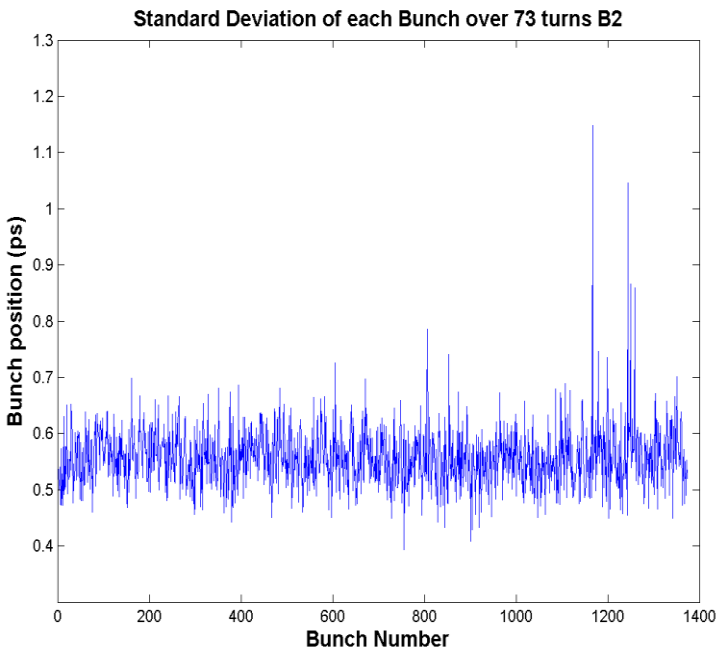
- Frequency Domain Analysis
- Time Domain Analysis
- Using Jitter Information

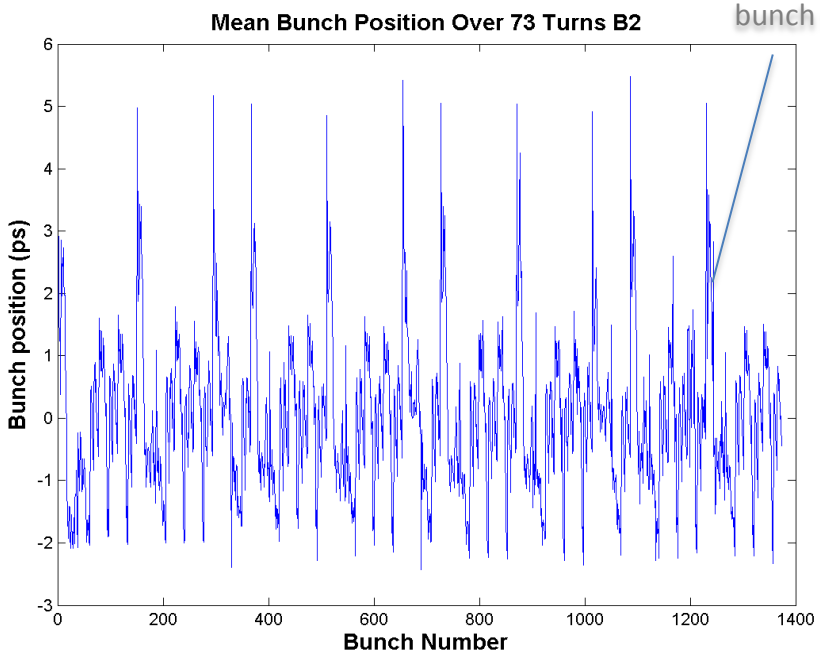
MEASURING THE CLOCK QUALITY


P
4
P
5
P2
CCR
P8
TTC backbone
TTC off-detector
TTC on-detector

- Beam jitter versus RF
  - phase variations of the beam with respect to its reference (400MHz RF)
  - Maintained and monitored by the RF low level loops
  - 1374 bunches
  - Bunch position pkpk<5ps, rms<1.3ps

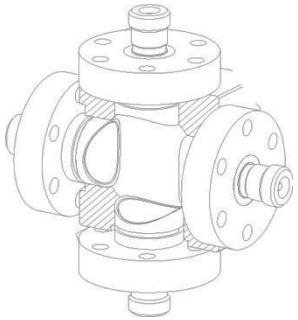
Beam loading effect reflecting the bunch structure





Beam jitter versus experiment Bunch Clock

BPTX systems

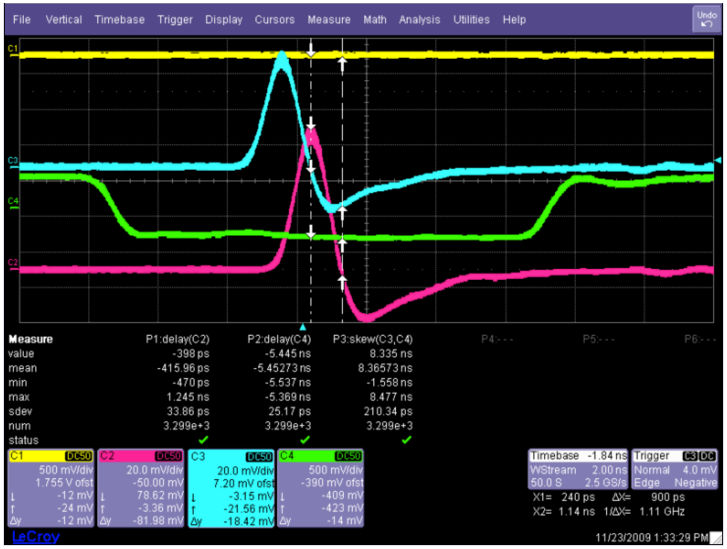


Use four screwed Electrostatic Button Electrodes to obtain Horizontal and Vertical position

<50ps resolution by averaging

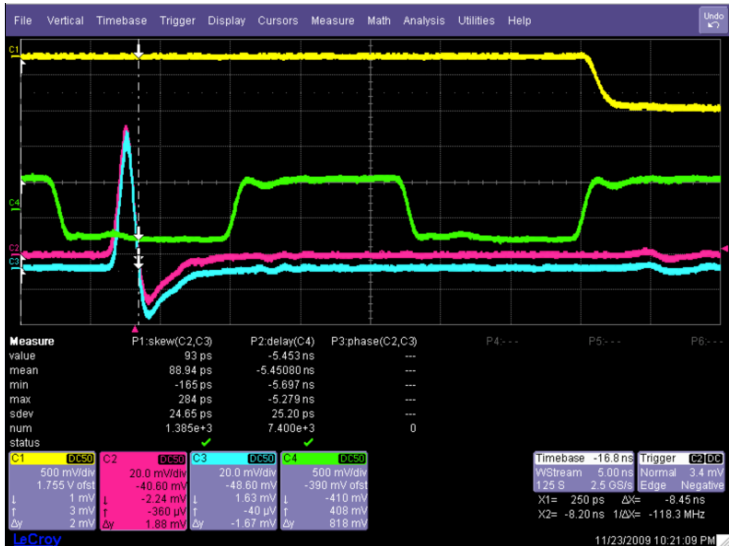
First phase adjustment just before first collisions, ATLAS, nov 2009:

Phase between 2 BPTX at ATLAS after cogging with 2 beams (900ps)



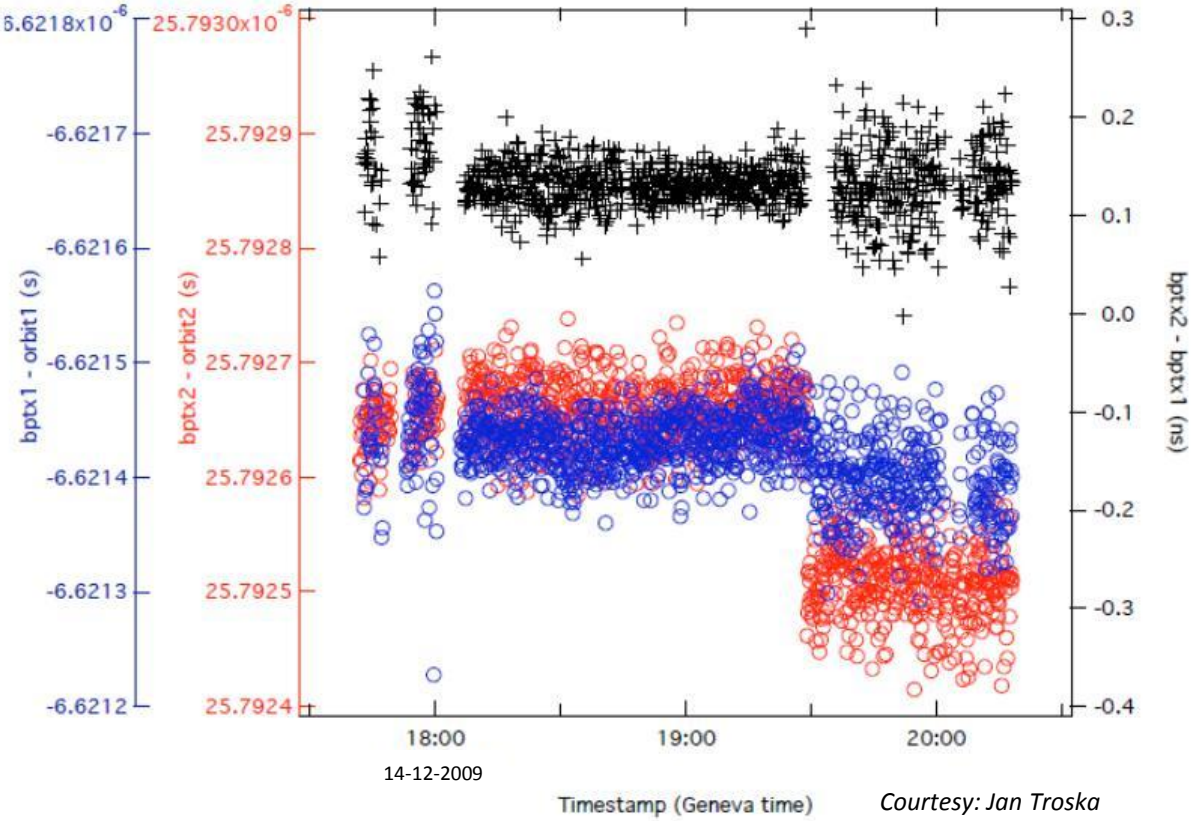
Courtesy: Thilo Pauly

Phase between 2 BPTX at ATLAS after fine phase with 2 beams just before collisions (90ps)

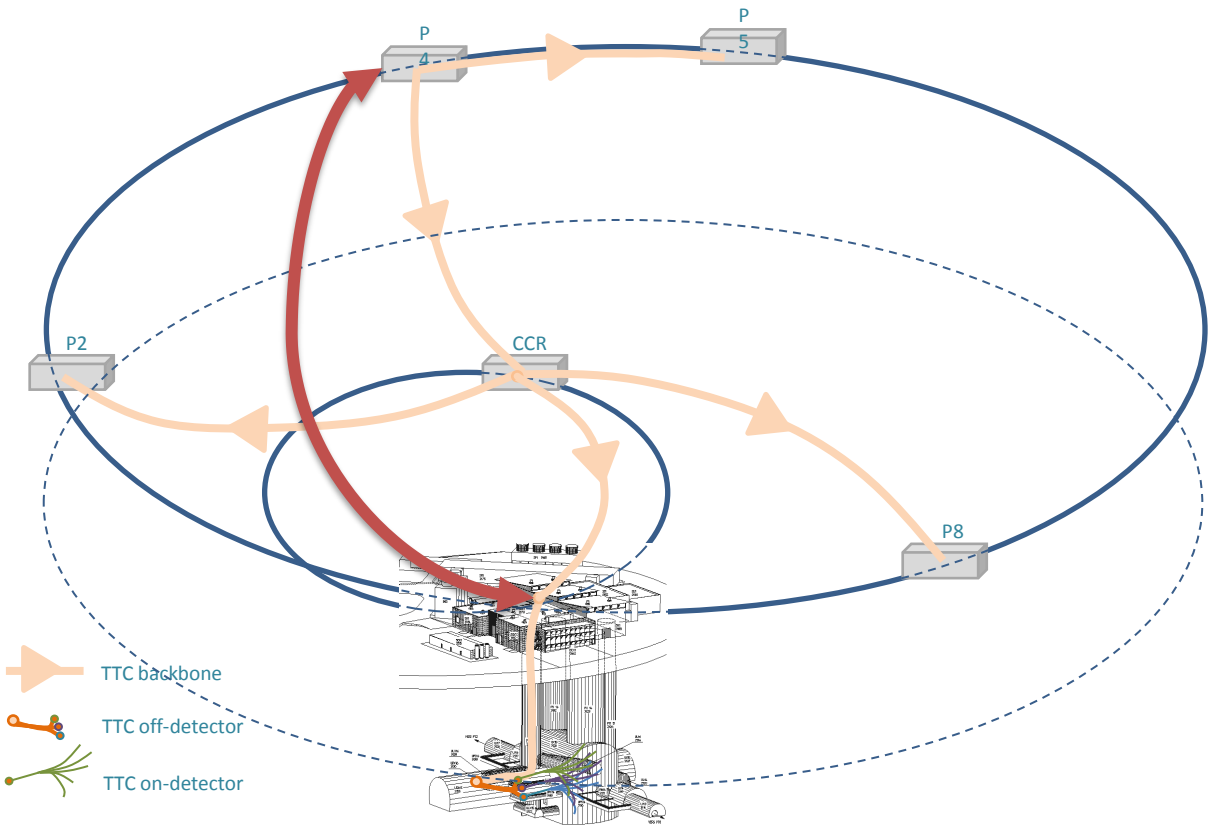


Courtesy: Thilo Pauly

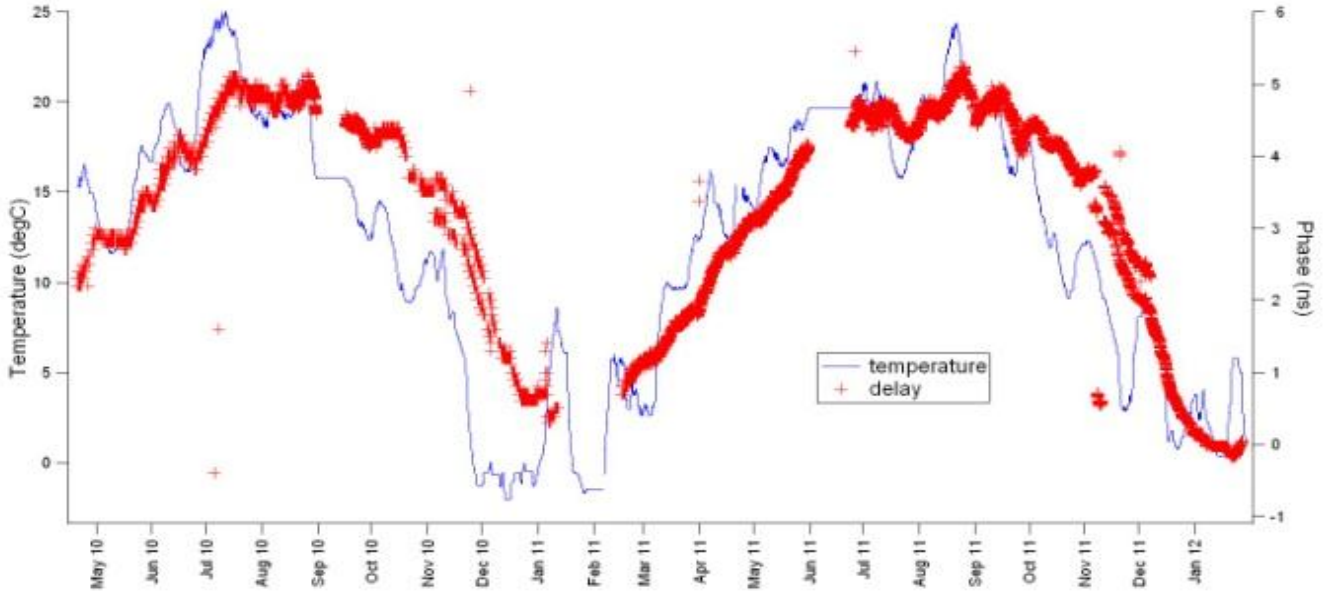
○ Analysis of BPTX data (example of CMS)

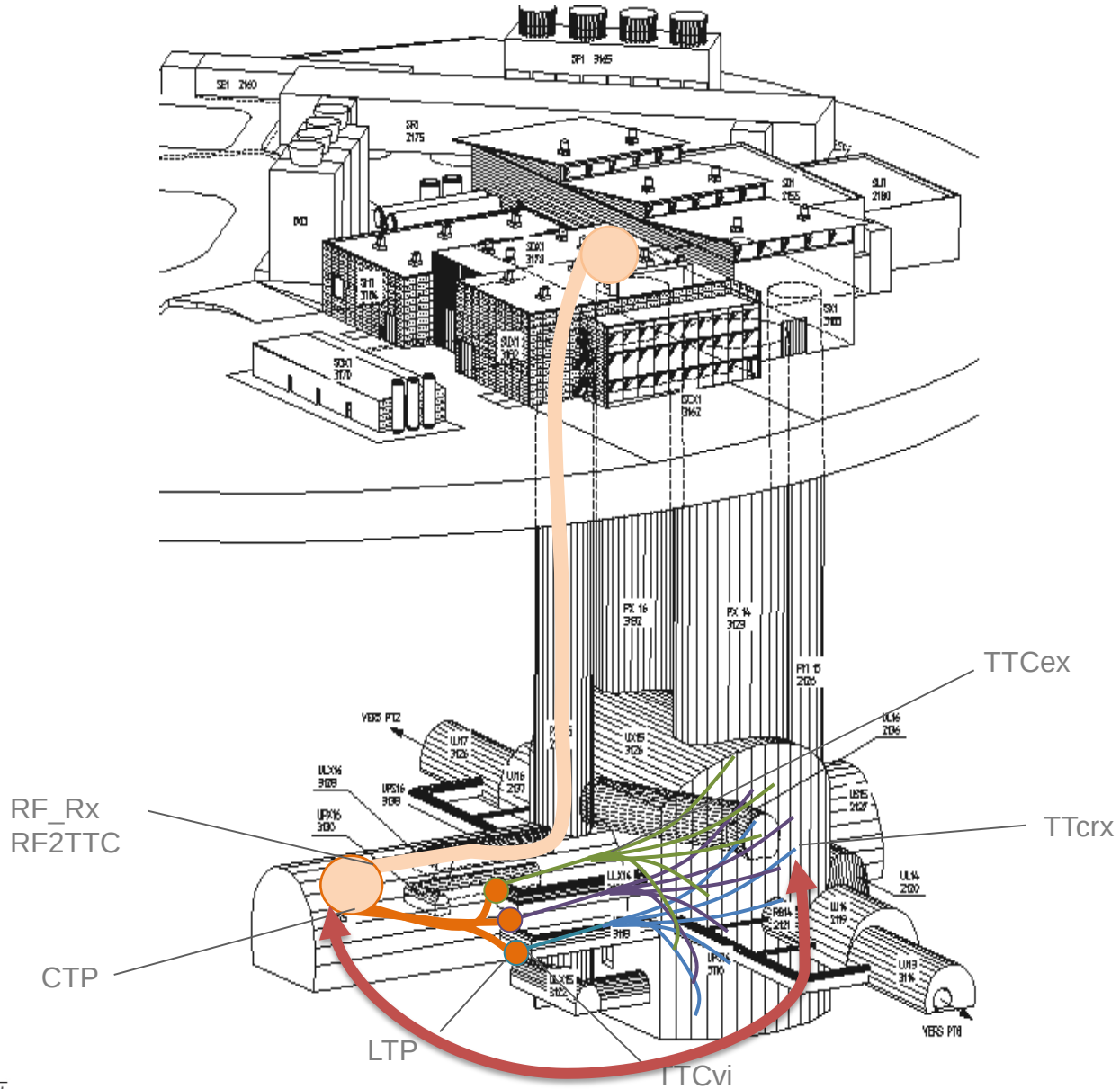


Courtesy: Jan Troska

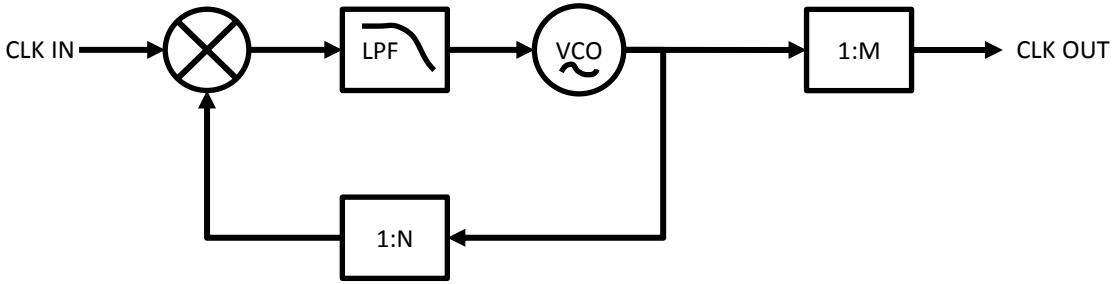

P
4
P
5
P2
CCR
P8
TTC backbone
TTC off-detector
TTC on-detector

- Up to 14km of burried fiber from SR4 to ALICE, ATLAS, LHCb (1m deep)
- The fibre length changes with temperature by 7ppm/degC
- Measurements on a spare fiber from CCC to ATLAS and back (9km)
  - 8ns seasonal drift for 14km
  - VERY slow variation of the phase between beam and clock (wander)
  - Need for regular calibration (usually before each run) with the help of BPTX and of the CORDE module for example
  - Keep in mind that : the diurnal variation can be 150 ps = expect drift during fills

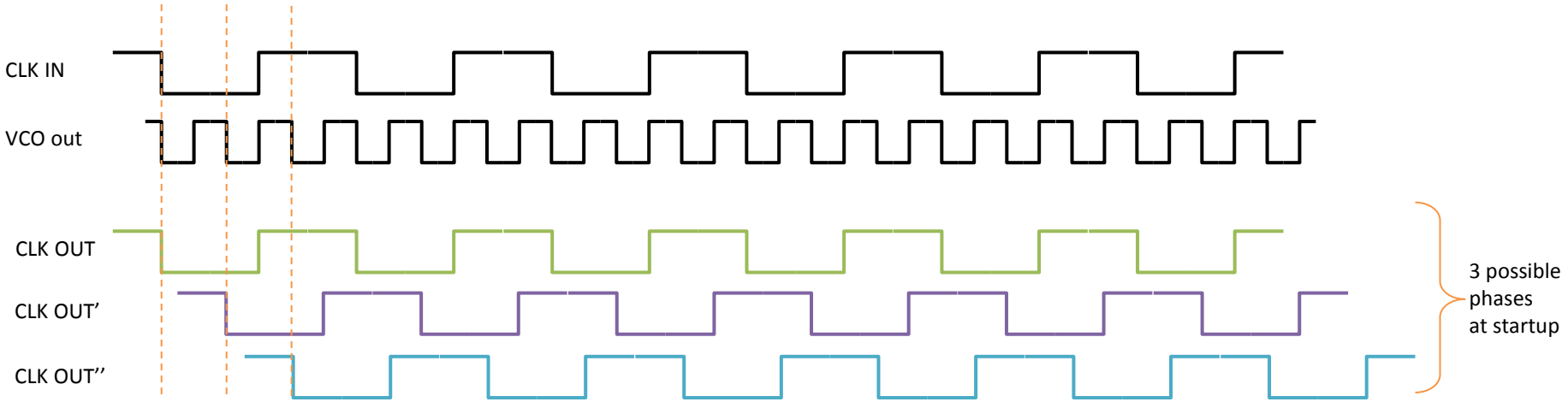



TTCex
TTCrx
RF_Rx
RF2TTC
CTP
LTP
TTCvi

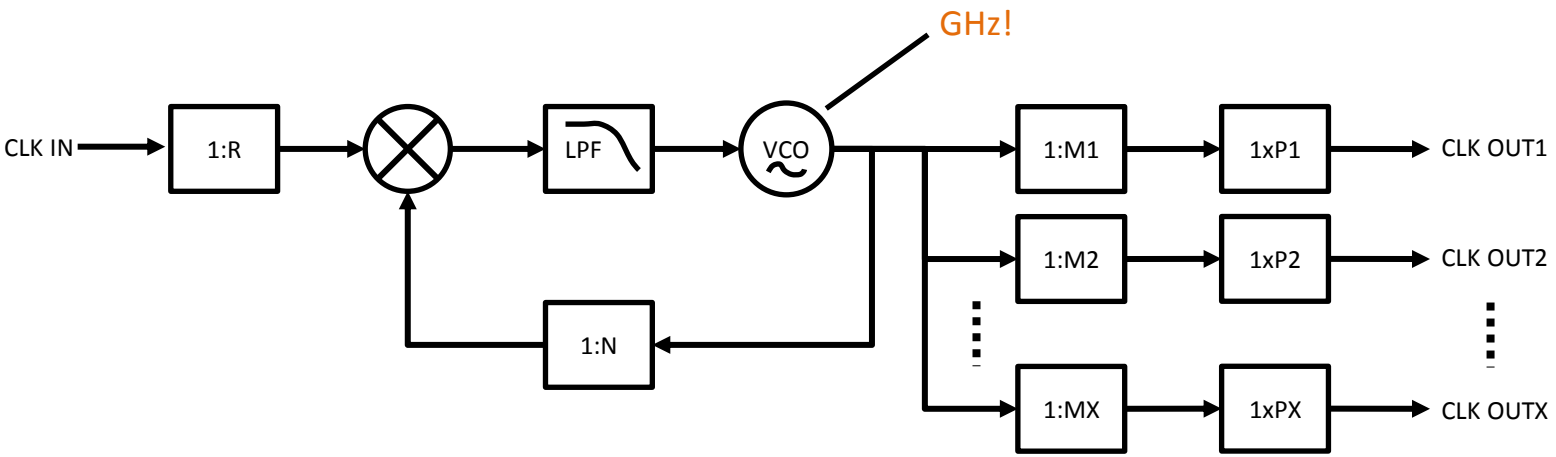
- Determinism
  - Typical issue with commercial PLLs



Example: N=M=3

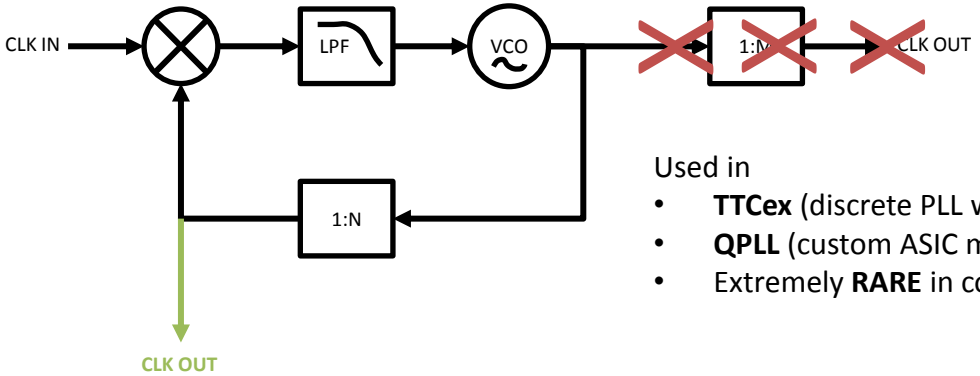


Commercial PLL usual design



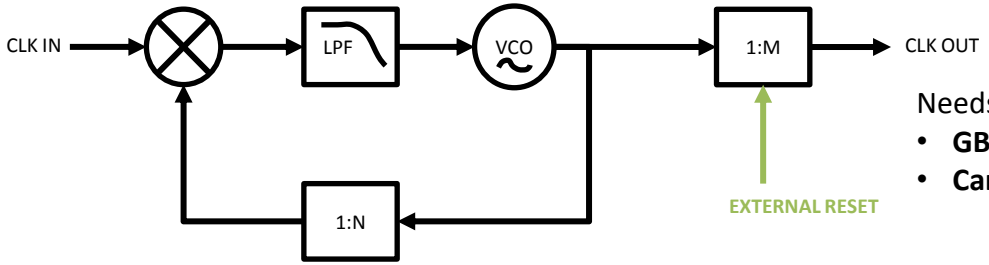
○ Solving phase determinism issues

Solution 1:



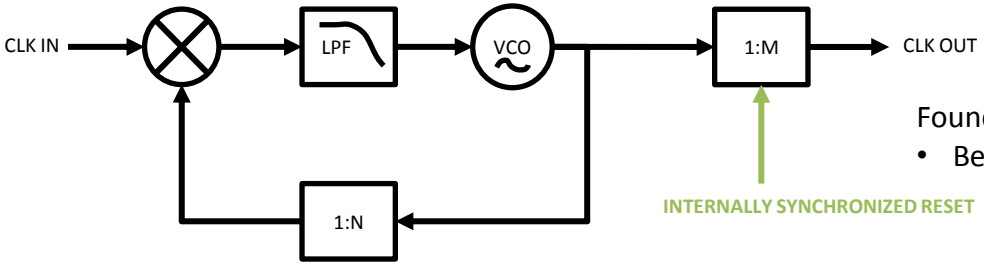
Used in
- **TTCex** (discrete PLL with 160MHz VCO)
- **QPLL** (custom ASIC made at CERN)
- Extremely **RARE** in commercial PLL (no commercial interest)

Solution 2:



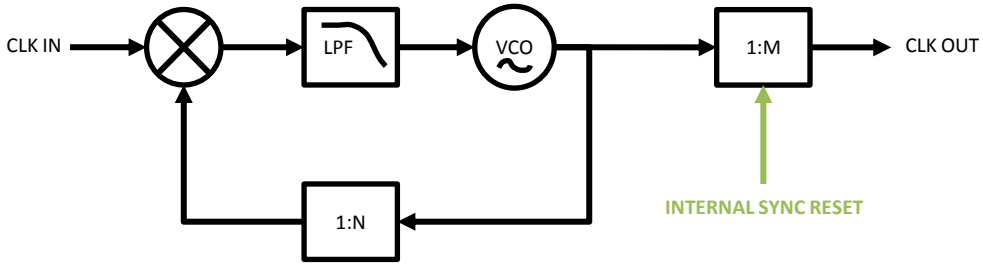
Needs external phase **monitoring**
- **GBT implements this option**
- **Can be provided by FPGA in counting rooms**

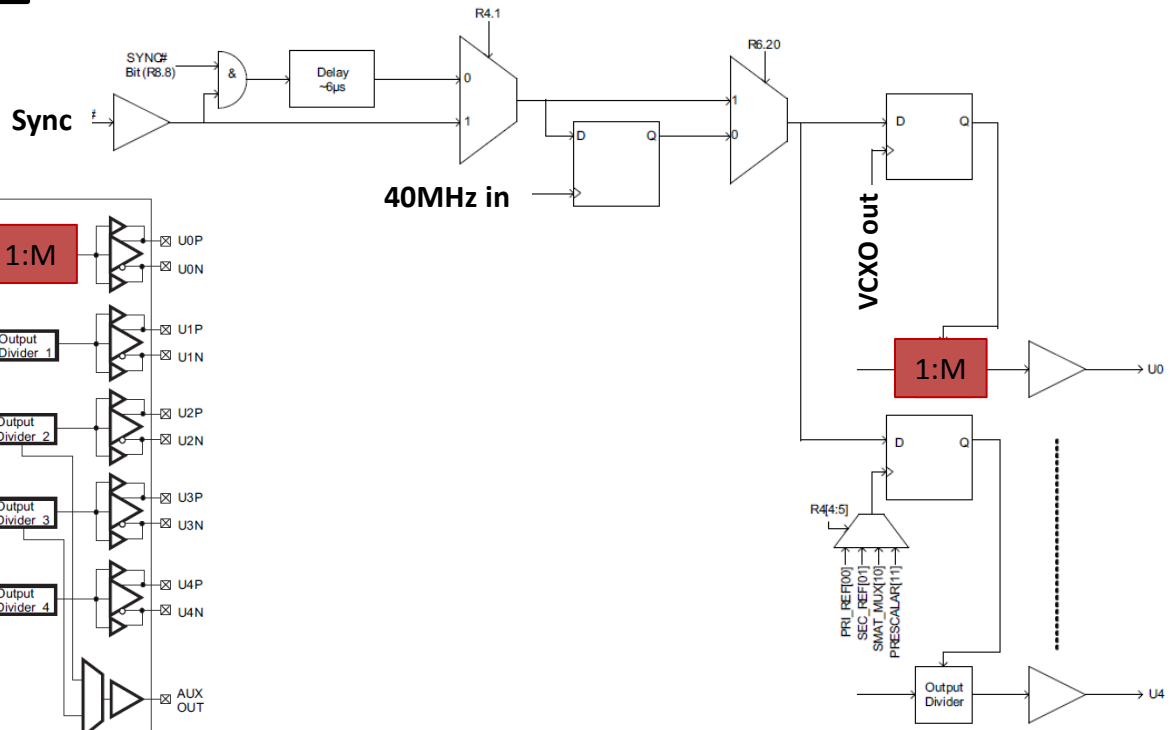
Solution 3:



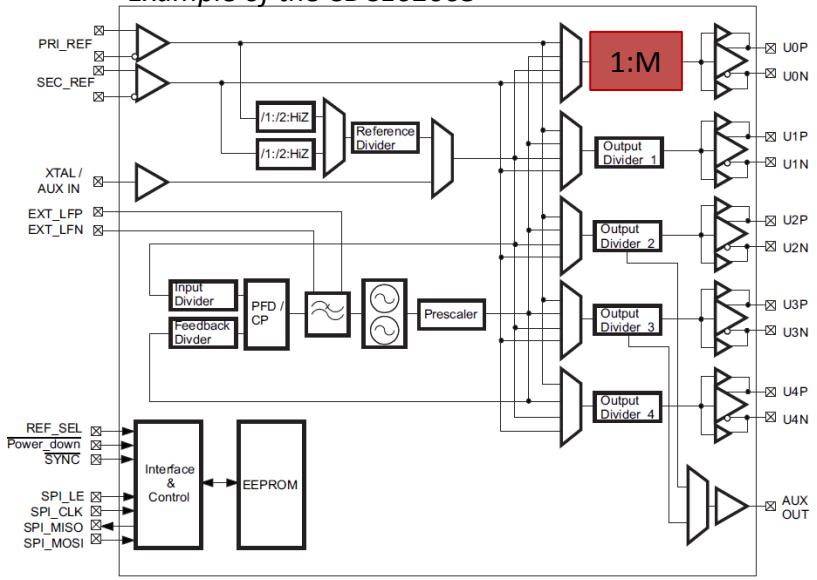
Found in some Commercial PLLs
- Beware of **METASTABILITY**

○ Solution 3: Metastability issues



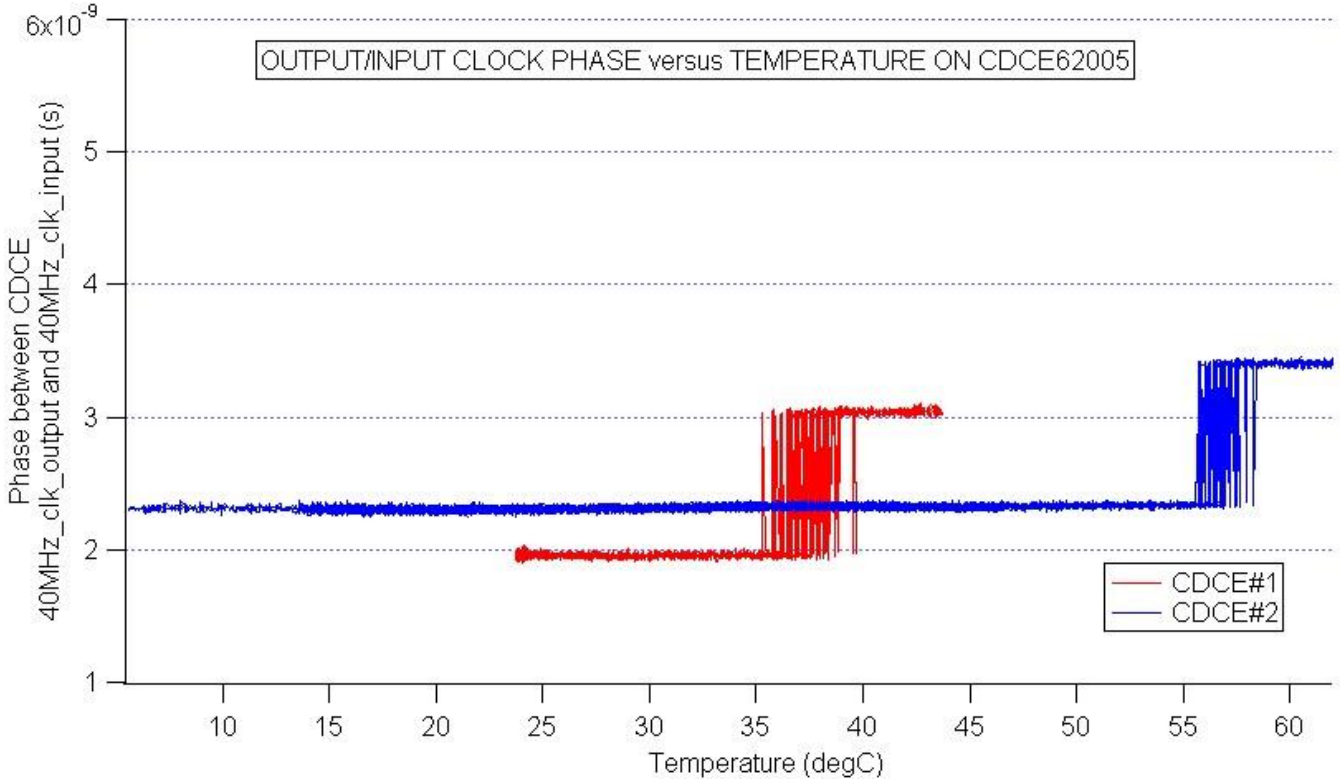


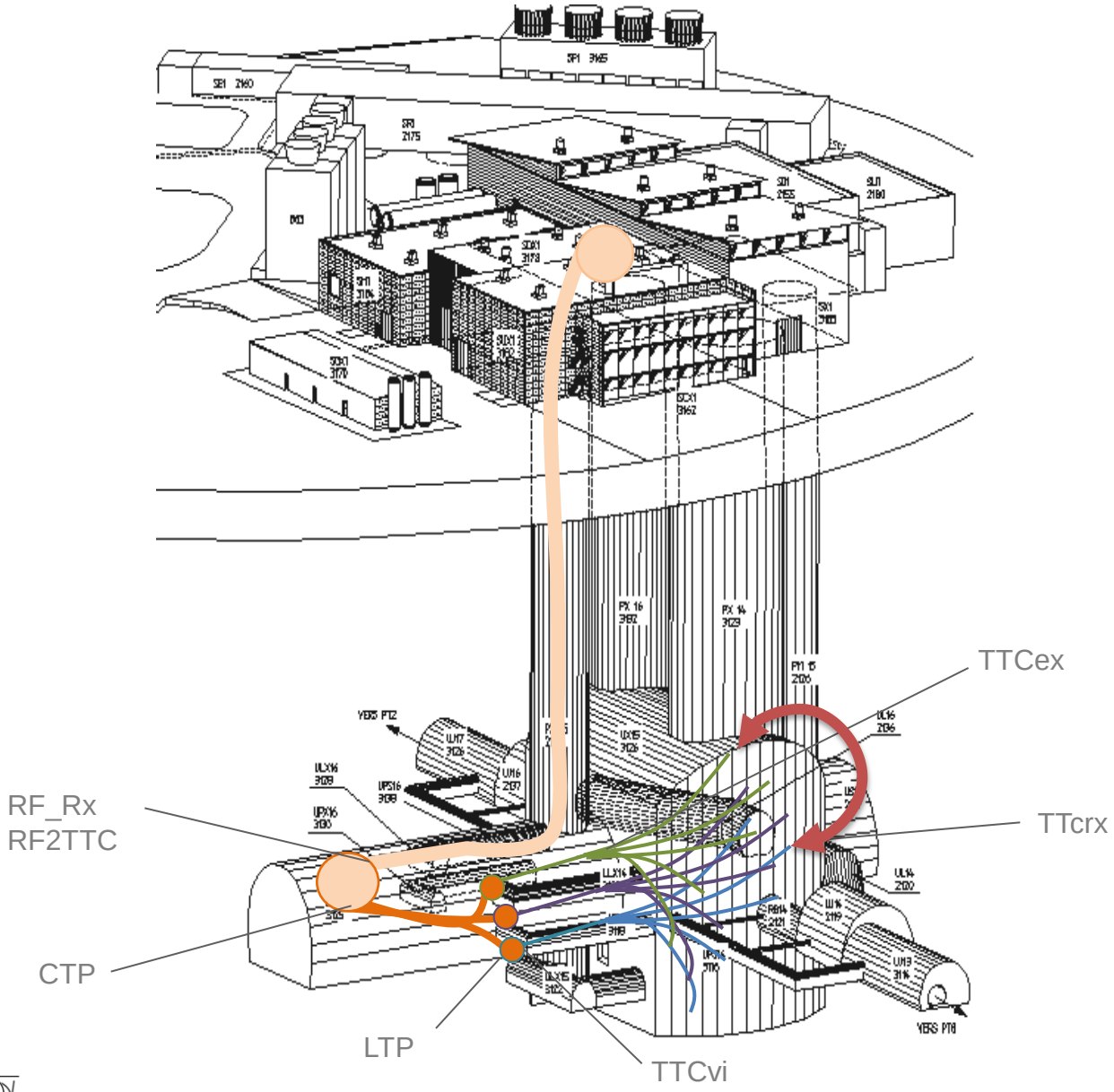
Example of the CDCE62005



Solution 3: Metastability issues

- Tests in climatic chamber




TTCex
TTcrx
RF_Rx
RF2TTC
CTP
LTP
TTCvi

- Channel-to-channel skew
  - For a good event reconstruction
  - Time Of Flight (TOF) detectors
    - need less than 10ps rms between channels for particle mass identification
  - Reducing it: Trade off for the PLLs in the clock tree
    - Narrow bandwidth to clean the clock as much as possible
    - Wide bandwidth to be sure PLLs do not drift too much from each other

TO SUMMARIZE …

- Beam jitter vs RF - very low < 1.5 ps rms
- Beware of
  - Temperature drift
  - Phase determinism
  - Channel to channel skew jitter
- But keep in mind that
  - The size of the luminous region (z) ~ 50mm – about 160ps
- All the detectors have the same type of requirements in term of phase and skew jitter

Phase

- Beam Jitter
- Temperature Drift
- Determinism
- Channel Skew Jitter

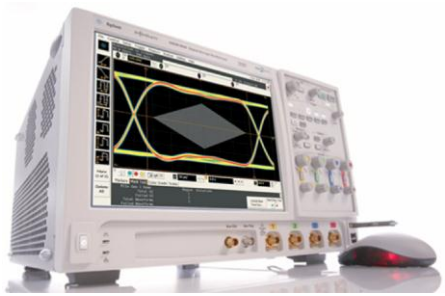
Jitter

- Frequency Domain Analysis
- Time Domain Analysis
- Using Jitter Information

MEASURING THE CLOCK QUALITY

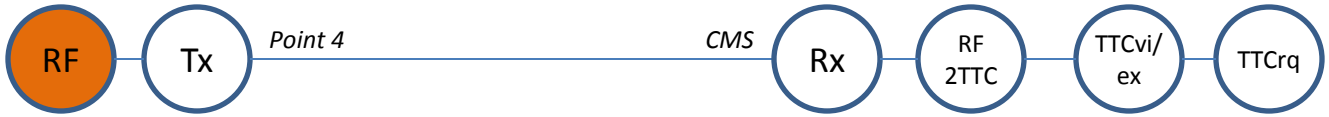
- Frequency Domain:
  - Phase Noise
  - using Agilent SSA E5052B
    - Only since 2012

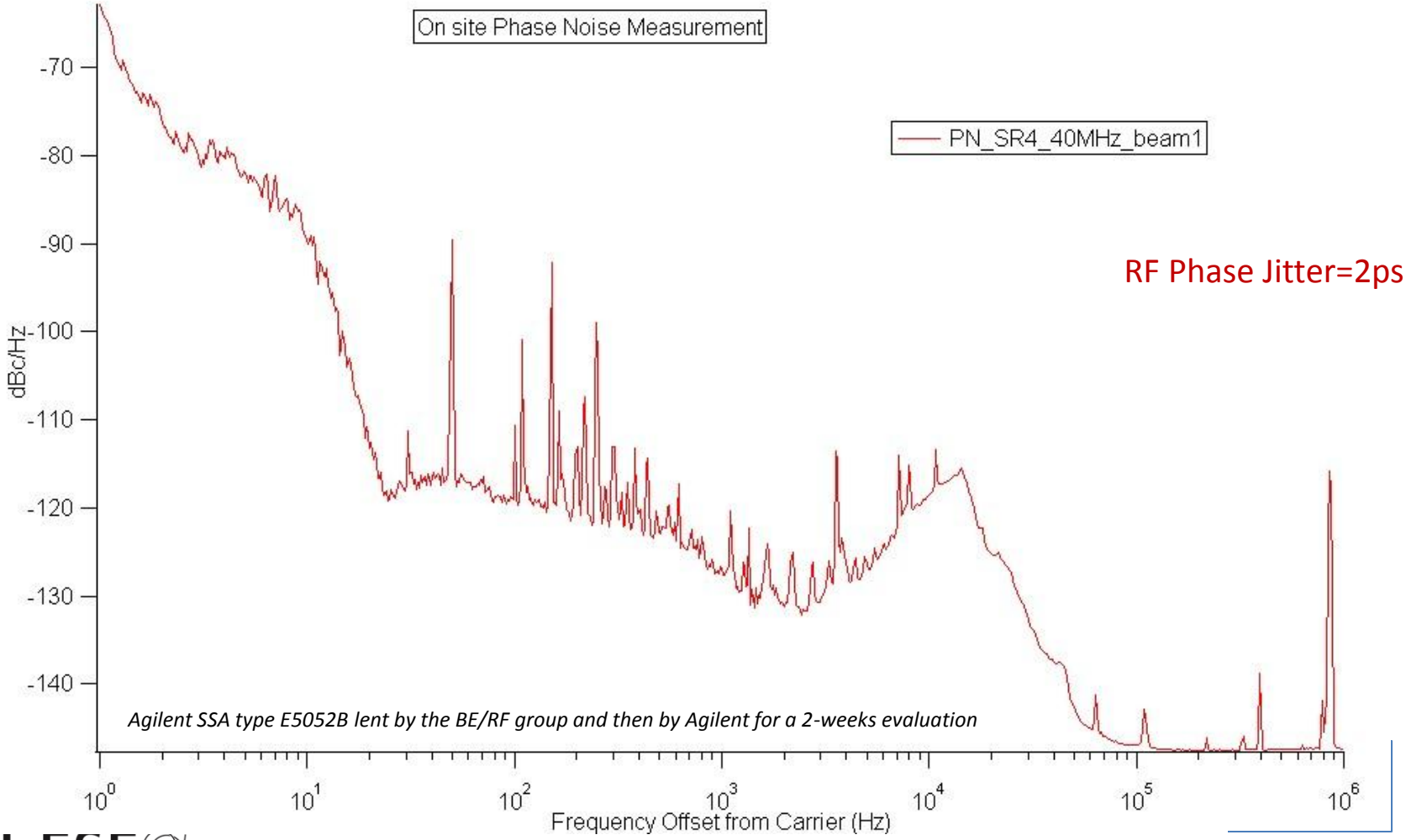
- Time domain:
  - Cy2cy
  - Period
  - TIE (Phase Jitter)
  - Using
    - Lecroy before 2011
    - Agilent since 2012



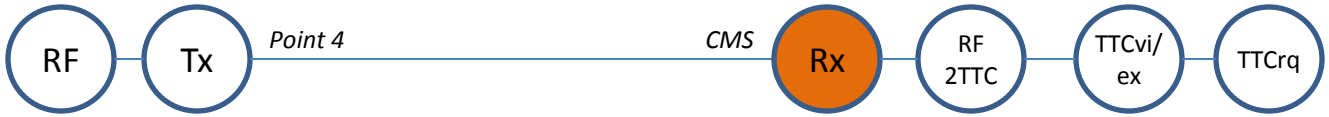
Agilent infiniium DSA91204A, 12GHz, 40GSa/s

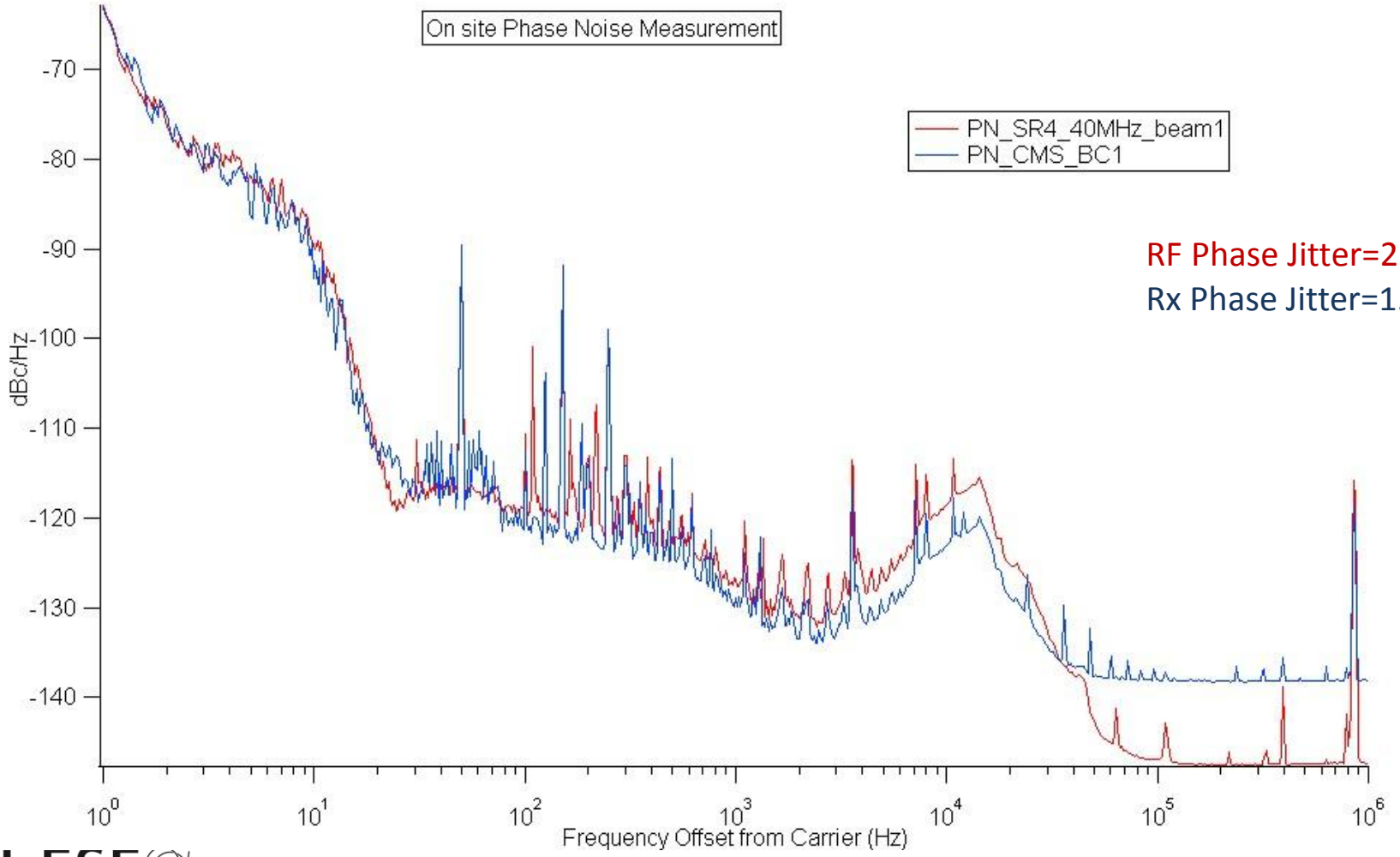
Lecroy Wavepro 7100, 1GHz, 10GSa/s





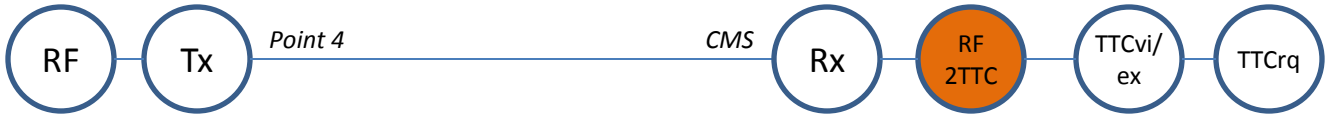
RF Phase Jitter=2ps rms

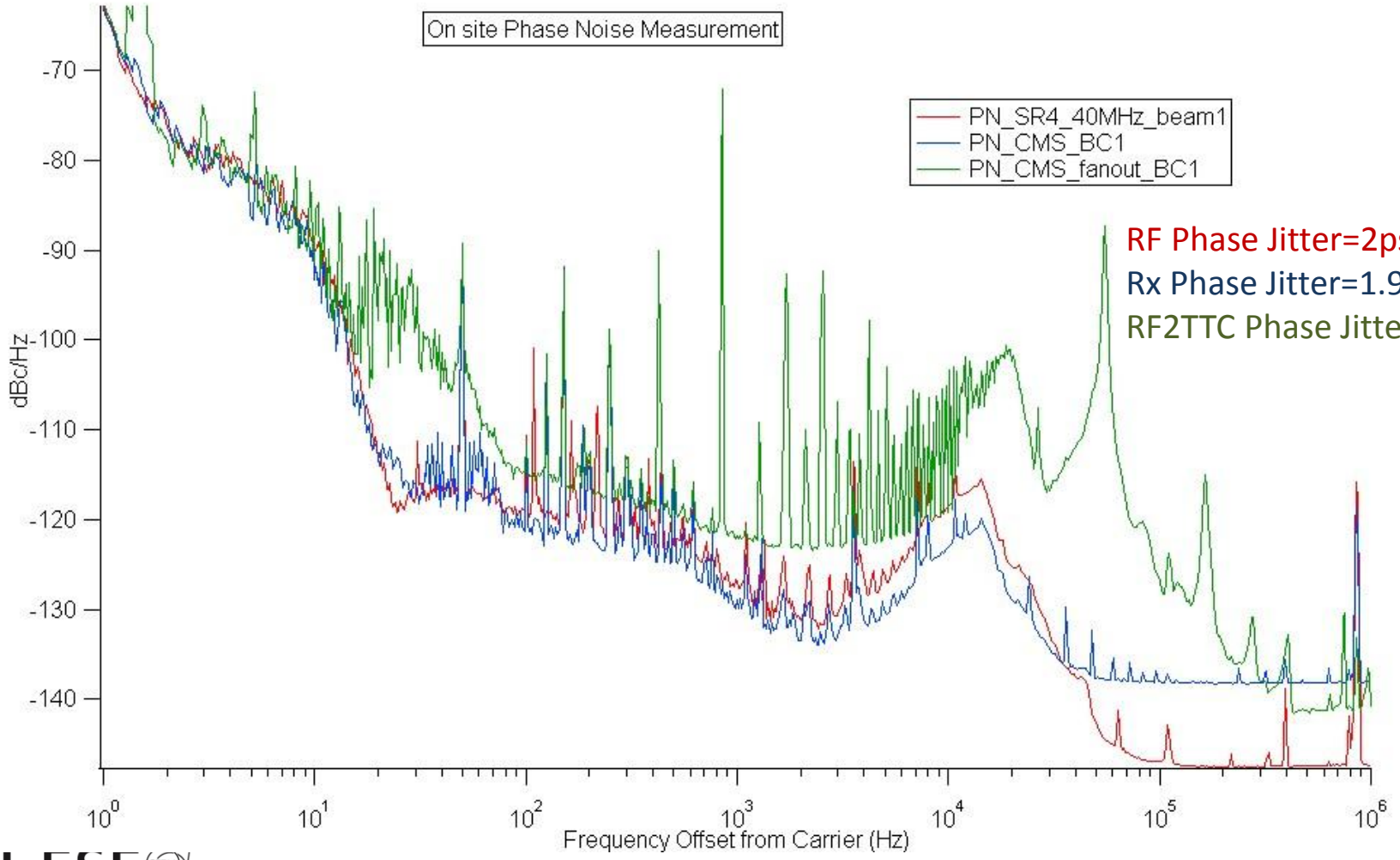




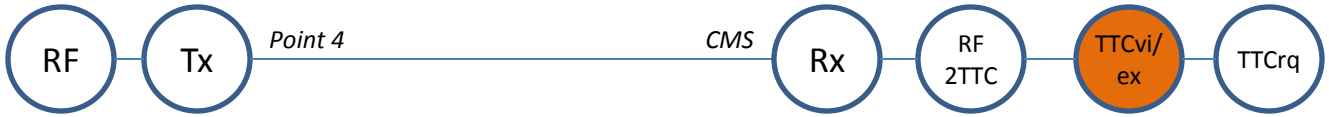
RF Phase Jitter=2ps rms

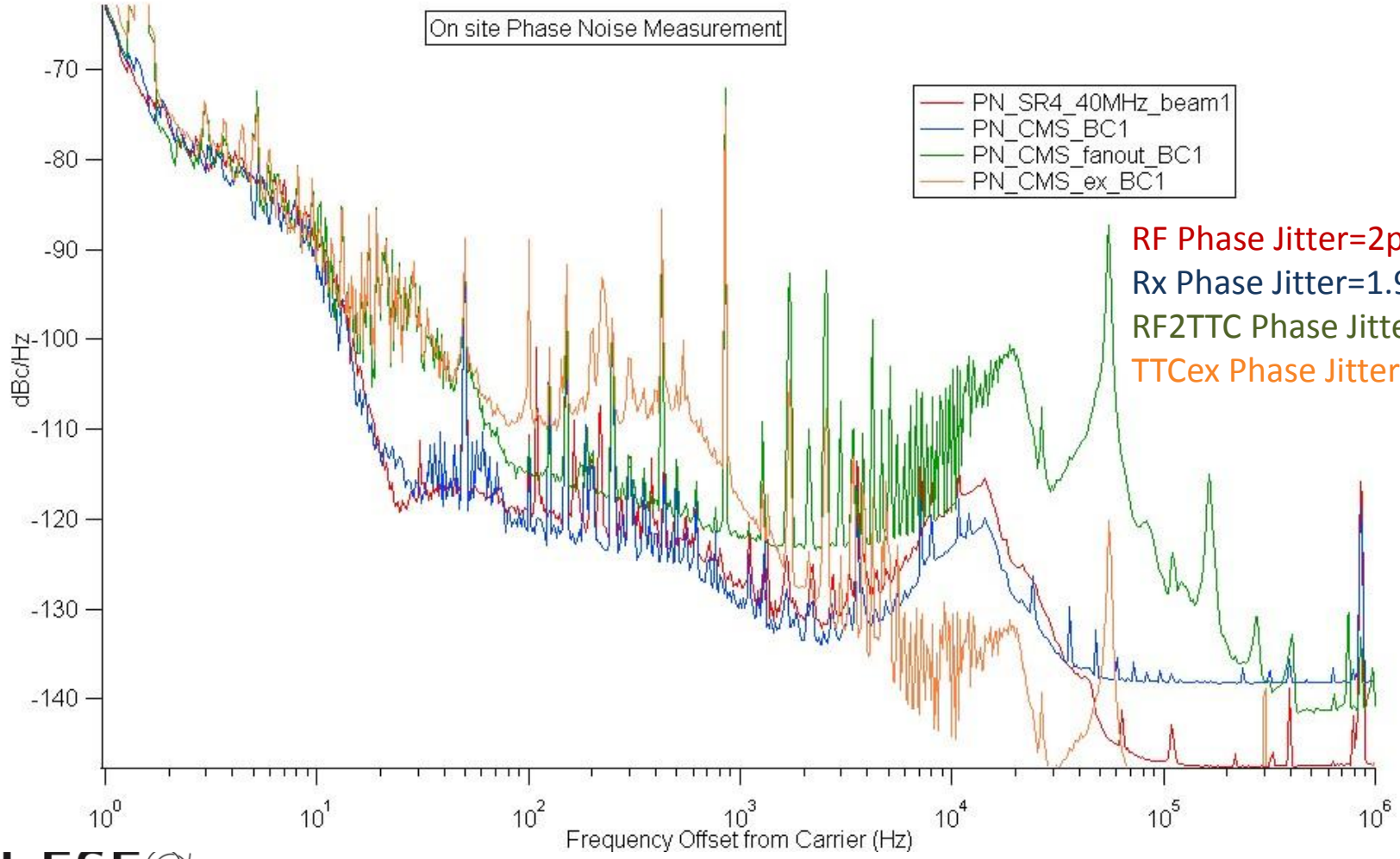
Rx Phase Jitter=1.9ps rms



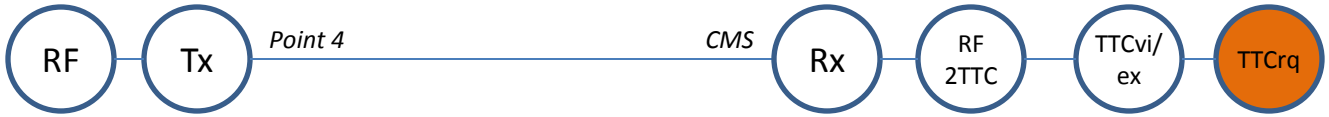


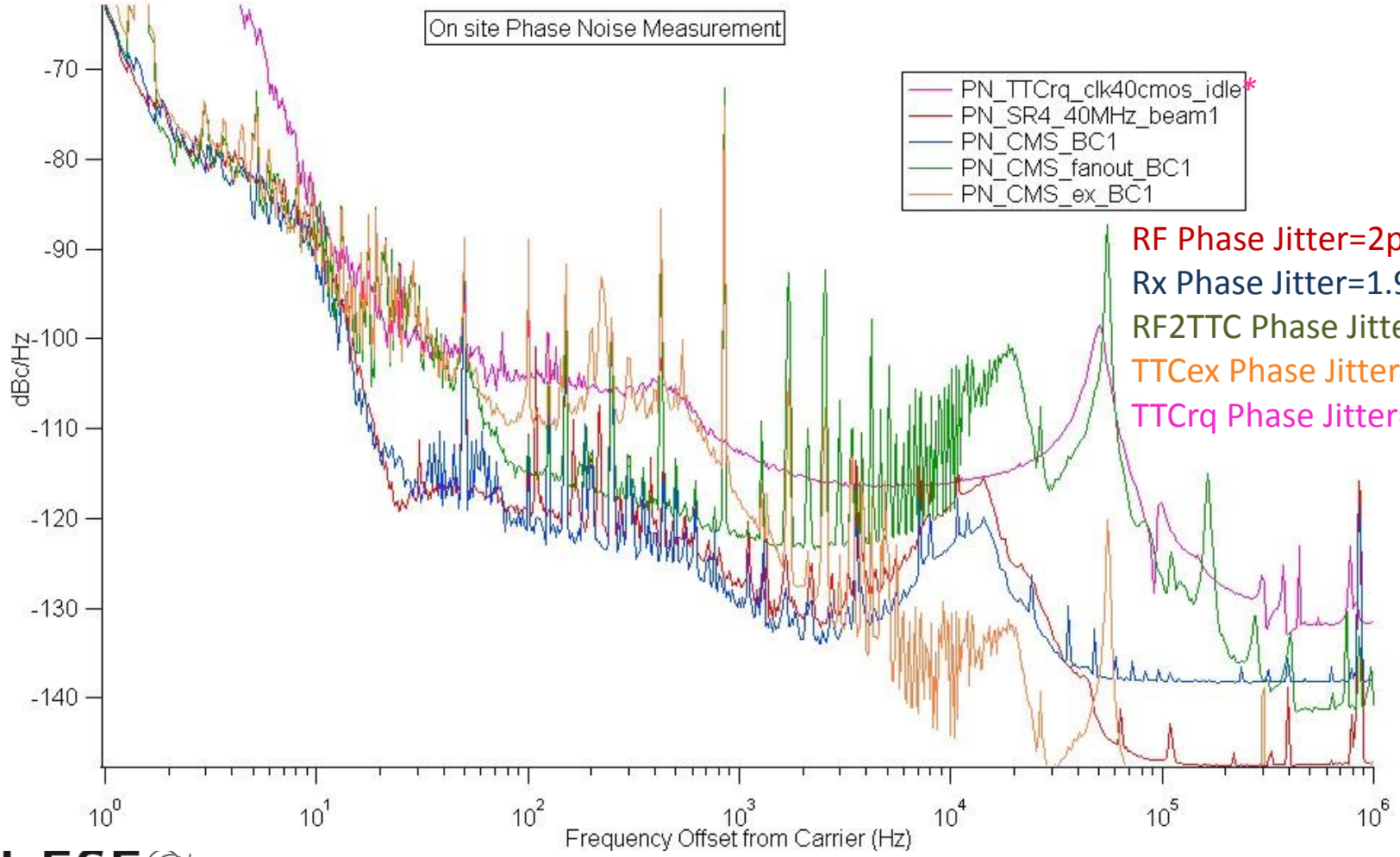
RF Phase Jitter=2ps rms
Rx Phase Jitter=1.9ps rms
RF2TTC Phase Jitter=10ps rms





RF Phase Jitter=2ps rms
Rx Phase Jitter=1.9ps rms
RF2TTC Phase Jitter=10ps rms
TTCex Phase Jitter=4.9ps rms



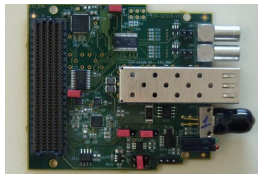


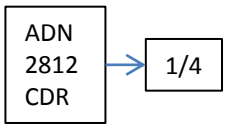
RF Phase Jitter=2ps rms
Rx Phase Jitter=1.9ps rms
RF2TTC Phase Jitter=10ps rms
TTCex Phase Jitter=4.9ps rms
TTCrq Phase Jitter=6-7ps rms*

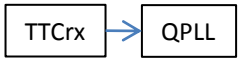
*approximated from lab measurement

- Comparing 3 “Clock Recovery” designs using time domain jitter analysis

Jitter (ps rms)	TTC FMC board (no PLL)	GBT Serdes Prototype	TTCrq 40 MHz output
TIE jitter	11	4	9
Cycle to cycle jitter	8	12	13
Random Jitter	4	5	7
Periodic Jitter	11.5	2	7
Skew jitter	13	Not measured	10

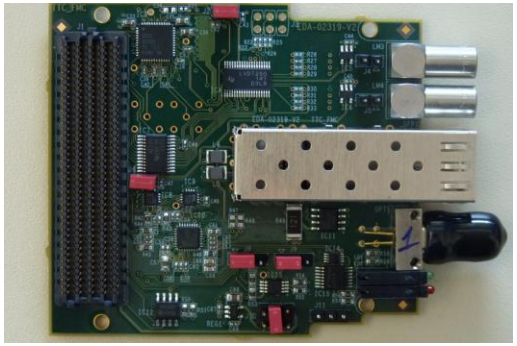






- TIE jitter and Cy2cy jitter give contradictory information => carefully choose the jitter you need
- High periodic jitter detected on TTC-FMC but no clue on the jitter frequency

- To use or not to use a pll in the TTC-FMC module?



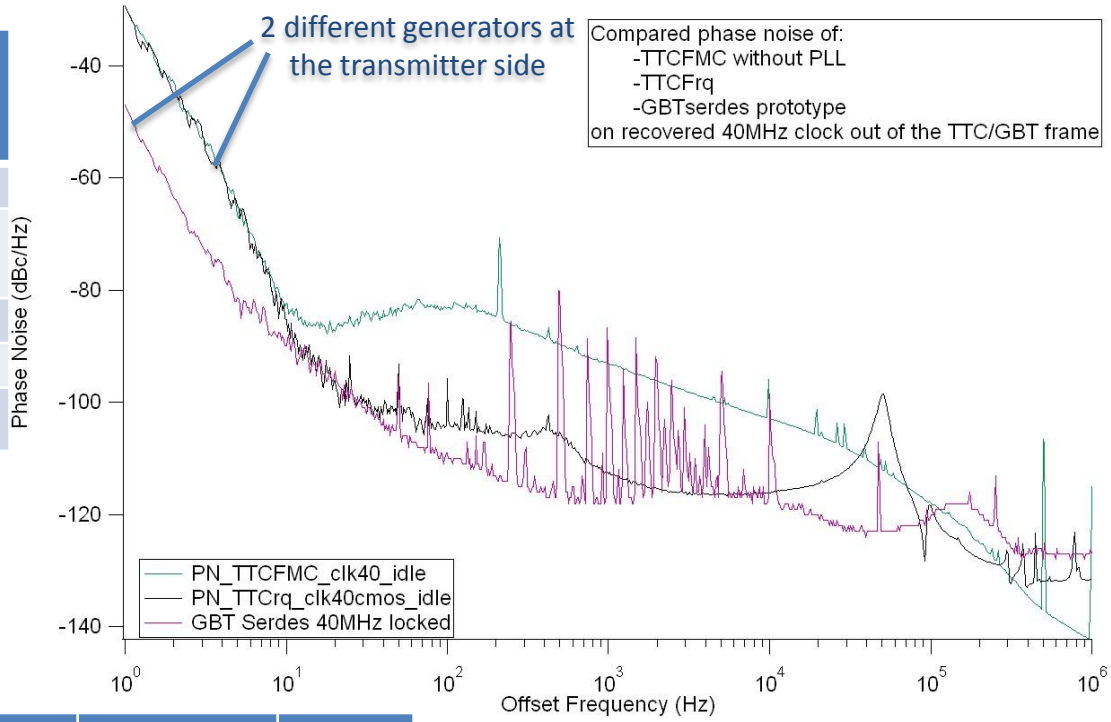
Courtesy: Paschalis Vichoudis

	TTCFMC NO PLL	TTCFMC WITH CDCE PLL
Skew /Refclk	16 ps	16 ps
Cycle to cycle jitter	7.3 ps	6.5 ps
Period jitter	4.3 ps	3.9 ps
TIE	8.7	9.05

A priori, very similar performance with and without PLL
TIE slightly higher for the WITH PLL schem, in contradiction with Cy2Cy and period jitter …why?

- Comparing 3 "Clock Recovery" designs using mixed domains jitter analysis

Jitter types (ps rms)	TTC FMC board (no PLL)	GBT Serdes Proto	TTCrq
TIE	11	4	9
Cycle to cycle jitter	8	12	13
Random Jitter	4	5	7
Periodic Jitter	11.5	2	7
Skew jitter	13	-	10



Phase Noise extracted jitter (ps rms)	TTC FMC (no pll)	GBT Serdes	TTCrq
Integrated over 1Hz-1MHz	68	9	64
Integrated over 10Hz-1MHz	8.8	4	5.3
Integrated over 1Hz-10Hz	67.2	8.1	63.6

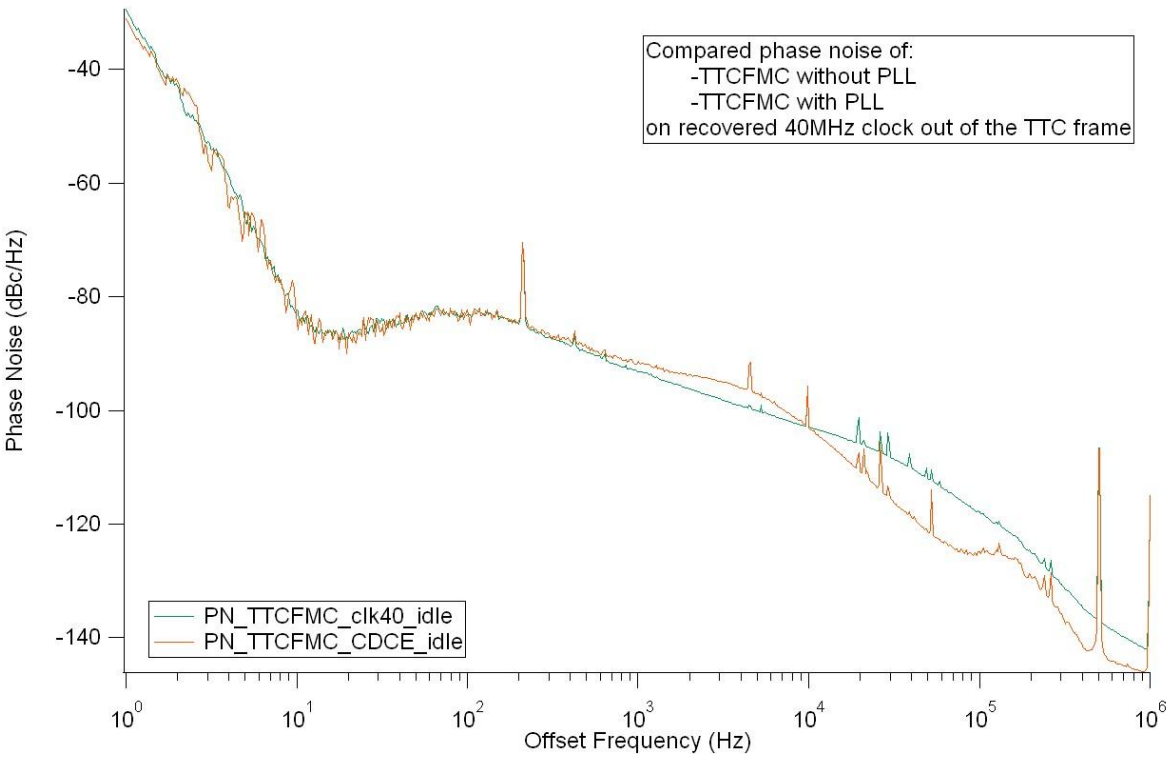
- TTCrq & GBT are better for serial data
- TTC_FMC might be better for ADC, but beware the 500kHz spur
- GBTserdes has no peaking frequency => good
- Various peaks on GBT plot are impressive but have Negligible impact on jitter

- To use or not to use a pll? Example of the TTC-FMC module

	TTCFMC NO PLL	TTCFMC WITH CDCE PLL
Skew /Refclk	16 ps	16 ps
Cy2cy jitter	7.3 ps	6.5 ps
Period jitter	4.3 ps	3.9 ps
TIE over 1ms	8.68	9.05

Phase Noise extracted jitter (ps rms)	TTC FMC (no pll)	TTC FMC with pll
Integrated over 1Hz-1MHz	68	60
Integrated over 10Hz-1MHz	8.8	9.1

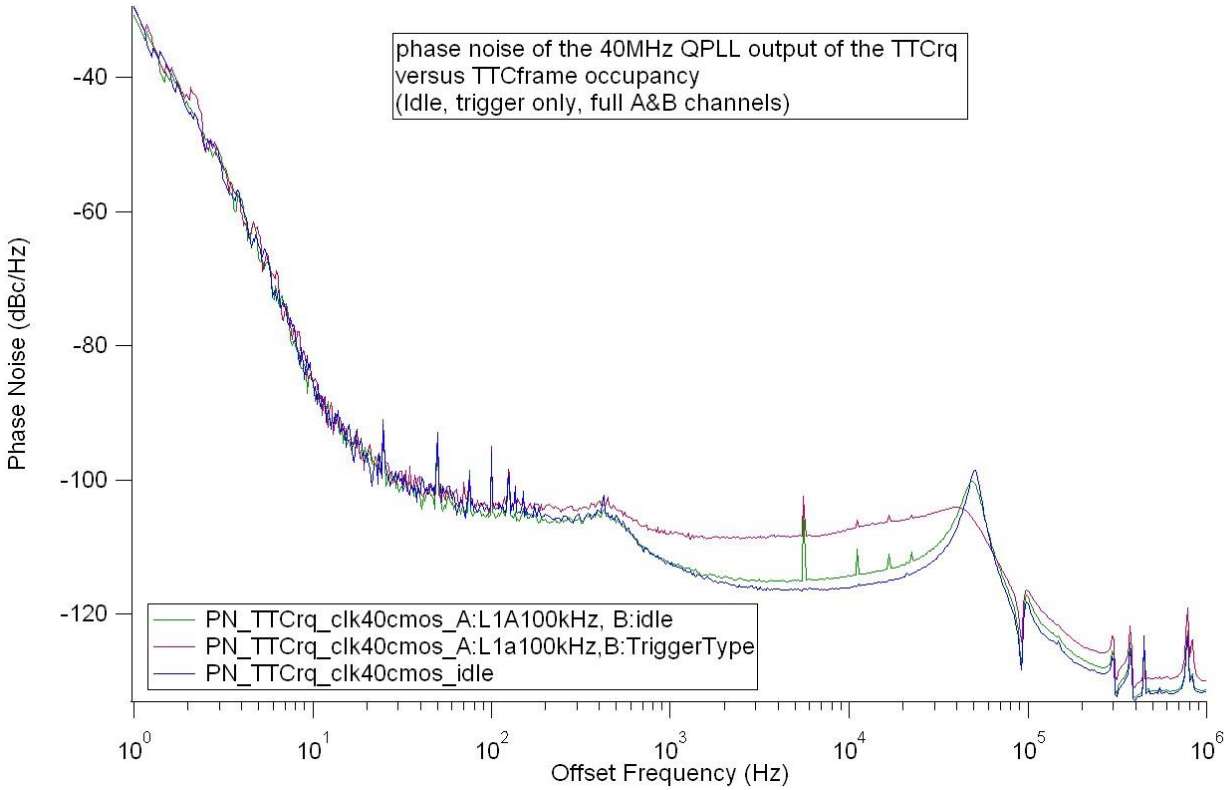
TIE and Phase noise jitter are very close
Scheme with PLL a bit more noisy as there is a bit more periodic jitter



TTCrq example – idle, trigger only, full A and B

Jitter types (ps rms)	TTCrq – Idle TTC	TTCrq – full A and B channels
Time Interval Error jitter	9	10
Cycle to cycle jitter	13	13
Period jitter	7.5	7.5
Integrated phase noise	8	10.1

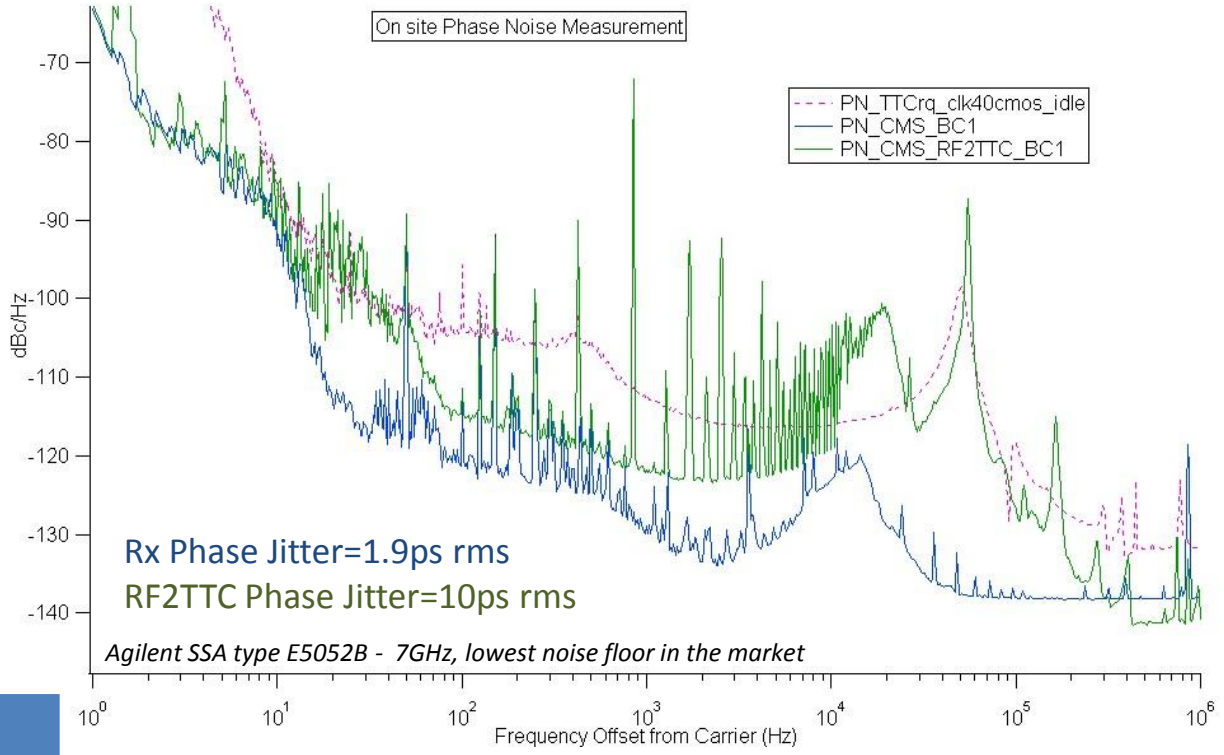
The QPLL filters out very well
the jitter of TTCrx
related to TTC channel occupancy



Improving the design of the RF2TTC

Jitter type (as measured in 2007)	RF2TTC
Cycle to cycle jitter	7 ps rms
Period jitter	10 ps rms
Skew (clkout vs clkin)	15 ps rms

Lecroy scope 7100, measured in 2007



The RF2TTC could have much less jitter if we…
Remove the QPLL
- the input clock is much cleaner than the QPLL intrinsic jitter
- Adding a QPLL required a lot of circuitry from ECL to LVDS and reversely

=> Impossible to guess without a phase noise plot

TO SUMMARIZE …

- Most of the jitter is added to the Bunch Clock after the long haul transmission (phase noise at experiment is identical to the phase noise at the point 4).
- Cy2cy, Period and TIE jitter values can bring contradictory information. It is useful to complete them by a phase noise plot.
- The jitter added by the TTC system can be further reduced, thanks to the analysis made by the phase noise plot.

CONCLUSION

- Each sub-system has its specific requirements in term of jitter
  - Know your system specificity and the type of jitter it is sensitive to
  - « 10 ps rms jitter » does not mean much!
  - Some sub-systems have jitter requirements more stringent than the ones demanded by the detector performance (for example, a serial data link)
- The jitter induced by RF, Beam or long haul transmission is negligible. The noise comes with complex modules, TTC frame encoding, etc.
- A good understanding of the jitter profile can help a lot to reduce it
  - A pll does not always reduce the jitter
  - Choosing the good pll is often a trade-off between stability and jitter performance
- …and a good understanding often means mixing time and frequency domains

- Jitter perspective for the TTC upgrade
  - The performance of the GBTserdes (prototype of the GBTx) in term of clock recovery is very promising
  - Knowledge and interest in jitter issues are growing up within the community, due to the increasing speed of serial data links
  - Much better instruments exist now to track the jitter source and understand how to reduce it
  - Special care will be taken with the design of the TTC upgrade (TTC-PON project) to keep this jitter as low as possible

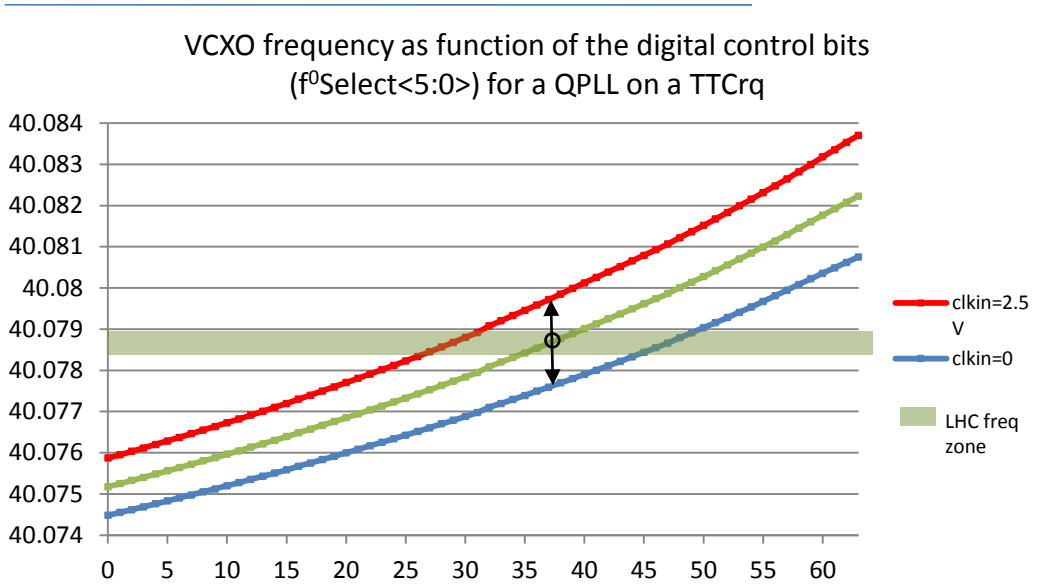
- White papers:
  - Agilent Application Note, *Using Clock Jitter Analysis to Reduce BER in Serial Data Applications,* Agilent Technologies Application Note, 2006, available from www.agilent.com .
  - Agilent Application Note, *Jitter Analysis Techniques for High Data Rates*, Agilent Technologies Application Note 1432, 2003, available from www.agilent.com .
  - J. Hancock et al., *Jitter-Understanding it, Measuring it, Eliminating it, Part1, Part2, Part3,* High Frequency Electronics, Summit Technical Media, April, May, June 2004, available from http://www.highfrequencyelectronics.com .
  - Silicon Labs Application Note, A Primer on Jitter, Jitter Measurement and Phase-Locked Loops, Silicon Laboratories AN 687, 2012, available from www.silabs.com .
- Projects:
  - TTC-project web page, http://ttc.web.cern.ch/TTC/
  - GLIB-project web page, https://espace.cern.ch/project-GBLIB/public/default.aspx
  - GBT-project web page, https://espace.cern.ch/GBT-Project/default.aspx
- Papers and presentations:
  - S. Baron, *Passive Optical Network for TTC*, ACES 2011 workshop, CERN, March 2011, https://aces.web.cern.ch/aces/aces2011/ACES2011.htm
  - JINST paper*, Jitter Impact on Clock Distribution in LHC Experiments*, S. Baron et al., TWEPP 2012, Oxford

THANKS!

SPARE SLIDES

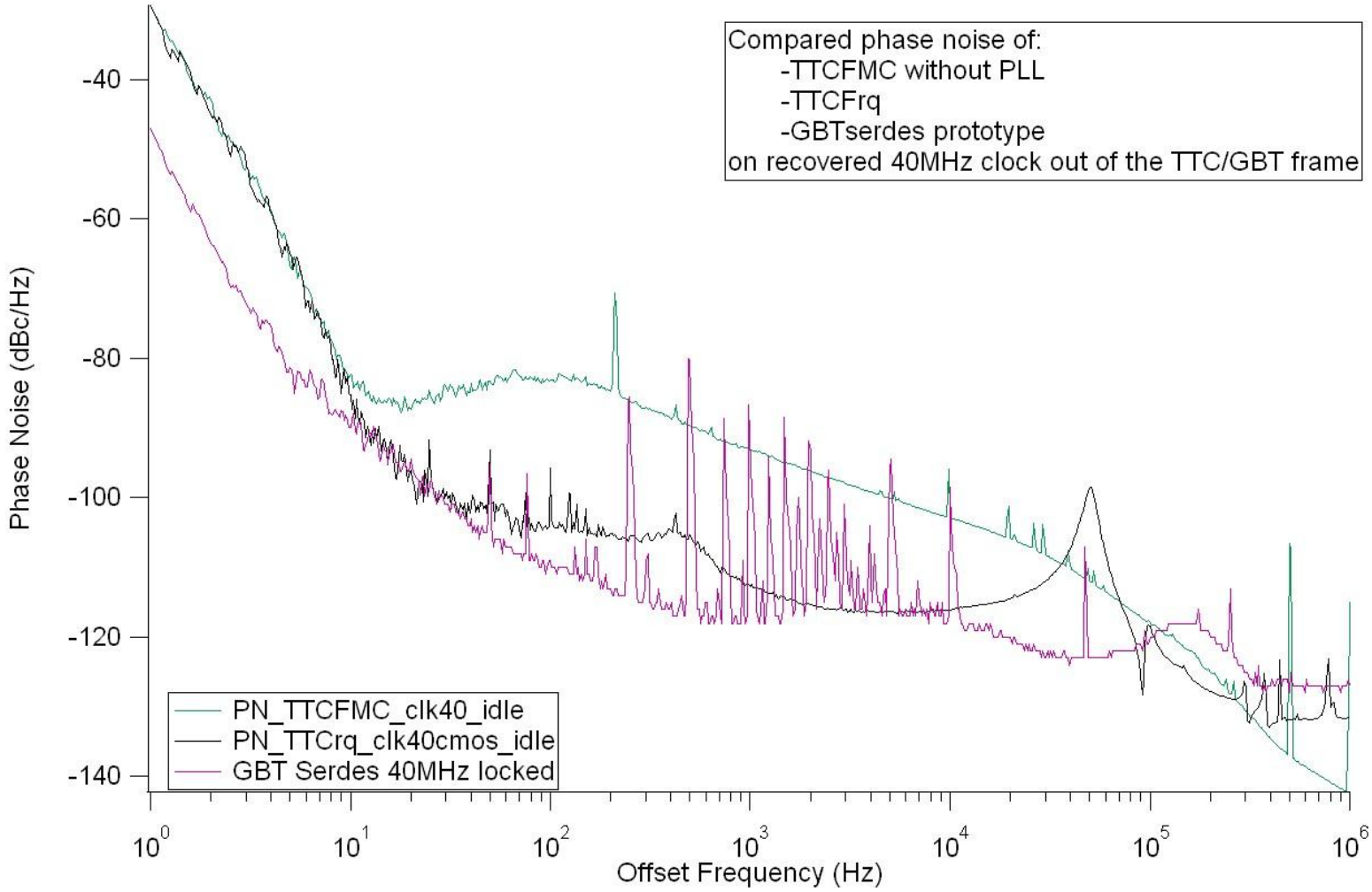
Spare Slide – QPLL characteristics

- Phase-Locked Loop based on a Voltage Controlled Crystal Oscillator
- Designed to frequency and phase-lock to the LHC master clock: f = 40.0786 MHz
- Locking range: Δ ≈ ±3.7 KHz around f = 40.0786 MHz
- Locking Mechanism: bang-bang (early/late phase)
- Loop bandwidth: < 7 KHz
- Locking time – including a frequency calibration cycle (mode 1): ~180 ms
- Locking time – excluding a frequency calibration cycle (mode 0): ~250 µs



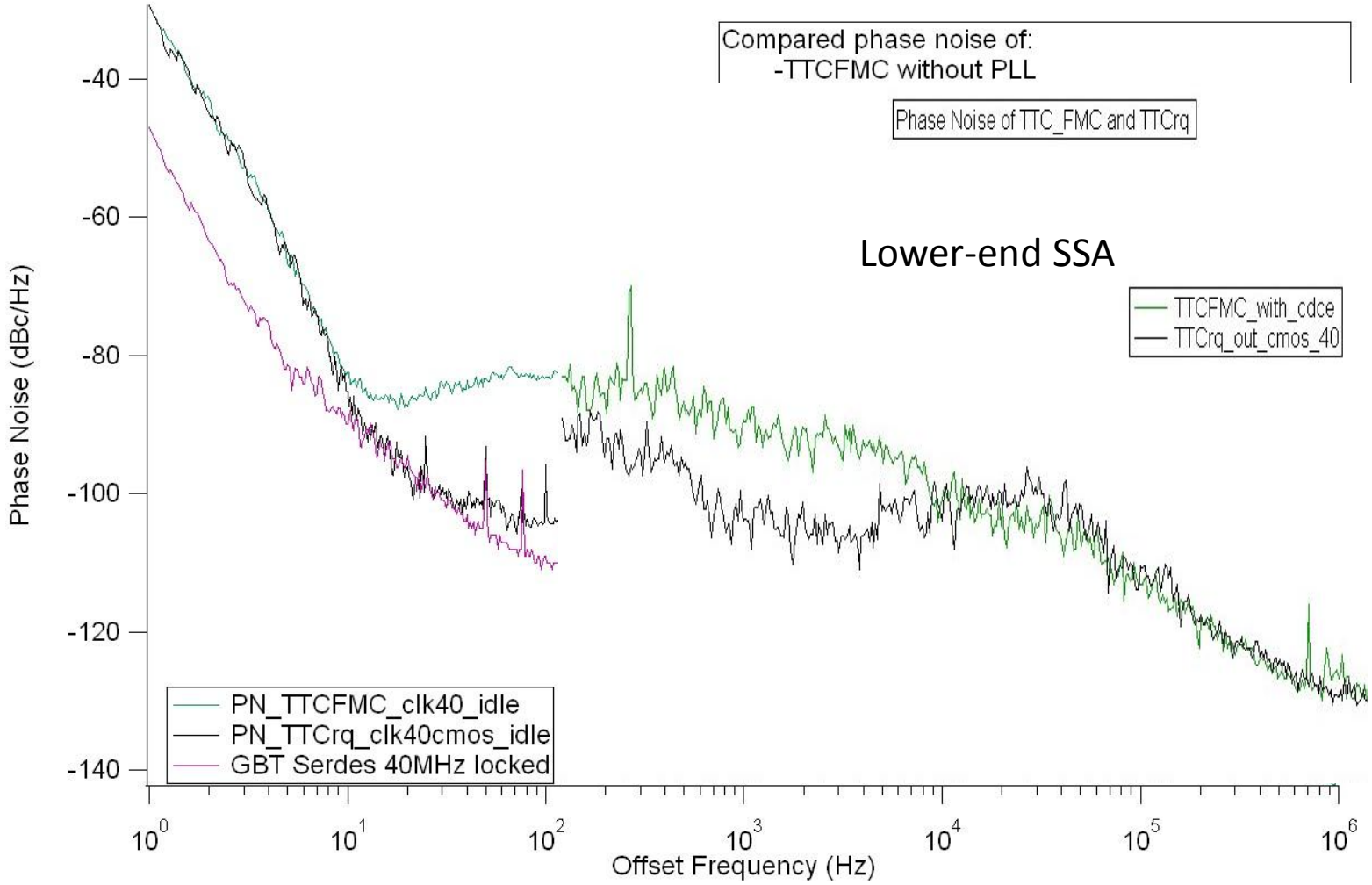
Beware of Noise floor - 1

- Example of frequency measurements



Beware of Noise floor - 2

- Example of frequency measurements



Typical RF frequency changes

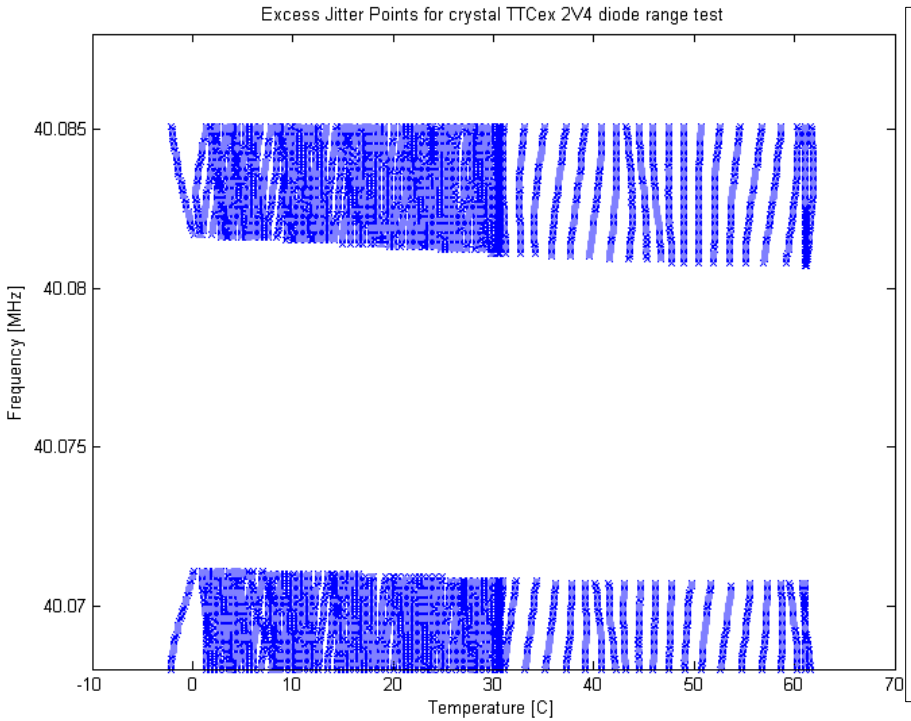
- An exhaustive list…

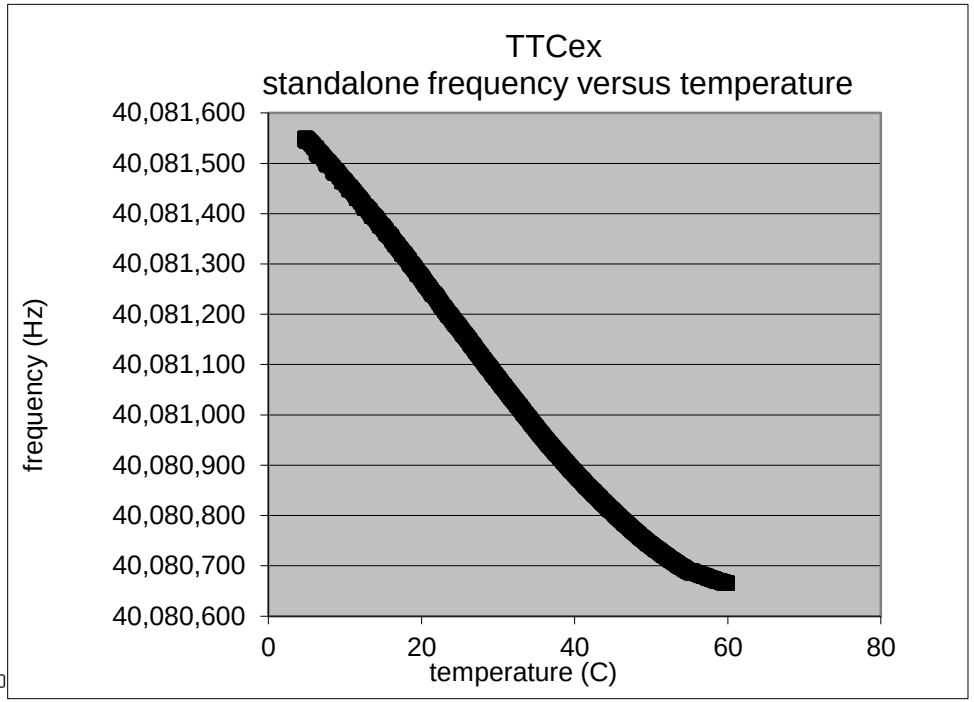
NAME	DESCRIPTION	MAGNITUDE**	RATE**	ACC MODES	BEAM MODES
RF resync	Unchanged, described in the EDMS document LHC MODES: LHC-OP-ES-0022,				
RF/DUMP check	RF-vs-dump cable inversion check, change individually RF1 and RF2 by 1000Hz then back.	+1000 Hz	220 Hz/s***	ALL	SETUP (before resync)
RAMP	RF goes from 450GeV to 7Tev (or 3.5TeV)	+870 Hz for protons, +5500 Hz for ions	<0.5 Hz/s	ALL	RAMP
RAMP DOWN	RF goes from 7Tev (or 3.5TeV) to 450GeV	-870 Hz for protons, -5500 Hz for ions	<0.5 Hz/s	ALL	RAMP DOWN
INJECTION test	Injection tests with offset energy	+/- 2400 Hz	220 Hz/s	BEAM SETUP, MD	INJ&DUMP,CIRC&DUMP
DUMP PROTECTION test	+/-1000 Hz for loss maps	+/- 1000 Hz	220 Hz/s	BEAM SETUP, MD	ADJUST
CHROMATICITY and/or DISPERSION measurements	Typically, done manually, both beam, at flat top or flat bottom, but could also be automated for any time (even in ramp)	+/-50 Hz	220 Hz/s	ALL	INJECTION MODES* (flat bottom), FLAT TOP
TIDAL adjustment	After reaching flat top, value to be set according to the tide of the moment	+/-15 Hz	220 Hz/s	ALL	FLAT TOP
Other ORBIT adjustments		+/-15 Hz	220 Hz/s	ALL	FLAT TOP

*INJECTION MODES = Injection Probe Beam, Injection Setup Beam, Injection Physics Beam.
**These values are applied to RF CLOCKS (400MHz). They have to be divided by 10 to be applied to the BUNCH CLOCKS (40MHz) delivered to experiments.
*** The rate of 220Hz/s used for all the trims is a constant that could easily be reduced if needed.

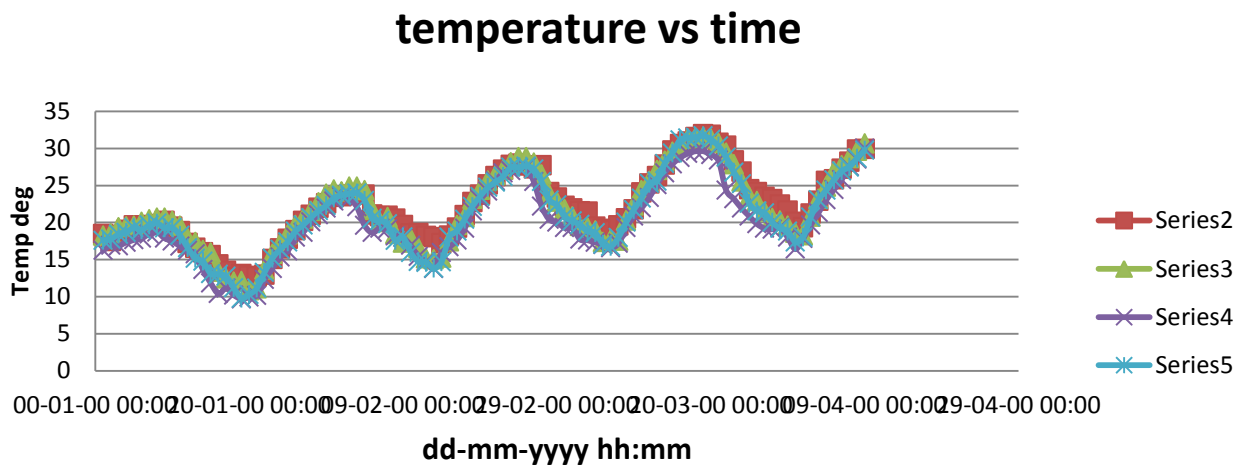
TTCex PLL characteristics

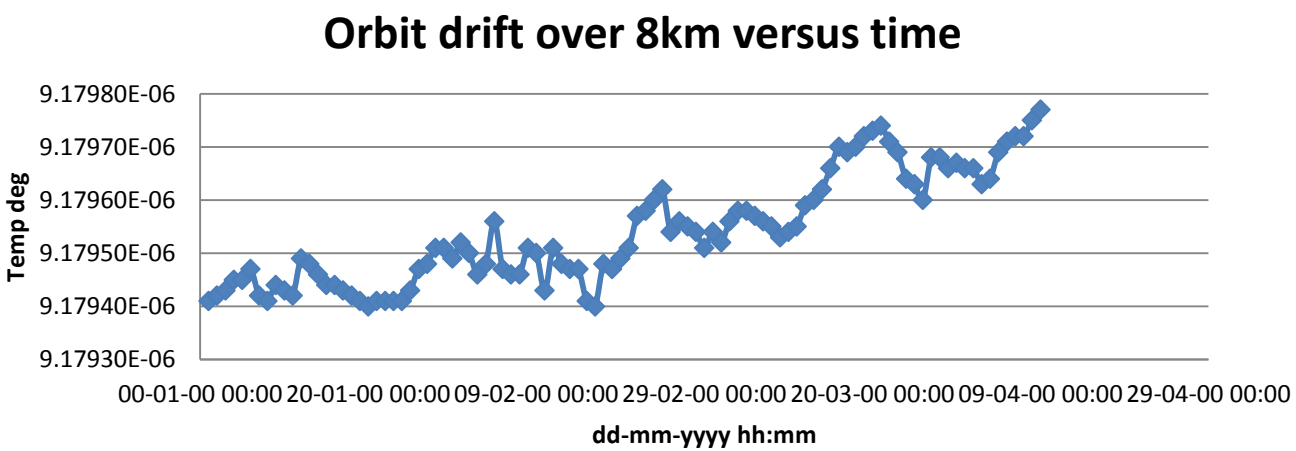
- Locking range:
  - 40.079MHz +/- 2kHz: 40.077MHz-40.081MHz





Diurnal phase drift





Time Domain versus Frequency Domain

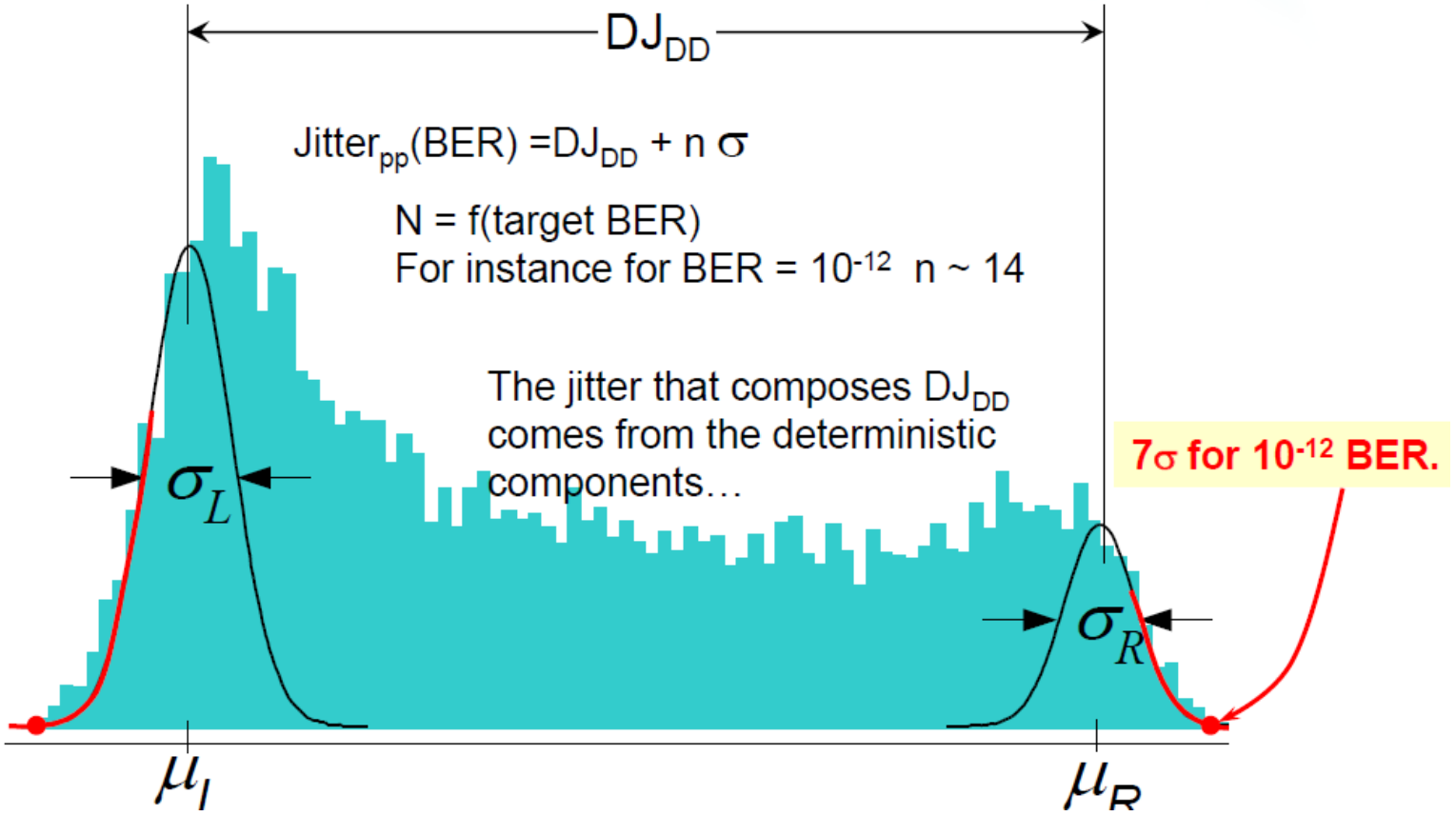
- Time domain equipment
  - has the virtue of being able to directly measure **peak-to-peak, cycle-to-cycle, period and TIE jitter**. This measurement approach permits the measurement of jitter **of very low frequency clock** (or carrier) signals. By post-processing the data with techniques, such as FFTs and digital filters, it is possible to integrate the phase noise value over a specific band of frequencies to generate RMS phase jitter values. Only time domain equipment can measure all of the jitter frequency components. Another key point is that time domain equipment is much better at measuring data-dependent jitter, which makes it very useful for high-speed serial links that use serializer/deserializer (SERDES) technology.
- Frequency domain equipment
  - cannot directly measure peak-to-peak, cycle-to-cycle, or period jitter because its native capability is to measure the RMS power of signals in a given frequency band. Frequency domain equipment is also awkward for measuring data-dependent jitter. However, the best frequency domain instruments have a lower noise floor than the best time domain instruments. This fact makes frequency domain instruments the first choice for ultra-low phase noise clock signal measurements that are free of data-dependent jitter.

	Time Domain	Frequency Domain
Native Measurements	Peak-Peak Jitter Cycle-to-Cycle Jitter Period Jitter	RMS Phase Jitter Phase Noise Jitter Frequency Information
Advantages	Good with Low-Frequency Clocks Good with Data-Dependent Jitter	Lower Noise Floor Easy Detection of Spurs vs. Random Jitter

Dual Dirac Method

Approach to Resolve 'random nature': the Dual Dirac Assumption

Fit the tails of the jitter PDF to two Gaussian curves



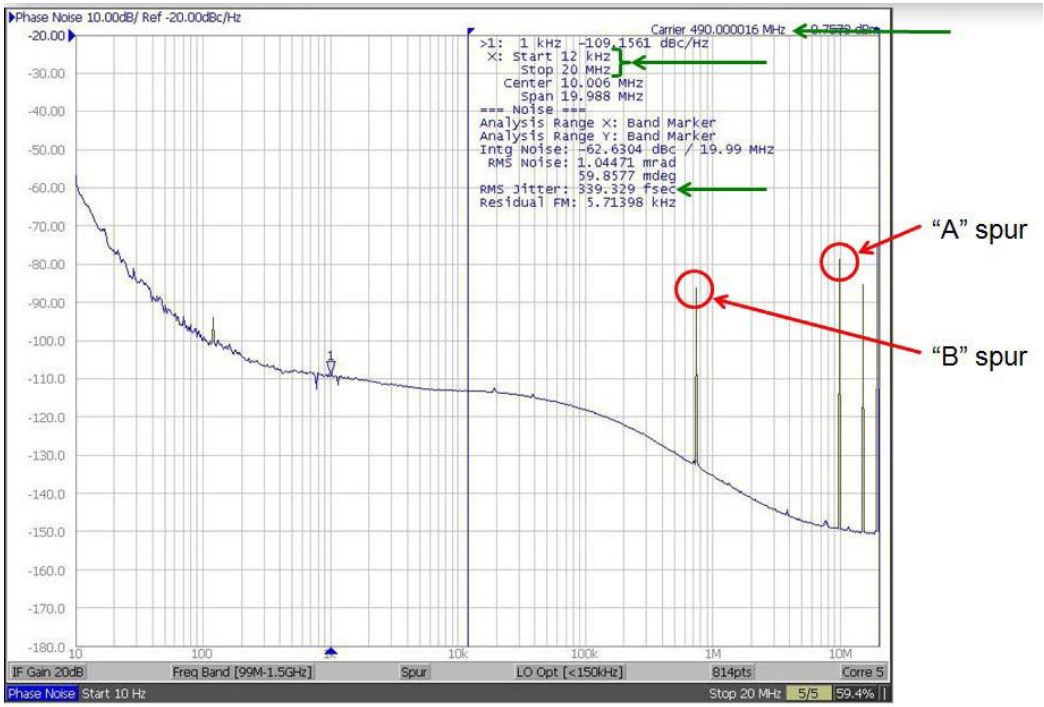
Spurs jitter

- periodic spurious noise
  - Spurs are modeled as sine, so to convert from RMS to peak-to-peak, multiply by 2 2.
  - Typically, only large spurs contribute significantly to the RMS noise. For S = dBc of a spur, the peak-to-peak jitter in UI (unit interval) is:

$$J_{pkpk} = \left(\frac{2}{\pi}\right) \times 10^{8/20}$$

$$J_{rms} = \frac{J_{pkpk}}{2.2}$$

Spur	Pk-pk jitter	RMS Jitter
A	146 fs	51.6 fs
B	58 fs	20.5 fs



Total Jitter & BER

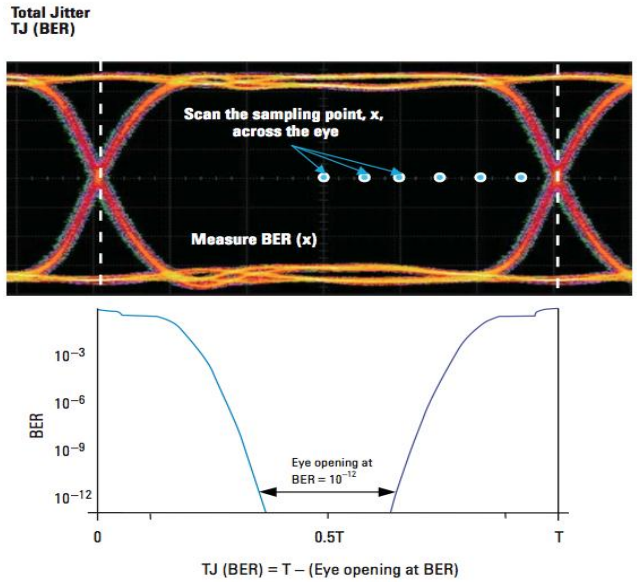


Figure 11. The bathtub plot shows BER as a function of the time-position of the sampling point

Table 1. The relationship between BER and peak-to-peak values of random jitter, $\sigma = J_{rms}^{RJ}$.

Bit Error Ratio (BER)	Peak-to-Peak RJ $J_{PP}^{RJ} = n \times \sigma$
10^{-10}	$12.7 \times \sigma$
10^{-11}	$13.4 \times \sigma$
10^{-12}	$14.1 \times \sigma$
10^{-13}	$14.7 \times \sigma$
10^{-14}	$15.3 \times \sigma$

$$J^{TJ} = n \times \sigma + J_{PP}^{DJ}$$
$$= n \times J_{rms}^{RJ} + J_{PP}^{DJ}$$

Figure 3. An eye diagram with Random Jitter (RJ) showing the effect of RJ on BER.

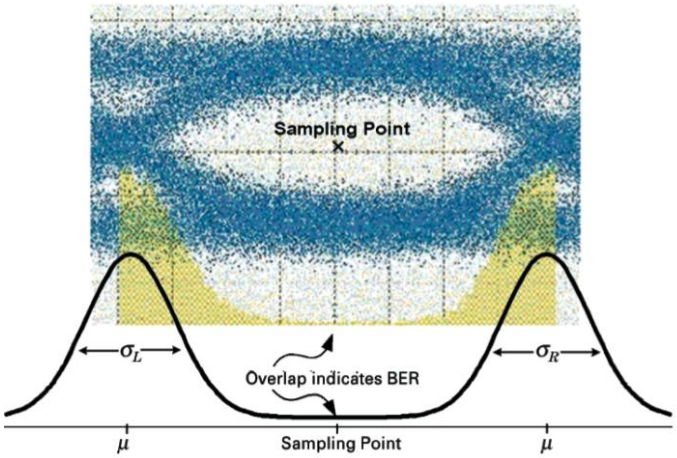


Figure 4. An eye diagram with both Random Jitter (RJ) and Deterministic Jitter (DJ) distinguishing the genuine rms jitter, from the rms jitter caused by RJ, J_{rms}^{RJ}, and the total peak-to-peak jitter, J_{PP}, from the peak-to-peak jitter caused by DJ, J_{PP}^{DJ}.