# Optimizing Impedance Discontinuity Caused by Surface Mount Pads for High-Speed Channel Designs

## Introduction

As data rates continue to increase, today's high-speed board designers face tremendous challenges upgrading their designs to meet increasing bandwidth requirements. When implementing high-speed designs, any small discontinuities in the physical geometries along the transmission path can significantly degrade the signal. This degradation includes loss of signal amplitude, reduction of signal rise time, and increased jitter. As a result, you must be able to identify these discontinuities in the high-speed channel and provide ways to mitigate their effects for better signal transmission.

Two commonly used components in a high-speed serial channel that can benefit from optimization are the DC blocking capacitors and SMA connectors. DC blocking capacitors are normally present in the channel to control the common mode voltage at the receiver while SMA connectors are widely used to allow you to interface the board to test instruments or other boards. This application note examines the discontinuities from the DC blocking capacitors and SMA connectors in detail, and provides optimization techniques to minimize their adverse effects in the channel.

### Plane Cutout under SMT Pads of DC Blocking Capacitors

DC blocking capacitors are common sources of impedance discontinuities in high-speed serial channels. Typically, narrow trace width and narrow trace spacing are used to construct the 100-$\Omega$ differential transmission line pair. However, as these narrow trace pairs are routed into the surface mount pads of a DC blocking capacitor, the sudden widening of the controlled impedance traces as they join with the capacitor pads cause an abrupt impedance discontinuity. The effect of this discontinuity appears as excess capacitance because the surface mount pads of the DC blocking capacitors act as a parallel plate with the reference plane underneath (see Figure 1).

To remove the excess parasitic capacitance associated with surface mount pads, remove a portion of the reference plane that is directly beneath the surface mount pads. This allows the signal that traverses through the DC blocking capacitor to reference a lower plane (further away) and reduce the parasitic capacitance, thereby minimizing the impedance mismatch.

*Figure 1. Ansoft HFSS Setup of DC Blocking Capacitors with and without Plane Cutout under SMT Pads*
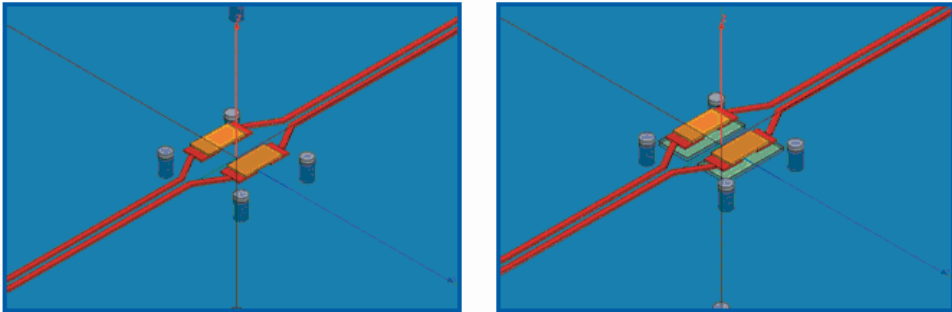


Simulations for the normal routing structure and optimized routing structure of DC blocking capacitors were compared using Ansoft's HFSS 3D Field Simulator tool. The HFSS setup is shown in Figure 1.

In Figure 1, the picture on the left is the normal structure without the plane cutout underneath; the picture on the right is the optimized structure with the plane cutouts included. For these simulations, the board stackup and trace geometries are designed to provide a 100 Ω differential signal. All traces and plane layers are set as 1 oz. copper. The width of the surface mount pads is initially set to 20 mils to match the width of the 0402 type capacitors that is modeled. Here, the critical parameter for optimization involves the width of the cutout underneath the surface mount pads. The length of the cutout is always equal to the end-to-end distance of two surface mount pads, which is set to 60 mils in this simulation. The ground vias near the DC blocking capacitors are recommended to provide the current return path. Additionally, simulation waveports are defined at the two ends of the differential traces. A simulation sweep performed by varying the width of the cutout from the initial 20 mils to 35 mils, in 5 mils increments, yields the optimum plane cutout size for this particular simulation.

Figure 2 shows the TDR impedance plot from the Ansoft HFSS simulation. The red line is the impedance profile of the high-speed differential traces without the plane cutout under the surface mount pads of the DC blocking capacitors. The blue, black, green, and purple lines are the impedance profiles with the width of cutout set to 20 mils, 25 mils, 30 mils, and 35 mils, respectively.

The simulation results show that the width of the plane cutout plays an important role in minimizing the impedance mismatch. The impedance without the plane cutout is approximately 75 Ω at the DC blocking capacitor pads. The minimum impedance mismatch is achieved when the width of the cutout is 25 mils. The optimum routing structure, which has a 25-mil wide cutout under the capacitor, gives approximately 95 Ω differential impedance, which falls within the typical ±10% tolerance requirements for the 100 Ω differential pair.

*Figure 2. Impedance Profile with Different Width of Plane Cutout underneath the SMT Pads*
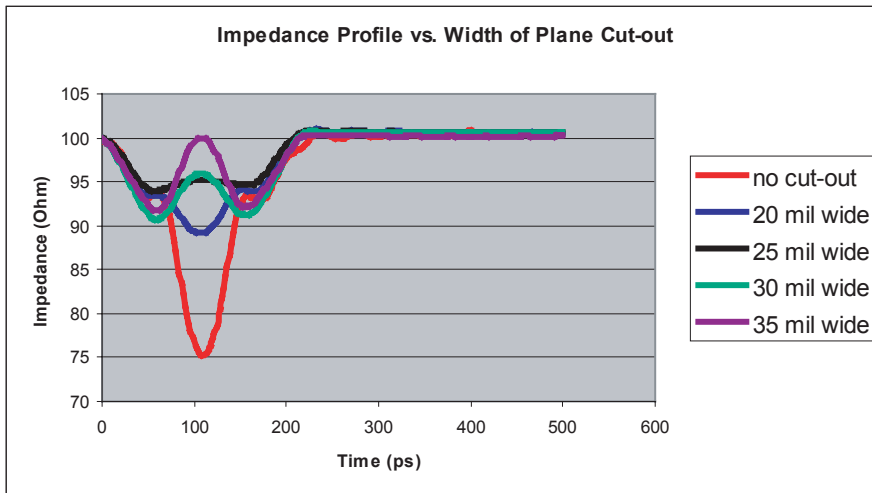


Figure 3 shows the plot of the differential return loss computed by HFSS. The return loss is a measure of the reflected energy from the discontinuities in an electrical link. It is the ratio of the reflected energy (PR) to the incident energy (PT) and expressed as $20\log_{10}$ (PR/PT) in negative decibels. For example, -20dB return loss means that 10% of the energy is reflected while 90% of the energy is transmitted through.

The red line in Figure 3 represents the differential return loss of the high-speed traces without the plane cutout underneath the surface mount pads. The blue, black, green, and purple lines in Figure 3 represent the differential return losses of the channel when the width of the plane cutout is set to 20 mils, 25 mils, 30 mils, and 35 mils, respectively.

In Figure 3, the return loss without the plane cutout crosses the -20dB point at 1.4 GHz, while the optimum structure with 25 mils wide cutout does not reach the -20dB line until above 20 GHz. The frequency response of the optimized routing structure is significantly improved over the normal routing structure.

*Figure 3. Differential Return Loss with Different Width of Plane Cutout under the SMT Pads*
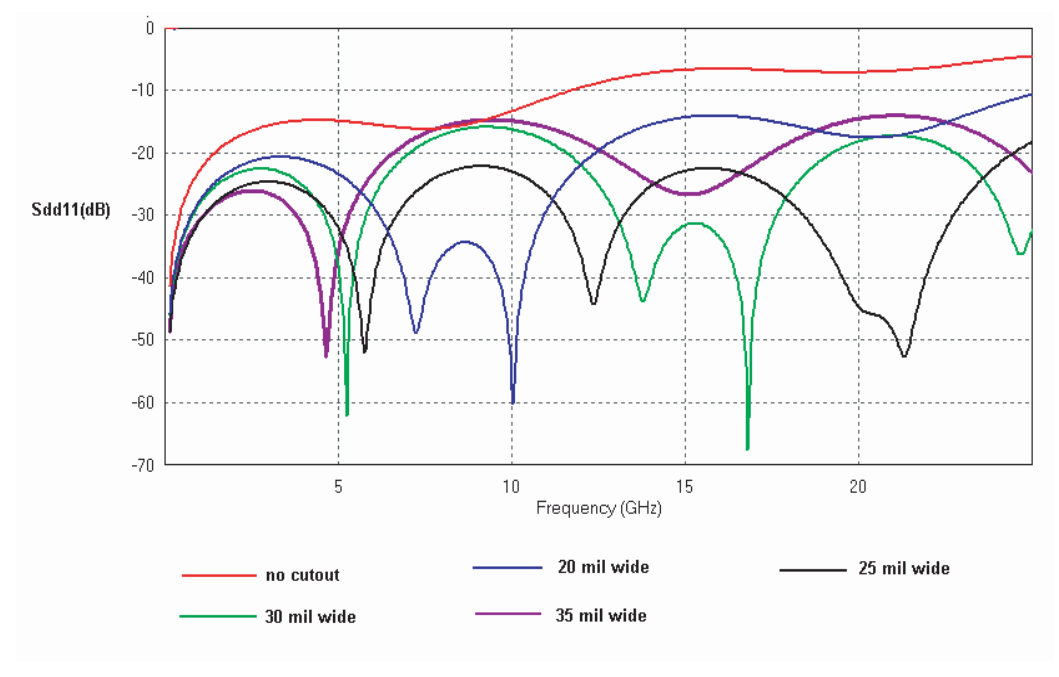


## Plane Cutout under SMT Pads of SMA Connectors

SMA connectors are widely used in high-speed PCBs to interface the board with a test instrument or with other boards. These connectors are typically surface mount type for the center conductor with four surrounding pins mounted as through-holes for grounding and connection strength (see Figure 4). This structure allows the stable attachment of the SMA cables while maintaining good signal integrity.

Using these connectors in the high-speed transmission path presents a similar problem to the characteristic impedance that was observed with the DC blocking capacitors. That is, the typically narrow trace that is used to construct the 50 $\Omega$ transmission line is routed into the surface mount pad of the SMA. The sudden widening of this trace as it meets the larger center conductor pad of the SMA causes the characteristic impedance to

be reduced. As a result, you can use the same technique of removing the ground plane underneath the surface mount pads to minimize the sudden impedance mismatch caused by the smaller signal trace abruptly meeting the larger surface mount pads of the SMA.

*Figure 4. Ansoft HFSS Setup of SMA Connector with and without Plane Cutout Underneath*
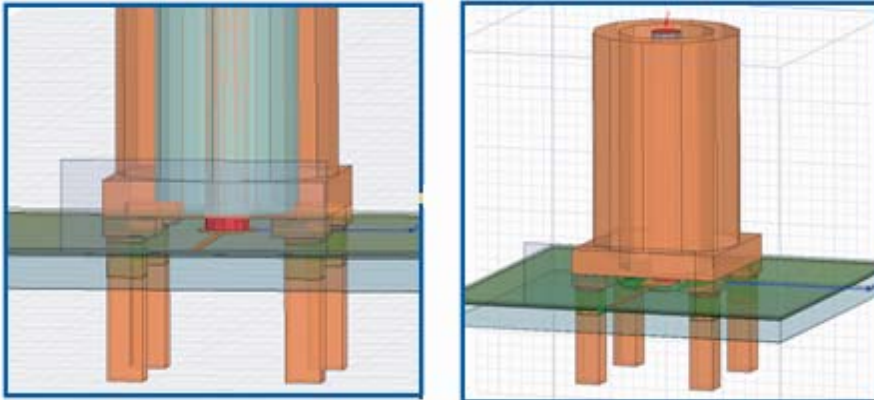


Simulations for the normal routing structure of an SMA (without plane cutout beneath the SMT pad) versus the optimized routing structure (with plane cutout underneath) were performed using HFSS. The simulation set up is shown in Figure 4.

In Figure 4, the picture on the left is the setup for the normal implementation where the center pin of the SMA is directly connected to the surface mount pad and there is no cutout below the center conductor's pad. In the picture on the right, the optimized routing structure has the same set up as the normal routing structure with the exception of a large circular ring cut out on the reference plane beneath. Providing this plane cutout allows the surface mount pad to reference to a lower plane and reduce the parasitic capacitance caused by the surface mount pad of the SMA. Reducing this parasitic capacitance improves the impedance matching between the signal trace and the center conductor pad of the SMA.

In the simulation, all traces and plane layers are set as 1 oz. copper. Waveport 1 is defined at the beginning of the 50-$\Omega$ trace that routes into the surface mount pad, while waveport 2 is defined at the end of the SMA connector. The critical parameter for optimization is the radius of the circular ring of the cutout. For this simulation, the radius of the circular ring cutout is swept from an initial value of 15 mils to 20 mils, and then to 25 mils.

Figure 5 shows the TDR impedance plot result comparison from HFSS. The red line is the impedance profile of the 50-$\Omega$ transmission line without the plane cutout. The blue, black, and green lines are the impedance profiles of the trace with the radius of the circular cutout set to 15 mils, 20 mils, and 25 mils, respectively.

The simulation results show that the radius of the cutout plays an important role in optimizing the impedance mismatch. The impedance mismatch without the plane cut out is greater than 25 $\Omega$ from the desired nominal impedance of 50 $\Omega$. The minimum impedance mismatch is achieved when the radius of the circular cutout is set to 25 mils for this particular simulation. This improvement yields less than 5 $\Omega$ of impedance mismatch, which is within the typical ±10% tolerance requirements of a 50-$\Omega$ transmission line.

*Figure 5. Impedance Profile with Different Radius of Circular Cutout under the SMT Pads of SMA*
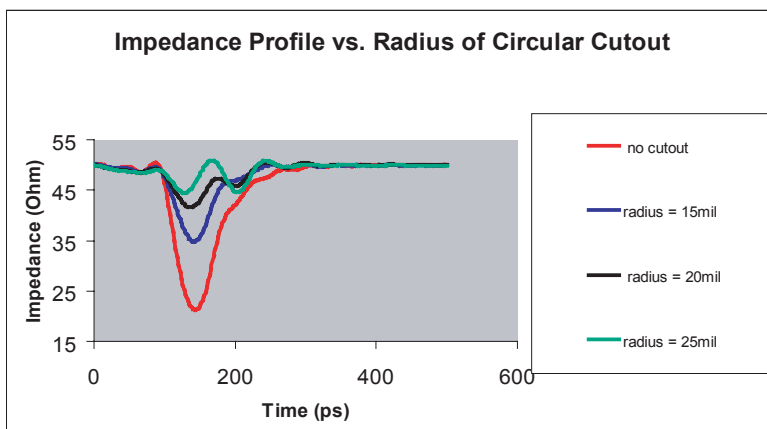


Figure 6 shows the plot of the return loss computed by HFSS. The red line is the return loss of the 50-$\Omega$ trace without the plane cutout underneath the surface mount pads. The blue, black, and green lines are the return losses of the channel when the radius of the circular cutout is set to 15 mils, 20 mils, and 25 mils, respectively.

The return loss for the normal implementation crosses the -20dB line at approximately 1.4 GHz, while the return loss of the optimum routing structure with 25 mil radius of the circular cutout does not reach the -20dB line until approximately 8 GHz. As shown in Figure 6, the frequency response of the optimized routing structure is significantly improved over the normal routing structure for frequencies up to 8 GHz.

*Figure 6. Return Loss with Different Radius of Circular Cutout under the SMT Pads of SMA*
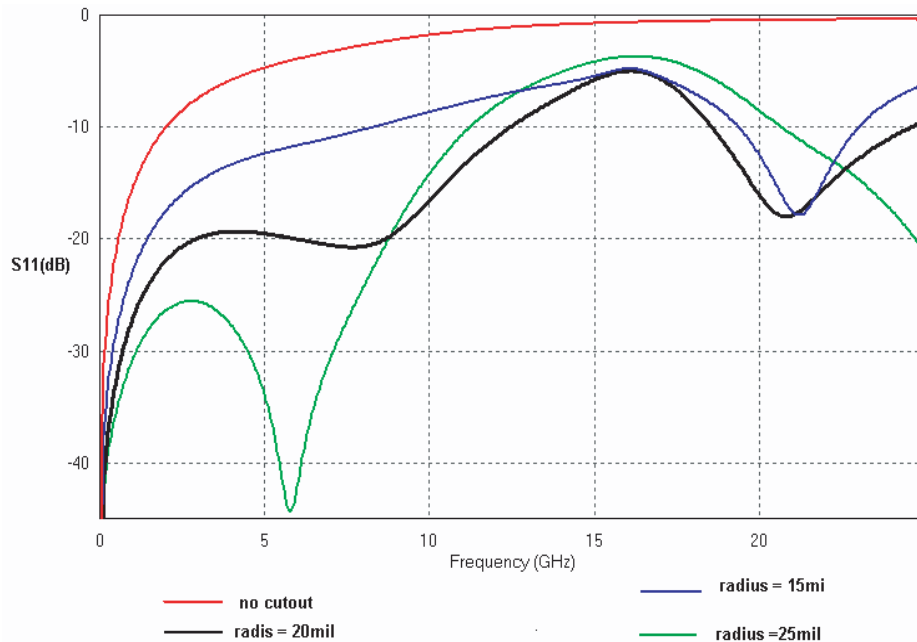


## Summary

The surface mount pads used in DC blocking capacitors and SMA connectors are two common sources of impedance discontinuities in high-speed serial channels. Impedance discontinuity can significantly degrade the performance of the signal. You must carefully analyze and design these structures to ensure optimal performance, especially at multi-gigabit data rates. The techniques described in this application note show you how to optimize impedance discontinuities for high-speed channel designs.

## References

- Altera® TB 095 *High-Speed Board Design Advisor: High-Speed Channel Design and Layout*.
- Altera net seminar *Gigabit Channel Design Guidelines* by Leonard Dieguez and Salman Jiva.

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