

As data rates increase, designers are increasingly moving away from wide parallel buses to serial buses with differential signaling. Differential signaling uses two output drivers to drive two independent transmission lines, one line carrying one bit and the other line carrying its complement. The difference of the two signals measured between the two traces carries the information. A differential pair is a pair of transmission lines with some amount of coupling between the two legs of the pair.

The issues with parallel buses include signal breakout, source-synchronous timing margins, and termination strategies while differential signaling centers on intra- and inter-pair skew, via stubs, dielectric material properties, and impedance discontinuities.

This application note is for printed circuit board (PCB) designers planning to use the high-speed transceivers available in Stratix® II GX and Stratix IV GX devices and addresses two key design topics:

- Dielectric material selection
- Additional skew introduced in differential pairs because of local variations in dielectric constant (ϵ_r), resulting from the fiberglass weave pattern in a dielectric material.

It also discusses the various strategies you can employ to compensate for the fiberglass weave effect, acknowledges and expands upon existing knowledge, and lists various technical papers for additional information.

Differential Signaling

Differential signaling is widely used in the industry today. High-speed serial interfaces such as PCI-E, XAUI, OC768, and CEI use differential signaling for transmitting and receiving data. [Figure 1](#) shows a typical point-to-point topology between a driver (TX) and receiver (RX) connected by a differential pair.

Figure 1. Point to Point Topology

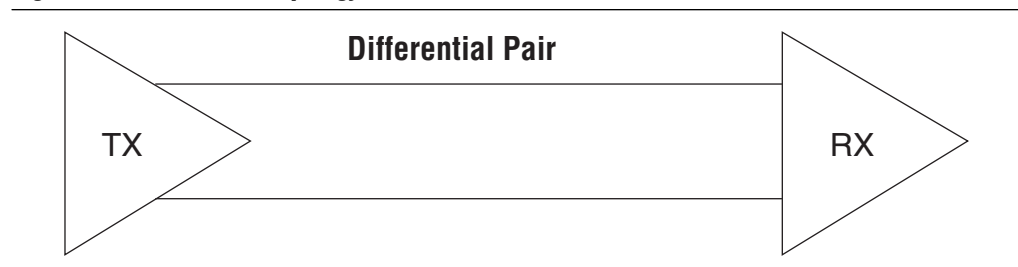
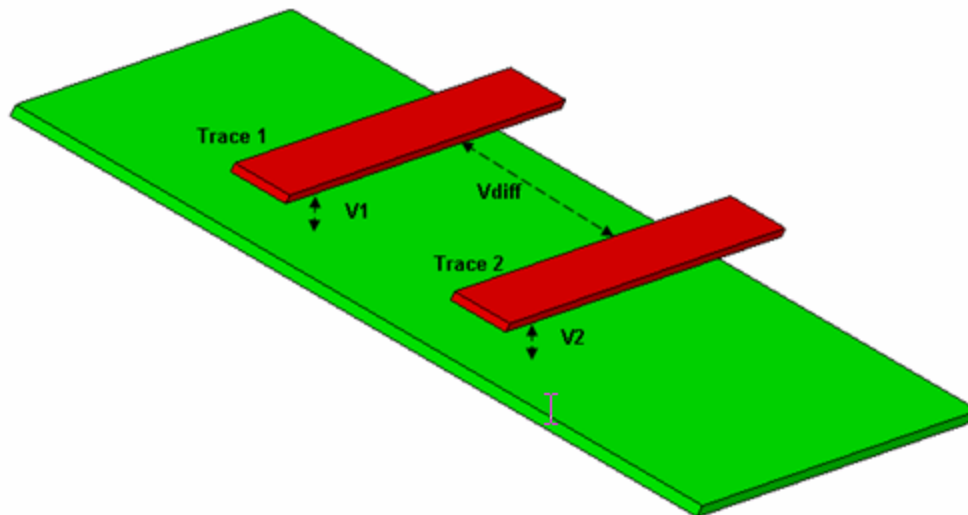


Figure 2 shows a schematic representation of a differential pair. Voltages V_1 and V_2 are the single-ended voltages measured between the respective traces and return path. In addition to the two single-ended signals, there is also a voltage difference between the two signal traces, referred to as “differential signal”.

Figure 2. Differential Pair



At the far end of the transmission line, a differential receiver measures the difference in voltage between the two traces and recovers the differential signal, expressed as:

$$V_{\text{DIFF}} = V_1 - V_2$$

where:

$$V_{\text{DIFF}} = \text{Differential signal}$$

V_1 = Voltage signal on Trace 1 with respect to return path

V_2 = Voltage signal on Trace 2 with respect to return path

The single-ended voltages on a differential pair can be described by a combination of common and differential signals, expressed as:

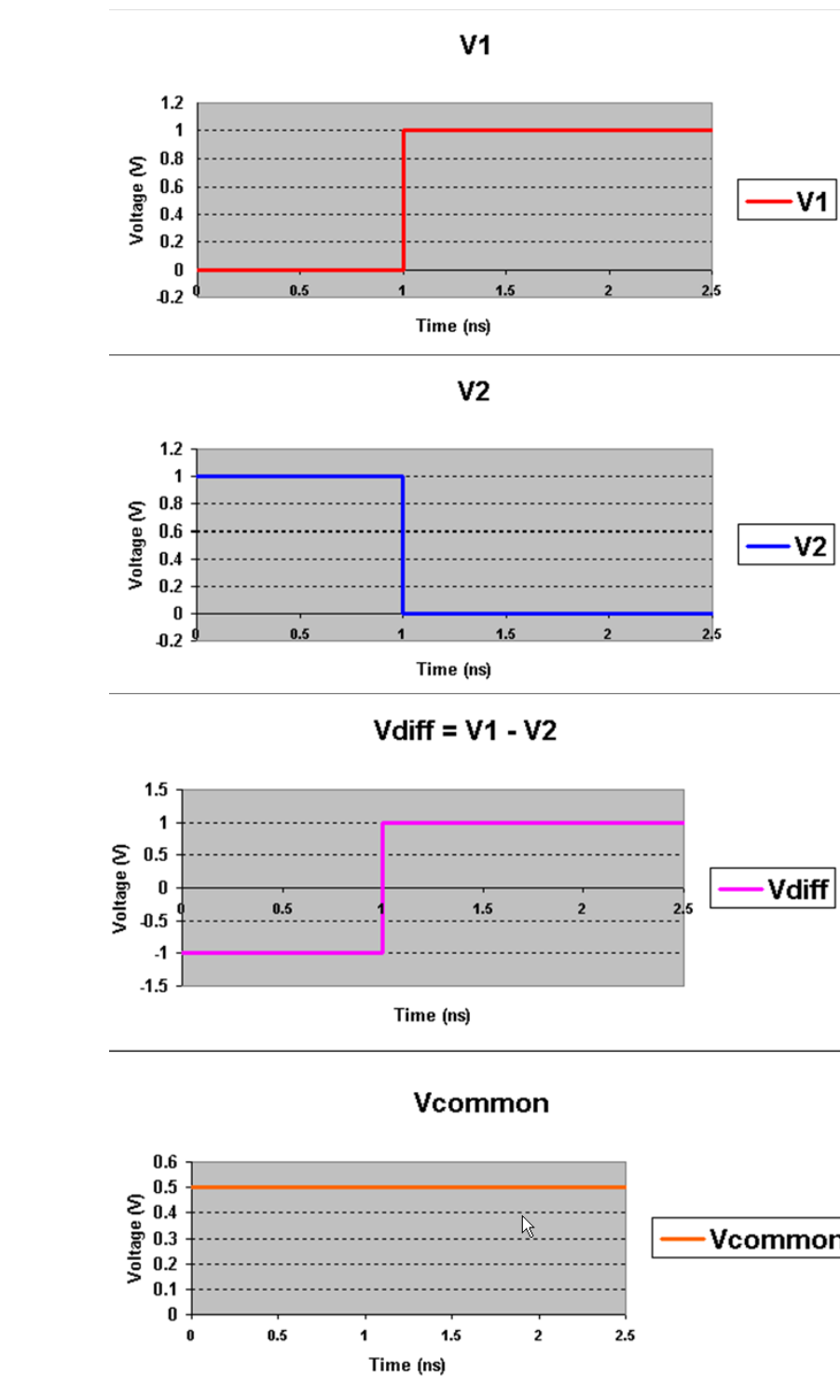
$$V_1 = V_{\text{COMMON}} + V_{\text{DIFF}}/2$$

$$V_2 = V_{\text{COMMON}} - V_{\text{DIFF}}/2$$

where $V_{\text{COMMON}} = (V_1 + V_2)/2$ and $V_{\text{DIFF}} = V_1 - V_2$

Figure 3 shows the waveforms of the differential and common mode signal seen on a differential pair.

Figure 3. Differential Signaling



Ideally, routing a differential pair on a PCB should meet two criteria:

- The two traces should look the same from an electrical standpoint.

This means that each trace of the differential pair should have the exact same cross sectional dimensions and must be surrounded by the same type or types of dielectric materials. The dielectric spacing between the two traces should also be the same for the entire length of the trace. This is referred to as a symmetrical structure. Having a symmetrical structure results in a constant impedance for the difference signal. Asymmetries result in impedance discontinuities and cause a mode conversion from a differential signal to a common signal.

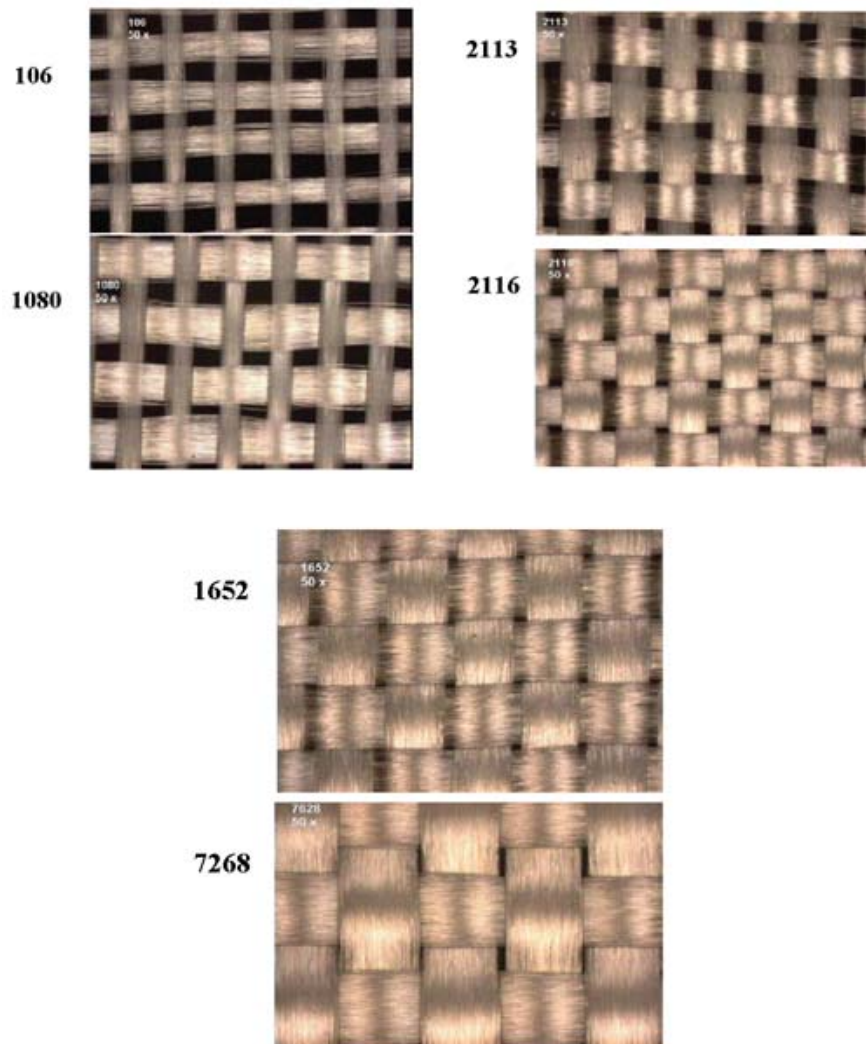
- The skew (time delay) between the two traces of the differential pair should be zero.

Electrically, make the total length of each trace exactly the same to ensure the skew between the two traces of the differential pair is zero. By doing this, edge of the difference signal is sharp and well defined. Any skew between the two traces causes the differential signal to convert into a common signal.

Dielectric Laminate Construction Background

Typical PCB dielectric (core/prepreg) substrates are constructed from various woven fiberglass fabrics strengthened and bound together with epoxy resin. The weaving technology is essentially the same for fiberglass as it is for any fabric. The warp yarn runs the length of the fabric roll, while the fill yarn runs the width. Figure 4 shows typical laminate weaves. The numbers next to each diagram identify the glass fabric style based on the fiberglass thickness, pitch, warp yarn, fill yarn, and the number of glass fiber strands used.

Figure 4. Different Types of Fiber Weaves



The glass and epoxy each have different relative permittivity (ϵ_r/D_k) values, thereby presenting a non-homogenous medium for signal propagation. Current FR-4 class PCB laminate materials and many high performance composite materials such as Nelco 4000-13SI, Rogers 4250B, among others, rely upon woven glass for strength and structural integrity.

The primary component of most fiberglass yarns is E-glass, S-glass, or NE-glass. E-glass or “electronic glass” is the most common in the fiberglass industry. This is the primary glass used in yarns that are used to construct fiberglass fabrics, and is the least expensive among the three. S-glass is generally used for non-electrical applications. NE-glass has improved electrical and mechanical performance over E-glass and is used in the Nelco 4000-13SI and N6000-21SI high-performance laminate product lines.

Table 1 shows the material property comparison between E-glass and NE-glass.

Table 1. Material Property Comparison between E-Glass and NE-Glass

| Property | E-Glass | NE-Glass |
|--|---------|----------|
| CTE (Coefficient of Thermal Expansion) – ppm/C | 5.5 | 3.4 |
| Dielectric Constant (Er) @ 1MHz | 6.6 | 4.4 |
| Dissipation Factor @ 1MHz | 0.0012 | 0.0006 |

NE-glass shows better temperature stability, lower Er, and lower loss than the equivalent E-glass. The reduced Er and dissipation factor yields important signal integrity benefits in high-speed signaling applications.

A laminate manufacturer layers the fiberglass fabrics of various styles (106, 1080, 2113, 2116, 1652, 7628, and so on) and fills them with cured epoxy to form core sheets, or fills them with semi-cured epoxy to form prepreg sheets. You can calculate the Er of any particular laminate with the following equation:

$$Er = Er(\text{epoxy}) \times \% \text{ of epoxy} / 100 + Er(\text{glass}) \times (1 - \% \text{ of epoxy}) / 100$$

where:

- Er (epoxy) is approximately 3.2 for FR4 class epoxy and 3.2 for low loss epoxy
- Er (glass) is approximately 5.6 for E-glass within the epoxy matrix and 4.4 for NE-glass

The nature of the epoxy/fiberglass mixture in a laminate changes with the style of the fiberglass used. The loose open weave of 1080 glass allows for a significant interstitial epoxy fill, compared to a denser weave such as 2116 or 7268.

For more information about the impact of PCB laminate weave, refer to Ref. 1 in “References” on page 18.



For more information about the selection of materials relating to PCB designs, refer to *AN 613: PCB Stackup Design Considerations for Altera FPGAs*.

Test Board

Altera developed a test board to study the various aspects of the high-speed channel design. This is an 8-layer board with four routing layers referencing different dielectric materials. It is a single-sided board with all the SMAs located on the top layer. Figure 5 shows the board stackup details.

Figure 5. Altera Test Board Stackup

| Lamination Stackup: | | Thickness and Tolerances: | | Base Material Rqmts: | | Dk @ |
|---------------------|------------------------|---------------------------|-------------------|----------------------|--------------|------|
| L#/Type | Description: | Cu+: | Laminate/PrePreg: | Type: | Description: | 1Ghz |
| 1 Sig | Core 0.0060 H/1 | .00060 | .0060 | | NP 4000-13 | |
| 2 Pln | | .00120 | | | | 3.71 |
| | Pre-Preg (1 x 2116) | | .0125 +/- 0.0013 | | NP 4000-13 | 3.79 |
| | Pre-Preg (1 x 2113) | | | | | |
| | Pre-Preg (1 x 2116) | | | | | |
| 3 Sig | Core 0.0060 1/1 | .00120 | .0060 | | NP 4000-13 | |
| 4 Pln | | .00120 | | | | 3.71 |
| | Pre-Preg (1 x 2113) | | .0036 +/- 0.0004 | | NP 4000-13 | 3.7 |
| | Filler Core 0.0210 0/0 | | .0210 | | NP 4000-13 | |
| | Pre-Preg (1 x 2113) | | .0036 +/- 0.0004 | | NP 4000-13 | |
| 5 Pln | Core 0.0060 1/1 | .00120 | .0060 | | NP 4000-6 | |
| 6 Sig | | .00120 | | | | 4.1 |
| | Pre-Preg (1 x 1080) | | .0120 +/- 0.0012 | | NP 4000-13 | 3.87 |
| | Pre-Preg (1 x 7628) | | | | | |
| | Pre-Preg (1 x 1080) | | | | | |
| 7 Pln | Core 0.0066 1/H | .00120 | .0066 | | Rogers 4350 | |
| 8 Sig | | .00060 | | | | 3.48 |

| | | |
|--|--|----------------|
| Target Post-Lam Thickness: 0.0850 +/- 0.0040 | | Stackup Notes: |
| Copper Oz Legend: H=1/2oz T=3/8oz Q=1/4oz E=1/8oz S=1/16oz | | |

As shown in Figure 5, this board uses three different cores (Nelco 4000-13, Nelco 4000-6, Rogers 4350) to allow for a comparison of the three different dielectric materials.

All the test structures on the board are routed to meet a 50 Ω ± 10% single-ended impedance or a 100 Ω ± 10% for differential impedance. To minimize conductor losses, wide trace widths were chosen to meet impedance targets. Table 2 shows the various trace widths chosen to meet the impedance targets.

Table 2. Trace Width Requirements on Altera Test Board (Part 1 of 2)

| Impedance Requirements | | Fin. Line | Ref Pin | 2nd Ref Pin | Target Desired Impedance | Impedance Tolerance | Actual Calculated Impedance | Diff Line Centers | Diff Line Space |
|------------------------|----------------------------------|-----------|---------|-------------|--------------------------|---------------------|-----------------------------|-------------------|-----------------|
| L# | Impedance Type | | | | | | | | |
| 1 | SE - Coated Microstrip | .00950 | 2 | — | 53.00 Ω | ± 10% | 53.59 Ω | — | — |
| 1 | DIF - Coated Microstrip Edg Cpld | .00950 | 2 | — | 100.00 Ω | ± 10% | 99.55 Ω | .024 | .0145 |
| 1 | SE - Coated Microstrip | .01075 | 2 | — | 50.00 Ω | ± 10% | 50.27 Ω | — | — |
| 3 | SE - Stripline | .00750 | 4 | 2 | 51.00 Ω | ± 10% | 50.87 Ω | — | — |
| 3 | DIF - Stripline Edg Cpld | .00750 | 4 | 2 | 100.00 Ω | ± 10% | 100.10 Ω | .026 | .0185 |
| 6 | SE - Stripline | .00700 | 5 | 7 | 51.00 Ω | ± 10% | 50.84 Ω | — | — |
| 6 | DIF - Stripline Edg Cpld | .00700 | 5 | 7 | 100.00 Ω | ± 10% | 100.27 Ω | .026 | .019 |
| 8 | SE - Coated Microstrip | .01050 | 7 | — | 55.00 Ω | ± 10% | 55.18 Ω | — | — |

Table 2. Trace Width Requirements on Altera Test Board (Part 2 of 2)

| Impedance Requirements | | Fin. Line | Ref Pin | 2nd Ref Pin | Target Desired Impedance | Impedance Tolerance | Actual Calculated Impedance | Diff Line Centers | Diff Line Space |
|------------------------|----------------------------------|-----------|---------|-------------|--------------------------|---------------------|-----------------------------|-------------------|-----------------|
| L# | Impedance Type | | | | | | | | |
| 8 | DIF - Coated Microstrip Edg Cpld | .01050 | 7 | — | 100.00 Ω | $\pm 10\%$ | 100.69 Ω | .024 | .0135 |
| 8 | SE - Coated Microstrip | .01250 | 7 | — | 55.00 Ω | $\pm 10\%$ | 50.36 Ω | — | — |

Dielectric Material Selection

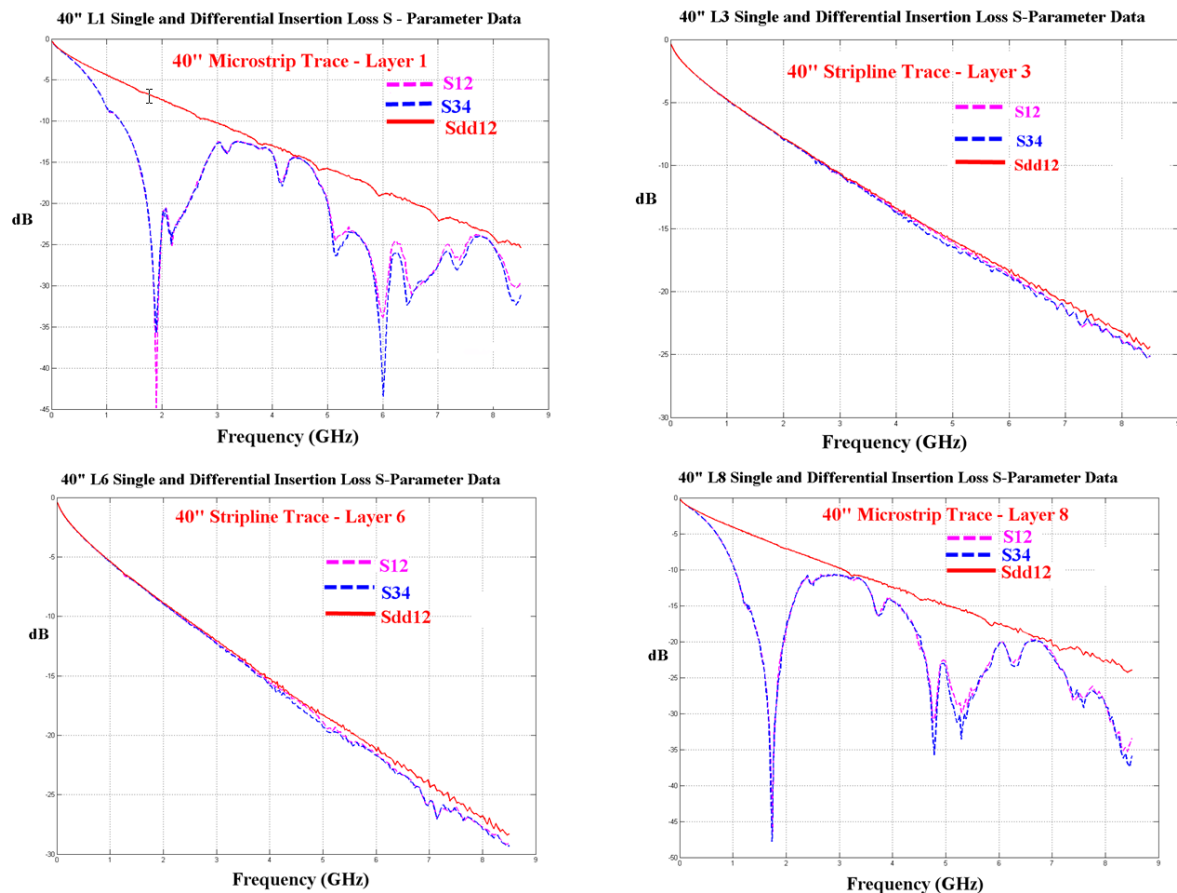
To test the performance of various dielectric materials, two identical differential pairs of 25" and 40" are routed on Layer 1, Layer 3, Layer 6, and Layer 8. The signal vias on Layer 3 and Layer 6 are backdrilled to remove unwanted stubs. Ground return vias next to the signal vias provide an optimal return path. [Table 3](#) provides the dielectric constant and loss tangent/dissipation factor for the various dielectric materials.

Table 3. Er and Dk Values for Various Dielectric Materials

| Material | Dielectric Constant (Er/Dk) | Dissipation Factor (Df) |
|------------------|-----------------------------|-------------------------|
| Nelco 4000-6 | 4.1 @ 1 GHz | 0.022 @ 1 GHz |
| Nelco 4000-13 EP | 3.7 @ 1 GHz | 0.009 @ 1 GHz |
| Rogers 4350B | 3.48 @ 10 GHz | 0.0037 @ 10 GHz |

To get consistent and repeatable results, all the test structures are designed with high-performance SMAs on the top layer of the board. Four port VNA and time-domain reflectometer (TDR) measurements are used to study the performance of the various dielectric materials. Figure 6 shows a snapshot of the measured single-ended insertion loss (S12/S34) and the extracted differential insertion loss (Sdd12) for the 40'' trace. Similar behavior is also observed for the 25'' trace on the various layers.

Figure 6. 40'' Single and Differential Insertion Loss Data



From the single-ended S-parameter measurements, the 40'' microstrip traces on Layer 1 and Layer 8 show resonance behavior (valleys in the single-ended S-parameter measurements), whereas the stripline 40'' traces on Layer 3 and Layer 6 show an expected monotonic (loss increases as a function of frequency and length) profile.

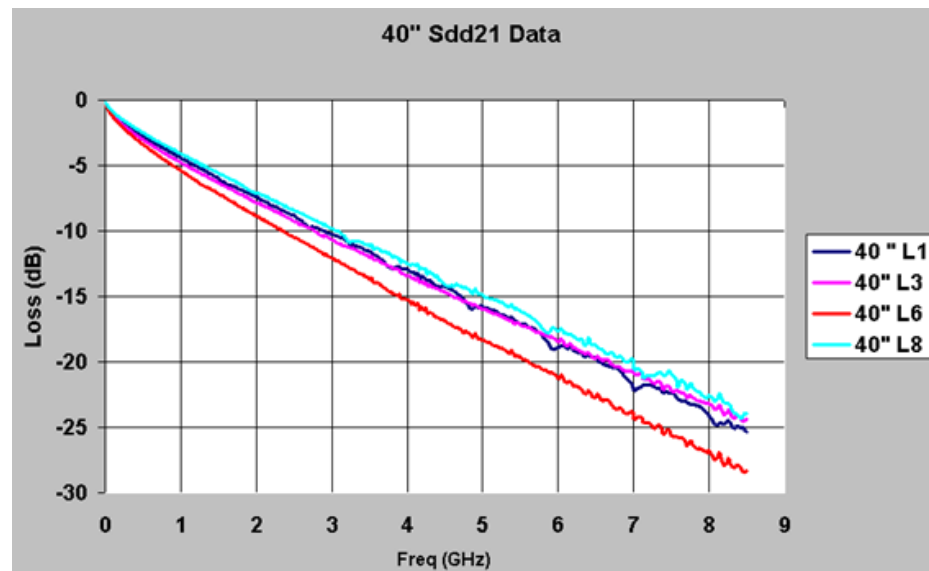
The resonance behavior in the loosely coupled microstrip traces is due to the difference in the propagation speed of the common and differential signals on microstrip traces during the four port S-parameter measurements. In stripline traces, this behavior is not seen due to the homogenous medium that a signal sees when propagating down the trace. When there is no coupling, the differential and common

signals travel at the same speeds and there is no transfer of energy from one trace to the other. As coupling increases in the microstrip traces, energy is coupled back and forth between the two traces as the signal propagates. The length to get the full coupling from one trace to the other trace depends on the difference in propagation speed and the phase difference between the differential and common signals.

This effect is the reason for the far end noise on the loosely coupled microstrip traces, rather than on stripline traces. This is not an issue if you plan to use the traces for sending a differential signal. If you use the traces to send single-ended signals, the result will be excessive crosstalk noise on the far end. Sources with an in-depth analysis of this behavior can be found in Refs. 3 and 4 in “References” on page 18.

Figure 7 is a comparison of the differential insertion loss (Sdd12) extracted from the single-ended S-parameter data shown in Figure 6 for the 40” traces on L1, L3, L6, and L8.

Figure 7. 40” Differential Insertion Loss (Sdd21) Data Comparison



The trace on Layer 8 shows the best performance because Rogers 4350B has the lowest Df. The microstrip and stripline traces on Layer 1 and Layer 3 show the next best performance because they reference a Nelco 4000-13 dielectric material (medium Df). As expected, the trace on Layer 6 shows the worst performance because it references Nelco 4000-6 material (high Df) on one side and Nelco 4000-13 (medium Df) on the other side. Most of the return currents for the trace on Layer 6 is on Layer 5 rather than on Layer 7, due to the difference in the thickness of the Nelco 4000-6 core (6 mil), compared to the Nelco 4000-13 pre-preg (12 mil). Similar behavior is observed on the 25” traces.

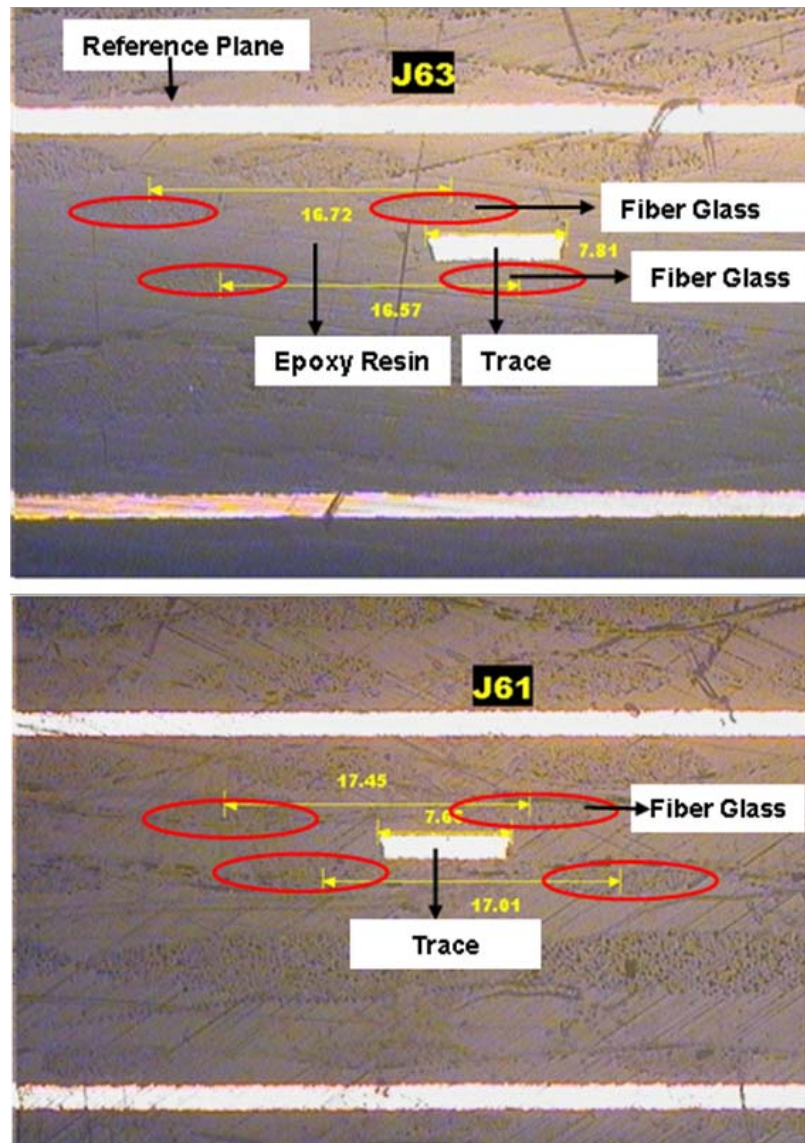
For cost sensitive designs, Altera recommends that you use Nelco 4000-6, regular FR4 type of substrates, and take a performance loss of about 2 dB compared to expensive substrates. You can use the built in pre-emphasis and equalizer settings in the transceivers available in the Stratix II GX or Stratix IV GX devices to compensate for some of the channel loss as the signal traverses through the backplane.

For the current edge rates (tens of ps) needed to output a 6.375 Gbps and higher signal, you can gain the optimal solution (price vs. performance) by moving from a regular FR4 substrate to a mid-performance substrate such as Nelco 4000-13, Isola FR408, or GETEK. The cost difference is relatively small ($1.25 \times$ the cost of regular FR4 type material) compared to moving to a high-performance Rogers 4350B type of material (approximately $5 \times$ or greater depending on the number of cores per board).

Fiber Weave Effect

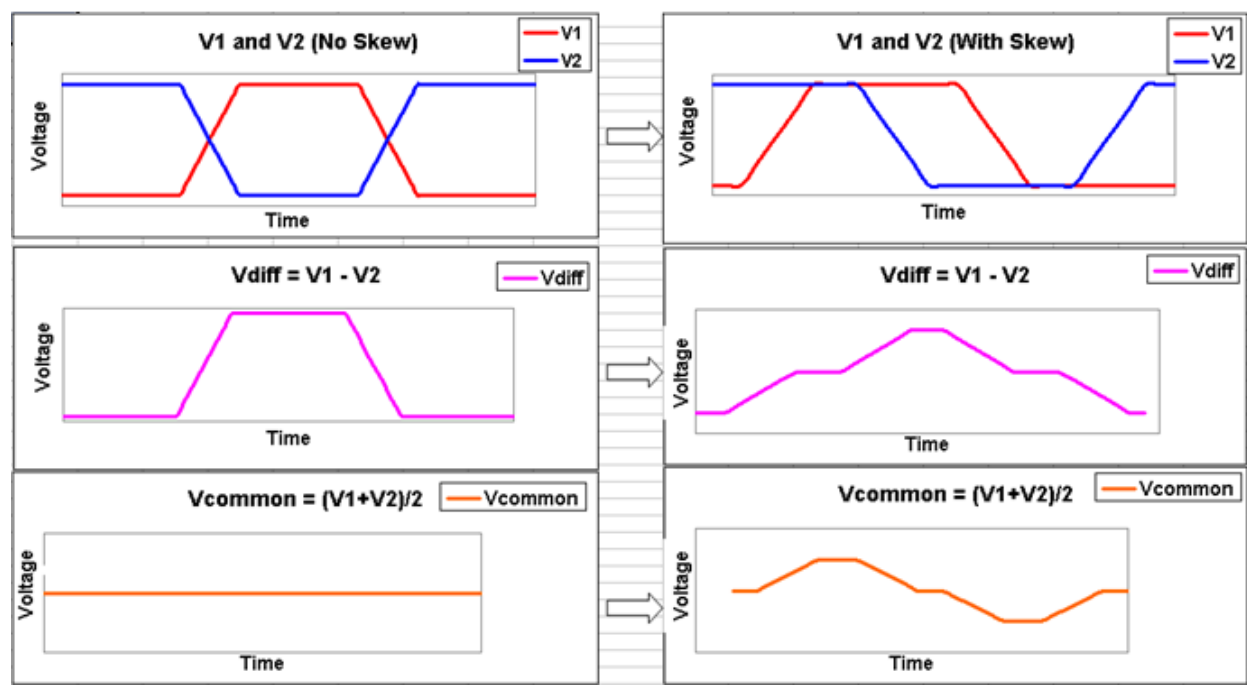
PCBs usually route traces in multiples of 90° angles. The routed trace can land directly on top of the warp yarn, top of the fill yarn, centered between the strands of warp yarn, or centered between the strands of the fill yarn. [Figure 8](#) is a microscopic view of single-ended traces taken from the test board that Altera has developed specifically for this purpose.

Figure 8. Microscopic Cross Section of Test Board



The trace on top directly lands on the weave. The trace on bottom lands on the epoxy resin. Assuming that the two traces make up the two legs of the differential pair (P and N), they see two different dielectric constant (ϵ_r) values. This in turn results in different propagation velocities and loss profiles. At high data rates, the difference in propagation velocities leads to skew between the two legs of the differential pair. Depending on the data rate, it can amount to a substantial fraction of the unit interval (UI). The skew between the P and N legs result in a common mode voltage and degradation of the differential signal. Figure 9 shows the effect of skew on a differential and common mode signal

Figure 9. Skew Due to Fiber Weave



Fiber Weave Effect Observed on the Test Board

On the Altera test board, four identical 8" straight traces were routed in parallel on Layer 3. The pitch between the traces was chosen to be a multiple of $1.5 \times$ the assumed glass pitch for 2116, as seen in the following equation:

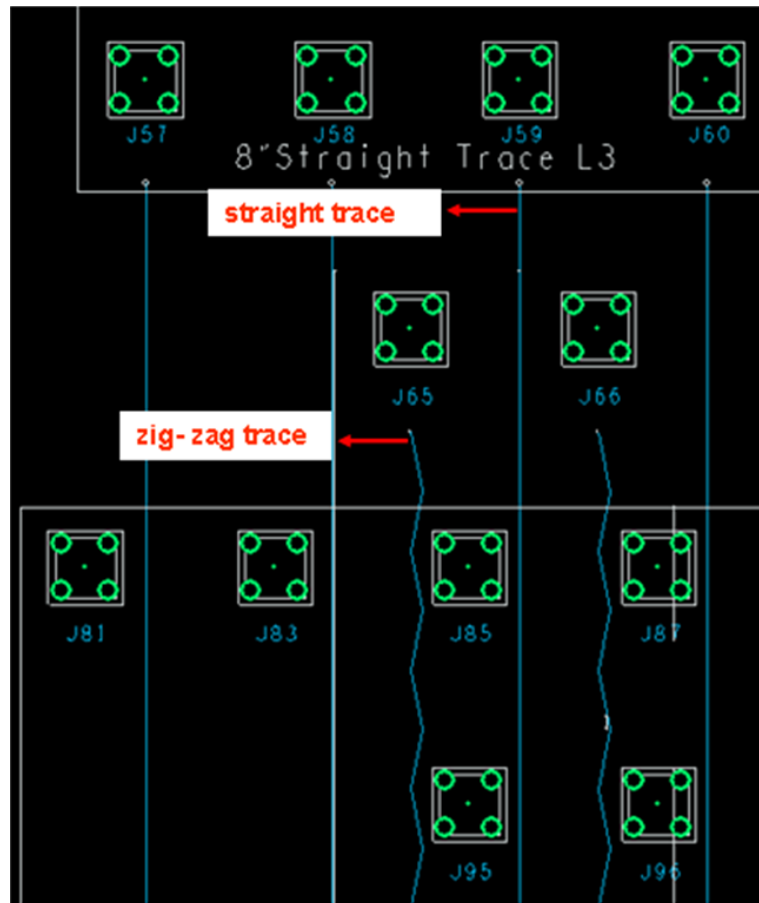
$$D = 1.5 \times K \times P$$

where:

- D = Distance
- K = any integer
- P = Pitch of 2116

Two zig-zag traces of the same length as the straight traces were also routed on Layer 3. The zig-zag traces were intended to compensate for any fiber weave effect because the trace is routed on and off weave repeatedly. The distance from the SMA locations to the via transitions from Layer 1 to Layer 3 was the same for both the straight and zig-zag traces, as shown in Figure 10.

Figure 10. Zig-Zag and Straight Trace Routing



Several TDR measurements were done to observe for any skew differences among the straight traces. The TDR was calibrated with just the cables to within 1 ps to avoid an offset when launching the pulse into the SMA. Figure 11 through Figure 13 show the TDR snapshots for calibration, skew between a pair of straight traces, and skew between the two zig-zag traces on Layer 3.

Figure 11. TDR Calibration

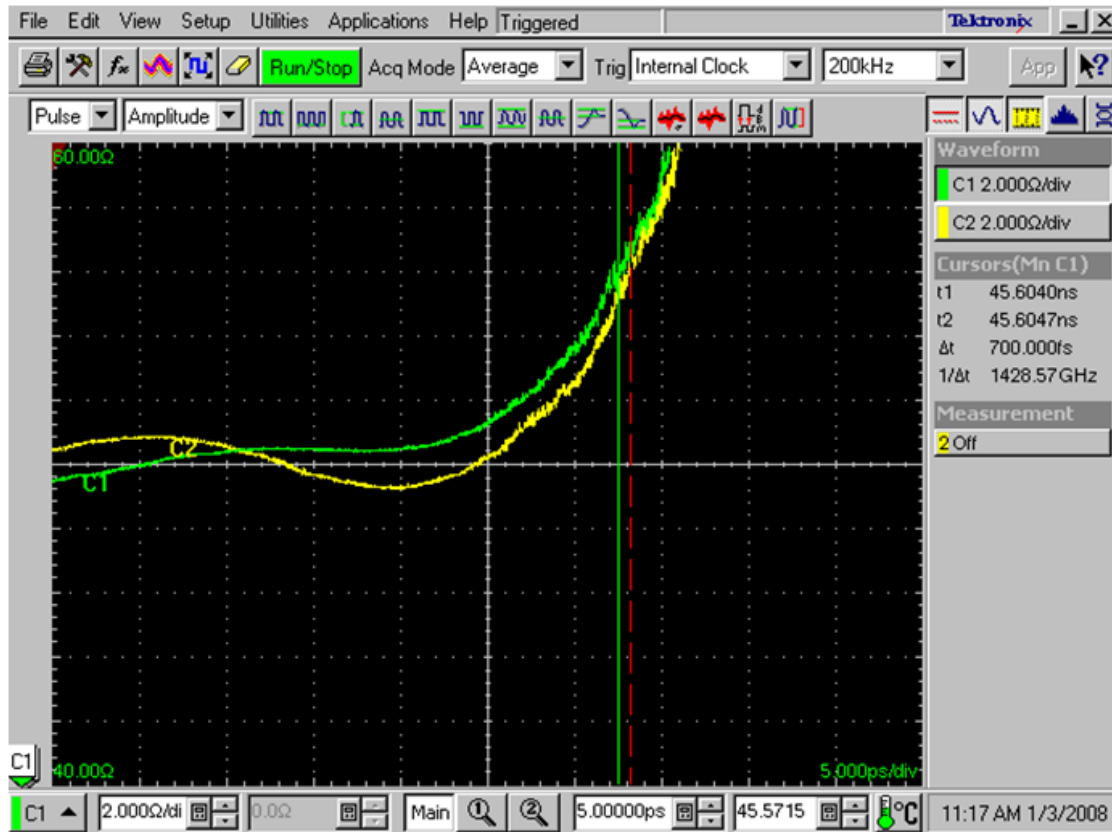


Figure 12. Skew Observed on Straight Traces

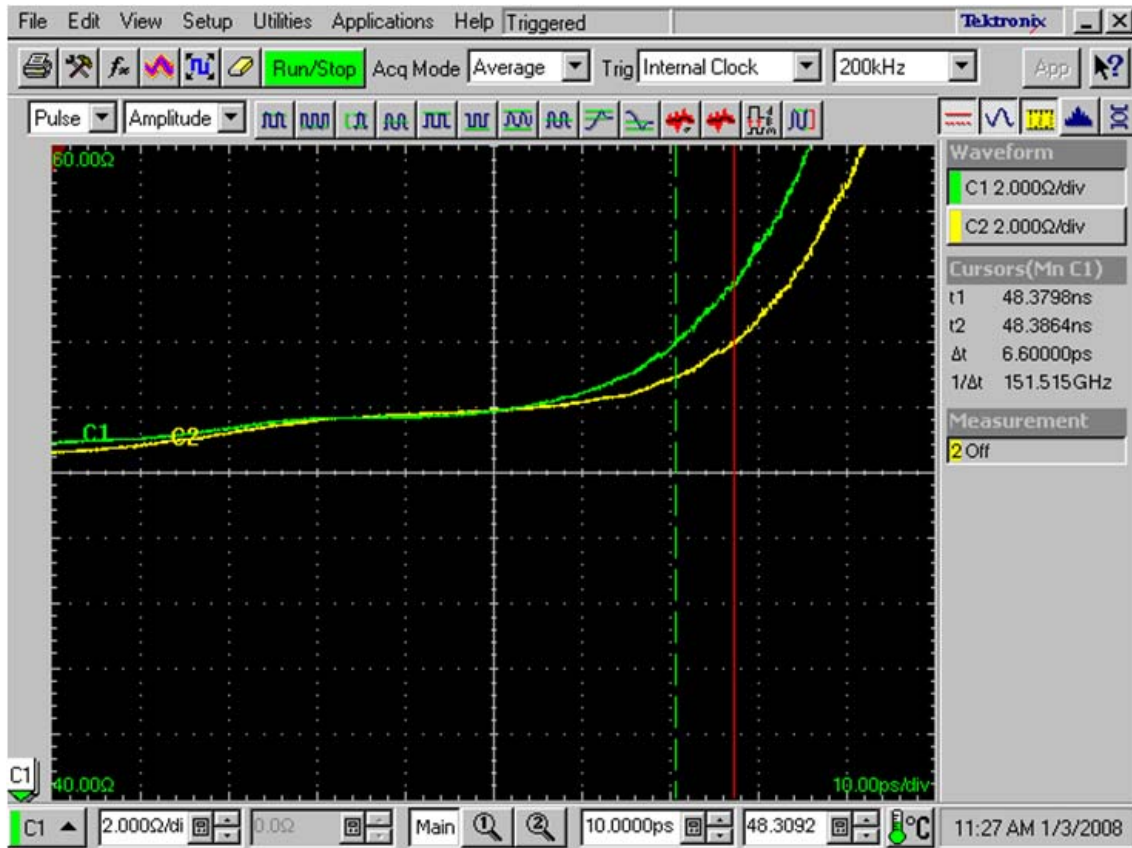


Figure 13. Skew Between Zig-Zag Traces



Measurements done on a different board revealed more skew (14 ps) between the straight traces on Layer 3. There was also some expected amount of skew observed between the two zig-zag traces. If a statistically significant number of measurements were taken, the expectation is that the amount of skew seen from the zig-zag traces will be much smaller compared to the skew observed from the straight traces. Refer to “References” on page 18 for additional data based on the work done at Intel Corporation, Sun Microsystems, and Teraspeed Consulting Group. The amount of skew observed on the Altera test boards was not as significant as some of the data cited in the references for the following reasons:

- The test board uses a dense weave (2116) rather than a sparse weave such as 106 or 1080 where this effect is predominant.
- Nelco 4000-13 laminates use NE-glass rather than the default E-glass. The dielectric constant for NE-glass is lower than E-glass; hence, the difference in ϵ_r between resin and glass is low, which leads to less skew.
- The traces that were routed on the board might not have the worst-case alignment with respect to weave (high ϵ_r) and epoxy resin (low ϵ_r).
- For identical dielectric materials, wider traces in general show less susceptibility to fiber weave skew compared to narrow traces. The traces on Layer 3 were routed with a wide (7.5 mil) trace width to achieve a nominal impedance of 50 Ω

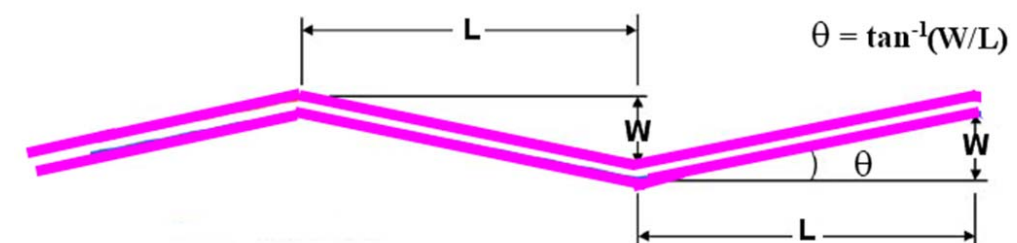
Altera recommends that you pay close attention to the skew associated with fiber weave effect. For high-speed data rates of 6.375 Gbps and above, this skew significantly cuts into the available UI budget and leads to a reduction in the observed eye width at the receiver.

Mitigation Techniques

Various techniques are available to mitigate the skew associated with the fiber weave. You can find an exhaustive list of the techniques in the resources listed in “References” on page 18. Some of the basic techniques that can be done during layout are as follows:

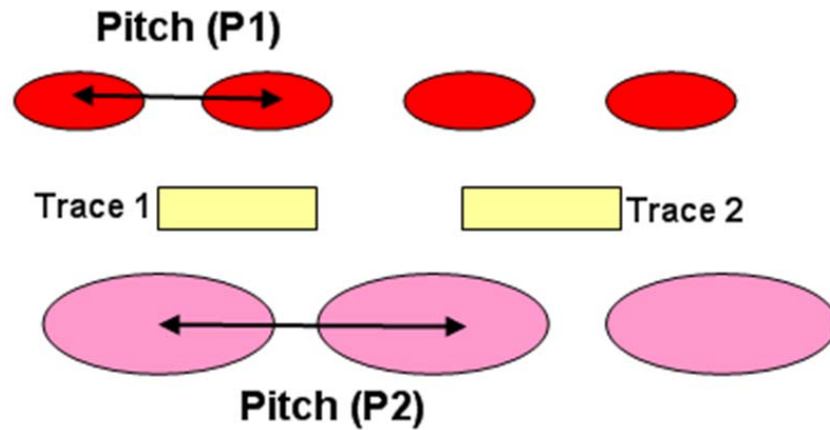
- Use wider trace widths rather than narrow trace widths to achieve your impedance targets. The drawback associated with this approach is the increase in board real estate required to route all the traces with wider geometries compared to narrow trace geometries.
- If the flexibility exists, specify a denser weave (2116, 2113, 7268, 1652) compared to a sparse weave (106, 1080).
- For marginal cost increase (1.25×) relative to FR4 (×), move to a better substrate such as Nelco 4000-13 substrate made of NE-glass (lower E_r) compared to the regular E-glass (higher E_r).
- Do the floor planning on the board in such a way that the routing ends up being at an angle rather than orthogonal.
- Make use of zig-zag routing. The trace can be routed so that it traverses a minimum of 3 times the fiberglass pitch ($W \geq 3 \times \text{glass pitch}$) before reversing the direction of routing. The drawbacks associated with this approach is the increase in board real estate along with the difficulty associated with routing at arbitrary routing angles other than the typical 0° , 45° , and 90° angles that CAD tools support. Figure 14 shows a schematic representation of the zig-zag routing.

Figure 14. Zig-Zag Routing



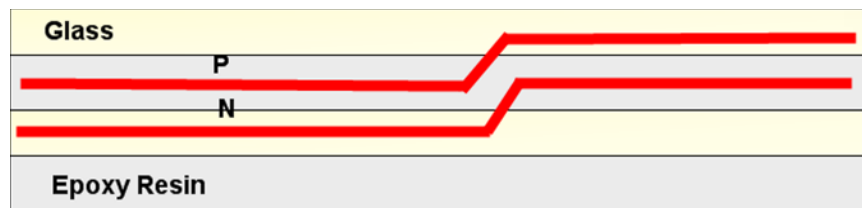
- For strip line traces, use two different weaves with different pitches for top and bottom substrates to average out the effect, as shown in Figure 15.

Figure 15. Weaves with Different Pitch



- Offset traces by the intra-pair spacing forcing each trace onto the path that its neighbor was on irrespective of the glass pitch, as shown in Figure 16.

Figure 16. Jogged Routing



Conclusion

Designers should pay close attention to the layout and the dielectric materials in the PCB design. At high frequencies, dielectric loss is dominant, and is dependent on the dissipation factor (loss tangent) for a given dielectric material. The orientation of the trace with respect to the glass weave determines the amount of skew seen, due to the fiber weave glass pattern. This application note briefly explains the dielectric loss and fiber weave skew that designers require when routing high-speed channels, and concludes by offering key recommendations to mitigate the skew due to fiber weave.

References

1. *DesignCon 2005: The Impact of PCB Laminate Weave on the Electrical Performance of Differential Signaling at Multi-Gigabit Data Rates* by Scott McMorrow (Teraspeed Consulting Group) and Chris Heard (Teradyne Connection Systems)
2. *DesignCon 2007: Fiber Weave Effect: Practical Impact Analysis and Mitigation Strategies* by Jeff Loyer, Richard Kunze, and Xiaoning Ye from Intel Corporation

3. *DesignCon 2007: Losses Induced by Asymmetry in Differential Transmission Lines* by Gustavo Blando, Jason R Miller, and Istvan Novak from Sun Microsystems
4. *Signal Integrity Simplified* by Eric Bogatin

Document Revision History

Table 4 shows the revision history for this document.

Table 4. Document Revision History

| Date | Version | Changes |
|--------------|----------------|-----------------------|
| January 2011 | 1.1 | Added link to AN 613. |
| May 2008 | 1.0 | Initial release. |

