

# ATLAS TDAQ RoI Builder and the Level 2 Supervisor system

**R. E. Blair, J. Dawson, G. Drake, W. Haberichter, J. Schlereth,  
M. Abolins, Y. Ermoline, B. G. Pope**

## **Acknowledgements:**

**David Francis, Stefan Haas, Markus Joos, Per Werner**

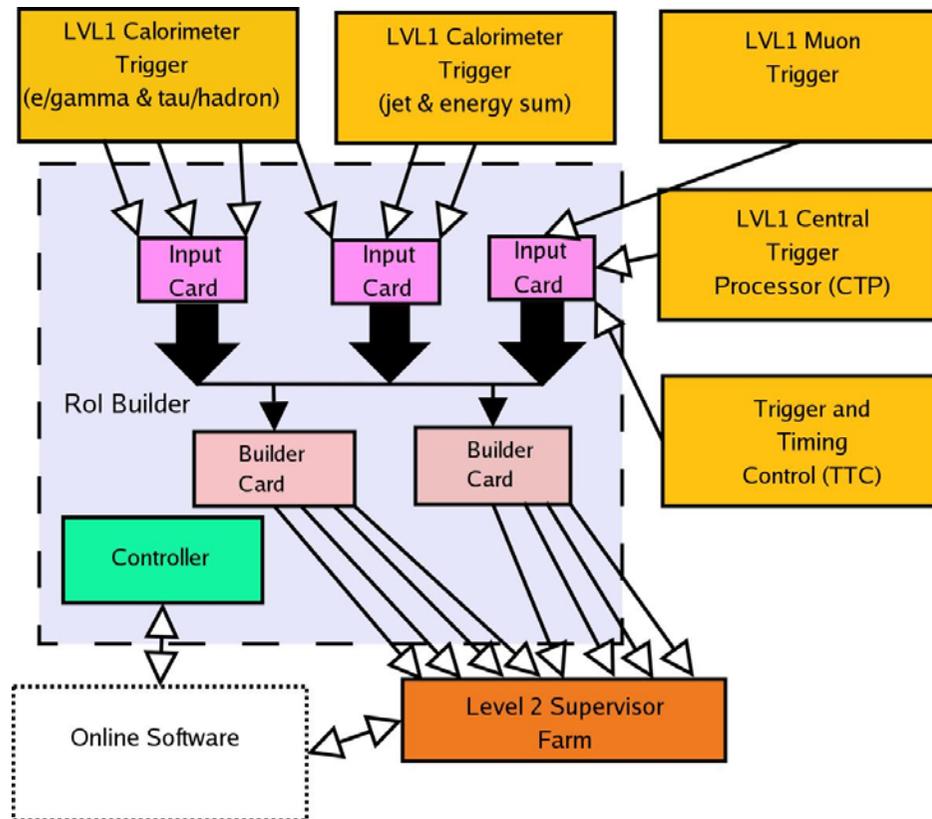
**12th Workshop on Electronics for LHC and future Experiments,  
25-29 September 2006, Valencia SPAIN**

## Region of Interest concept

---

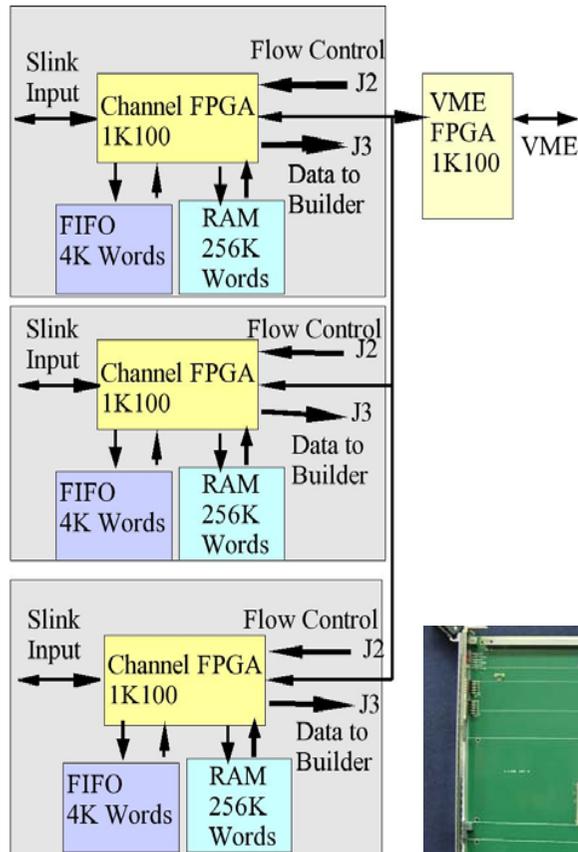
- The Level 1 Trigger system (LVL1) identifies a number of Rols for the HLT - spatially limited areas ('roads') in the detector
- The information from Level 1 includes the selected trigger type and the details of where in  $\eta$  and  $\phi$  the trigger objects are located
- Using this information as guidance, HLT processors request a subset of the event data from the ROSs to perform the event selection.
- In this way only a few per cent of the event data need to be transferred initially to the HLT system — thus considerably reducing the network bandwidth required
- The Region of Interest Builder (RoIB) takes raw event fragments from various Level 1 Trigger sources and assembles all the fragments of a given event into an Rol record
- The Level 2 Supervisor (L2SV) receives the Rol records and distributes them to HLT processors that require it for further event selection and disposition.

# RoIB/L2SV system overview



- VMEbus system
- The input stage consists of Input Cards that receive and buffer the RoI fragments
- The Builder Cards in the assemble the RoI fragments into RoI records
- The Single Board Computer (SBC) for the purposes of configuration, control and monitoring
- ATLAS standard S-LINKs for inputs and outputs
- 4 Input Cards, 4 Builder Cards and 16 L2SVs

# RoIB Input Card



- All transfer from the Input Cards to the Builder cards is via J3 high density 250 pin connector and a custom backplane

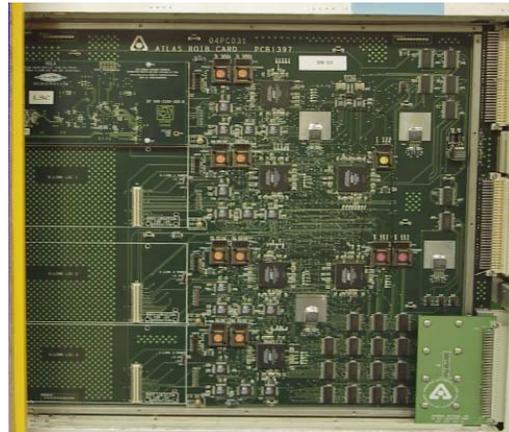
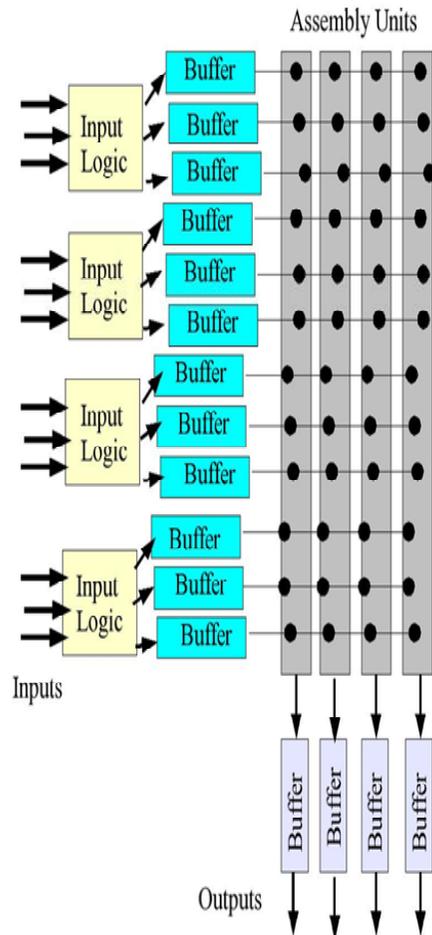
- Several modes of operation:

- Diagnostic Run Mode
- Sniffer Mode
- No Sniffer Data Mode



- Data from the FIFO are parsed, formatted into two 20 bit words, and transferred to the Builder Cards
- The flow control signals are transferred via User Defined pins on J2.

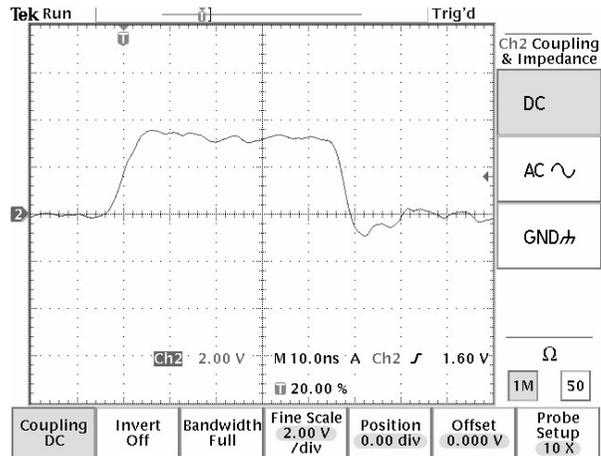
# RoIB Builder Card



- The Level 1 information required for the HLT system is the concatenation of all RoI fragments for an event (RoI record)
- The subsystem on the Builder Card that builds the RoI record is the Assembly Unit
- The Input Cards pass RoI fragments to a set of Builder Cards using round robin algorithm

- The hardware is set to deal automatically with the number of cards, number of channels number of L2SVs, etc.
- Flow Control between the input buffer in the Builder Card and the Input Card

# RoIB custom backplane

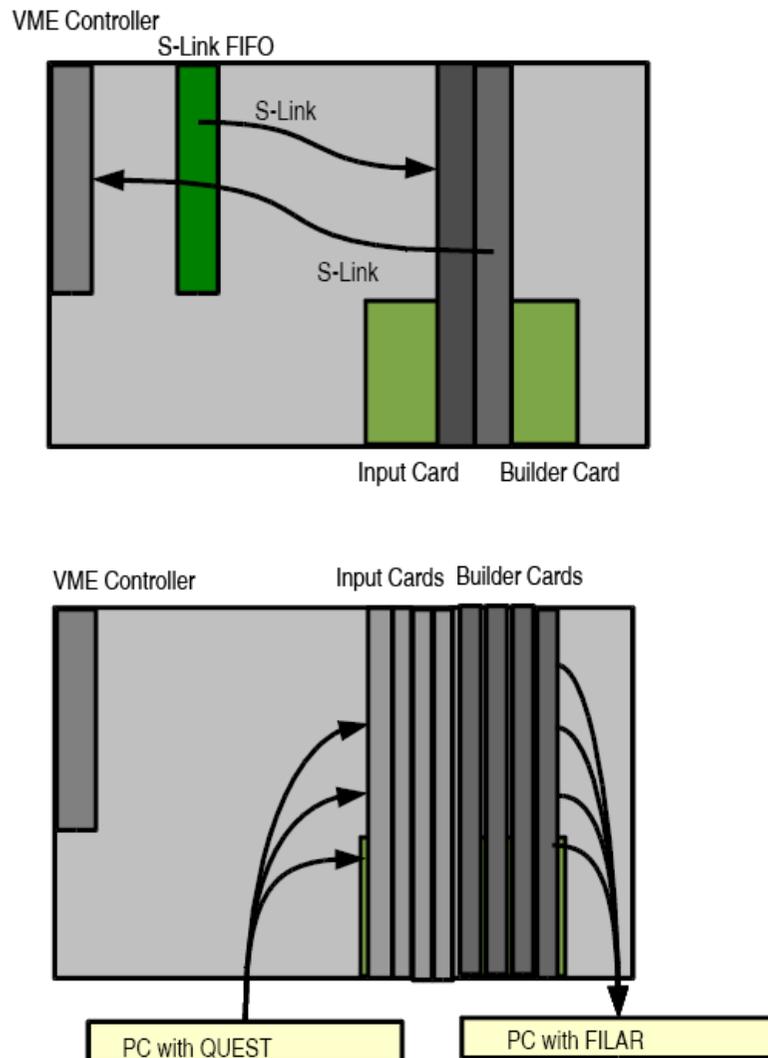


- Signals are carried via a custom backplane at 3.3 volt logic levels.
- Special attention is paid in the custom backplane to avoiding crosstalk:
  - reduced the clock frequency (20 MHz)
  - limiting the number of Builder Cards to 4



- In order to check possible transmission errors, a checksum is generated in the Input Cards on each fragment, transferred to the Builder Card, and compared with a checksum being generated.

# RoIB standalone tests



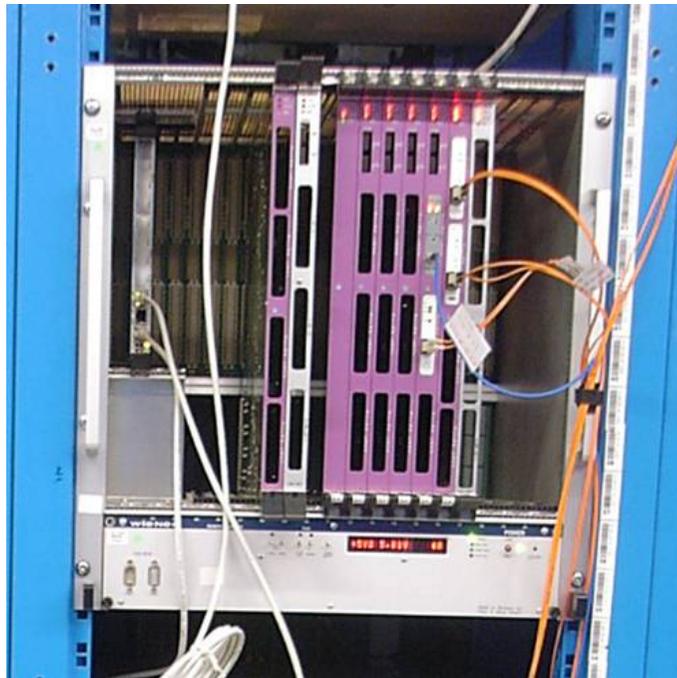
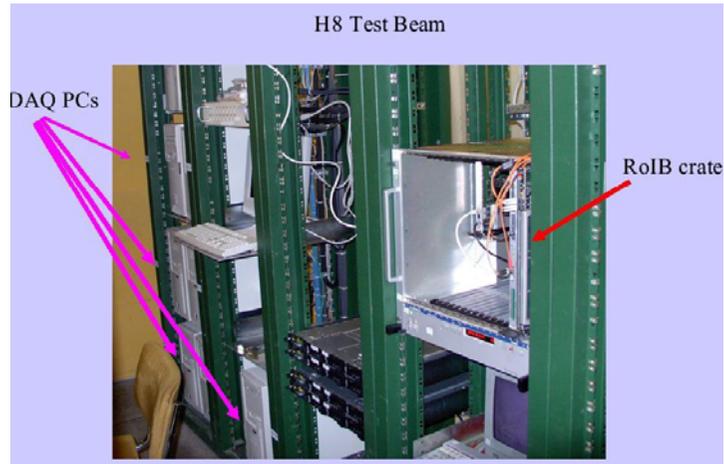
- A VME is used as a Controller in the RoIB crate
- It allows two levels of testing of the RoIB
- Basic single card initial checkout
  - **Input Card**
    - ⇒ single S-Link to sniffer RAM test
    - ⇒ write/read RAM test,
  - **Builder Card**
    - ⇒ spy FIFO
    - ⇒ single S-Link output
- Multi-card integrated checkout
  - **use external PCs for data sources/sinks**
  - **3 levels of complexity**
    - ⇒ spy FIFO (requires no external sources/sinks)
    - ⇒ check readout (requires external sink)
    - ⇒ check readout with external data source and external sink, sample monitoring data

## L2SV processor farm

---

- The Level 2 Supervisor farm - up to 16 commercial rack mounted PCs
- Connected to the RoIB via ATLAS standard SLINKs and to the High Level Trigger – via Ethernet
- Each PC is equipped with FILAR card - quad S-LINK LDCs to PCI Interface.
- Each processor in the farm is responsible for distributing RoI records to the HLT processors farm and effectively managing the processing resources of the HLT farm via a load balancing algorithm.
- It receives the final decision on an event based on the result of the HLT processor.
- The decision results are communicated to the Data Flow Manager (DFM) so that accepted events can be further analyzed and rejected events can be flushed from the Readout System .

# RoIB integration tests and commissioning



- Initial test of the small RoIB system (one input and one builder board) was in H8 test beam, it was integrated with Level 1 Trigger outputs from muon calorimeter trigger.
- The RoIB installed recently in USA15 underground counting room contain 4 Input Cards and 3 Builder cards,
- 2 L2SV processors are used in the SDX1 counting room.
- The size of the L2SV farm will be supplemented according to need determined by the increasing event rate during commissioning.