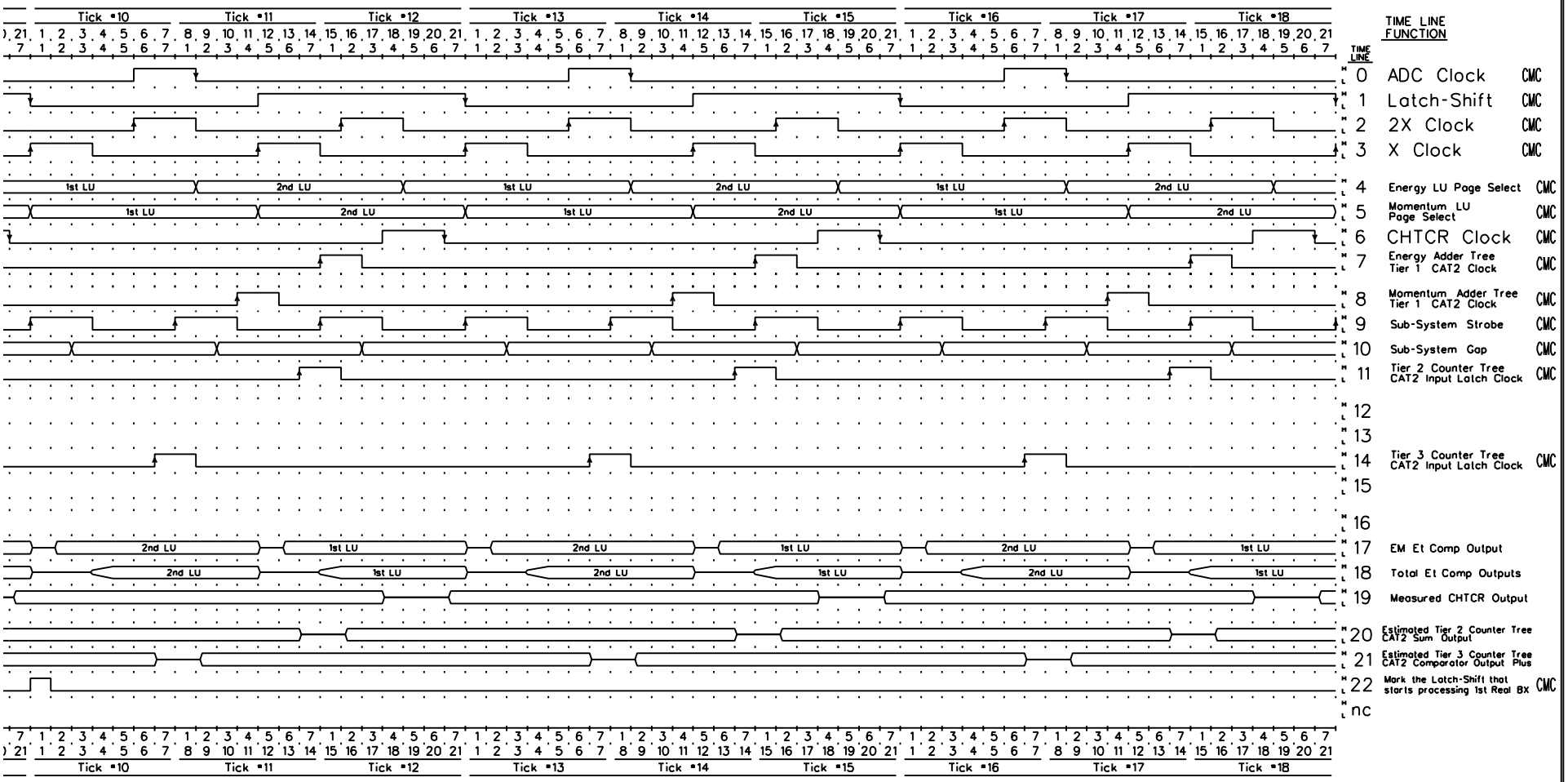
Calorimeter Trigger Tier 1 and Counter Tree Timing Diagram



in the Cal_Trig_Readout_Helper FPGA, the ERPB_Input_Clk
l_Tot_Clk actually occur about 20 nsec later, with respect
2, and Tier 3 signals, than shown in this diagram.

Because of Cable, FanOut, and MBD Delays in the Timing & Control Signals to Tier 1, Tier 2 and Tier 3, the outputs from Tier 1, Tier 2, and Tier 3 are really about 50 nsec later, with respect to Sub System Strobe, than shown in this diagram.

CMC → Generated by Carmen Master Clock on the Indicated Time Line

Date: 11-OCT-02