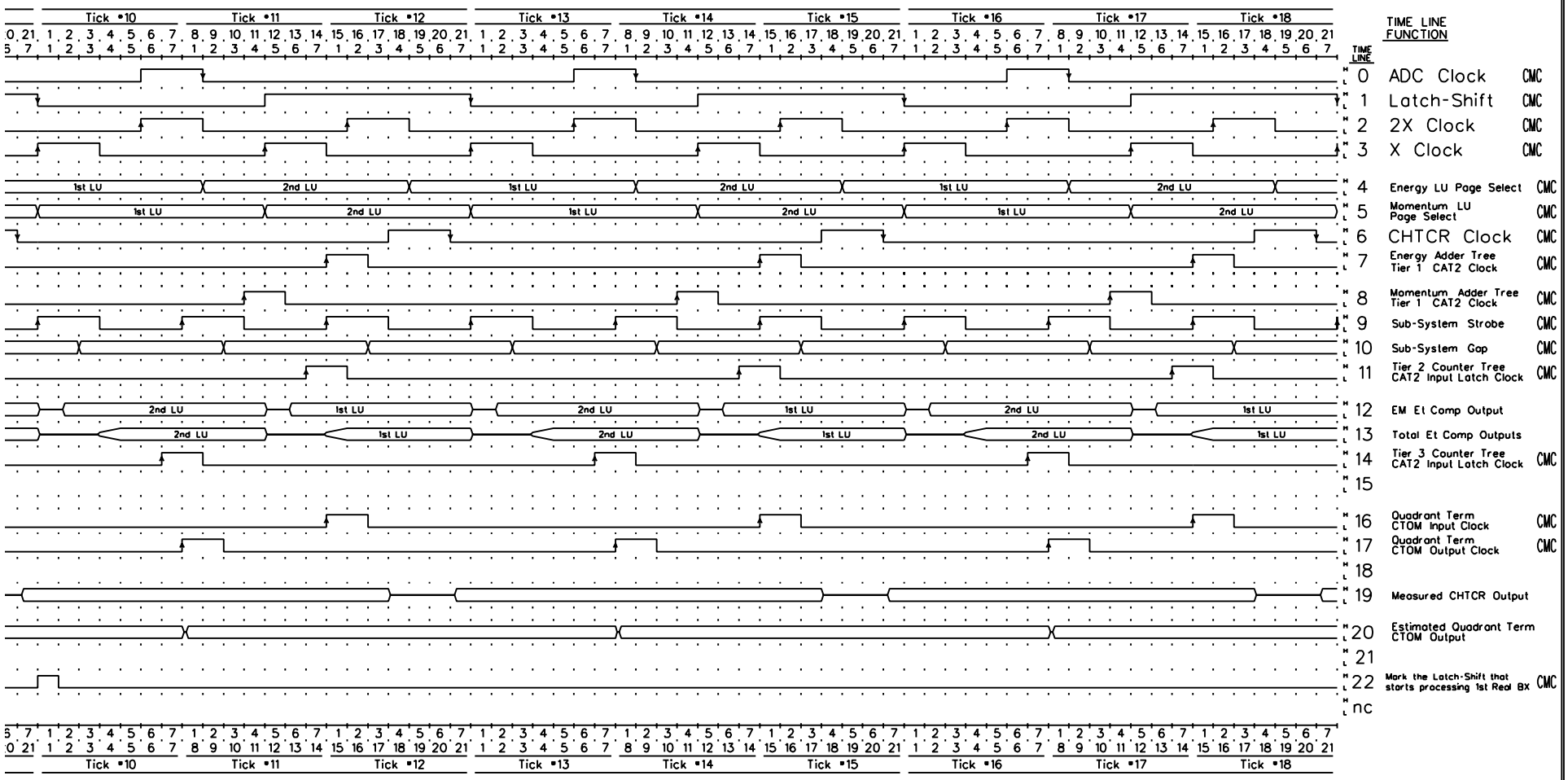
# Calorimeter Trigger Tier 1 and Quadrant Term Timing Diagram




y in the Cal_Trig_Readout_Helper FPGA, the ERPB_Input_Clk
M_Tot_Clk actually occur about 20 nsec later, with respect
er 2, and Tier 3 signals, than shown in this diagram.

Because of Cable, FanOut, and MBD Delays in the Timing & Control Signals to Tier 1, Tier 2 and Tier 3, the outputs from Tier 1, Tier 2, and Tier 3 are really about 50 nsec later, with respect to Sub System Strobe, than shown in this diagram.

CMC → Generated by Carmen Master Clock on the Indicated Time Line

Date: 23-DEC-03

Clock to new stable output logic delay is about 30 nsec more in Tier 3 than in the M101 CTOM.

The Cable Delay for T&SS to reach the Quadrant Term CTOM card in Rack M101 is less than the Cable, FanOut, and MBD Delays for T&SS to reach the Tier 1 crates by about 54 nsec.
On the other hand, once on the CTOM card the P1_TS's are delayed by the BSF FPGA for about 30 nsec.

The cable delay from the Quadrant Term CTOM Card Output to the patch panel that carries L1 Cal Trig And-Or Terms to the TFW is about 35 nsec longer than for the cables that carry Tier 3-4 signals to this patch panel.