## Work on the Level 1 Calorimeter Trigger that is Currently Under Way

D-Zero Trigger Workshop Presented by D. Edmunds 22-APR-2002

- Work on the CTFE cards at SiDet
  - Hardware work on the 320 CTFE cards
    - \* ReWork the Trigger Pick Off Signal Analog Input Section
    - $\ast\,$  Install the Term-Attn-Brd's
    - \* Instructions are on the Web
    - $\ast\,$  Will finish this work in 2 to 3 weeks
  - PROM re-programming 5,120 lookup PROM's
    - \* PROM data files are ready for checking
    - \* Programming and Verification a combination of SiDet and LaPaz
- Timing and Control Signal: Generation, FanOut, Cabling
  - Requirements for normal operation and for Tester Exerciser
    - \* TCC control of what Lookup Memory Pages are used per rack pair
    - \* Different signals require different processing for Tester Exerciser
  - Setup for operation at 396 nsec
    - \* Not doing work to operate at 132 nsec at this time
    - \* All work being done supports 132 nsec operation
  - Sequencer No. 2 and Calorimeter Trigger Timing Helper
    - \* Designs similar to what is used for testing Trigger Framework
- Work on Tier's 2 and 3
  - Need to start running Tier 3
    - \* With next pair of racks operation will require Tier 3
    - \* See http://www.pa.msu.edu/hep/d0/ftp/run1/l1/drawings/ for the layout
  - Generation of Global L1 Cal Trig And-Or Terms
    - \* How much eta coverage is needed before missing Et is of use
    - \* Should be using the CTRO but can probably skip it for initial operation
- Readout system work
  - Header/Trailer for L2
  - Seed Masks for L2
  - "Monitor Capture" of the readout data

- \* The above 3 items require work on the Bougie FPGA
- \* Modern, big, easy to work on design
- Speed up by a factor of 2
  - \* Should be straight forward to get to 6 or 7 usec.
- Readout data besides the Trigger Tower related quantities, CTRO cards
  - \* Only functional description and design sketch exist
  - $\ast\,$  Not hard to work on
  - $\ast\,$  Needed for full rational operation
- DeBug the BLS cabling and bad channel issues
  - Lots of problems and different types of problems
    - \* Cables, Hybirds, Connectors
  - Need to keep track of information
  - Need to be able to make quick pulser runs
    - \* Debug problems
    - \* Periodic verification that all is OK for Physics operation
- Routine Cal Trig Operation
  - Need to start running the Power Supply Voltage Monitoring
    - \* Hardware is ready
    - \* Documented what is plugged in where
  - Repair of Power Supplies
    - \* 3 of the 4 types are still supported
    - $\ast\,$  The unsupported type can be replaced
  - ReStart the full cooling system
    - \* Speed up the air blower
    - $\ast\,$  Drip detection is on in all racks
- How well is the L1 Cal Trig Working ?
  - Study the Calibration and Resolution
  - Monitor and Study the Triggers turn on curves and such
- Control Software Work

L1 Calorimeter Trigger TCC Software Work

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15-April-2002
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GENERATING LOOKUP PROMS

Software support 100% done
Needed
Crisp summary (in words) of what needs to be done
 [Monday -> sign-off Tuesday morning]
Source file to describe the PROMs
 [Tuesday -> sign-off Wednesday morning]
Generate the PROM files
 [Wednesday]
Scrutanize, consistancy, etc
 [Wednesday]
Declared official
 [Thursday]

DO Note about how these numbers were picked [2 month ago?]

CONFIGURATION

new analog front-end

75% done

underlying work already 100% done for prototype testing
needs to be integrated as part of running system
 (and coexist with legacy system for a while)
 [1 week]
need new pedestal finder (~ calibration)
 [1 week]

readout

75% done

similar to L1FW [1 week]

## COOR PROGRAMMING

\_\_\_\_\_

90% done

missing quadrant term support in L1FW [1 week]

misc other [1 week]

MONITORING

\_\_\_\_\_

75% done

misc other [1 week]

needs hardware support to capture event snapshot

## TESTING

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in situ PROM checker

CTFE and CHTCR [1 week]

Test/Diagnostics/Exercizer:

## 25% done

we have the bricks to program the resources (= COOR programming) but we need the exercizer software to exercize the system at design speed implement in stages [5 weeks] need additional hardware support to control PROM pages and data capture