Order this data sheet by MC68153/D

MOTOROLA
SEMICONDUCTORS
P.O. BOX 20912 • PHOENIX, ARIZONA 85036

# MC68153

## BUS INTERRUPTER MODULE

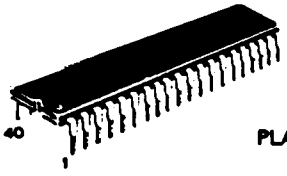
The bipolar LSI MC68153 Bus Interrupter interfaces a microcomputer system bus to multiple slave devices requiring interrupt capabilities. It handles up to four independent sources of interrupt requests and is fully programmable.

- VMEbus Compatible
- MC68000 Compatible
- Handles Four Independent Interrupt Sources
- Eight Programmable Read/Write Registers
- Programmable Interrupt Request Levels
- Programmable Interrupt Vectors
- Supports Interrupt Acknowledge Daisy Chain
- Control Registers Contain Flag Bits
- Single +5.0 Volt Supply
- Total Power Dissipation = 1.5 W Typical
- Temperature Range of 0°C to 70°C
- Chip Access Time = 200 ns Typical with 16 MHz Clock
- 40-Pin Dual-In-Line Package

**TTL**

**BUS INTERRUPTER MODULE**

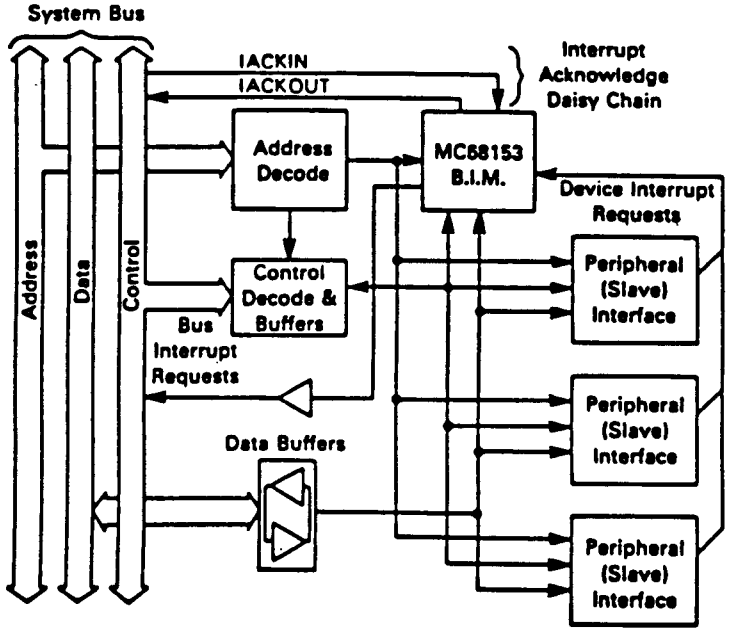
**ADVANCED LOW POWER SCHOTTKY**



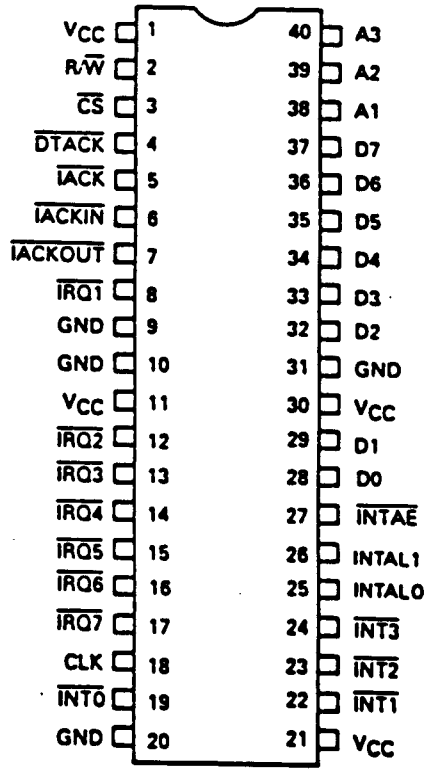

P SUFFIX
PLASTIC PACKAGE
CASE 711-03


L SUFFIX
CERAMIC PACKAGE
CASE 734-04

FIGURE 1 — MC68153 SYSTEM BLOCK DIAGRAM




PIN ASSIGNMENTS




©MOTOROLA INC., 1987

DS9705
(Replacing ADI1057)

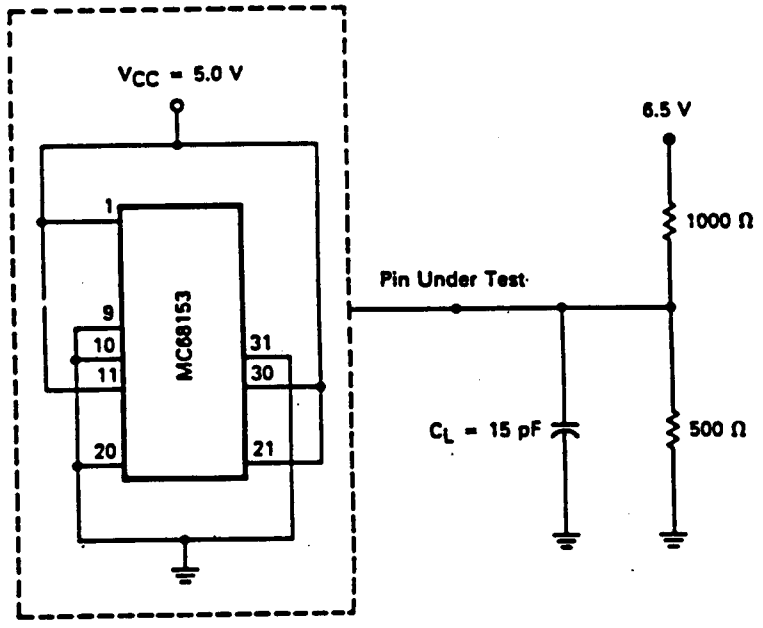
**ABSOLUTE MAXIMUM RATINGS** (Beyond which useful life may be impaired.)

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −0.5 to +7.0 | V |
| Input Voltage | $V_{in}$ | −0.5 to +7.0 | V |
| Input Current | $I_{in}$ | −30 to +5.0 | mA |
| Output Voltage | $V_{out}$ | −0.5 to +5.5 | V |
| Output Current | $I_{OL}$ | Twice Rated $I_{OL}$ | mA |
| Storage Temperature | $T_{stg}$ | −65 to +150 | °C |
| Junction Operating Temperature | $T_J$ | −55 to +175 | °C |

**DC ELECTRICAL SPECIFICATIONS** ($V_{CC}$ = 5.0 V ±5%, $T_A$ = 0°C to 70°C)

| Parameter | Symbol | Min | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| High Level Input Voltage | $V_{IH}$ | 2.0 | — | V | |
| Low Level Input Voltage | $V_{IL}$ | — | 0.8 | V | |
| Input Clamp Voltage | $V_{IK}$ | — | −1.5 | V | $V_{CC}$ = MIN, $I_{IN}$ = −18 mA |
| High Level Output Voltage(1) | $V_{OH}$ | 2.7 | — | V | $V_{CC}$ = MIN, $I_{OH}$ = −400 μA |
| Low Level Output Voltage | $V_{OL}$ | — | 0.4 | V | $V_{CC}$ = MIN, $I_{OL}$ = 8.0 mA |
| Output Short Circuit Current(2) | $I_{OS}$ | −15 | −130 | mA | $V_{CC}$ = MAX, $V_{OUT}$ = 0 V |
| High Level Input Current | $I_{IH}$ | — | 20 | μA | $V_{CC}$ = MAX, $V_{IN}$ = 2.7 V |
| Low Level Input Current | $I_{IL}$ | — | −0.4 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 0.4 V |
| Supply Current | $I_{CC}$ | 225 | 385 | mA | $V_{CC}$ = MAX |
| Output Off Current (High) | $I_{OZH}$ | — | 20 | μA | $V_{CC}$ = MAX, $V_{OUT}$ = 2.4 V |
| Output Off Current (Low) | $I_{OZL}$ | — | −20 | μA | $V_{CC}$ = MAX, $V_{OUT}$ = 0.4 V |

**AC TEST CIRCUIT — AC Testing of All Outputs**




NOTES:
1. Not applicable to open-collector outputs.
2. Not more than one output should be shorted at a time for longer than one second.
3. $\overline{CS}$ Low to CLK High (Setup Time) of 15 ns Min must be observed.
4. $\overline{IACK}$ Low to CLK High and $\overline{IACKIN}$ Low to CLK High (Setup Times) of 15 ns Min must be observed.
5. See Table 1 for additional performance guidelines.

**AC ELECTRICAL SPECIFICATIONS** ($V_{CC}$ = 5.0 V ±5%, $T_A$ = 0°C to 70°C)

| Parameter | Test Number[5] | Max (ns) |
|---|---|---|
| CLK High to Data Out Valid (Delay)[3] | 1 | 55 |
| CLK High to $\overline{\text{DTACK}}$ Low (Delay)[3] | 2 | 40 |
| $\overline{\text{CS}}$ High to $\overline{\text{DTACK}}$ High (Delay) | 3 | 35 |
| CLK High to Data Out Valid (Delay)[4] | 4 | 55 |
| CLK High to $\overline{\text{INTAE}}$ Low (Delay)[4] | 5 | 40 |
| $\overline{\text{IACK}}$ High to Data Out High Impedance (Delay) | 6 | 60 |
| $\overline{\text{IACK}}$ High to $\overline{\text{DTACK}}$ High (Delay) | 7 | 45 |
| $\overline{\text{CS}}$ High to Data Out High (Delay) | 8 | 45 |
| CS High to IRQ High (Delay) | 9 | 60 |
| $\overline{\text{IACK}}$ High to $\overline{\text{INTAE}}$ High (Delay) | 10 | 35 |

## GENERAL DESCRIPTION

The MC68153 Bus Interrupter Module (BIM) is designed to serve as an interrupt requester for peripheral devices in a microcomputer system. Up to 4 independent devices can be interfaced to the system bus by the MC68153. Intended for asynchronous master/slave bus operation, the BIM can be used with VMEbus, MC68000 device bus, and other system buses. Figure 1 shows a block diagram of a typical configuration. In this example, three peripheral devices (bus slaves) are connected to the system data bus. Each of these devices could be parallel I/O, serial I/O, or some other function. An interrupt request from any device is routed to the MC68153, and the BIM handles all interface to the system bus. It generates a bus interrupt request as a result of the device interrupt request. When the system interrupt handler or processor responds with an interrupt acknowledge cycle, the MC68153 can answer supplying an interrupt vector and handling all timing.

The functional block diagram of the MC68153 is shown in Figure 2. The device contains circuitry to accept four separate interrupt sources ($\overline{\text{INT0}}$ – $\overline{\text{INT3}}$). Interface to the system bus includes generation of bus interrupt requests ($\overline{\text{IRQ1}}$ – $\overline{\text{IRQ7}}$), response to a bus interrupt acknowledge cycle (either supplying a vector or passing on a daisy chain signal), and releasing the bus interrupt request signal at the proper time. The BIM has flexibility provided by eight programmable read/write registers. Four 8-bit vector registers (VR0 – VR3) contain status/address information and supply a byte vector in response to an interrupt acknowledge cycle for the corresponding interrupt source. Four other 8-bit control registers (CR0 – CR3) contain information that oversees operation of the interrupt circuitry. The control information is programmable and includes interrupt request level and interrupt enable and disable. Also contained in the control registers are flag-bits. These flags are useful for task coordination, resource management, and interprocessor communication.

## SIGNAL DESCRIPTION

Throughout the data sheet, signals are presented using the terms asserted and negated independent of whether the signal is asserted in the high voltage or low voltage state. Active low signals are denoted by a superscript bar.

### BIDIRECTIONAL DATA BUS — D0 – D7

Pins D0 – D7 form an 8-bit bidirectional data bus to/from the system bus (D7 is MSB). These are active high, 3-state pins.

### ADDRESS INPUTS — A1 – A3

These active high inputs serve two functions. One function is to select one of the eight possible registers during a read or write cycle. Secondly, during an interrupt acknowledge A1 – A3 show the level of interrupt being acknowledged, and the BIM uses these to determine if a match exists with an internal level.

### CHIP SELECT — $\overline{\text{CS}}$

$\overline{\text{CS}}$ is an active low input used to select the BIM's registers for the current bus cycle. Address strobe, data strobe, and appropriate address bits must be included in the chip select equation.

### READ/WRITE — R/$\overline{\text{W}}$

The R/$\overline{\text{W}}$ input is a signal from the system bus used to determine if the current bus cycle is a read (high) or write (low).

### DATA TRANSFER ACKNOWLEDGE — $\overline{\text{DTACK}}$

$\overline{\text{DTACK}}$ is an open-collector, active low output that signals the completion of a read, write, or interrupt acknowledge cycle. During read or interrupt acknowledge cycles, $\overline{\text{DTACK}}$ is asserted by the MC68153 after data has been provided on the data bus; during write cycles it is asserted after data has been accepted from the data bus. A pullup resistor is required to maintain $\overline{\text{DTACK}}$ high between bus cycles.

FIGURE 2 — MC68153 FUNCTIONAL BLOCK DIAGRAM

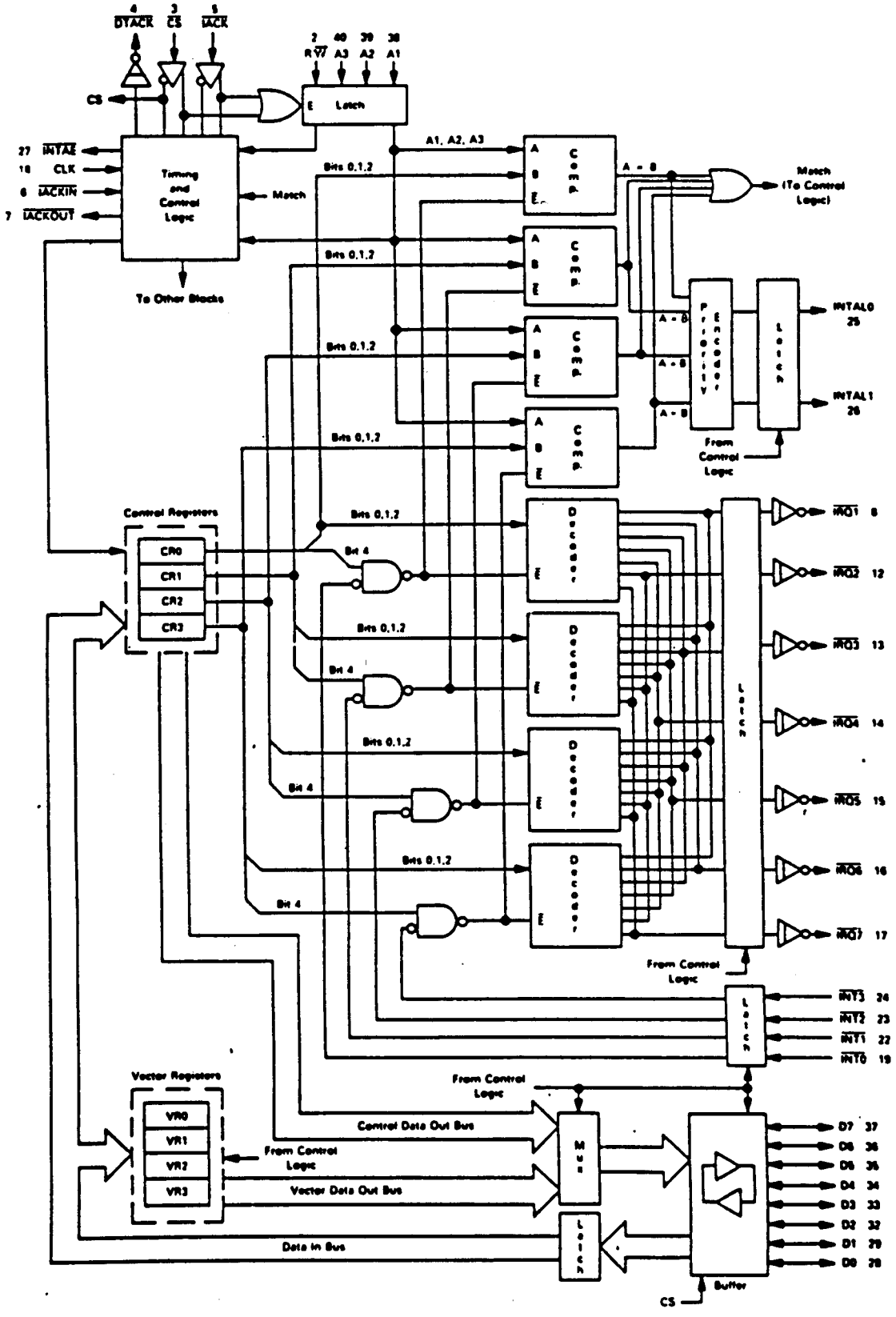
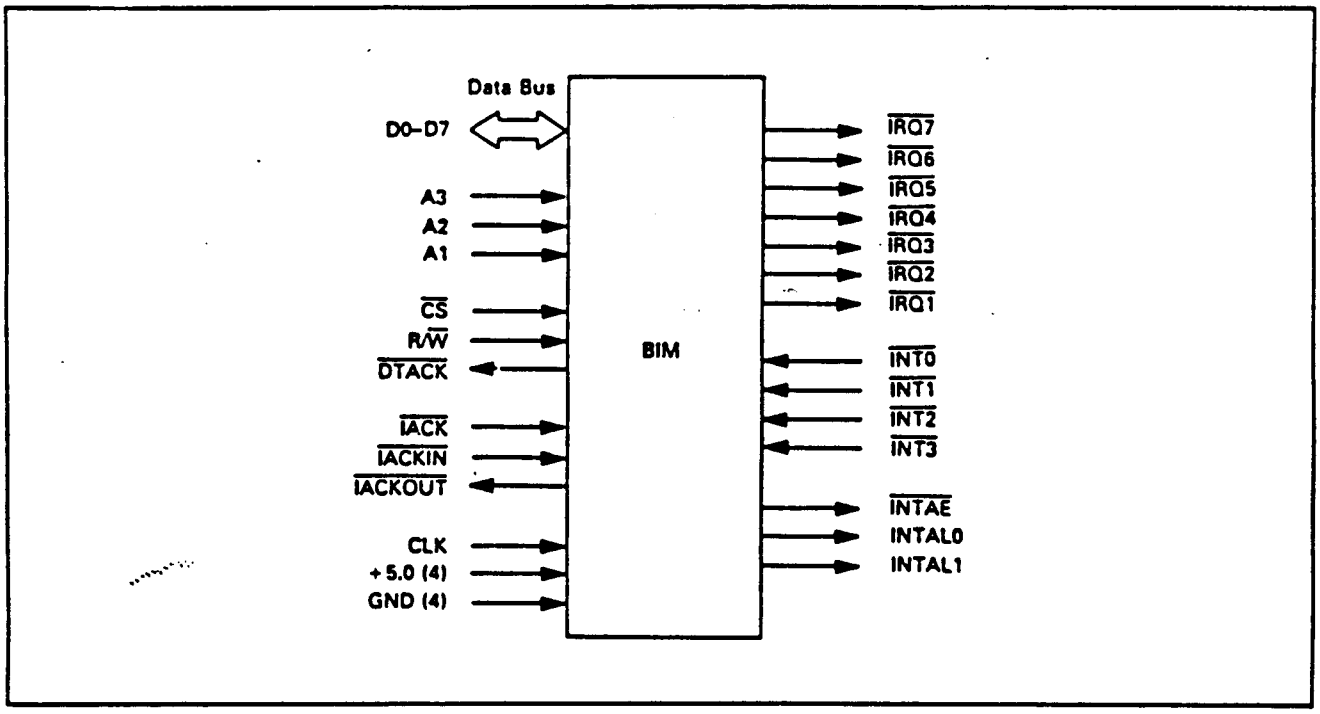


FIGURE 3 — LOGICAL PIN ASSIGNMENT




**INTERRUPT ACKNOWLEDGE SIGNALS — IACK, IACKIN, IACKOUT**

These three pins support the interrupt acknowledge cycle. A low level on the IACK input indicates an interrupt acknowledge cycle has been initiated. This signal is conditioned externally with Address Strobe and the lower data strobe of an MC68000 type bus. After IACK is asserted the BIM compares the interrupt level presented on address lines A1, A2, and A3 with the current levels generated internally (INTX inputs are latch during IACK asserted) and determines if a match exists. Then, if input IACKIN is asserted (driven low), the BIM will either complete the interrupt acknowledge cycle if a match exists or assert output IACKOUT if *no* match exists.

IACKIN and IACKOUT form part of a prioritized interrupt acknowledge daisy chain. The daisy chain prioritizes interrupters and guarantees that two or more devices requesting an interrupt on the same level will not respond to the same cycle. The requesting device (or interrupter) must wait until IACKIN is asserted and not pass the signal on (assert IACKOUT) if it is to complete the interrupt acknowledge cycle.

**BUS INTERRUPT REQUEST SIGNALS — IRQ1 – IRQ7**

These open-collector outputs are low when asserted, indicating a bus interrupt is requested at the corresponding level. An open-collector buffer is normally required for sufficient drive when interfacing to a system bus. A pullup resistor is required to maintain IRQ1 – IRQ7 high between interrupt requests.

**DEVICE INTERRUPT REQUEST SIGNALS — INT0–INT3**

INT0–INT3 are active low inputs used to indicate to the BIM that a device wants a bus interrupt. These inputs should be kept asserted (held low) until the interrupt is acknowledged.

**INTERRUPT ACKNOWLEDGE ENABLE — INTAE**

During an interrupt acknowledge cycle, this output pin is asserted low to indicate that outputs INTAL0 and INTAL1 are valid. These two outputs contain an encoded number (x) corresponding to the interrupt (INTx) being acknowledged. This feature can be used to signal interrupting devices, which supply their own vector, when to respond to the interrupt acknowledge cycle with the vector and a DTACK signal.

**INTERRUPT ACKNOWLEDGE LEVEL — INTAL0, INTAL1**

These active high outputs contain an encoded number corresponding to the interrupt level being acknowledged. They are valid only when INTAE is asserted low.

**CLOCK — CLK**

The CLK input is used to supply the clock for internal operations of the MC68153.

**RESET — CS, IACK**

Although a reset input is not supplied, an on-board reset is performed if CS and IACK are asserted simultaneously.

FIGURE 4 — MC68153 REGISTER MODEL

| ADDRESS BIT A3 | A2 | A1 | FLAG | FLAG AUTO-CLEAR | EXTERNAL/INTERNAL | INTERRUPT ENABLE | INTERRUPT AUTO-CLEAR | INTERRUPT LEVEL | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | F | FAC | X/$\overline{IN}$ | IRE | IRAC | L2 | L1 | L0 | CONTROL REGISTER 0 |
| 0 | 0 | 1 | F | FAC | X/$\overline{IN}$ | IRE | IRAC | L2 | L1 | L0 | CONTROL REGISTER 1 |
| 0 | 1 | 0 | F | FAC | X/$\overline{IN}$ | IRE | IRAC | L2 | L1 | L0 | CONTROL REGISTER 2 |
| 0 | 1 | 1 | F | FAC | X/$\overline{IN}$ | IRE | IRAC | L2 | L1 | L0 | CONTROL REGISTER 3 |
| 1 | 0 | 0 | V7 | V6 | V5 | V4 | V3 | V2 | V1 | V0 | VECTOR REGISTER 0 |
| 1 | 0 | 1 | V7 | V6 | V5 | V4 | V3 | V2 | V1 | V0 | VECTOR REGISTER 1 |
| 1 | 1 | 0 | V7 | V6 | V5 | V4 | V3 | V2 | V1 | V0 | VECTOR REGISTER 2 |
| 1 | 1 | 1 | V7 | V6 | V5 | V4 | V3 | V2 | V1 | V0 | VECTOR REGISTER 3 |
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | REGISTER NAME |
| | | | REGISTER BIT | | | | | | | | |

## REGISTER DESCRIPTION

The MC68153 contains 8 programmable read/write registers. There are four control registers (CR0 – CR3) that govern operation of the device and four vector registers (VR0 – VR3) that contain the vector data used during an interrupt acknowledge cycle. Figure 4 illustrates the device register model.

## CONTROL REGISTERS

There is a control register for each interrupt source, i.e., CR0 controls $\overline{INT0}$, CR1 controls $\overline{INT1}$, etc. The control registers are divided into several fields:

1. Interrupt level (L2, L1, L0) — The least significant 3-bit field of the register determines the level at which an interrupt will be generated:

| L2 | L1 | L0 | IRQ LEVEL |
|---|---|---|---|
| 0 | 0 | 0 | NOT ALLOWED* |
| 0 | 0 | 1 | IRQ1 |
| 0 | 1 | 0 | IRQ2 |
| 0 | 1 | 1 | IRQ3 |
| 1 | 0 | 0 | IRQ4 |
| 1 | 0 | 1 | IRQ5 |
| 1 | 1 | 0 | IQR6 |
| 1 | 1 | 1 | IRQ7 |

*To disable the interrupt, use the IRE bit.

2. Interrupt Enable (IRE) — This field (Bit 4) must be set (high level) to enable the bus interrupt request associated with the control register. Thus, if the $\overline{INTX}$ line is asserted and IRE is cleared, *no* interrupt request ($\overline{IRQX}$) will be asserted.
3. Interrupt Auto-Clear (IRAC) — If the IRAC is set (Bit 3), IRE (Bit 4) is cleared during an interrupt acknowledge cycle responding to this request. This action of clearing IRE disables the interrupt request. To re-enable the interrupt associated with this register, IRE must be set again by writing to the control register.
4. External/Internal (X/$\overline{IN}$) — Bit 5 of the control register determines the response of the MC68153 during an interrupt acknowledge cycle. If the X/$\overline{IN}$ bit is clear (low level) the BIM will respond with vector data and a $\overline{DTACK}$ signal, i.e., an internal response. If X/$\overline{IN}$ is set, the vector is not supplied and no $\overline{DTACK}$ is given by the BIM, i.e., an external device should respond.
5. Flag (F) — Bit 7 is a flag that can be used in conjunction with the test and set instruction of the MC68000. It can be changed without affecting chip operation. It is useful for processor-to-processor communication and resource allocation.
6. Flag Auto-Clear (FAC) — If FAC (Bit 6) is set, the Flag bit is automatically cleared during an interrupt acknowledge cycle.

## VECTOR REGISTERS

Each interrupt input has its own associated vector register. Each register is 8 bits wide and supplies a data byte during its interrupt acknowledge cycle if the associated External/Internal (X/$\overline{IN}$) control register bit is clear (zero). This data can be status, identification, or address information depending on system usage. The information is programmed by the system user.

## DEVICE RESET

When the MC68153 is reset, the registers are set to a known condition. The control registers are set to all zeros (low). The vector registers are set to $0F. This value is the MC68000 vector for an uninitialized interrupt vector.

## FUNCTIONAL DESCRIPTION

### SYSTEM OVERVIEW

The MC68153 is compatible with many system buses, however, it is primarily intended for VMEbus, and MC68000 applications. Figure 5 shows a system configuration similar to VMEbus. In the figure only one system Data Transfer Bus (DTB) master is used. The Priority Interrupt structure provides a means for peripheral slave devices to ask for an interrupt of the processor (DTB master) activity and receive service from the processor. The MC68153 BIM acts as an interface device requesting and responding to interrupt acknowledge cycles for up to 4 independent slaves.

In Figure 5, functional modules are identified as Interrupters and an Interrupt Handler. An Interrupter (which can use the MC68153) receives slave requests for an interrupt and handles all interface to the system bus required to ask for and respond to interrupt requests. The Interrupt Handler receives the bus interrupt requests, determines when an interrupt acknowledge will occur and at which level, and finally either performs the interrupt acknowledge (IACK) cycle or tells the DTB master to execute the IACK cycle.

The signal lines in the Priority Interrupt structure include (* — indicates active low):

1. IRQ1*–IRQ7* — seven prioritized interrupt request lines.
2. IACK* — signal line that indicates an interrupt acknowledge cycle is occurring.
3. IACKIN*/IACKOUT* — two signals that form part of a daisy chain that prioritizes interrupters.

In addition Data Transfer Bus control signals are involved in the IACK bus cycle:

1. AS* — the Address Strobe asserted low indicates a valid address is on the bus.
2. DSO* — the lower Data Strobe asserted low indicates a data transfer will occur on bus bits D00–D07.
3. WRITE* — the Read/Write is negated indicating the data is to be read from the Interrupter.
4. A01–A03 — Address lines A01–A03 contain the encoded priority level of the IACK cycle.
5. D00–D07 — Data bus lines D00–D07 are used to pass the interrupt vector from the responding Interrupter to the Interrupt Handler.
6. DTACK* — Data Transfer Acknowledge asserted low signals that the Interrupter has put the vector on the data bus.

FIGURE 5 — SIMPLE VMEbus CONFIGURATION

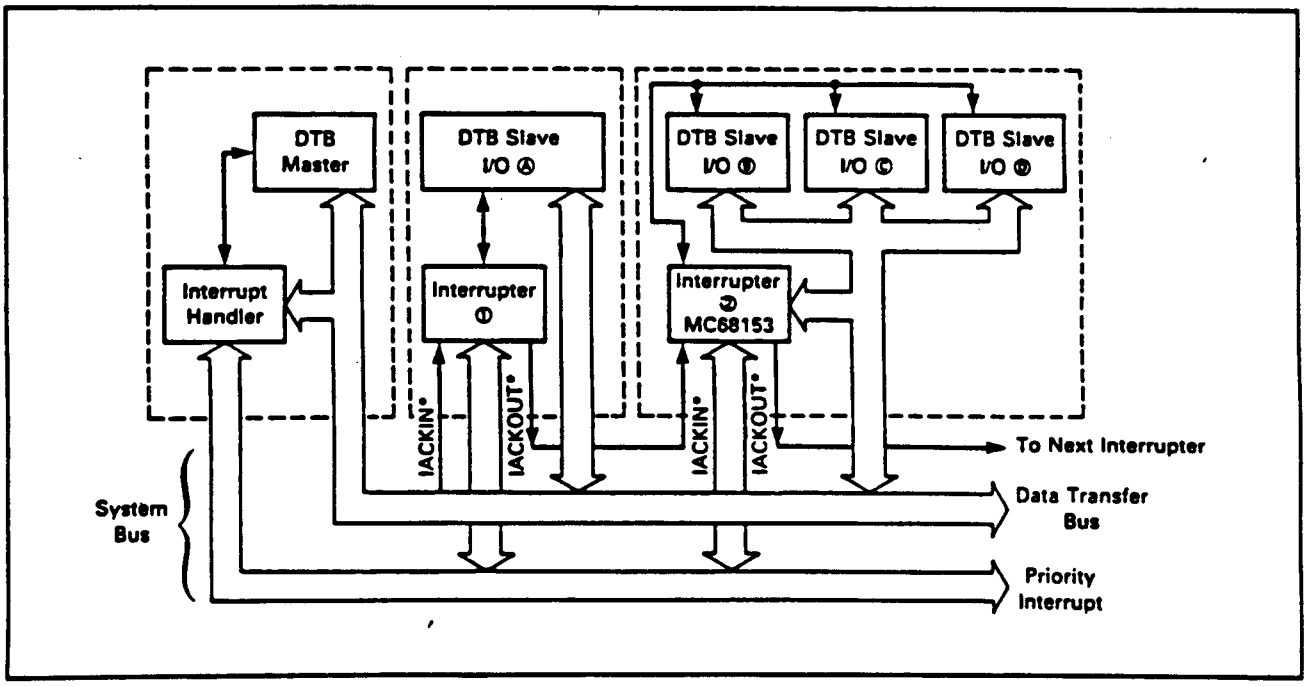
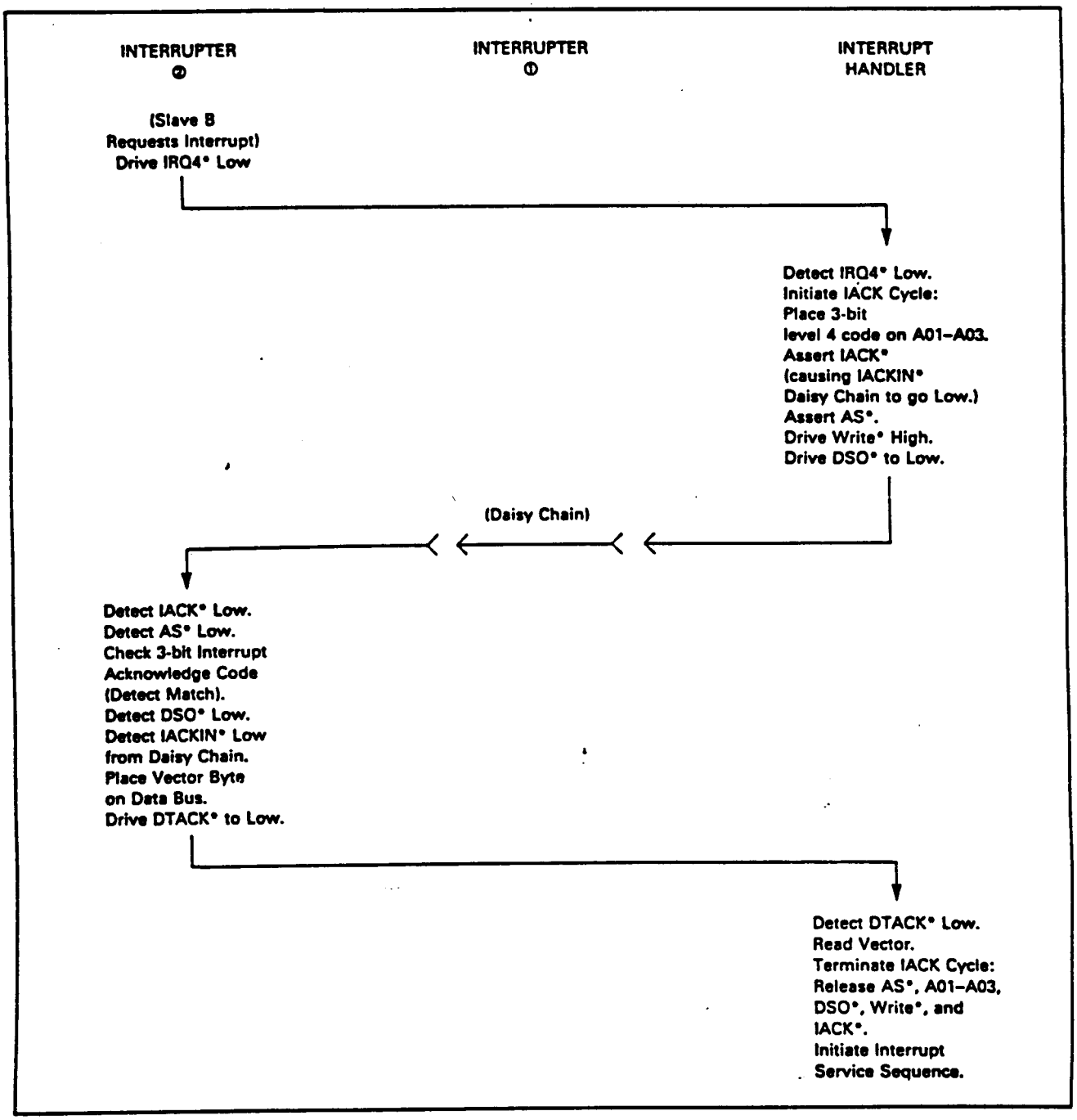


Figure 6 shows a flow diagram of a typical interrupt request and acknowledge operation. Briefly, the sequence of events is first, an Interrupter makes a request, next the Handler responds with an IACK cycle, then the Interrupter passes a vector to the Handler completing the IACK cycle, and finally the Handler uses the vector to determine additional action. Typically, an interrupt service routine is stored in software and the vector points to its starting address.

Note the daisy chain operation. If the IACK level (on A01–A03) does not match the Interrupter's request level or if no request is pending, the Interrupter passes the IACKIN* signal on and asserts IACKOUT*. This sequential action automatically prioritizes Requesters on the same level (first one in line with a request pending gets serviced) and prevents two or more Interrupters from responding simultaneously.

This discussion is a very cursory look at the bus operation. For more details including situations with multiple bus masters, the user is directed to the VMEbus Specification. Also, the MC68153 can be used with other buses having similar interrupt structures.

**FIGURE 6 — INTERRUPT REQUEST AND ACKNOWLEDGE OPERATION FLOW DIAGRAM**



## BIM BUS INTERFACE

Figure 7 shows a simplified block diagram of the BIM interfaced to the VMEbus. The MC68153 is used as a D08 (O) type interrupter. Address decode is dependent on the application although the inputs should be latched using DSO*. $\overline{\text{ADDEN}}$ (see Figure 7) is asserted when there is a read or write cycle to the BIM. Buffers are provided where shown to comply with VMEbus loading and drive specifications. Note that in most applications the address decode, control logic, and buffers can be shared with other slave devices.

Additional information is given in the VMEbus applications section of this data sheet. (See page 14.)

## READ/WRITE OPERATION

All eight BIM registers can be accessed from the system bus in both read and write modes. The BIM has an asynchronous bus interface, primarily designed for MC68000-like buses. The following BIM signals are used during read and write cycles: Chip Select ($\overline{\text{CS}}$), Read/Write (R/$\overline{\text{W}}$), Address Inputs (A1–A3), Data Bus (D0–D7), and Data Transfer Acknowledge ($\overline{\text{DTACK}}$). During read and write cycles the internal registers are selected by A1, A2, and A3 in compliance with the Figure 4 Truth Table.

Figure 8 shows the device timing for a read cycle. R/$\overline{\text{W}}$ and A1–A3 are latched on the falling edge of $\overline{\text{CS}}$ and must meet specified setup and hold times. Chip access time for valid data and $\overline{\text{DTACK}}$ are dependent on the clock frequency as shown in the figure.

Figure 9 shows the device timing for a write cycle. R/$\overline{\text{W}}$, A1–A3, and D0–D7 are latched on the falling edge of $\overline{\text{CS}}$ and must meet specified setup and hold times. Chip access time for $\overline{\text{DTACK}}$ is dependent on the clock frequency as shown in the figure.

FIGURE 7 — VMEbus D08 (0) INTERRUPTER BLOCK DIAGRAM

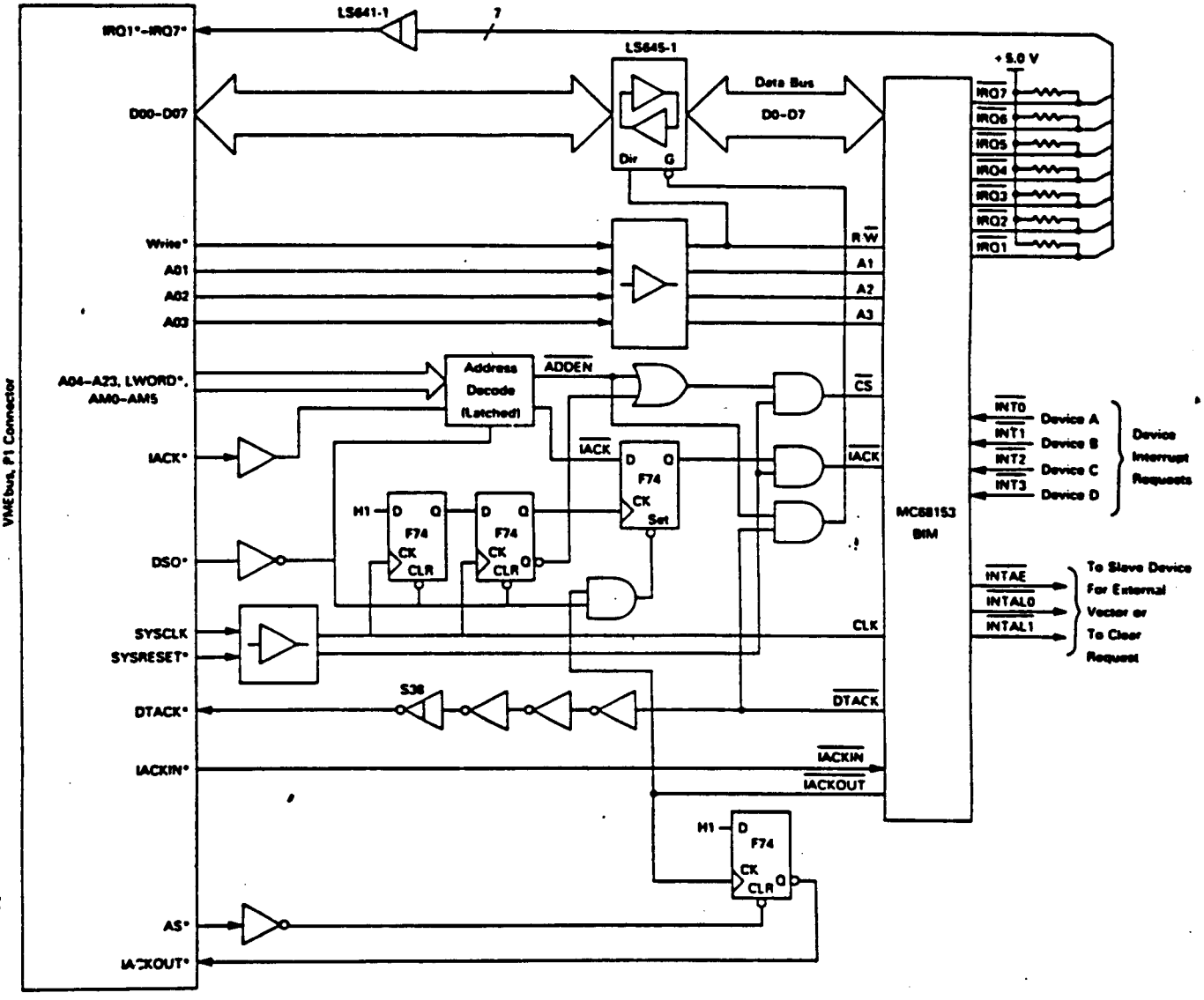


FIGURE 8 — READ CYCLE

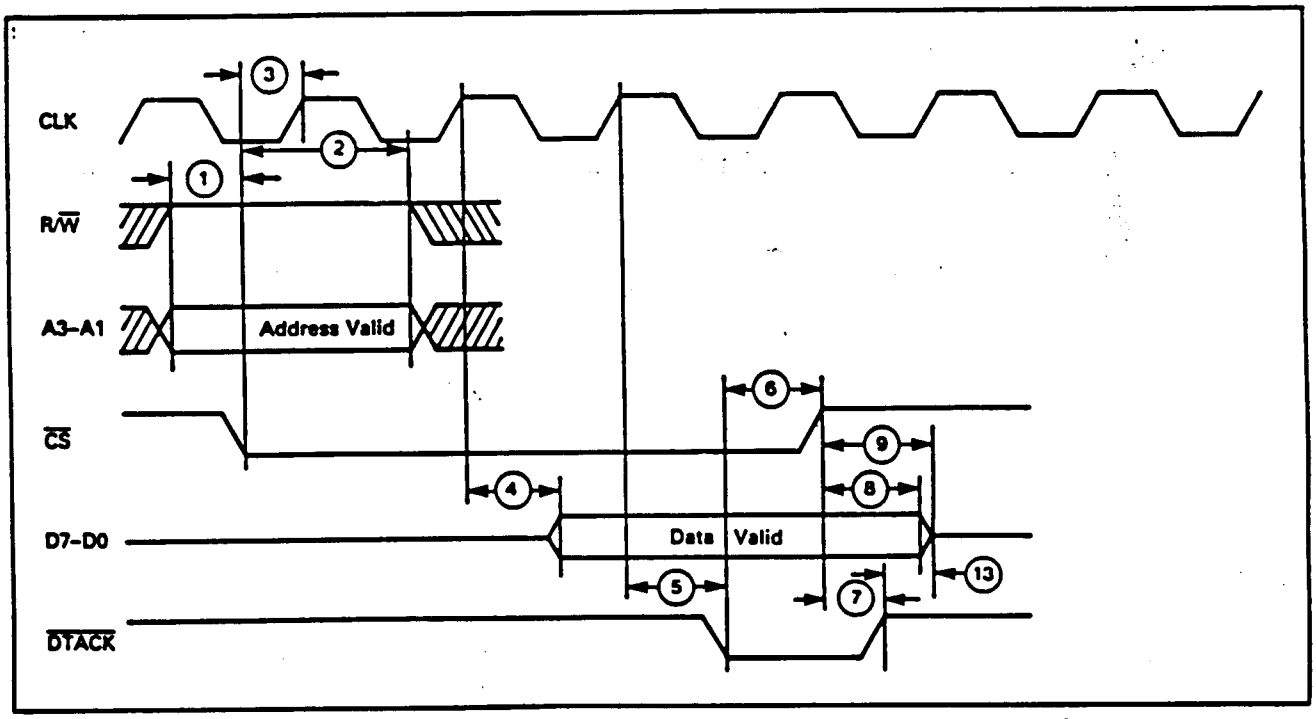
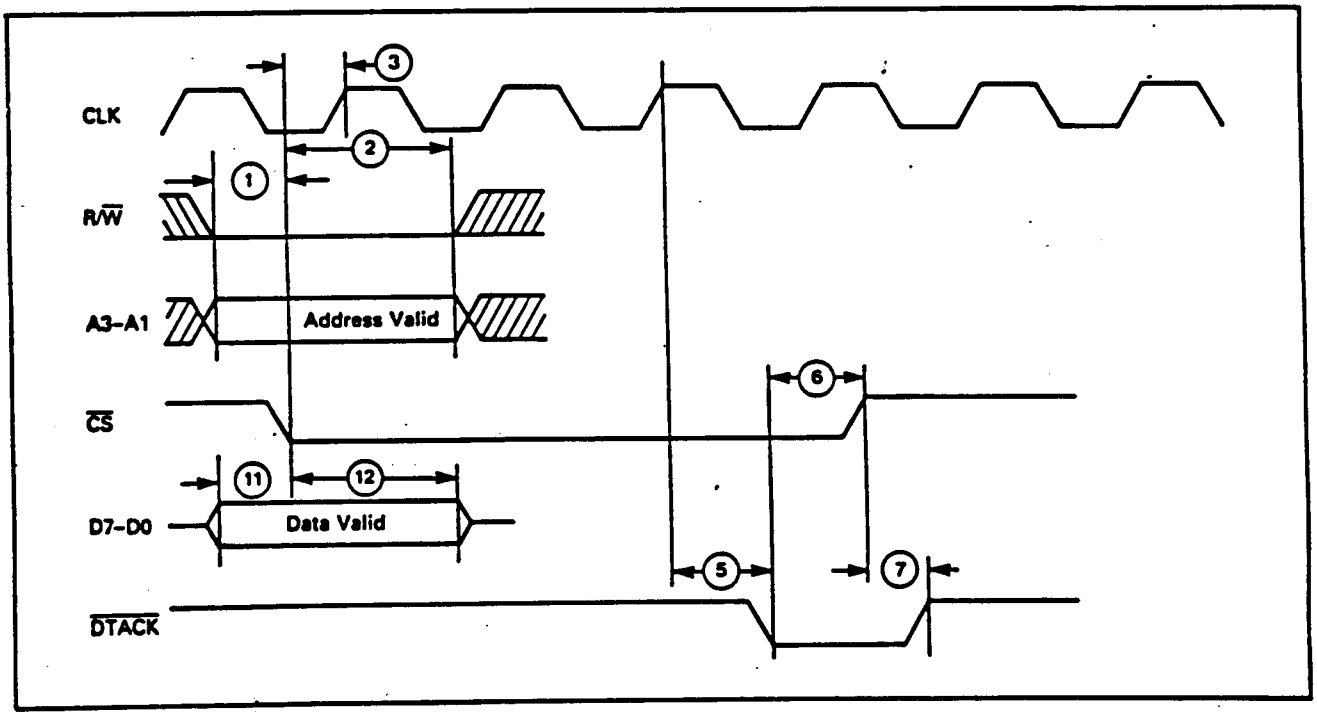



FIGURE 9 — WRITE CYCLE



## INTERRUPT REQUESTS

The MC68153 accepts device interrupt requests on inputs $\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, and $\overline{INT3}$. Each input is regulated by Bit 4 (IRE) of the associated control register (CR0 controls $\overline{INT0}$, CR1 controls $\overline{INT1}$, etc). If IRE (Interrupt Enable) is set and a device input is asserted, an Interrupt Request open-collector output ($\overline{IRQ1}$–$\overline{IRQ7}$) is asserted. The asserted $\overline{IRQX}$ output is selected by the value programmed in Bits 0, 1, and 2 of the control register (L0, L1, and L2). This 3-bit field determines the interrupt request level as set by software.

Two or more interrupt sources can be programmed to the same request level. That $\overline{IRQX}$ output will remain asserted until multiple interrupt acknowledge cycles respond to all requests.

The device interrupt request signals ($\overline{INT0}$–$\overline{INT3}$) must be driven with a level, that is, they are not edge-triggered. The transparent latch on these inputs shown in Figure 2 is only latched during an $\overline{IACK}$ cycle to lock-out new interrupt requests and prevent a race condition on the $\overline{IACKIN}$–$\overline{IACKOUT}$ daisy chain. The requesting device should provide a level to the MC68153 $\overline{INTX}$ inputs.

The device request can be cleared by the processor as part of the interrupt service routine or via a hardware signal generated from the INTALX and $\overline{INTAE}$ lines. If a local interrupt request is being acknowledged during an $\overline{IACK}$ cycle, $\overline{INTAE}$ is asserted low to indicate that INTAL0 and INTAL1 are valid. The encoded number indicates which $\overline{INTX}$ input is being acknowledged. These signals can be used to clear the device interrupt request.

## INTERRUPT ACKNOWLEDGE

The response of an Interrupt Handler to a bus interrupt request is an interrupt acknowledge cycle. The IACK cycle is initiated in the MC68153 by receiving $\overline{IACK}$ low. R/$\overline{W}$, A1, A2, A3 are latched, and the interrupt level on line A1–A3 is compared with any interrupt requests pending in the chip. Further activity can be one of four cases:

1. No further action required — This occurs if $\overline{IACKIN}$ is not asserted. Asserting $\overline{IACK}$ only starts the BIM activity. If the daisy chain signal never reaches the MC68153 ($\overline{IACKIN}$ is not asserted), another Interrupter has responded to the $\overline{IACK}$ cycle. The cycle will end, the chip $\overline{IACK}$ is negated, and no additional action is required.
2. Pass on the interrupt acknowledge daisy chain — For this case, $\overline{IACKIN}$ input is asserted by the preceding daisy chain Interrupter, and $\overline{IACKOUT}$ output is in turn asserted. The daisy chain signal is passed on when no interrupts are pending on a matching level or when any possible interrupts are disabled. The Interrupt Enable (IRE) bit of a control register can disable any interrupt requests, and in turn, any possible matches.
3. Respond internally — For this case, $\overline{IACKIN}$ is asserted and a match is found. The MC68153 completes the IACK cycle by supplying an interrupt vector from the proper vector register followed by a $\overline{DTACK}$ signal asserted. $\overline{IACKOUT}$ is not asserted because the interrupt acknowledge cycle is completed by this device.

   For the MC68153 to respond in this mode of operation, the EXTERNAL/$\overline{INTERNAL}$ control register bit (X/$\overline{IN}$) must be zero. For each source of interrupt request, the associated control register determines the BIM response to an IACK cycle, and the X/$\overline{IN}$ bit sets this response either internally (X/$\overline{IN}$ = 0) or externally (X/$\overline{IN}$ = 1).
4. Respond externally — For the final case, $\overline{IACKIN}$ is also asserted, a match is found and the associated control register has X/$\overline{IN}$ bit set to one. The MC68153 does not assert $\overline{IACKOUT}$ and does assert $\overline{INTAE}$ low. $\overline{INTAE}$ signals that the requesting device must complete the IACK cycle (supplying a vector and $\overline{DTACK}$) and that the 2-bit code contained on outputs INTAL0 and INTAL1 shows which interrupt source is being acknowledged.

These cases are discussed in more detail in the following paragraphs.

### Internal Interrupt Acknowledge

For an internal interrupt acknowledge to occur, the following conditions must be met:

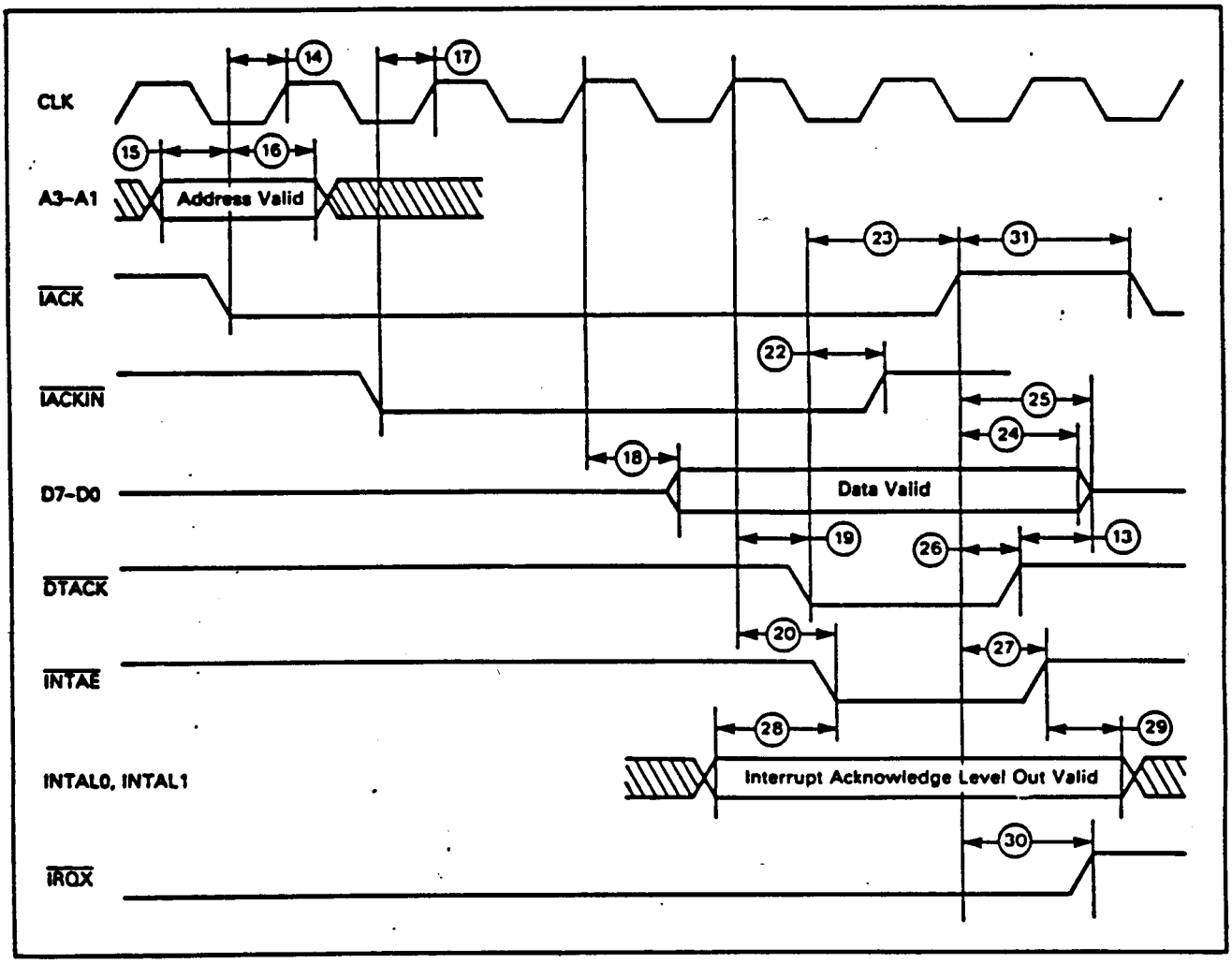
1. One or more device interrupt inputs ($\overline{INT0}$–$\overline{INT3}$) has been asserted and corresponding control bit IRE value is one.
2. $\overline{IACK}$ asserted.
3. A match exists between [A3, A2, A1] and the [L2, L1, L0] field of an enabled, requesting control register. If two or more devices are requesting at the same interrupt level, preference is given to the highest number requester, that is, $\overline{INT3}$ has highest priority and $\overline{INT0}$ has lowest.
4. Control register bit X/$\overline{IN}$ of matching interrupt source must be zero.
5. $\overline{IACKIN}$ asserted.

The internal interrupt acknowledge cycle timing is shown in Figure 10. The 8-bit interrupt acknowledge vector is presented to the data bus and $\overline{DTACK}$ is asserted. Note also that INTAL0 and INTAL1 are valid and $\overline{INTAE}$ is asserted during this cycle although they would normally not be used. The cycle is terminated (data and $\overline{DTACK}$ released) after $\overline{IACK}$ is negated.

During the IACK cycle, the INTERRUPT AUTO-CLEAR control bit (IRAC) comes into play. If the IRAC = one for the responding interrupt source, the INTERRUPT ENABLE (IRE) bit is automatically cleared during the IACK cycle, thus disabling the associated interrupt input and any $\overline{IRQX}$ output asserted due to this interrupt input. Before another interrupt can be requested from this source, IRE must be set to one by writing to the control register.

Note that $\overline{IACKOUT}$ is not asserted because this device is responding to the IACK and does not pass the daisy chain signal on. Also, new device interrupt requests occurring on $\overline{INT0}$–$\overline{INT3}$ after $\overline{IACK}$ is asserted are locked out to prevent any race conditions on the daisy chain.

FIGURE 10 — INTERRUPT ACKNOWLEDGE CYCLE — INTERNAL VECTOR




**External Interrupt Acknowledge**

For an external interrupt acknowledge, the same conditions as listed above are met with one exception. Control register bit X/$\overline{IN}$ of matching interrupt source must be set to one. The timing is shown in Figure 11. For this cycle, the interrupt vector and $\overline{DTACK}$ must be supplied by an external device. $\overline{INTAE}$ is asserted indicating that INTAL0 and INTAL1 are valid. The external device can use these signals to enable the vector and $\overline{DTACK}$. The cycle is terminated after $\overline{IACK}$ is negated.

The IRAC control bit acts in the external interrupt acknowledge the same as described for the internal response (see above). Also, $\overline{IACKOUT}$ is not asserted and new device interrupts are disabled for reasons discussed above.

**Pass On IACK Daisy Chain**

If the MC68153 has no interrupt request pending at the same level as the interrupt acknowledge, the IACK daisy chain signal is passed on to the next device if $\overline{IACKIN}$ is asserted. The following conditions are thus met:

1. $\overline{IACK}$ asserted.
2. No match exists between [A3, A2, A1] and the [L2, L1, L0] field of an enabled, requesting control register.
3. $\overline{IACKIN}$ is asserted.

$\overline{IACKOUT}$ is asserted if these conditions are valid. This output drives $\overline{IACKIN}$ of the next Interrupter on the daisy chain, passing the signal along. Figure 12 shows the timing for this case. $\overline{IACKOUT}$ is negated after $\overline{IACK}$ is negated.

FIGURE 11 — INTERRUPT ACKNOWLEDGE CYCLE — EXTERNAL VECTOR

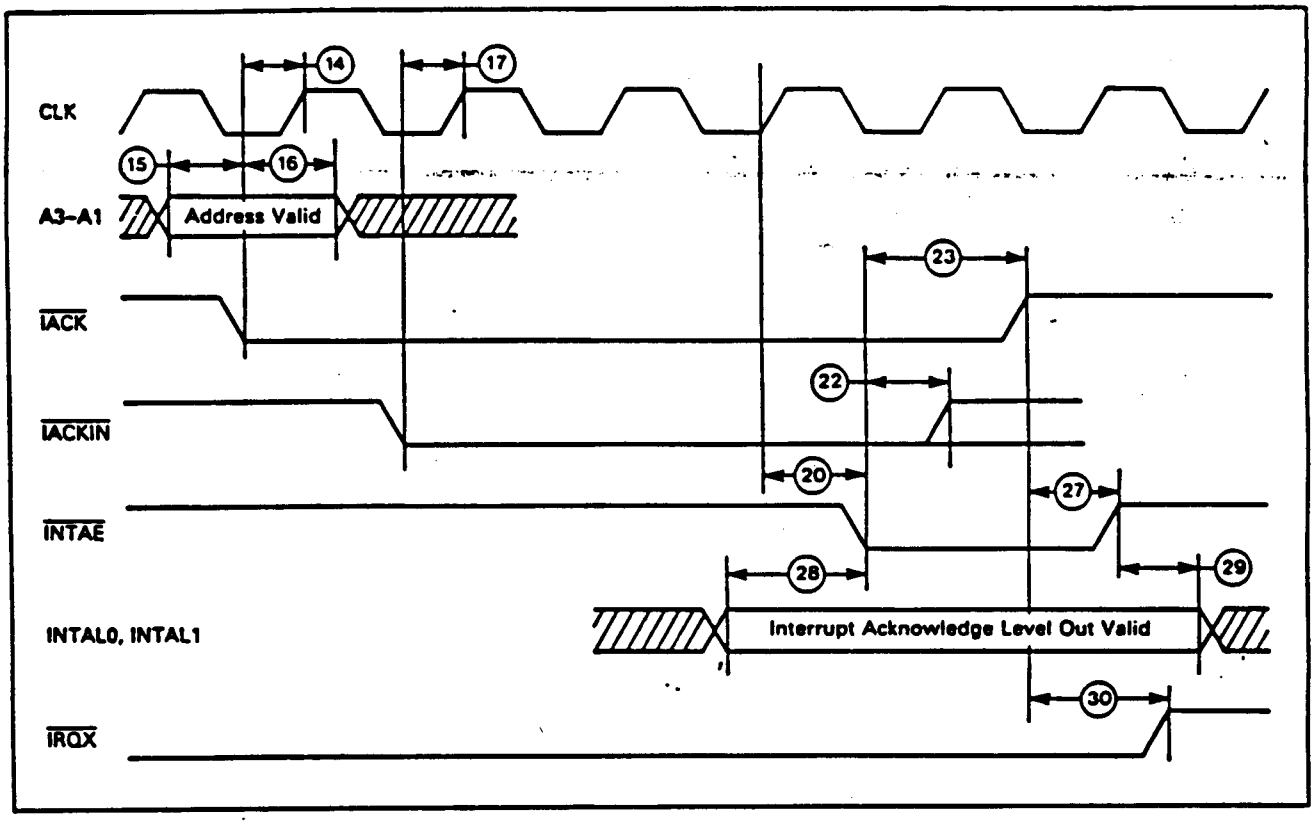
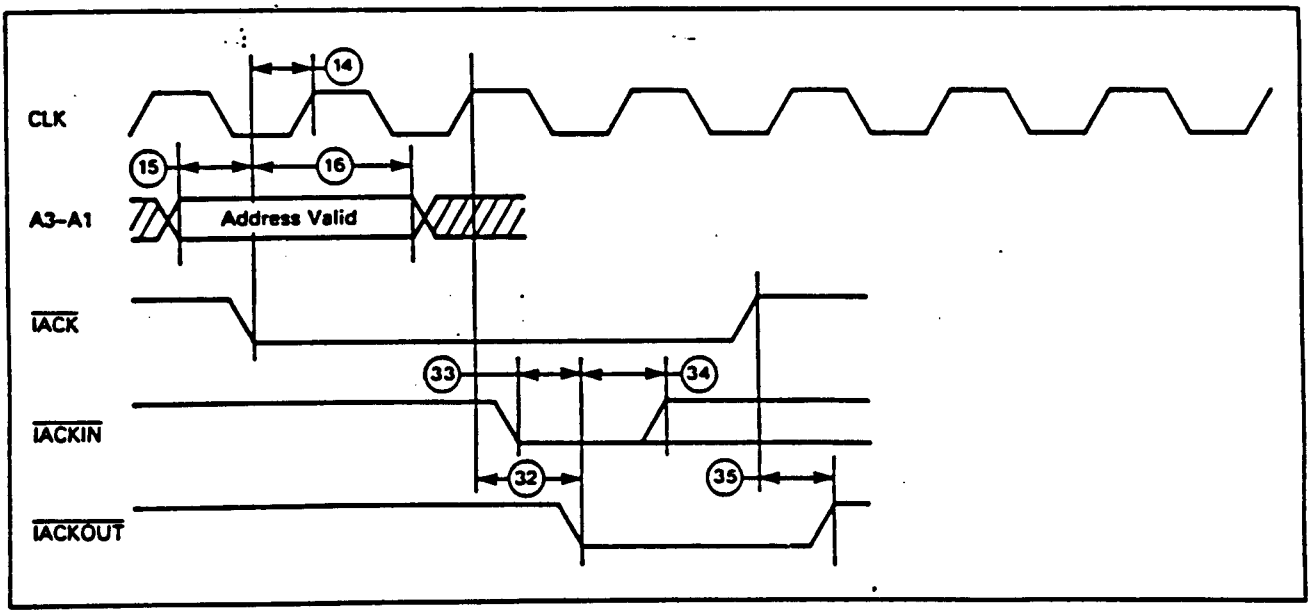



FIGURE 12 — INTERRUPT ACKNOWLEDGE CYCLE — $\overline{\text{IACKOUT}}$



## CONTROL REGISTER FLAGS

Each control register contains a Flag bit (F) and a Flag Auto-Clear bit (FAC). Both bits can be read or altered via a register write without affecting the interrupt operation of the device. The Flag is useful as a status indicator for resource management and as a semaphor in multitasking or multiprocessor systems. Flag (F) is located in bit position 7 and can be used with the MC68000 Test and Set (TAS) instruction.

The Flag Auto-Clear (FAC) is used to manipulate the Flag bit. If the Flag is set to one and the FAC is also one, an interrupt acknowledge cycle to the associated interrupt source clears the Flag bit. This feature is useful in determining the interrupt status and passing messages.

## RESET

There is no reset input, however, a chip reset is activated by asserting both $\overline{CS}$ and $\overline{IACK}$ simultaneously (Figure 13). These inputs should be held low for a minimum of two clock cycles for a full reset function. The control registers are reset to all zeroes and the Vector Registers are set to a value of $0F. This vector value is the uninitialized vector for the MC68000. See the MC68000 Users Manual for more details on this vector.

## CLOCK

The chip clock is required for internal operation to occur. Typical frequency is 16 MHz in VMEbus derived from the system clock. Any frequency can be used, however, up to 25 MHz (Figure 14). Note that $\overline{CS}$, $\overline{IACK}$, and $\overline{IACKIN}$ are all double-clocked to help prevent metastable problems.

## VMEbus APPLICATIONS

The MC68153 is commonly used as a VMEbus interrupter. In addition to meeting normal VMEbus loading and timing rules, the designer should note other factors:

1. The MC68153 may be used as a Release On Acknowledge (ROAK) INTERRUPTER for VMEbus (see VMEbus Specification, Rev. C.1, section 4.3.7). The ROAK interrupter should release its IRQX* signal at the end of the interrupt acknowledge cycle that reads its STATUS/ID. To cause the MC68153 $\overline{IRQX}$ signal to be released, the IRAC bit (interrupt auto-clear) should be set.

   To enable an interrupt request, the IRE bit of the appropriate control register must be set. If the IRAC bit is also set, the IRE bit will be cleared during an interrupt acknowledge cycle answering that interrupt and the interrupt request is disabled. The IRE bit is normally re-enabled as part of the interrupt service routine in software.

2. VMEbus requires that IACKOUT* (when asserted) be released within 30 nanoseconds after the rising edge on AS* toward the end of an interrupt acknowledge cycle (see VMEbus Specification, Rev. C.1, Figure 4-17 and RULE 4.41). The MC68153 cannot meet this specification with the $\overline{IACK}$ High to $\overline{IACKOUT}$ High Delay of 35 nanoseconds max (this being the means to negate $\overline{IACKOUT}$). Figure 7 shows how an F74 flip-flop is added to solve this problem.

   If the BIM $\overline{IACKOUT}$ is asserted, this condition is fed back and used to negate $\overline{IACK}$ to the BIM. The negative going edge of $\overline{IACKOUT}$ being asserted does not affect the F74 clock that it drives. However, the negation of $\overline{IACK}$ causes the negation of $\overline{IACKOUT}$ high which clocks the F74 flop loading a high (or a "one"). The $\overline{Q}$ output goes low passing IACKOUT* to the VMEbus.

   Now when AS* goes high, this condition clears the F74 flop and brings IACKOUT* back high. The delay of the AS* buffer and the F74 flop is less than the required 30 nanoseconds.

3. The MC68153 $\overline{DTACK}$ must be used to enable the VMEbus data buffers (LS645-1 in Figure 7) during an interrupt acknowledge cycle in which the BIM is responding. (The data buffers are enabled by the address decode $\overline{ADDEN}$ signal during a read or write cycle). As a result $\overline{DTACK}$ must be delayed to the VMEbus sufficiently long to allow the data buffers to settle. Setup time for the VMEbus data with respect to DTACK* is 0 nanoseconds minimum.

FIGURE 13 — RESET

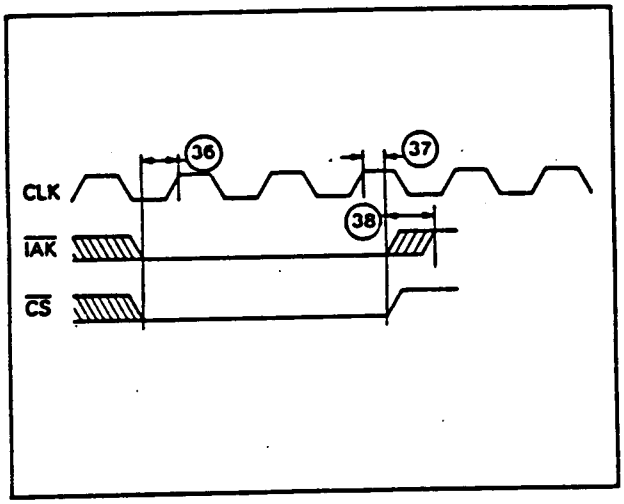



FIGURE 14 — CLOCK WAVEFORM