VMEbus Vertical Interconnect

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1.0 INTRODUCTION

The Vertical Interconnect module allows a standard VMEbus crate to be expanded, by accessing other remote VMEbus crates over a 60 MHz serial link. The Vertical Interconnect consist of a master and one to four slave cards. The master's memory map is segmented into 16 Mbytes blocks that are assigned to each of the four slave crates, so that a simple move instruction causes a read or write to occur on the backplane of the appropriate slave crate (See figure 4.0).

2.0 GENERAL DESCRIPTION

The Vertical Interconnect consists of a master module connected to four slave modules via a serial transmit and receive twisted pair cable for each slave. The Vertical Interconnect uses AMD's Taxi chip set (AM7968 and AM7969) to communicate at 60 MHz. A Vertical Interconnect module can serve as either a master or slave module, determined by the jumpers and PLD's (programmable logic device) on the module. All slave accesses are transparent to the master crate. The slave reads and writes data, returning DTACK to the master crate, as though the VMEbus cycle was done on the master's backplane. The Vertical Interconnect allows byte, word or long word, supervisory or non-privileged memory or short I/O cycles.

The Vertical Interconnect also allows the slave and master to cause an interrupt in each other's crate. The interrupt cycle returns the vector stored in a BIM (bus interrupter module) by the crate CPU in which the interrupt was done. The vertical Interconnect also allows the master crate to cause a reset in the slave crate.

The Vertical Interconnect module can be jumpered to serve as a VMEbus slot one controller. As a slot one controller, the module can be a four level arbiter, for either priority or round robin arbitration. When configured as a slot one controller the module can supply the SYSCLK. The module, as a controller, has two time-out timers, one for arbitration and one for data accesses.

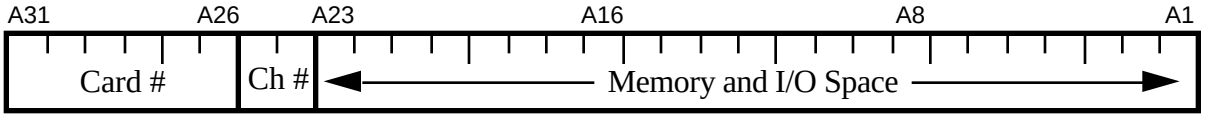
There are seven LED's on the master module front panel. The LED's indicate module select, BERR, transmission violations and which of the four slaves is being accessed. There are four LED's and a pushbutton on the slave module front panel. The LED's show module select, BERR, transmission violations and master accesses. The pushbutton, when the module is configured as a slot one controller, causes a reset.

2.1 FUNCTIONS OF THE MASTER

The Vertical Interconnect master is an A32:D32,D16,D08(EO) module. It appears as a 64 Mbyte block of memory. Full VMEbus handshaking is provided, and a BERR will be driven onto the master's VMEbus if DTACK is not received within a preselected time. The master is also an A16:D16,D08(EO) module. It appears as 512 bytes of short I/O. Located in this block of memory are the BIM and locations, that when written to, cause interrupts and resets in the slave crates.

2.2 MASTER ADDRESS DECODING

The master Vertical Interconnect compares addresses A32 thru A26 to an onboard switch to determine in which 64 Mbytes the module resides. Address bits A25 and A24 then determine which one of four slave crates is being addressed. If the master has been selected and address bits A23 thru A16 are ones ($FF), Then the master changes the address modifiers sent to the slave. This causes a short I/O cycle to be done in slave crate.



Master Memory Address Space
Figure 1.0

Host Address	Slave Crate	Slave Crate Address
$X0000000-$X0FEFFFF	Crate 0 Memory	$000000-$FEFFFF
$X0FF0000-$X0FFFFFF	Crate 0 I/O	$0000-$FFFF
$X1000000-$X1FEFFFF	Crate 1 Memory	$000000-$FEFFFF
$X1FF0000-$X1FFFFFF	Crate 1 I/O	$0000-$FFFF
$X2000000-$X2FEFFFF	Crate 2 Memory	$000000-$FEFFFF
$X2FF0000-$X2FFFFFF	Crate 2 I/O	$0000-$FFFF
$X3000000-$X3FEFFFF	Crate 3 Memory	$000000-$FEFFFF
$X3FF0000-$X3FFFFFF	Crate 3 I/O	$0000-$FFFF

X= SW1 Setting
Master Memory Space
Table 1.0

Examples:
1. *If the onboard address switch is set as 000100 then $11A00000 goes to crate 1 address $A00000.*
2. *If the onboard address switch is set as 000100 then $11FF1000 goes to crate 1 short I/O address $1000.*

If A32 thru A16 is $FFFF and A15 thru A9 compares to the onboard address switch, then the master's I/O is selected. The first sixteen bytes are the BIM IC. (see the MC68153 data sheet for the register addresses) BIM data is accessed only on D7 - D0, but DTACK is returned on both bytes. Writing to next eight bytes causes interrupts in the slave crates. Resets are caused by writing the next eight bytes.

Host Address	Action	Device
$FFFFX000-$FFFFX00F	Read/Write	BIM
$FFFFX010	Write	Interrupt Slave Crate 0
$FFFFX012	Write	Interrupt Slave Crate 1
$FFFFX014	Write	Interrupt Slave Crate 2
$FFFFX016	Write	Interrupt Slave Crate 3
$FFFFX018	Write	Reset Slave Crate 0
$FFFFX01A	Write	Reset Slave Crate 1
$FFFFX01C	Write	Reset Slave Crate 2
$FFFF001E	Write	Reset Slave Crate 3

X = SW1 Setting
Master I/O Space
Table 2.0

Example: *If the onboard address switch is the same as in the previous example (000100), then the BIM IC is at $FFFF1001 - $FFFF100F (odd bytes). Writing to $FFF1012 causes an interrupt in the slave crate 1. Writing to $FFFF101C causes a reset in the slave crate 2.*

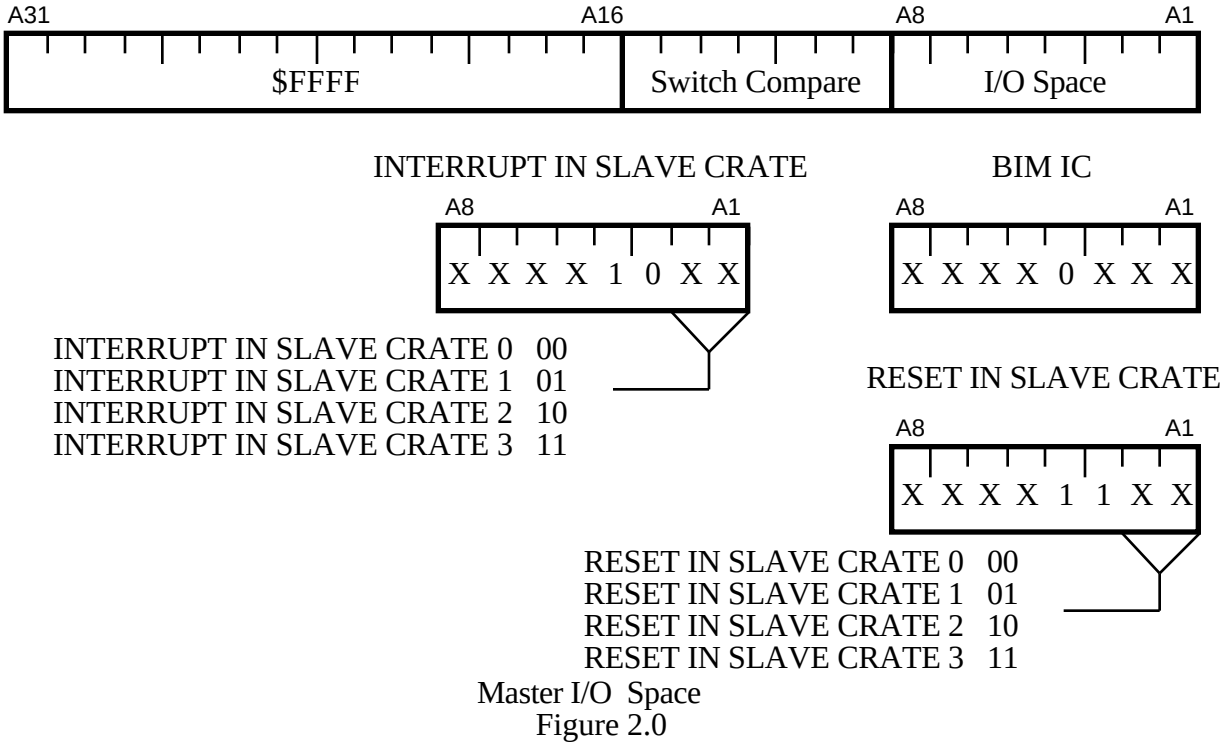


Figure 2.0

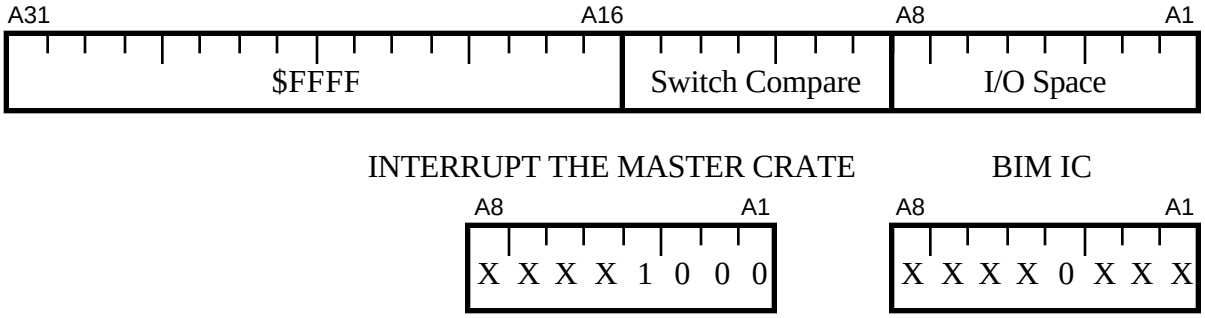
2.3 FUNCTIONS OF THE SLAVE

The slave Vertical Interconnect is a master in the local crate. As a master, it does A24:D32,D16,D08(EO) transfers. The slave Vertical Interconnect is also a slave in the local crate. As a slave, the Vertical Interconnect is an A16:D16,D08(EO) module. The slave Vertical Interconnect appears as 512 bytes of short I/O in the local crate. Located in this space is the BIM for vectors for the master to slave interrupt and a byte that when written, causes an interrupt in the master crate.

2.4 SLAVE ADDRESS DECODING

The slave Vertical Interconnect accesses the VMEbus using the address, data and control signals supplied by the master. The slave does a VMEbus cycle as determined by these signals supplied by the master. The DTACK and any data (read cycle) is then returned to the master.

The slave does respond to an A16:D16,D08(EO) local cycle. The slave compares A15 thru A9 to the onboard switch to access the slave local I/O. The first sixteen bytes of I/O is a BIM IC. Again, as in the master, data is return only on D7 thru D0, but DTACK is return on both bytes. Writing to either of the next two bytes causes the slave to interrupt the master. The slave cannot cause a reset of the master.



Slave I/O Address Space
Figure 3.0

Slave Address	Action	Device
$X000-$X00F	Read/Write	Bim
$X0100	Write	Interrupt Master

X= SW1 Setting
Slave I/O Space
Table 3.0

Example: *If the onboard switch is set so A16 thru A9 is 000100 and the access is short I/O, then $1000 thru $100F is the BIM IC address space . Writing to $1010 or $1011 causes the slave to interrupt the master.*

2.5 SLOT ONE CONTROLLER FUNCTIONS

The slot one controller functions are provided by a Mizar's VME1000 IC. This is a completely VMEbus compatible system controller on a chip. It provides arbitration, both priority or round-robin. It has power-up reset circuity, 16 MHz SYSCLK driver, BERR watchdog timer, and an arbitration watchdog timer.

The BERR watchdog timer simply monitors the VMEbus data strobes and asserts the BERR signal if either of the strobes have been asserted for more than 64/128 microseconds. The VME1000 also monitors the progress of a given bus arbitration and re-arbitrates if the bus is not taken by a master within 16 to 32 microseconds.

2.6 SWITCH AND JUMPER USES

There are only two switches on the Vertical Interconnect. Switch SW1 is a nine position DIP switch used for the address comparison. A PLD on the master module compares both A32 thru A 26 and A16 thru A9 to this switch depending on the address modifiers. Therefore, if the master resides at $10000000 for master to slave accesses, then the master's short I/O address for the local VMEbus accesses is at $1000.On the slave module, SW1 is used only for address comparisons for short I/O accesses to the slave from the local VMEbus. Switch SW2 is the front panel pushbutton switch. If the Vertical Interconnect is configured as a slot one controller, then this switch causes a reset in the local crate.

Jumpers J1 - J8, when installed, connect the cable shield to the local ground. Typically this is done at the master end of the cables only.Jumper J9 selects which of the bus grant levels is enable or passed on. Jumper J12 selects the level of the bus request.

J9 and J12 must be set together (see table 5.0). Jumper J15 enables the VMEbus slot one controller arbiter. Jumper J14 then determines the type of arbitration, priority or round robin. Jumper J10 enables the slot one controller's system clock on to the VMEbus. Jumper J11 enables the slot one controllers BERR signal on to the bus.Jumper J13, in conjunction with the correct PLDs, determines whether the Vertical Interconnect is a master or slave.

JUMPER	FUNCTION	OPTIONS
J1	GND.Shield	Connect ground to channel #0 transmitter shield (enable = in)
J2	GND. Shield	Connect ground to channel #0 receiver shield (enable = in)
J3	GND. Shield	Connect ground to channel #1 transmitter shield (enable = in)
J4	GND. Shield	Connect ground to channel #1 receiver shield (enable = in)
J5	GND. Shield	Connect ground to channel #2 transmitter shield (enable = in)
J6	GND. Shield	Connect ground to channel #2 receiver shield (enable = in)
J7	GND. Shield	Connect ground to channel #3 transmitter shield (enable = in)
J8	GND. Shield	Connect ground to channel #3 receiver shield (enable = in)
J9	VMEbus priority grant level	Select level o,1,2,3 or isolated configuration (see table 2.0)
J10	SYSCLK Enable	If the arbiter is enabled (J15) then J10 enables the sysclock onto the VMEbus (enable = in)
J11	BERR Enable	Enable BERR onto the module if not slot one controller or onto the VMEbus backplane if slot one controller (enable = in)
J12	VMEbus Requester Priority level	Select level o,1,2,3 or isolated configuration (see table 2.0)
J13	Enable Master	With the master PLD's installed, enables the module to be a master (enable = in)
J14	Enable Priority	If the arbiter is enable, J14 sets the type of arbitration. (Out = priority In= Round Robin)
J15	Enable Arbiter	Enable arbiter and slot one functions (enable = in)
J16	Enable Receiving Transmission violations	Enable transmission violations to halt the on going cycle in the slave (enable = in)

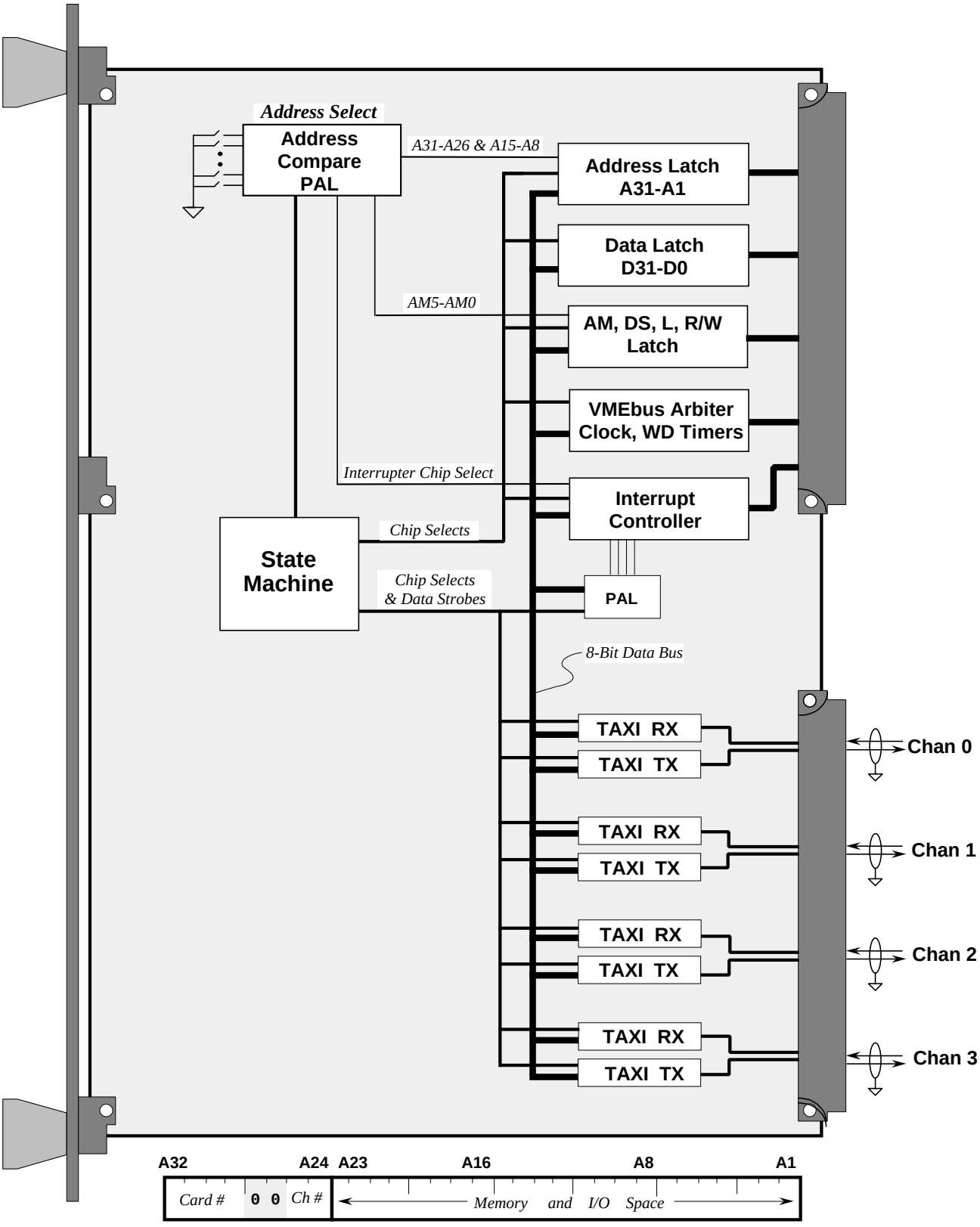
Jumper Settings
Table 4.0

J9 AND J10	SELECTED PRIORITY LEVEL
J9 1-16, 2-15, 13-14, 11-12, 9-10 J12 4-5	VMEbus requester level 3
J9 15-16, 3-14, 4-13, 11-12, 9-10 J12 3-6	VMEbus requester level 2
J9 15-16, 13-14, 5-12, 6-11, 9-10 J12 2-7	VMEbus requester level 1
J9 15-16, 13-14, 12-11, 7-10, 8-9 J12 1-8	VMEbus requester level 0
J9 15-16, 13-14, 11-12, 9-10 J12 none	Module requester isolated from the VMEbus, but passes requests through

Bus Request/Grant Settings
Table 5.0

3.0 CONCLUSION

The Vertical Interconnect is configured as a master slave connection that allows the master crate to read and write 16 Mbytes of memory in each of four remote crates. By structuring the Vertical Interconnect to be completely memory mapped, software overhead is minimized. Even a simple "bug"-type monitor program can be used to test equipment in a mult-crate system There is no message protocol. The remote crate simply appears as slow memory, so no resource reservation is needed. Byte, word, and long word accesses in standard 24-bit and short 16-bit addressing is supported in the slave crate. A long word read or write is typically 4 uS.



VMEbus Serial Vertical Interconnect

60 MHz Serial Bit Rate

m/s 101989