Fermi National Accelerator Laboratory

DZERO Central Tracking Upgrade
VME Readout Buffer Controller - VRBC

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--PRELIMINARY--

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1 GENERAL INFORMATION

1.1 System Introduction

1.2 Description of Component & how it fits Into The System

The VME Readout Buffer Controller **VRBC** is a module designed to remove control traffic from the VME bus during data acquisition; this function is performed by instructing the VRB modules[1] via a custom J3 backplane in a standard VME VIPA crate. In addition, the VRBC allows for a centralized interface to the Trigger System so that Event Data can be readout from the VRB's in the correct order. Trigger information is received through the SCL[2] receiver mezzanine card, which carries all the information required by the VRBs to be able to operate in a DZERO Run II environment. Figure 1, Shows the location of this module within the overall Central Tracking readout electronics.

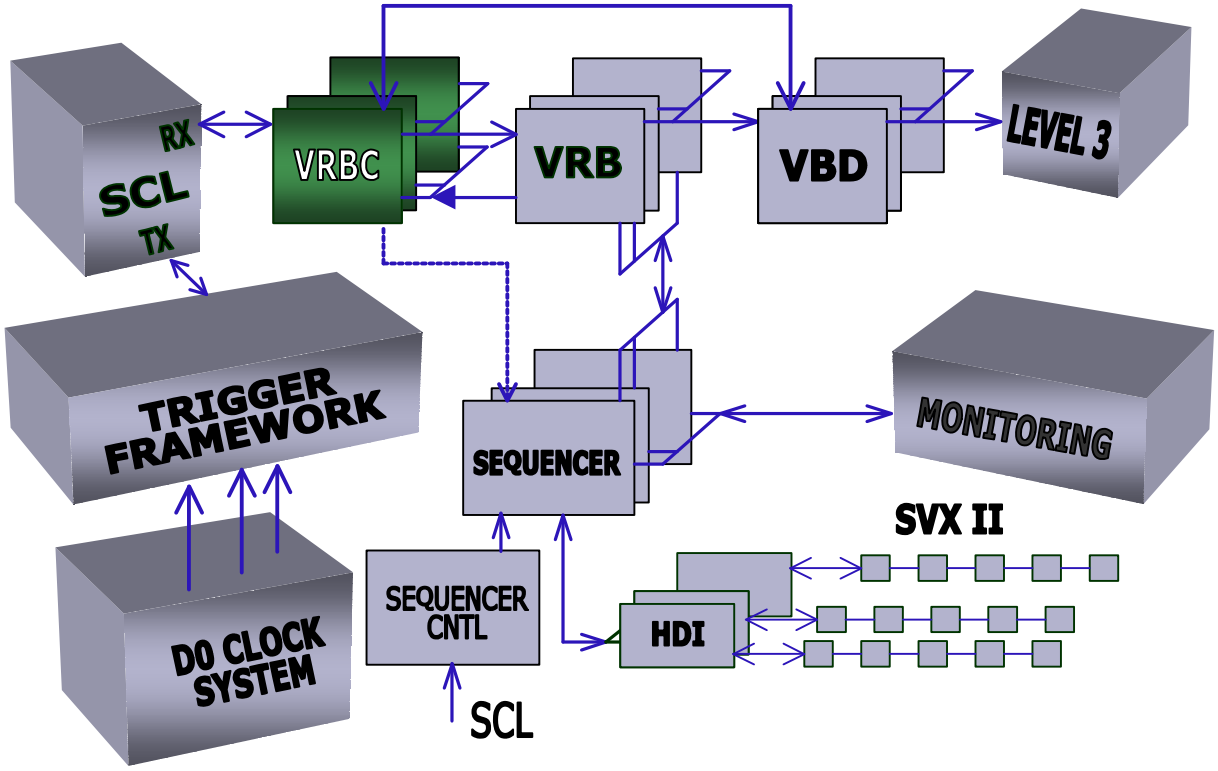


Figure 1. The VRBC in the Central Tracking Readout Electronics

[1] VME Readout Buffer. Description available at http://www-ese.fnal.gov/eseproj/svx/vrb/vrb.htm
[2] SCL, Serial Command Link. Description available at http://www.pa.msu.edu/hep/d0/ftp/scl description

1.3 Features and Functions

- 9U x 400mm VME board
- VME Slave capabilities. Modes: A32/A24/A16 // D32/D16/D8 read and write cycles
- Controls up to 14 VRBs in a single VME crate through the J5/6 backplane connector
- Internal 53.104 MHz. Clock (used in "Autotest" mode)
- *In-Situ* re-programmability
- Provides a Crate ID number
- Operates in Auto-test mode if the SCL is not present
- Operates as a VME level programmable, interrupt requester
- Records relevant real time event information for diagnostic purposes when certain types of errors occur.
- Front panel connectors available for various signals for diagnostics and monitoring purposes.
- Front Panel LEDs indicate the status of the System.

1.4 Block Diagram

Figure #2 depicts a block diagram of the VRBC module and a cursory description follows.

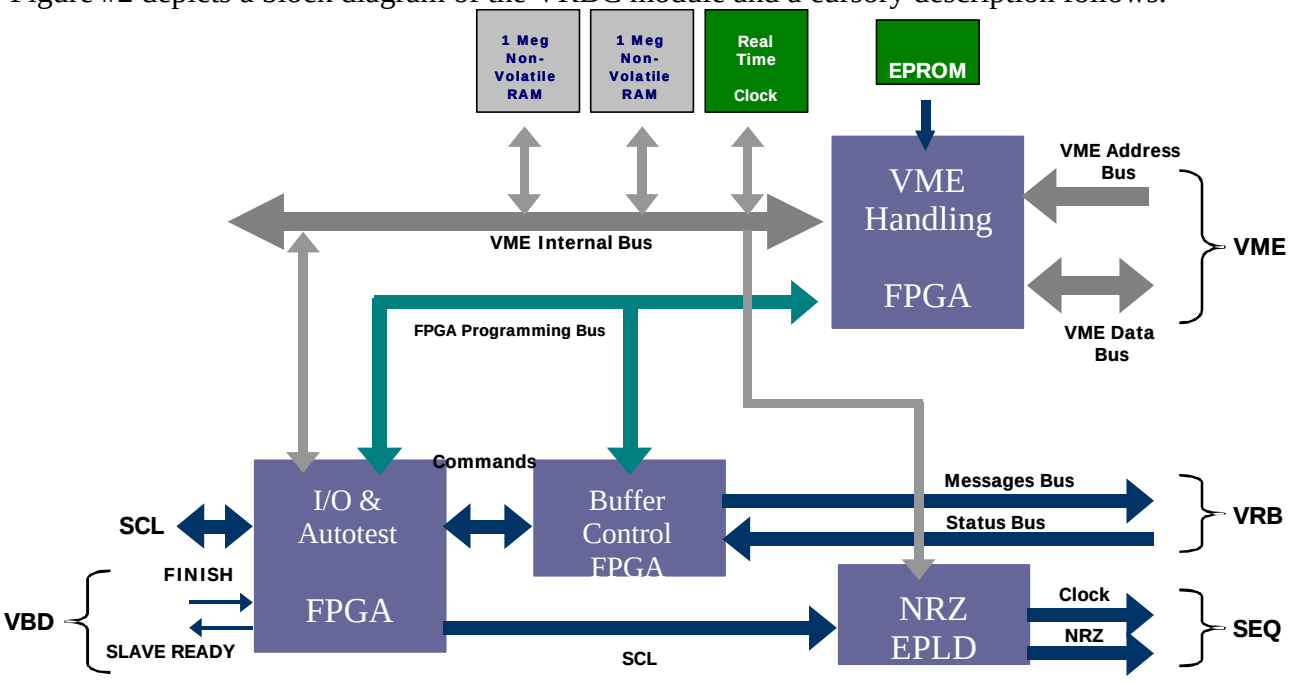


Figure # 2. VRBC Block diagram

The VRBC acts as the interface between the VRB modules and the D0 Clock System and Trigger Manager System. Signals received from these systems are decoded and distributed to the VRBs in the crate. The transport of the commands from VRBC to VRB is done via a custom J3 backplane.

Internally, the VRBC consists of four main functional blocks, shown in blue color in Figure#2.

- VME Handling,
- Autotest and I/O
- Buffer Control
- Non- Return to Zero Code Generator (NRZ)

Each one of these blocks is implemented in an Altera Field Programmable Field Array (FPGA) device, except the NRZ generator, which fits into an Erasable Programmable Logic Device (EPLD).

Being the FPGAs SARAM-based devices, an EPROM configuration device (Altera part # EPC1) with an on-chip oscillator and its own length counter, allows the *VME Handling* FPGA to be either, reprogrammed whenever the design changes, or initialized at power up. At power-up the other two FPGAs are reconfigured, over an internal programming bus. This is accomplished by transferring into them programming data previously stored in non-volatile memories.

Alternatively, all these devices support the JTAG (Joint Test Action Group) programming method, which is IEEE Std. 1149.1-1 compliant. In this case the FPGAs loose their programming information whenever a power shutdown takes place.

1.5 Addressing Modes and Memory Map

The VRBC responds to Short I/O, Standard and Extended addressing modes and data transfers are achieved in 8,16 and 32-bit formats. Table #1 shows the assignment of VME space and the different addressing modes to access it.

Addressing Mode	*Address Range (Hex)*
Short I/O	C000 – C0FF
Standard I/O	480000 – 48FFFF
Extended I/O	80480000 – 8048FFFF

Table #1. VRBC Addressing Modes

A total of 64K bytes are assigned to each module in a given crate in the DZERO environment.

The distribution of this memory space assignment, is carried out according to the following memory map:

Address	Description	R/W	Size
XX480000	Non volatile RAM 0 *	R/W	Byte
XX480002	Non volatile RAM 1 *	R/W	Byte
XX480006	Non volatile RAM (Start/Stop) *	R/W	Byte
XX480008	Crate ID Number	R	Word
C0D0	Crate ID Number (Short I/O space)	R	Word
XX48000A	Reset *	R/W	Word
XX48000C	Interrupt Status/ID Register (vector address)	R/W	Byte
XX48000E	Interrupt Control Register	R/W	Byte
XX480010-XX48008E	Event error & diagnostic information (non-volatile Time-Keeping RAM)	R	Word
XX480090	Time Set – seconds	R/W	Word
XX480092	Time Set – minutes	R/W	Word
XX480094	Time Set – hour	R/W	Word
XX480096	Time Set – day	R/W	Word
XX480098	Time Set – date	R/W	Word
XX48009A	Time Set – month	R/W	Word
XX48009C	Time Set – year	R/W	Word
XX48009E	Time Set – century	R/W	Word
XX4800A0	Program FPGA s *	R/W	Word
XX4800A4	Write Command to NRZ	R/W	Byte
XX4800B0	Modulus Counter - Interrupts frequency	R/W	Word
XX4800B2	Path Control – Data Path setting	R/W	Byte
XX4800B4	Serial Number	R	Byte
XX4800D0	SlaveRdy & Finish Register	R/W	Byte

Address	Description	R/W	Size
XX4800D2	Status Register	R	Word
XX48800E	Autotest mode 2	R/W	Word
XX488010	Autotest mode 3	R/W	Word
XX488012	Normal Operation *	R/W	Word
XXXXC0D2	L3 Transfer Number (short I/0 space)	R	Word
(*) These memory locations are not registered on the board; they act as memory locations to issue commands. For instance, writing to the VME memory location 8048000A causes a RESET signal to be generated. It should be interpreted as a command.			

Table #2. VRBC Memory Map

Internally, the address bus is 16 bits wide and the data bus is 32 bits wide.

1.6. Interfaces

The VRBC Module communicates with the outside world according to the diagram shown in Figure #2. The systems that communicate with this board, unidirectional or bi-directionally are:

- VME Processors (VME)
- Serial Command Link (SCL)
- VME Readout Buffer (VRB)
- VME Buffer Driver (VBD)
- SVX Sequencer

1.6.1. VME

The VRBC can be accessed from any VME processor in the crate capable of performing the following addressing modes and data cycles:

Address Modifier	Description	Data Cycles	Add. Range
3D	Standard Supervisory Data Access	D8/D16/D32	480000–48FFFF
39	Standard Non-privileged Data Access	D8/D16/D32	480000–48FFFF
0D	Extended Supervisory Data Access	D8/D16/D32	80480000–048FFFF
09	Extended Non-privileged Data Access	D8/D16/D32	80480000–048FFFF
2D	Short Supervisory Data Access	D8/D16/D32	C000 – C0FF
29	Short Non-privileged Data Access	D8/D16/D32	C000 – CFFF

All the required signals for accessing VRBC's internal registers and memory locations are available through the standard J1 & J2 VIPA compliant connectors.

1.6.2 SCL

Communication with the Serial Command Link is carried out via the proposed PC-MIP Type II Receiver mezzanine card[3]. Signals and their description are shown in Table #4.

Signal	Description
SCL_READY	**Serial Command Link Ready Status**
SCL_SYNC_ERROR	**Serial Command Link Synchronization Error**
SCL_DATAERROR *	**Serial Command Link Data Error**
SCL_ACK	**Acknowledge & Clear SCL Error Flags**
CLK_53	**53 MHz Clock**
CLK_7	**7.5 MHz Clock**
CURRENT_TURN[15..0]	**Current Turn Number**
CURRENT_BX[7..0]	**Current BX Number in this Turn**
FIRST_PERIOD *	**First Period in a Turn Marker**
BEAM_PERIOD *	**Period with Beam Marker**
SYNC_GAP	**Sync Gap Marker (no L1 Accepts)**
COSMIC_GAP *	**Cosmic Gap Marker (only Cosmic L1 Accepts)**

[3] Specifications available in http://www-ese.fnal.gov/d0trig/sclrcv.pdf

SPARE_PERIOD *	Spare Period Marker
L1_PERIOD *	Period with L1 Accept Issued
L1_ACCEPT	L1 Accept to this Geo Section
L1_TURN[15..0]	Level 1Turn Number
L1_BX[7..0]	Level 1 BX Number in this Turn
L1_QUAL[15..0]	L1 Accept Qualifiers
L2_PERIOD *	Period with L2 Decision Issued
L2_REJECT	This Geo Section L2 Reject
L2_ACCEPT	This Geo Section L2 Accept
INIT_SECTION	Initialize Geographic Section Flag
L1_BUSY	Busy L1 Status
L2_BUSY	Busy L2 Status
L1_ERROR	Error L1 Flag
L2_ERROR	Error L2 Flag
INIT_ACK	Init Acknowledge Signal to Hub-End
SYNC_LOST *	SCL Receiver Synchronization Lost
SPARE_STATUS [1..0]	Spare Status Signals to Hub-End

Table 4. SCL – Signals as seen by the VRBC

(*) Signal no used in the present version [as of 10/22/99]

All these signals are fed into the Autotest and I/O FPGA for subsequent use and processing.

1.6.3. VRB

Communications with the VME Readout Module is performed via a Message Bus and a Status Bus across the J5/6 backplane connector. The primary function of this interface to the VRB boards, is to provide control on how the buffers on the VRB are selected (for reading and writing) during SVX data acquisition and VME readout. Upon reception of a L1 Accept signal, the VRBC provides the VRB with a buffer number for storing data. Upon reception of a L2 Accept signal, the VRBC provides the VRB with the buffer number whose data will be transferred to the VBD module over VME.

A well-defined protocol allows communication between the VRBC and the VRB boards. A 12-bit Message Bus transports information to the VRB, which, in turn, reports its status through a 10-bit Status Bus to the VRBC, so that the proper actions are taken in normal data taking or for diagnostic purposes.

The ***Message Bus*** consists of a 4-bit field indicating the type of message and an 8-bit field with the message value

The following table contains a cursory description of these signals; the reader is encouraged to read reference [1] for a more detailed explanation.

Message Type		Message Value Description
#	Name	
1	Readout Buffer Number	Contains the value of the next buffer number for VRB Input. Value ranges from 0 to 63. Received After L1 Accept
2	Not used	N/A
3	Bunch Xing Number	Contains the Bunch Crossing Number, which forms the lower 8 bits of the 24-bit Geographic Section Beam Xing Number. Received After L1 Accept
4	Scan Buffer Number	Contains the value of the next buffer number for VRB Output. Value ranges from 0 to 63. Received After L2 Accept.
5	Event Number	Contains the Event Number to be inserted into the data stream. Received After L2 Accept.
6-12	Not used	N/A
13	Clear Errors	Clears any error condition on the Status Bus
14	Reset / Re-Start	Value Reset: Resets the input FIFOS on the VRB. Value Re-Start: Reinitializes the entire VRB.

As for the ***Status Bus***, each bit indicates a status signal from the VRBC. These signals are ALL *active low* and are latched at the VRBC. Their description follows:

Bit #	Name	Description
0	Readout Busy	Kept ***active*** when the active channels on the VRB are receiving data. ***Released*** when ALL the channels have received data.
1	Scan Busy	Kept ***active*** when transferring data to the VBD. ***Released*** when all the event data has been transferred over VME
2	Sync Error	Becomes ***active*** when a G-Link sync. Error has been detected. Kept ***asserted*** while the error condition exists
3	Frame error	Becomes ***active*** when an invalid data word has been detected on an active channel. Remains ***asserted*** until the next Message Type 1.
4	Identifier Error	Becomes ***active*** when an invalid event identifier has been detected. Remains ***asserted*** until the next Message Type 1
5	Format Error	Becomes ***active*** when a data format error has been detected. Remains ***asserted*** until the next Message Type 1.
6	Controller Error	Becomes ***active*** when an invalid message has been sent to the VRB. Remains ***asserted*** until a Message Type 13 is received.
7	VRB Error	Becomes ***active*** when the VRB is enabled to process an event correctly. Remains ***asserted*** until a Message Type 1 is received.
8,9	Reserved	N/A

1.6.4. VBD

The VBD module moves event data over VME from the VRBs after the Trigger Framework has issued a L2 Accept. DMA transfers are used to move data to one of the two 256 Kbytes buffers on the VBD.

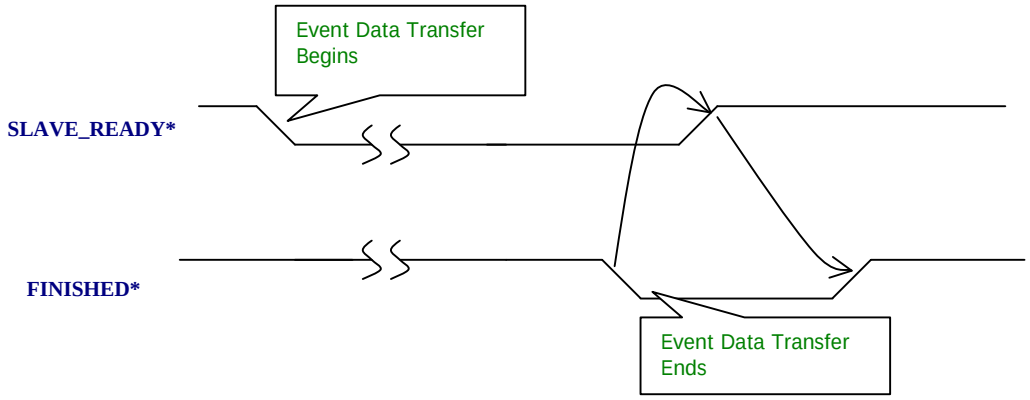
Two signals are required to execute the handshaking between the VME Buffer Driver module and the VRBC: SLAVE READY* and FINISHED*. They are both assumed to be open collector signals and negative true logic. Their description follows:

SLAVE READY*: An active LOW signal that informs the VBD that the VRB buffers are filled with event data and ready to be readout.

FINISHED*: An active LOW signal that informs the VRBC that the VBD has finished reading the VRB buffers.

The acquisition cycle begins when the VRBC announces that a new event data transfer is about to occur after a L2 Accept, this is done by asserting its SLAVE READY signal; the VBD then arbitrates for the bus. Once the mastership of the bus is granted, it is not relinquished until the entire event has been transferred; at that time, FINISHED is asserted and SLAVE READY becomes inactive allowing a subsequent event data transfer.

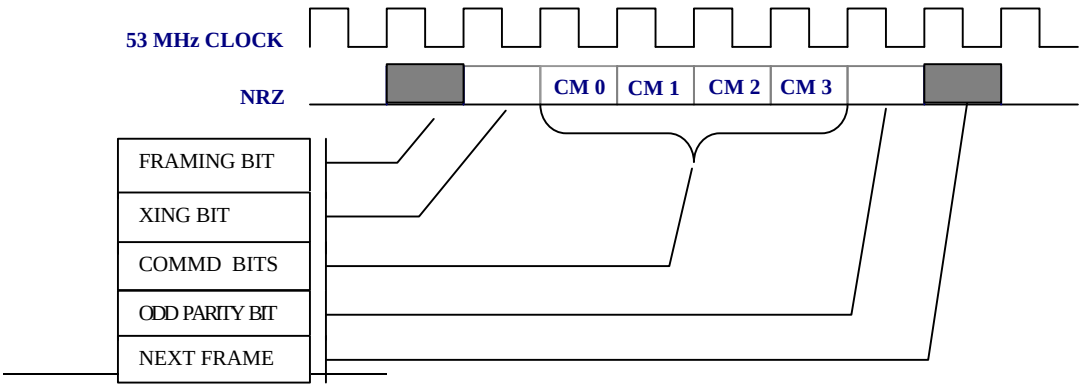
A timing diagram may help to illustrate this hand-shaking concept:



1.6.5. SVX Sequencer[4]

The VRBC provides an alternate path for the Master Clock (53.104 MHz), synchronous to the Tevatron, and the serial 7-bit frame Non-Return-to-Zero (NRZ) encoded signal. These signals are required by the SVX Sequencer board to control the SVX chips for data acquisition. These signals are ECL compatible and available on the front panel twinax connectors. No phase adjustment method is provided on board to compensate for delays due to different length cables or any other factor of skewing. Those adjustments should be provided at the receiver end.

Four bits, out of the seven in the 7-bit NRZ packet are encoded commands. The other three are a framing bit, a parity bit and a crossing bit. Their location within the 7-bit frame is shown below.



[4] SVX Sequencer Board. Description available at http://d0server1/users/utes/default.htm

The decoding of the 4-bit commands is as follows:

Command Bits					Description
Binary				Hex	
CM3	CM2	CM1	CM0		
0	0	0	0	0	Idle
0	0	0	1	1	Acquire
0	0	1	1	3	Trigger
1	0	1	0	A	Ramp
0	0	1	0	2	Digitize
0	1	1	0	6	Readout
0	1	0	1	5	Reset_Preamp
0	1	1	1	7	Cal_Inject
1	0	0	0	8	Reserved
1	0	0	1	9	Reserved
0	1	1	0	4	Reserved
1	0	1	1	B	Reserved
1	1	0	0	C	Reserved
1	1	0	1	D	Reserved
1	1	1	0	E	Reserved
1	1	1	1	F	Reserved

1.7 Interrupts

The VRBC is capable of generating interrupt request on the VME bus allowing synchronization with the embedded processor residing in the VME crate. This feature may allow moving data over the network whenever the L3 System becomes inactive.

Release Mechanism

In the DZERO environment, the code for interrupts uses the computational model RORA, (Release On Register Access) as the release mechanism. With this approach, the interrupt generator (VRBC) only releases its request when the INTERRUPT HANDLER, within the interrupt service routine, accesses a specific register. In the present version of the VRBC, this register is named “INTERRUPT CONTROL REGISTER”.

Phases

Three phases are required to accomplish a successful RORA interrupt operation:

i. Phase 1. Interrupter awaits service

ii. Phase 2: Interrupt Handler reads Status/ID from the Interrupter:

iii. Phase 3: Execution of Interrupt Service Routine

Status/ID (Vector Address) Register

This is an 8-bit R/W register that contains the VRBC's identification required by the Interrupt Handler to determine which module in the crate requested service to an interrupt. The processor into this register must place the ID before any attempt to issue an interrupt request transaction.

Interrupt Control Register

This is an 8-bit R/W register that, when accessed, is used by the Interrupt handler to release the interrupt request line according to the RORA scheme. It also provides three (3) signals that may be utilized by the handler in the Interrupt Service Routine. These signals are:

- ***Interrupt Enable/Disable***[5]: Bit 0

  This signal, allows/disallows the generations of interrupt requests when a new data event was received or when an interrupt request was forced by the Interrupt Reset signal. The power-up value of this bit is LOW (disable)

- ***Interrupt Reset Signal***[5]. Bit 1.

  When read indicates the status of the interrupt request:

  0 – No Interrupt Requested

  1 – Interrupt Request in Progress

  When written:

  0 - The interrupt request line is dropped.

  1 – Generates an interrupt request transaction.

  The power-up value of this bit is LOW.

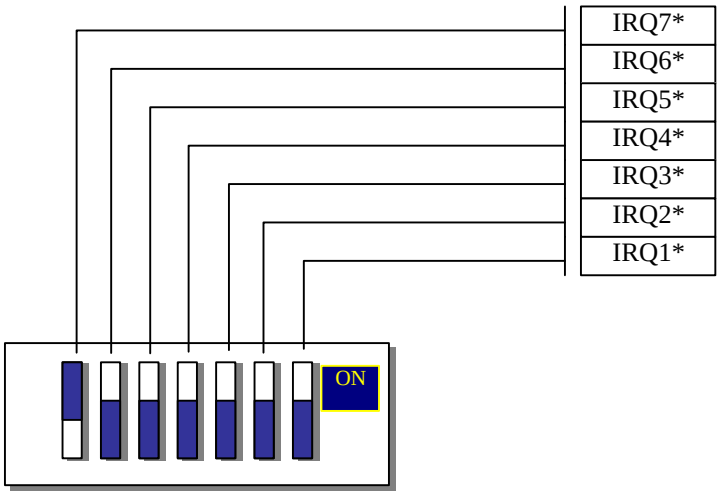
- ***Veto***[5]. Bit 2

  This signal, allows/disallows the processing of further events by the VRBC. The power-up value of this signal is 0. (Processing allowed***)***

Interrupt Levels. Seven priority levels are used on the VRBC, IRQ1* through IRQ7*. All of them are active LOW signals, being IRQ7* the one with highest priority. Only one of them

[5] By document written by Fritz Bartlett, JUL/99

can be used at a time. (IRQ1* OR IRQ2* OR…OR IRQ7*). This is accomplished by setting the dip- switch S1 to the required level as show below.



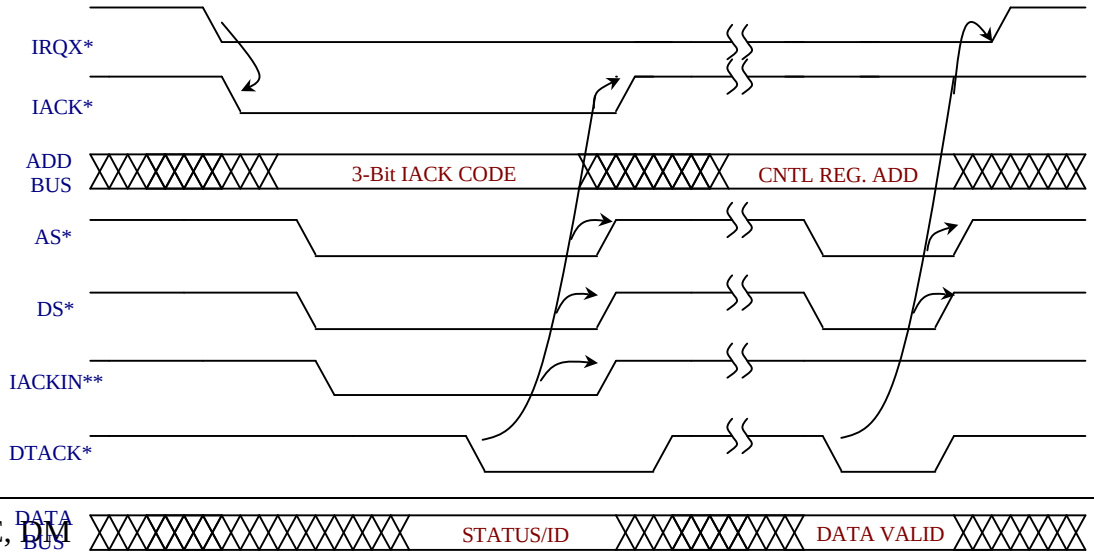
Dipswitch S1, Interrupt Level Setting (IRQ7* is set as an example)

Sources of Interrupt Requests

Either software or hardware can generate an interrupt request. The former is referred to the Interrupt Control Register explained earlier in this section, and the latter is referred to the front panel LEMO connector input. This input is TTL compatible, 50-ohm terminated and buffered inside the board. When the Secondary Data Path is enabled (discussed later in this document), the arrival of an event can cause an Interrupt as well, upon selecting the appropriate mode of operation; in this case the frequency of the interrupts programmed through VME.

Timing Diagram

A timing diagram is presented next to illustrate how an interrupt request is processed. The relevant signals are presented.



Register Addresses

The pertinent VME addresses used to process an interrupt request are:

XX48000C	Interrupt Status/ID Register (vector address)	R/W	Byte
XX48000E	Interrupt Control Register	R/W	Byte
XX4800B0	Counter for Interrupt frequency Setting	R/W	Word

The meaning of each register will be explained in 2.5 in this document.

2 THEORY OF OPERATION AND OPERATING MODES

This section will discuss in some detail several of the VRBC components as shown in the Block Diagram in Figure #2.

2.1 Registers Description

2.1.1. Non-Volatile RAMs

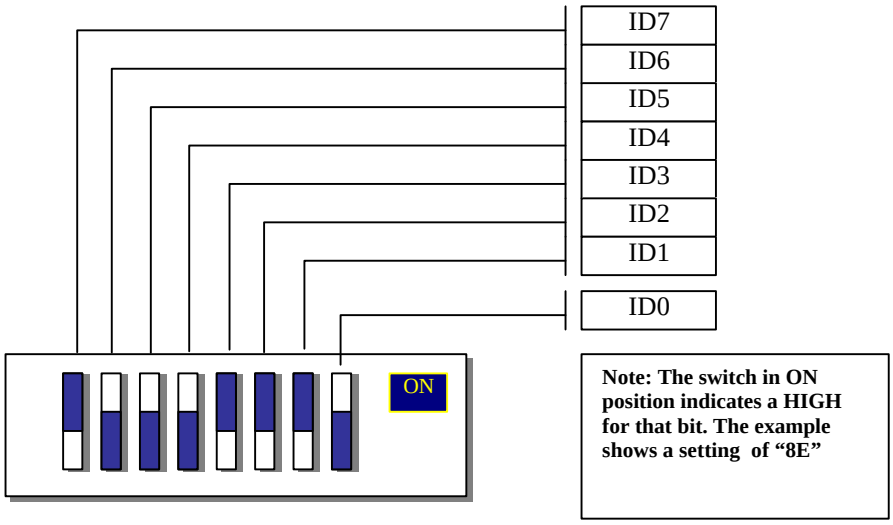
The non-volatile RAMs are used to store the programming data for the AUTOTEST and BUFFER CONTROL FPGAs. These devices are not mapped onto the VME address space; therefore provisions are taken to write into them by addressing the memory locations indirectly. Three (3) VME addresses are provided to achieve this; they are shown in the table below.

VMEADD	Description	Cycle	Size
XX480000	Non volatile RAM 0	W	Byte
XX480002	Non volatile RAM 1	W	Byte
XX480006	Non volatile RAM (Start/Stop)	W	Byte

. The mechanism is as follows: By reading the memory location 480006 hex, the writing cycle begins for a particular device (RAM0 or RAM1). If, for instance, the RAM0 is selected by a write operation in the memory location 480000 hex, data will be written into the device's memory location 0 hex. Further accesses to this address will increment the address pointer one by one. The procedure ends when a new VME "***write***" operation is performed on the memory location 480006 H finishing the write cycle for that particular device.

2.1.2. Crate ID

This is 16-bit, ***read-only*** register. The low order byte indicates the 8-bit crate ID set at the front panel selector; the high order byte indicates the 8-bit crate ID set by the on-board dip-switch **S1** as shown in the figure below.



VME ADD	Description	Cycle	Size
XX480008	Crate ID Number	R	Word

2.1.3 Software Reset

A ***write*** cycle on this memory location will perform a RESET function to the logic of the Autotest and Buffer Control FPGAs

VME ADD	Description	Cycle	Size
XX48000A	Reset *	W	Word

2.1.4. Interrupt Status/ID Register

VME ADD	Description	Cycle	Size
XX48000C	Interrupt Status/ID Register (vector address)	R/W	Byte

This is an 8-bit R/W register used to identify the module that is causing an interrupt and requires to be serviced by the Interrupt handler. This register must be downloaded prior to the enable of the interrupt requests generated by the VRBC.

2.1.5. Interrupt Control Register

VME ADD	Description	Cycle	Size
XX48000E	Interrupt Control Register	R/W	Byte

This is an 8-bit R/W register that, when accessed, is used by the Interrupt handler to release the interrupt request line according to the RORA scheme. It also provides three (3) signals that may be utilized by the handler in the Interrupt Service Routine. These signals are:

- ***Interrupt Enable/Disable***[7]: Bit 0

  This signal, allows/disallows the generations of interrupt requests when a new data event was received or when an interrupt request was forced by the Interrupt Reset signal. The power-up value of this bit is LOW (disable)

- ***Interrupt Reset Signal***[5]. Bit 1, when read indicates the status of the interrupt request:

  0 – No Interrupt Requested

  1 – Interrupt Request in Progress

  When written:

  0 - The interrupt request line is dropped.

  1 – Generates an interrupt request transaction.

  The power-up value of this bit is LOW.

- ***Veto***[5]. Bit 2

  This signal, allows/disallows the processing of further events by the VRBC. The power-up value of this signal is 0. (Processing allowed***)***

[7] By document written by Fritz Bartlett, JUL/99

2.1.6. Real Time Clock Settings

A group of write-only memory locations (from 480090 through 48009E) allows programming the settings of the Real Time Clock embedded into the Non-volatile Time-keeping RAM. The VME addresses and their functions are shown in the table below.

VME ADD	Description	Cycle	Size
XX480090	Time Set – seconds	R/W	Word
XX480092	Time Set – minutes	R/W	Word
XX480094	Time Set – hour	R/W	Word
XX480096	Time Set – day	R/W	Word
XX480098	Time Set – date	R/W	Word
XX48009A	Time Set – month	R/W	Word
XX48009C	Time Set – year	R/W	Word
XX48009E	Time Set – century	R/W	Word

These addresses are basically a translation of the device's memory locations to the VME address space. For completeness the reader is encouraged to get more detailed information and parameters entry format at the Web site

http://www.dalsemi.com/DocControl/PDFs/1743p.pdf

2.1.7. FPGAs Programming

VME ADD	Description	Cycle	Size
XX4800A0	Program FPGA s *	W	Word

A VME ***write*** cycle on this memory location, will perform the re-programming of the AUTOTEST & IO FPGA and the BUFFER CONTROL FPGA with the contents of the programming data previously stored in the non-volatile RAMs. This process is identical to that done at power-up.

2.1.8. AUTOTEST Modes

In the absence of the Serial Command Link, the VRBC can operate in AUTOTEST mode, meaning that some of the SCL signals can be emulated and external input signals can be used to test the VRBC functionality and its communication with the outside world. When working in any of the ***Autotest modes***, a local crystal oscillator provides the 53.104 MHz clock required by the logic to properly emulate the SCL link signals. The setting of any of these modes will override the clock signal originated at the Trigger Framework.

There is provision for three different Autotest modes:

Autotest mode 1: In this mode, some SCL signals can be emulated using VME commands. These commands are stored sequentially into an internal Dual Port Memory (DPM) and executed one at the time every 132 ns. Up to16 commands can be stored in the DPM and their definition follows:

Value	Description
1	Init
2	L1 Accept
3	L2 Accept
4	L2 Reject
5	Sync Gap
6	Finished
7-15	Spare

The “Value” (1-15) specified in the first column is the number to be written into the VME address specified below in order to emulate the signal specified in the second column.

VME ADD	Description	Cycle	Size
XX48800A	Write commands in Autotest mode	W	Word

To execute the sequence of signals previously written into the DPM, a VME ***Write*** transaction should be performed on the following VME address:

VME ADD	Description	Cycle	Size
XX48800C	Autotest mode 1	W	Word

Autotest mode 2: In this mode an external L1 trigger signal, L1 Test Beam (see front panel diagram for its location) is required to launch the sequence of signals required to process an event in the absence of the SCL. The associated VME address to issue this command is:

VME ADD	Description	Cycle	Size
XX48800E	Autotest mode 2	W	Word

The following table illustrates the different modes of operation when this option is used:

Value	Action performed	Description
0	Continuos Mode	A series of events are processed upon the arrival of an external trigger signal.
1	One Event	One event is processed upon the arrival of an external trigger signal.
2	Stop	Stops the continuous mode.

Autotest mode 3: Same as above, except that it requires an external Laser L1 Trigger and the resulting trigger signal is delayed by 396 ns. The associated VME address to issue this command is:

VME ADD	Description	Cycle	Size
XX488010	Autotest mode 3	W	Word

2.1.9. Normal Operation Mode

This is the mode of operation of the VRBC by default. In this mode, all the signals required to perform a DAQ cycle come directly from the SCL Mezzanine Card. After the selection of any of the Autotest modes, a Normal Operation can be resumed by issuing a VME ***write*** command to the memory location shown below.

VME ADD	Description	Cycle	Size
XX488012	Normal Operation	W	Word

2.1.10. Slave Ready and Finish Handshaking emulation Register

When using the SDAQ path, VRB data can be moved over VME to either the VBD or to the embedded processor. If the latter is the case, the VRBC provides a mechanism to emulate the SLV RDY & FINISH protocol using an 8-bit VME accessible register.

VME ADD	Description	Cycle	Size
XX4800D0	Slave Ready & Finish Register	R/W	Byte

The bit assignments is as follows:

Bit 0 – Slave Ready* - Asserted when in low state

Bit 1 – Finish* - asserted when in low state

The software should comply with the timing diagram shown in page 10 of this document.

2.1.11. L3 Transfer Number

VME ADD	Description	Cycle	Size
XXXXC0D2	L3 transfer Number (Short I/0 memory space)	R	Word

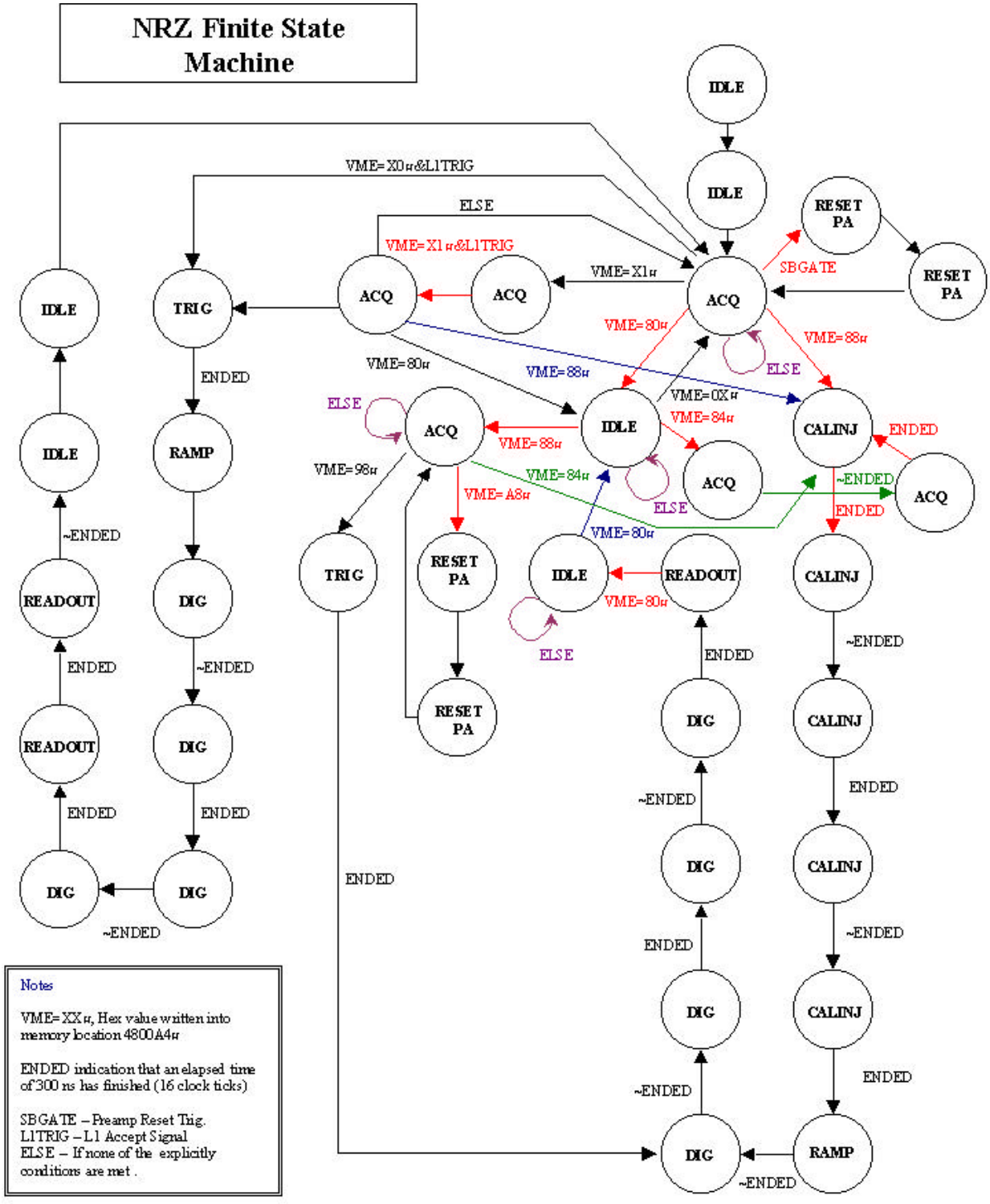
This is a 16-bit read-only register whose contents is the Geographic Section Level 3 Transfer Number that is being 16 assigned to the event that just received an L2 Confirm during a 132 nsec period.

2.1.12. VME NRZ coding

VME ADD	Description	Cycle	Size
XX4800A4	Write Command to NRZ	W	Byte

By writing an encoded byte into this memory location, a sequence of NRZ commands is generated depending upon the current state of the NRZ finite state machine (FSM). The latter ensures that the SVX II chip timing requirements are met. The following diagram of the FSM illustrates the different sequences of commands that can be obtained to instruct the SVX II.

NOTE: The Sequencer Controller has been chosen as the primary source for sending NRZ encoded commands to the sequencers. The code for this section of the VRBC may not match that of the Sequencer Controller.


NRZ Finite State Machine
IDLE
IDLE
RESET PA
RESET PA
VME=X0μ&L1TRIG
ELSE
VME=X1μ&L1TRIG
VME=X1μ
SBGATE
ACQ
ACQ
ACQ
IDLE
TRIG
VME=80μ
VME=88μ
ELSE
VME=80μ
VME=88μ
ENDED
VME=0Xμ
ELSE
ACQ
IDLE
CALINJ
ENDED
IDLE
RAMP
VME=84μ
VME=88μ
VME=98μ
VME=84μ
ACQ
~ENDED
ACQ
VME=A8μ
ELSE
ENDED
~ENDED
VME=80μ
READOUT
DIG
TRIG
RESET PA
IDLE
READOUT
CALINJ
ENDED
ENDED
VME=80μ
~ENDED
~ENDED
RESET PA
ELSE
READOUT
DIG
DIG
CALINJ
ENDED
ENDED
~ENDED
ENDED
DIG
DIG
ENDED
DIG
CALINJ
~ENDED
ENDED
DIG
CALINJ
~ENDED
ENDED
DIG
CALINJ
~ENDED
ENDED
DIG
RAMP
~ENDED
Notes
VME=XXμ, Hex value written into memory location 4800A4μ
ENDED indication that an elapsed time of 300 ns has finished (16 clock ticks)
SBGATE – Preamp Reset Trig.
L1TRIG – L1 Accept Signal
ELSE – If none of the explicitly conditions are met .

2.1.13. Data Path Control Register

VME ADD	Description	Cycle	Size
XX4800B0	Modulus Counter - Interrupts frequency	R/W	Word
XX4800B2	Path Control	R/W	Byte

The VRBC is capable of controlling the path that event data will follow during data taking. To understand this concept, let's define two possible paths the data may take:

Primary Data Acquisition Path (PDAQ)

This is the normal path the data follows during data taking, that is, data is transferred from all the VRB modules to the VBD and subsequently moved to the Level-3 Trigger System.

Secondary Data Acquisition Path (SDAQ)

For run II, it is likely to have a SDAQ path for all of the DZERO sub-detectors. The SDAQ is intended for use during commissioning, calibration runs and whenever the Level-3 Trigger System and its attendant high-speed data path become unusable. It provides a mechanism to move data over the network from the embedded processor in the VME crate to the host servers of the on-line systems. When this path is adopted, the VRBC will generate an interrupt request (whose frequency is programmable) to the embedded processor, which in turn, will respond issuing a veto and so inhibiting further event acquisitions.

In order to accomplish a full data path control, two VME registers are supplied on the VRBC board. A path control register, which allows programming the way the data will follow during data taking, and a Modulus Counter Register, whose contents defines the number of events preceding an interrupt (modulus counter).

The registers' bit assignment follows:

Bit 0 - Path control

Bit 1 – Path Control

Bit 2 – Buffer Size

Bit 3 – L1 BUSY

The Path Control bits have the following function:

REGISTER	Description	Value (hex)
Path Control	None of the Paths is used	00
Path Control	PDAQ Path is used*	01
Path Control	SDAQ Path is used	02
Path Control	Both Paths are used	03

Note: The path must be specified as part of the DAQ initialization process.

Bit 2, defines the size of the VRB buffers. Two buffer sizes schemes are available: 16 buffers of 2K bytes each or 8 Buffers of 4K each.

Bit 2 = 0 – 16*2K

Bit 2 = 1 – 8*4K

Bit 3 – The user can generate a software induced L1 BUSY signal to the Trigger Framework by setting this bit. The BUSY condition is cleared when the bit is reset.

2.1.14. Serial Number

VME ADD	Description	Cycle	Size
XX4800B4	Serial Number	R	Byte

Each one of the VRBC modules has a Serial Number readable through VME as a means to be identified for monitoring and diagnostic purposes. The setting of the bits is hardwired on the board.

2.1.15. Serial Command Link Status Register

XX4800D2	Serial Command Link Status Register	R	Word

This register allows to monitor the front end busy signals (L1 Busy & L2 Busy) and SCL error signals (L1 Error & L2 Error), according to the following bit assignment:

- Bit 0 (LSB) – L1 Busy, asserted when HIGH.
  This signal becomes active when:

  - All the buffers in the available buffers queue on the VRB are FULL. In this case, L1 Busy remains active until one or more buffers are emptied.
  - After a L1 Trigger. In this case, L1 Busy will remain active during data transfer to the VRB's.

- * Bit 1 – L2 Busy, asserted when HIGH.
  This signal becomes active when the queue of pending events -those waiting for a L2 decisions-, is FULL. It will remain active until one or more events receive a L2 decision.

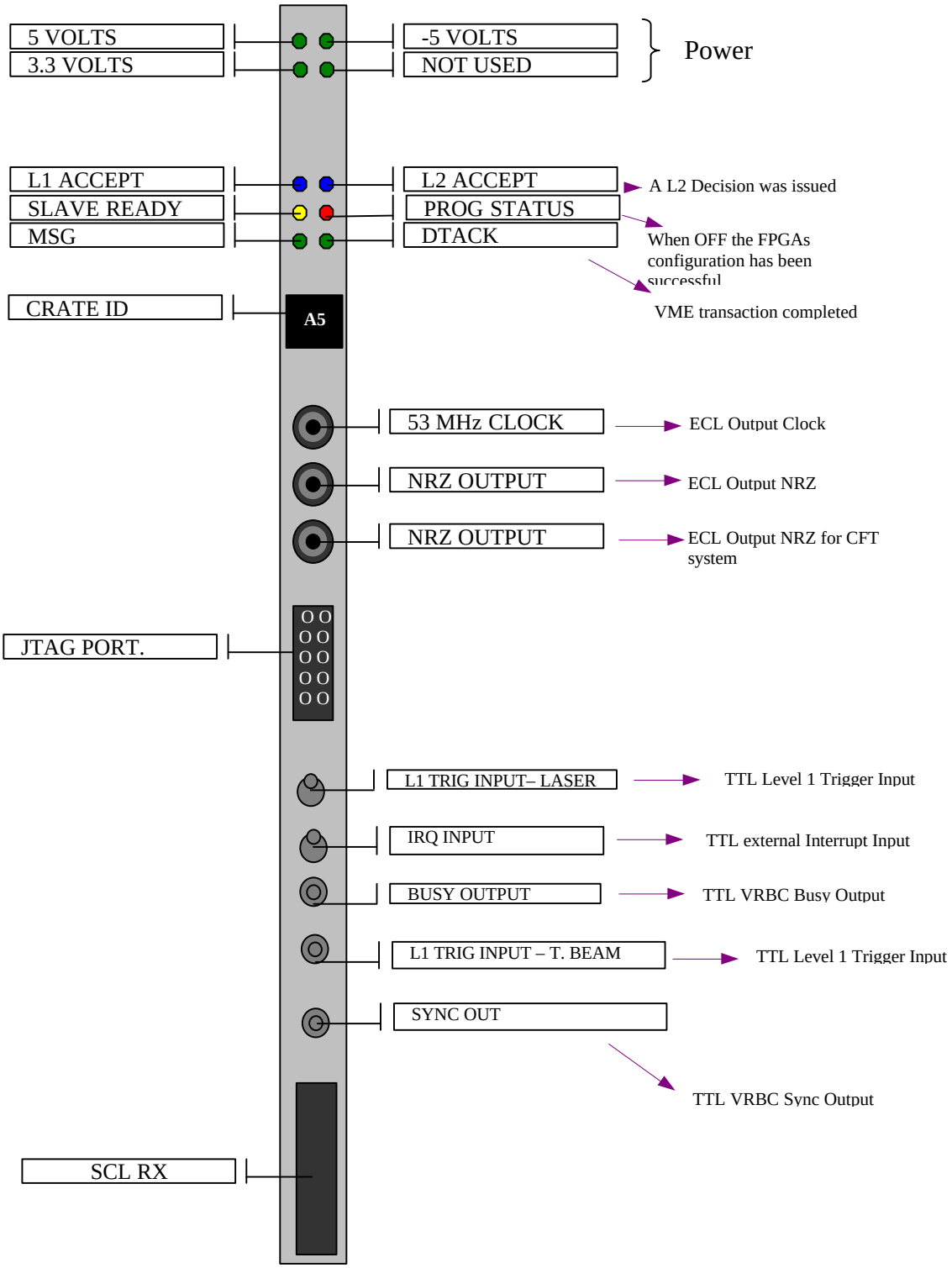
- * Bit 2 – L1 Error, asserted when HIGH.

  Active when there is a mismatch error between the L1 Trigger number and L3 transfer number for a particular event.* Bit 3 – L2 Error, asserted when HIGH.

  Active when there is a mismatch error between a L2 Decision and L3 transfer number for a particular event.

- * Bit4 = Readout Busy* -- (see VRB document)
- * Bit5 = Scan Busy* -- (see VRB document)
- * Bit 6 = Finished* -- (see VBD document)
- * Bit 7 = Success -- This signal is active HIGH when an event has been has completed the whole DAQ cycle (L1 Accept – > L2 Accept –> Finish)
- * Bit 8 = SCL Ready -- Active HIGH. Signals if the SCL Rx card is receiving valid trigger and timing information
- * Bit 9 = SCL Error – Active HIGH. Signals if the receiver has lost frequency lock with the incoming serial data stream.

3. Front Panel Indicators and Connectors



LABEL	FORM	DESCRIPTION
5 Volts	GREEN LED	5 Volts present on the board
-5 Volts	GREEN LED	- 5 volts present on the board
3.3 Volts	GREEN LED	3.3 volts present on the board
L1A	BLUE LED	When it flashes, a L1 Accept signal was issued
L2A	BLUE LED	When it flashes, a L2 Accept signal was issued
SLVRDY	YELLOW LED	When it flashes a Slave Ready Signal was asserted by the VRBC
PROG	RED LED	When ON, the programming of the On-board FPGAs is taking place. When OFF, the programming was successful.
MSG	GREEN LED	When it flashes, a message was sent to the VRB via J3 backplane conn.
DTK	GREEN LED	When it flashes A VME transaction took place
CRATE ID	SELECTOR	Lower portion (8 bits) of the Crate ID
NRZ	TWINAX CONN.	ECL output of the NRZ signal
CLK	TWINAX CONN.	ECL output of the 53 MHz Clock
NRZ_CFT	TWINAX CONN.	ECL Output of the NRZ signal (to the Central Fiber Tracker if needed)
L1 LASER	LEMO CONN	TTL Input – L1 Trigger signal for Laser scan test
IRQ	LEMO CONN	50-0hm terminated TTL Input – External Interrupt Request signal
BUSY	LEMO CONN	TTL Output VRBC Busy signal. Active HIGH when an event data transfer takes place. The Secondary Data Path must be enabled.
L1 T.BEAM	LEMO CONN	TTL Input – L1 Trigger signal for Test Beam test
SYNC OUT	LEMO CONN	TTL Output – Trigger Enable Signal
SCL	NA	Opening to bring in the LM R-200 Coax cable from the Serial Link fan-out modules (Trigger System)

4. Electrical & Mechanical Specifications

4.1. Packaging

The VRBC is a 9Ux400mm (14.437" x 15.748") VME module. The printed circuit board is FR4 with an approximate thickness of 0.092" with a tolerance of Tolerance .008. The board has 8 layers with nominal 50-ohm (±9%) controlled impedance. Four of these layers are for Power/Ground planes and four are for signals. The layers distribution and their thickness follow:

Top	**Layer 1**	**Signal**
		Dielectric .0055"
	Layer 2	**Plane**
		Dielectric .013"
	Layer 3	**Signal**
		Dielectric .013"
	Layer 4	**Plane**
		Dielectric .030" **
	Layer 5	**Plane**
		Dielectric .013"
	Layer 6	**Signal**
		Dielectric .013"
	Layer 7	**Plane**
		Dielectric .0055"
Bottom	**Layer 8**	**Signal**

4.2 Power Requirements

The VRBC power consumption varies from ---- in idle state, to ----- approximately in operation. The Module is fused at 5V, ---A; -5V, ---A; 3.3V ---A.

A APPENDICES

A1 List Of Component Documentation

N/A as of 9/15/00

A2 Schematics

N/A as of 9/15/00

A3 PAL, FPGA Equations

N/A as of 9/15/00

A4 Timing Diagrams

N/A as of 9/15/00

A5 Parts List

N/A as of 9/15/00

A6 Additional Appendices

N/A as of 9/15/00