DAVE FPGA  Input Section

Select a 16 Bit Input Block or the Test Data Register Controlled by Register 11

128 Bits MSA Input Data

Read FIFO Input Data Register 10

Read FIFO Input Data Register 12

Write Enable

16 Bit x 128 Words Dual Port Static RAM

Write Enable

Write Addr

Read Addr

FIFO Output Data

Write Addr

FIFO Output Register 20

Write Enable

Delay

Inc

Zero

FIFO Write Pointer Counter

Inc

Zero

FIFO Read Pointer Counter

"P1_TS_x"

Backplane Timing and Control Signals

Common to all DAVE FPGA's

Write Pointer Reset

Read Pointer Reset

Read Pointer Increment

Rev. 23-MAR-2002