Design and Test of Prototype Boards for the L1 Calorimeter Trigger Upgrade at the D0 Experiment

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***Abstract*—This paper presents the development and test of some of the electronic boards that have been designed for the upgrade of the L1 calorimeter trigger at the D0 experiment. The analog to digital converter and filter board (ADF) digitizes 32 calorimeter channels, applies digital filtering, and sends data to the next processing stage via 2 Gb/s links. The board is designed for sustained operation at 7.57 MHz with an end-to-end latency of less than ~1 μs. In order to test the high-speed output links of the ADF board, we made a tester that comprises a custom made Channel Link receiver card. To connect a prototype ADF board to the D0 detector without disturbing the existing trigger system, we designed a splitter board that duplicates the analog signals from 8 calorimeter channels. The serial command link distribution card (SCLD) is designed to accurately distribute synchronization signals to the 80 ADF boards of the final system. We made single channel versions of the ADF and SCLD boards. These cards run in a simple desktop PC environment and are helpful for tests and collaborative work. We describe the hardware, firmware and software aspects of the various developments and show the operation of the different boards. We present performance measurements made on the prototype ADF board, and explain how we defined the production model of this board.**

I. Introduction

THE D0 collaboration has proposed in 2002 the upgrade of the L1 calorimeter trigger system of the D0 experiment running at the Tevatron, Fermilab, IL [1]. The new system will implement more selective selection algorithms and a new calorimeter signals digitization system capable of performing the digital processing required for operation with 132 ns bunch spacing, and optional when running with 396 ns bunch spacing. The architecture of the new L1 calorimeter trigger consisting of two main parts: the analog to digital conversion and filter section (ADF) and the trigger algorithm boards (TAB) has been described in a previous paper [2]. This paper presents our hardware, firmware and software developments related to the ADF system.

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II. Outline of the ADF system

A. Requirements

The role of the ADF system is to digitize the 2560 calorimeter trigger pick-off channels of D0, estimate the value of the transverse energy deposited in each channel for each beam crossing, and deliver to the TABs the successive sets of energy values. The ADF system is designed to operate at a sustained rate of 7.57 MHz (i.e. a beam crossing period of 132 ns), but will only be exploited at 2.52 MHz because the upgrade of the Tevatron that was anticipated will probably not take place. The end-to-end latency of the ADF system must be fixed and ~1 μs. All 2560 output values are coded with 8-bit precision; the total flow of data generated is ~145 Gb/s.

B. System architecture

The basic modular component of the system is the ADF board that processes 32 calorimeter channels. In total, the system comprises 80 ADF boards housed in 4 commercial 6U VME-64x crates. Each crate contains 20 ADF boards and a controller interface. All analog input and digital output cables are plugged at the back of the crates. Synchronization signals from D0 are distributed to all ADF boards by the serial command link distribution card (SCLD). A PC equipped with a commercial PCI/VME adapter is used to control the 4 ADF crates through 4-pairs of Fermilab made "VME Vertical Interconnect" cards [3]. A fifth 6U VME crate is used to house the SCLD card, the VME part of the PCI/VME adapter, and the 4 VME Vertical Interconnect master modules. The controller in each ADF crate is a VME Vertical Interconnect slave module. When only one ADF crate is being tested, the PCI/VME adapter is used to control that crate directly.

III. THE ADF BOARD

A. Architecture and features

The ADF board processes 32 calorimeter channels. All channels are identical and are treated in parallel. The operations to perform are the following: receive the differential analog signal, subtract a programmable constant pedestal value, convert the analog input to a digital format, estimate from successive input samples the value of the transverse energy in the corresponding calorimeter cells for the current beam crossing period, and serialize the estimated energy value for transfer via high speed links to the TABs.

1) Analog section

The analog section on each channel of the ADF board comprises a passive termination network with the appropriate impedance followed by a fully differential amplifier. This amplifier provides the required attenuation to bring signals in the desired range (0 to +6 V at the input, -1 V to +1 V at the output), subtracts the pedestal voltage generated by a digital to analog converter (DAC), shifts the common mode input voltage to the desired value (1.25 V), and low-pass filters signals for anti-aliasing. This circuit drives the input of a 10-bit analog to digital converter (ADC) clocked at 30.28 MHz (i.e. 4 samples per 132 ns period). Pipelined ADCs feature latency proportional to their clock period. Analog inputs are over sampled to cut conversion time because latency is critical in this application. Subsequent logic stages may decimate or combine successive samples as desired.

2) Digital filter section

Because the analog signals from the calorimeter electronics are long (~800 ns for the complete pulse) compared to the beam-crossing period of 132 ns, estimating the energy deposit in a cell for each beam crossing is not straightforward. A specific digital filtering algorithm has been proposed in [2]. It consists of an 8-tap finite impulse response filter followed by a 3-point peak detector and a look-up table for final calibration, clipping around zero, etc. The digital filter is run at 15.14 MHz. Running at a speed higher than the minimum required (7.57 MHz) is done to improve performance and cut latency. Filter coefficients are tuned on a per channel basis. The optimal set of coefficients is determined off-line using waveforms acquired by the ADF system on each calorimeter channel during special runs. In order to capture these waveforms, the ADF board includes on each channel a 512-word deep buffer for storing digitized calorimeter input signals. The PC controlling the system reads the corresponding data over the VME bus. For monitoring purposes, each channel includes a history buffer that stores raw ADC samples, some intermediate results and final transverse energy values. History buffers can be read slowly over VME. When a level 1 trigger accept occurs, the SCLD board can optionally instruct all ADF boards to fetch from their history buffers the series of unfiltered ADC samples corresponding to the event that caused the trigger to fire, and send these data to the TABs. This scheme allows embedding the relevant parts of raw calorimeter data in the main data acquisition path of the experiment.

3) Output links

The ADF board produces 32 8-bit energy values per 132 ns period. Because the algorithm performed by the TABs requires that data produced by each ADF board be used in 3 trigger algorithm boards, some duplication of data is needed. For some technical reasons, the decision was made to implement the
fanout in the ADF system at the expense of a three-fold increase in the number of links between the two systems. Each ADF board sends 3 identical copies of its data through 3 separate output links. Each link is composed of a Channel Link chip pair [4] and a 5-meter 8-pair 2 mm hard-metric cable. The local bus on the transmitter is clocked at 60.56 MHz; 36-bits (out of 48) are used. The net bandwidth for each link is 2.18 Gb/s resulting in an aggregate bandwith of ~520 Gb/s for the 240 links between the 80 ADF boards and the TABs.

B. Design, fabrication and test

A prototype ADF board was designed and built. The board houses ~1300 components on a 14-layer class 6 printed circuit board: the 32 analog blocks previously described, 16 dual 10-bit ADCs, 4 octal serial DACs, 4 Xilinx Virtex II 500 K gates field programmable gate arrays (FPGAs), 3 Channel Link transmitters, a VME interface, power conversion circuits, and passive components. A picture of the board is shown on Fig. 1.

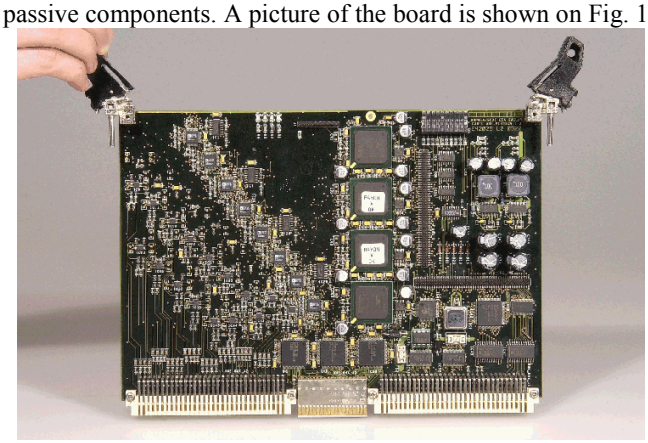

Fig. 1. Prototype ADF board.

Two boards have been assembled and tested. Several design errors were corrected on the analog section and component values were tuned to meet the requirements in terms of input signal dynamic range, bandwidth, range of pedestal adjustment and stability with temperature changes. Although all channels are functional, noise is above our goal of 1 LSB r.m.s. in some cases: with analog inputs grounded, some channels feature a noise of ~0.5 LSB r.m.s., while up to ~2.5 LSBs r.m.s. is observed on noisy channels. Corrective actions have been taken in the design of the production version of the ADF board to meet the noise specification on all channels (see section IX).

The digital part has been extensively tested and debugged. Pre-defined series of input samples have been loaded in the appropriate memory buffer of the ADF board and have been

input to the digital filter logic at the nominal rate. The output results captured in history buffers have been collected over the slow VME path and have been successfully cross-checked with the output of a C program running the proposed digital filter algorithm on the same set of input data. A programmable waveform generator was used to test complete ADF channels (analog and digital parts). A typical result is shown in Fig. 2.

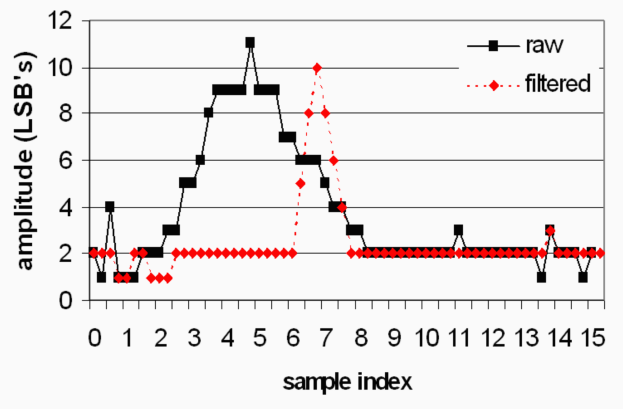

Fig.2. Operation of a channel of the ADF board. The solid line is the output of the analog to digital converter. The dashed lined is the output of the digital filter (the peak detector is turned off). The processing algorithm cleans up most of the noise, significantly narrows the width of the input pulse, and would correctly identifies the corresponding energy value and time position if the peak detector were enabled.

The end-to-end latency of the ADF board (measured from the time of the peak of the analog input pulse until the last bit of the digital result is available at the end of the output cable) is 0.87 μs to 1.23 μs (depending on filter coefficients), and is 400 ns when the digital filter is bypassed.

We measured the performance of the three 2 Gb/s output links of an ADF board with a 20 Gsps oscilloscope and a custom made tester (see section IV). At the tester end (4 meter cable to the ADF board), the eye pattern is still widely opened (~70% of the bit time duration). In the laboratory set-up, all links operate in a very stable and reliable manner. Tests were stopped after 12 days with no bit error found. This translates to an upper limit for the bit error rate of $\sim 10^{-15}$ with 90% confidence level. The correct operation of the output links of the ADF board with one TAB prototype was also verified.

IV. The Channel Link Tester

In order to test the high-speed output links of the ADF board in a simple environment, a specific tester was designed and assembled. This tester is composed of a custom-made mezzanine card equipped with a 2 Gb/s Channel Link de-serializer chip plugged on top of a commercial Xilinx Virtex II FPGA evaluation kit. This is shown in Fig. 3. A PC is used for control via a parallel interface or a RS232 serial port. The tester allows capturing up to 2048 frames of data sent by an ADF board. Recorded data are displayed on the PC. An alternate mode of operation allows checking the integrity of the data sent by the ADF board over extended periods of time. In this mode of operation, the ADF board and the tester are programmed to generate the same pseudo-random stream of data. The tester performs bit-to-bit comparisons of the received pattern against the expected one to detect and count bit errors.

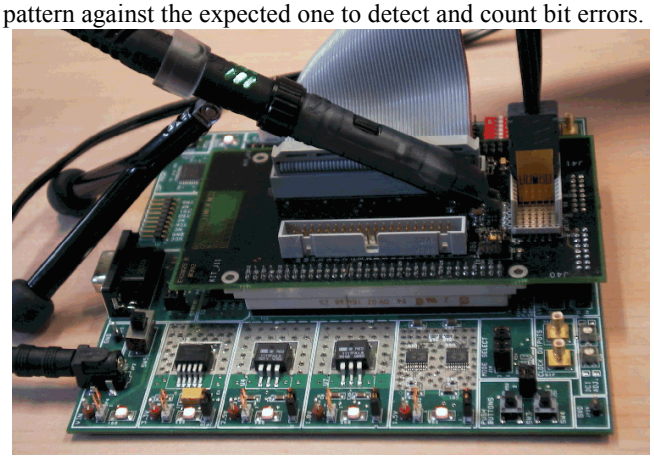

Fig. 3. Channel Link tester. An oscilloscope probe is connected next to the high speed link.

To qualify the tester, forced errors were generated in the ADF board and were effectively detected. It is therefore legitimate to claim the exactness of the received data when the tester does not report any error.

V. The Analog Signal Splitter Card

A. Architecture and design

In order to connect a prototype ADF board to the D0 detector without disturbing data taking, we designed a calorimeter signal splitter card that duplicates the analog signals from 8 calorimeter channels. The card uses active devices to compensate for the loss in signal amplitude due to impedance termination networks. A splitter card installed at D0 is shown in Fig. 4.

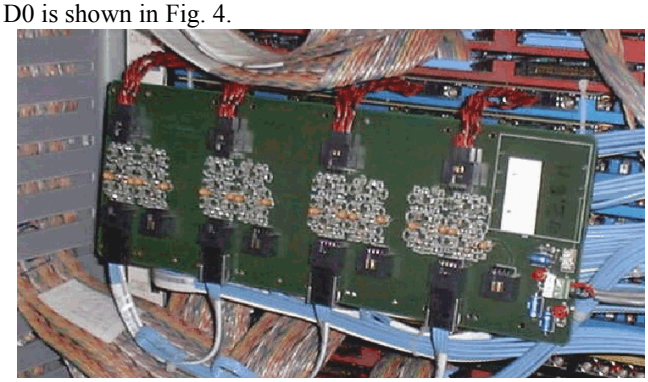

Fig. 4. A splitter card installed at D0.

B. Test and operation

At present, 4 splitter cards have been fabricated; 32 calorimeter channels can be spied on at D0. This is sufficient to test 1 ADF board. We analyzed the data taken by the experiment before the insertion of the splitter and after, and we verified that no noticeable degradation of the signals is introduced.

VI. The SCLD Card

A. Architecture and design

The ADF system must be synchronized with other sub-systems in D0. Synchronous signals are distributed in D0 using the "serial command link" [5]. We designed the serial command link distribution card (SCLD) to fanout the reference clock and other synchronous signals to up to 5 crates of ADF boards. The SCLD board is linked to one ADF board within each crate via an 8-pair hard-metric cable (similar to that used to connect to the TABs). Each of the ADF boards connected to the SCLD distributes signals within its crate using some of the (normally reserved) bussed lines available on the VME64x backplane bus. The SCLD board is interfaced to the existing system at D0 with a Fermilab made serial command link receiver (SCLR) mezzanine card [5] plugged into the SCLD. Most of the SCLD logic is implemented in a 500 K gate Xilinx Virtex II FPGA device. External logic is needed for 5 V to 3 V translation. The SCLD board does not incorporate a VME interface because it does not interact with the slow control of the experiment. This card of low complexity (compared to the ADF board) contains 230 components placed on an 8-layer class 6 printed circuit board. A view of the SCLD board is shown in Fig. 5 (left side).

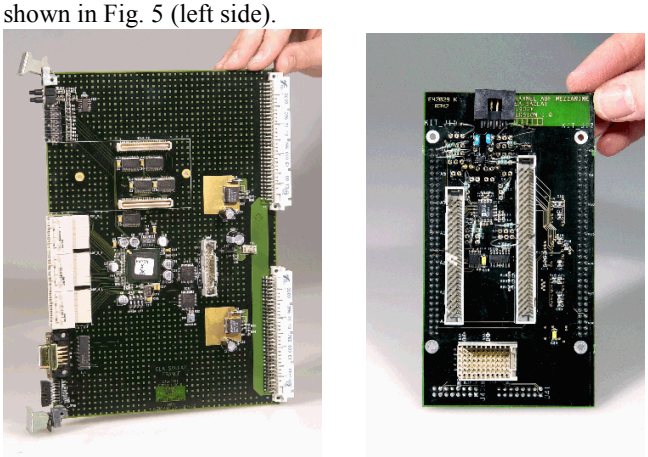

Fig.5. SCLD board (left) and single channel ADF mezzanine card (right).

B. Test and operation

The correct operation of the SCLD board with one of the prototype ADF boards was verified. Because synchronization signals from the D0 experiment are not available in this laboratory setup, a standalone version of the SCLR mezzanine card is used. Testing at D0 will be performed in fall 2004.

VII. The Single Channel SCLD and ADF cards

To validate several design concepts quickly, a single channel version of the SCLD board (i.e. capable of distributing signals to 1 crate of ADF boards) was made before building the full-size card. The reduced SCLD consists of a SCLR mezzanine card plugged into a custom-made mezzanine card attached to a commercial FPGA evaluation kit (similar to the model used for the Channel Link tester). This is shown in Fig. 6. The single channel SCLD was tested at D0 with one of the prototype ADF boards and correct operation was verified.

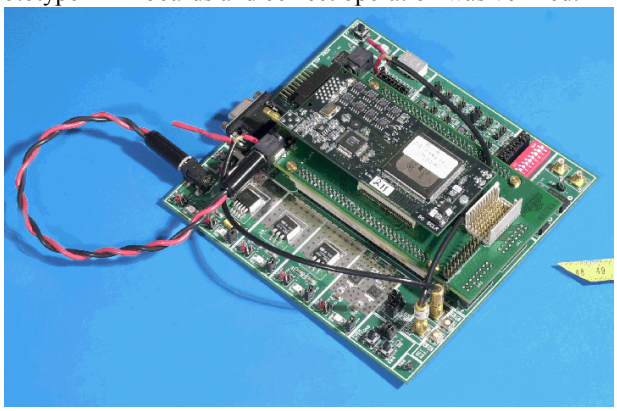

Fig. 6. Single channel SCLD board.

We also developed a single channel version of the ADF board: the analog section is placed on a custom-made mezzanine board (Fig. 5. right) attached to the commercial FPGA evaluation kit used throughout the project. This small set-up provides a very convenient platform for tuning the analog section, developing and checking firmware, etc. The desktop version of the ADF board is fully firmware/software compatible with the 32-channel VME version. This simple and inexpensive set-up can easily be transferred to other collaborators willing to participate in specific developments (e.g. designing and implementing alternate digital filter algorithms) without the need of installing a costly and comparatively complex VME environment.

VIII. Firmware and Control Software Developments

The firmware of the ADF, SCLD and Channel Link tester boards is entirely written in VHDL (~50,000 lines of source code). The necessary software to configure, test and control the various boards is written in C (~50,000 lines of source code). The software controlling the ADF board can be produced in a rather large number of flavors. Versions exist to drive:

- the VHDL model of the 32-channel VME board (to validate jointly firmware and software)
- the actual ADF board hardware controlled by a PC through a VME/PCI interface or VME Vertical Interconnect modules,
- the ADF hardware controlled by a single board computer plugged in the VME crate,
- several ADF boards (possibly located in different crates),
- the single channel ADF card,
- a software stub emulating the ADF system (useful when developing the control software).

All these programs are variations around the same core of code. We defined modular and flexible software with clearly defined layers and interfaces to support these many different possible combinations of hardware, platforms and operating system. Windows 2000/XP, Linux and LynxOS (for some

configurations) are supported. The interface between the ADF software and other programs can be made via TCP/IP sockets transporting human-readable commands.

The software controlling the Channel Link tester board is also available in different flavors to drive either the VHDL model of the tester or the actual hardware through a parallel I/O card or a RS232 serial port.

IX. The Production Model of The ADF Board

Although most concepts were successfully validated during the prototype phase, major changes were made to the ADF board. The design has been transferred from the Cadence environment used at CEA to the Mentor Graphics environment used at MSU[1]. For operation with 7.57 MHz beam-crossing rate, a rather sophisticated digital filter algorithm on each channel of the ADF is required, as well as logic to gather raw samples of data and transfer unfiltered ADC samples to the TABs after a level 1 trigger accept. Because the beam-crossing rate at the Tevatron is likely to remain at 2.52 MHz, simpler digital filtering (if any at all) is adequate, and the effective operating rate of the ADF system is only 1:3 of the initial design value. The logic of the ADF is therefore substantially trimmed, and fewer FPGA devices are needed. The now obsolete VME bridge chip used on the prototype board is replaced by programmable logic. A more robust clock distribution circuitry is devised. The analog section is entirely reworked to aim for lower noise: dedicated reference voltage sources are used for the pedestal DACs (in place of the reference voltage delivered by the ADCs), all ADC to FPGA connections are terminated by series resistors, a denser and more regular layout is achieved, power supply distribution and decoupling is improved, etc. At the time of writing, the production model of the ADF board is being finalized and will be tested by the end of 2004.

X. Summary and Future Work

We presented the development of several prototype boards for the upgrade of the level 1 calorimeter trigger of the D0 experiment. The ADF board performs digitization and digital filtering of 32 channels of the calorimeter, and delivers results on three 2 Gb/s links. Expected performance is reached on the digital section, but excessive noise on some channels is found. Adding to that issue the fact that the requirements for the ADF system (in terms of operating speed and functionality) have been significantly reduced, the design of the ADF board prototype has been re-worked to devise the production version of the board. The SCLD board distributes synchronization signals to the ADF system. The prototype board fulfills the requirements and will be used in the final system. Analog signal splitter cards have been designed and installed at D0. These cards allow spying on 32 calorimeter channels without interfering with the existing trigger system. A specific tool to check the operation of the 2 Gb/s output links of the ADF was assembled. This tester was used to validate ADF prototype boards. It will be used to bench test production boards and for system diagnosis and maintenance. Single channel versions of the ADF and SCLD boards have been designed. These simple mezzanine cards plugged on a commercial FPGA evaluation kit allowed fast and cost-effective prototyping. A multi-platform and versatile software package was developed to exploit the different boards.

The series of 80 ADF boards will be produced in 2005 and the upgraded level 1 calorimeter trigger is expected to be in operation by the end of that year.

[1] This institute is responsible for the production of the final ADF boards, while CEA contributed mainly to the prototype phase and provides the final SCLD board, the splitter cards and the Channel Link tester.

XI. Acknowledgment

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