Design and Test of Prototype Boards for the L1 Calorimeter Trigger Upgrade at the D0 Experiment

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Plan

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- Context
- Hardware developments
- Firmware and software
- Project status
- Summary

D0 L1 Calorimeter Trigger Upgrade

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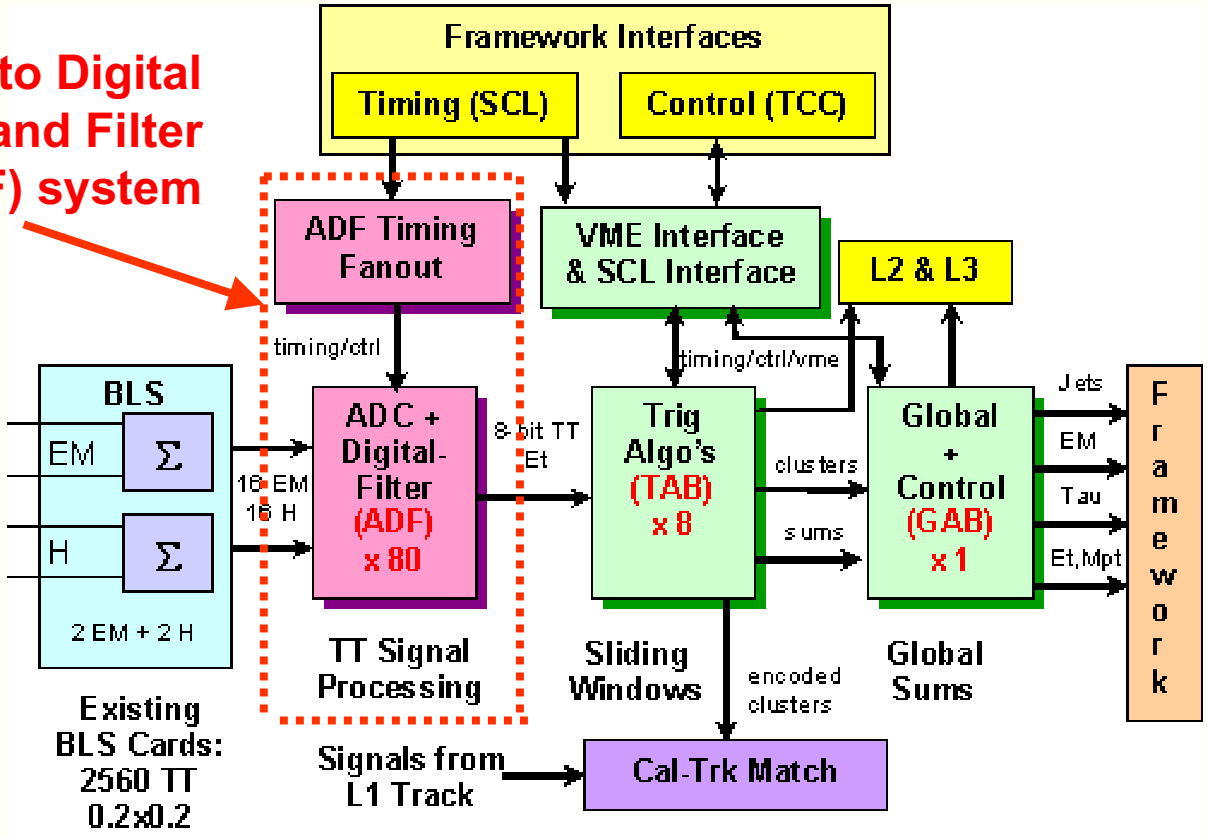
Analog to Digital converter and Filter (ADF) system



Purpose of the ADF system

- Every 132 ns and within a ~1 μs latency budget : digitize and estimate E_T for each 2560 calorimeter channels; send all E_T values to TAB's

Architecture

- 80 ADF boards (4 crates) linked to 8 TABs by 240 x 2 Gbit/s links

A/D converter and filter (ADF) board

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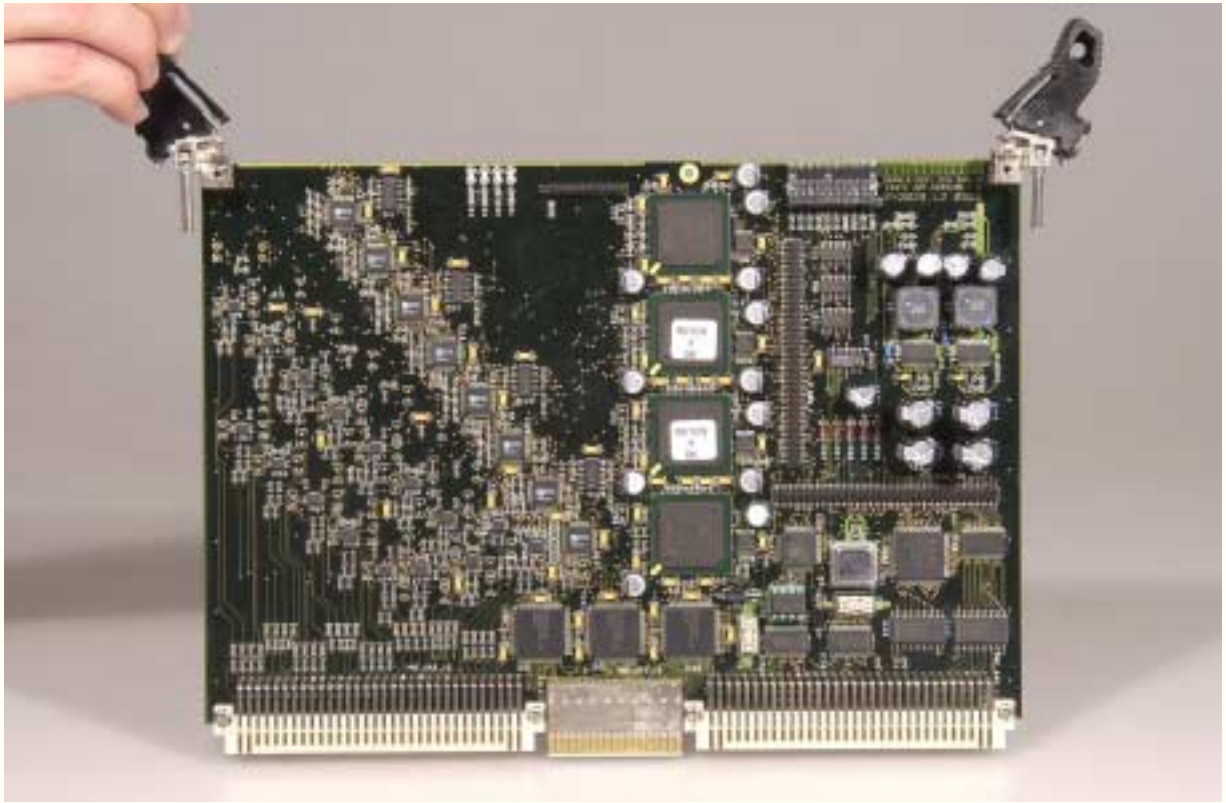
Purpose

- Digitize and process 32 calorimeter channels



Features

- 32 x (30 MHz ADC 10-bit + 15 MHz 8-tap FIR filter + peak detector)
- 3 ouptut links 2 Gbit/s; history buffers, VME interface configuration/control

Analog section test

- Programmable waveform generator to mimic calorimeter signals
- ADC output recorded in history buffer, read-out slowly over VME

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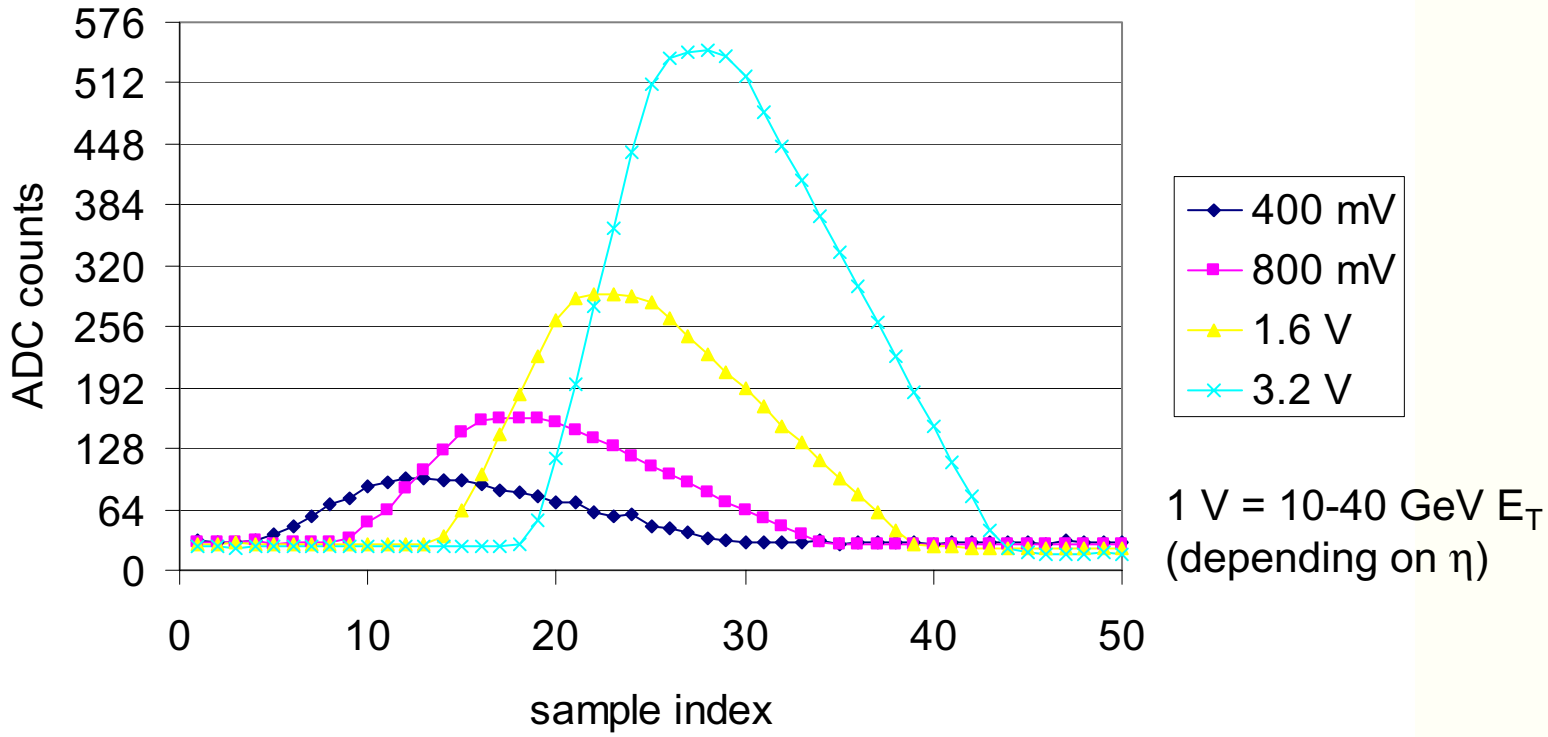

1 V = 10-40 GeV E_T (depending on η)

- Compliant with requirements for input scale, bandwidth, pedestal adjustment range, stability with temperature drift

Analog section noise

- ADC output when no source connected at input

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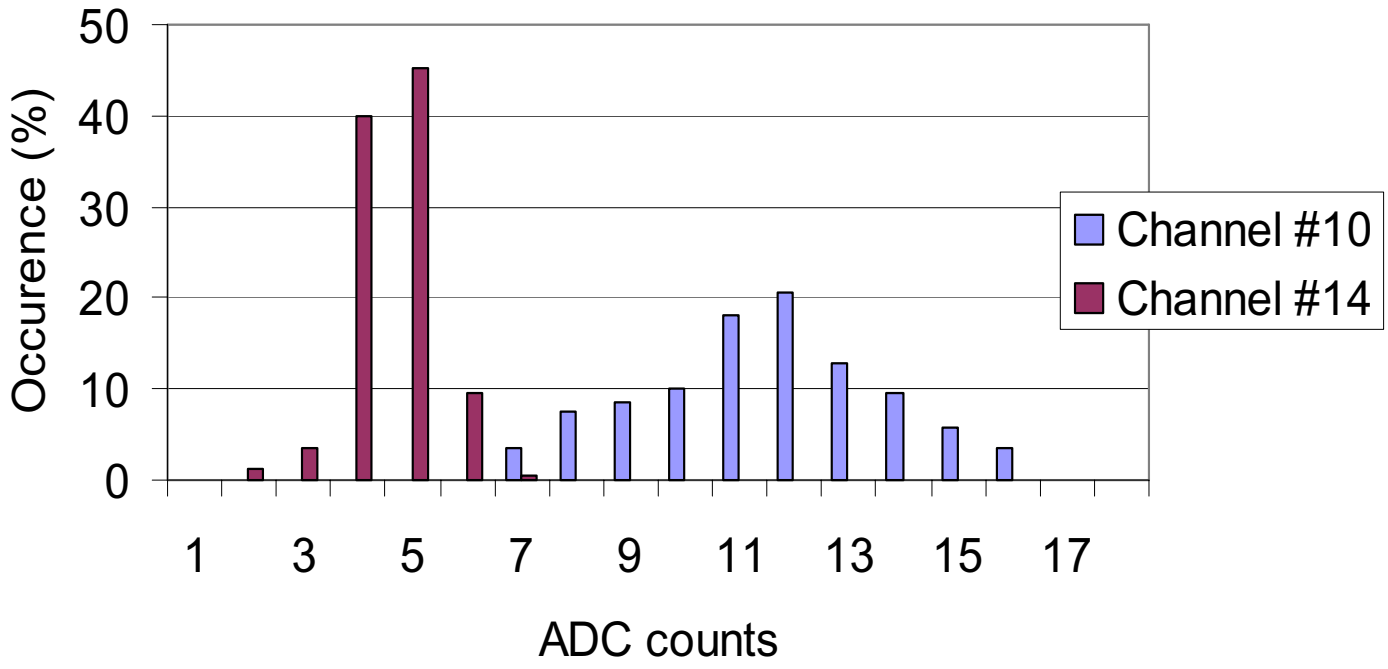

- Noise from 0.5 LSB RMS to 2.5 LSB RMS on some channels; above requirement of 1 LSB RMS
- Corrective actions for production ADF: design changes and re-layout

Digital filter operation

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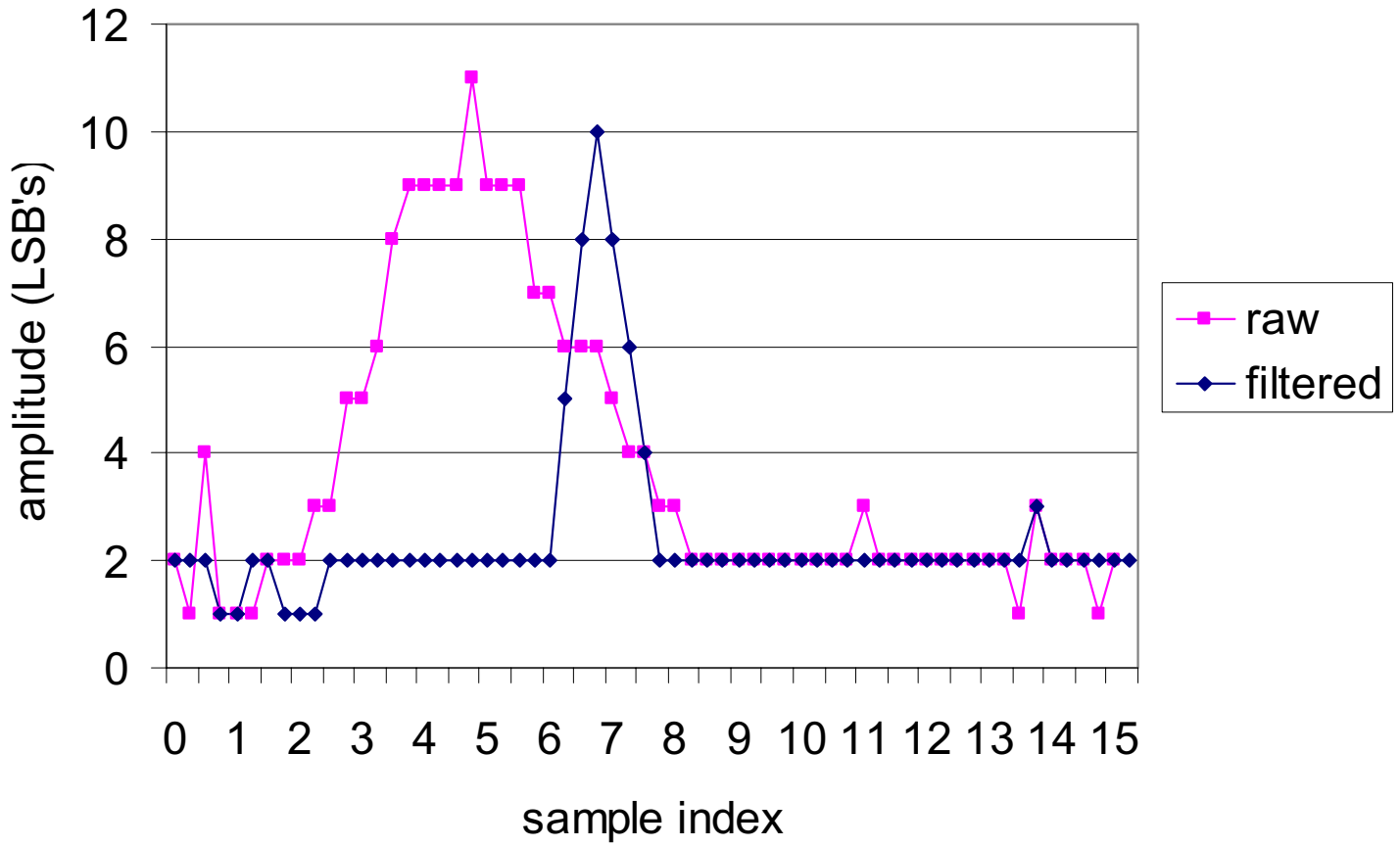

- Algorithm: 8-tap matched filter; peak-detector turned off
- Noise improvement and correct identification of energy and time position
- End-to-end latency: 0.87 µs to 1.23 µs (depending on filter coefficients)

Channel Link tester

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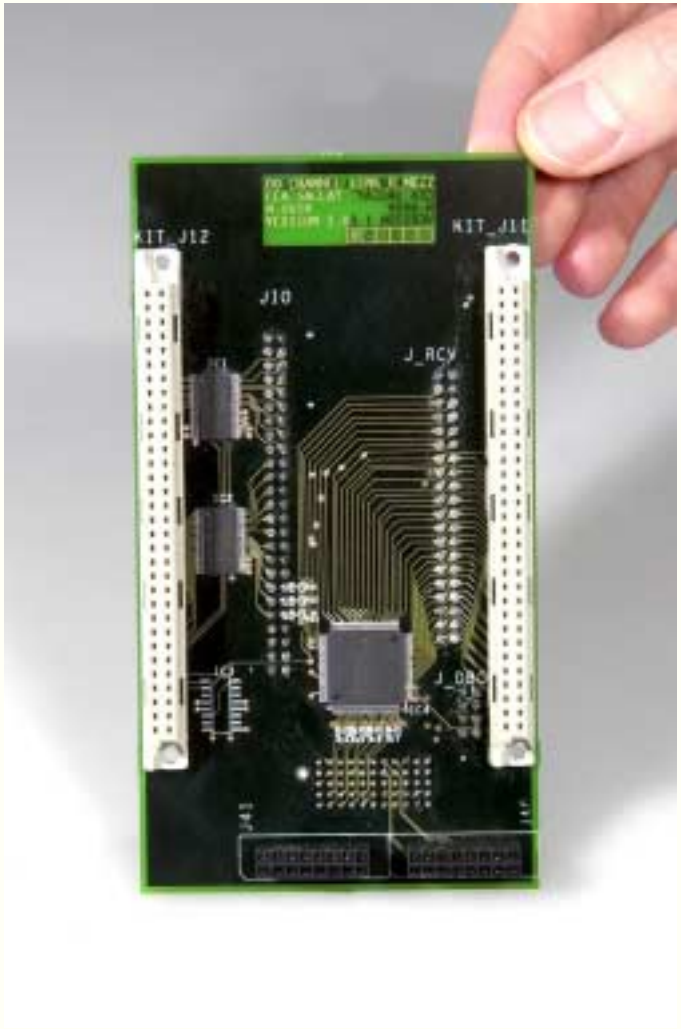
Purpose

Provide a tool to test/diagnose the 2 Gbit/s output links of ADF boards



Features

- Custom-made mezzanine card + commercial Xilinx Virtex II evaluation kit
- Control by a PC over RS 232 or // I/O
- Data mode:
  - capture up to 2048-frames
  - check received parity
- Error counting mode:
  - Compare received data to pre-defined pseudo-random pattern
  - Accumulate bit errors and statistics

Tester in operation

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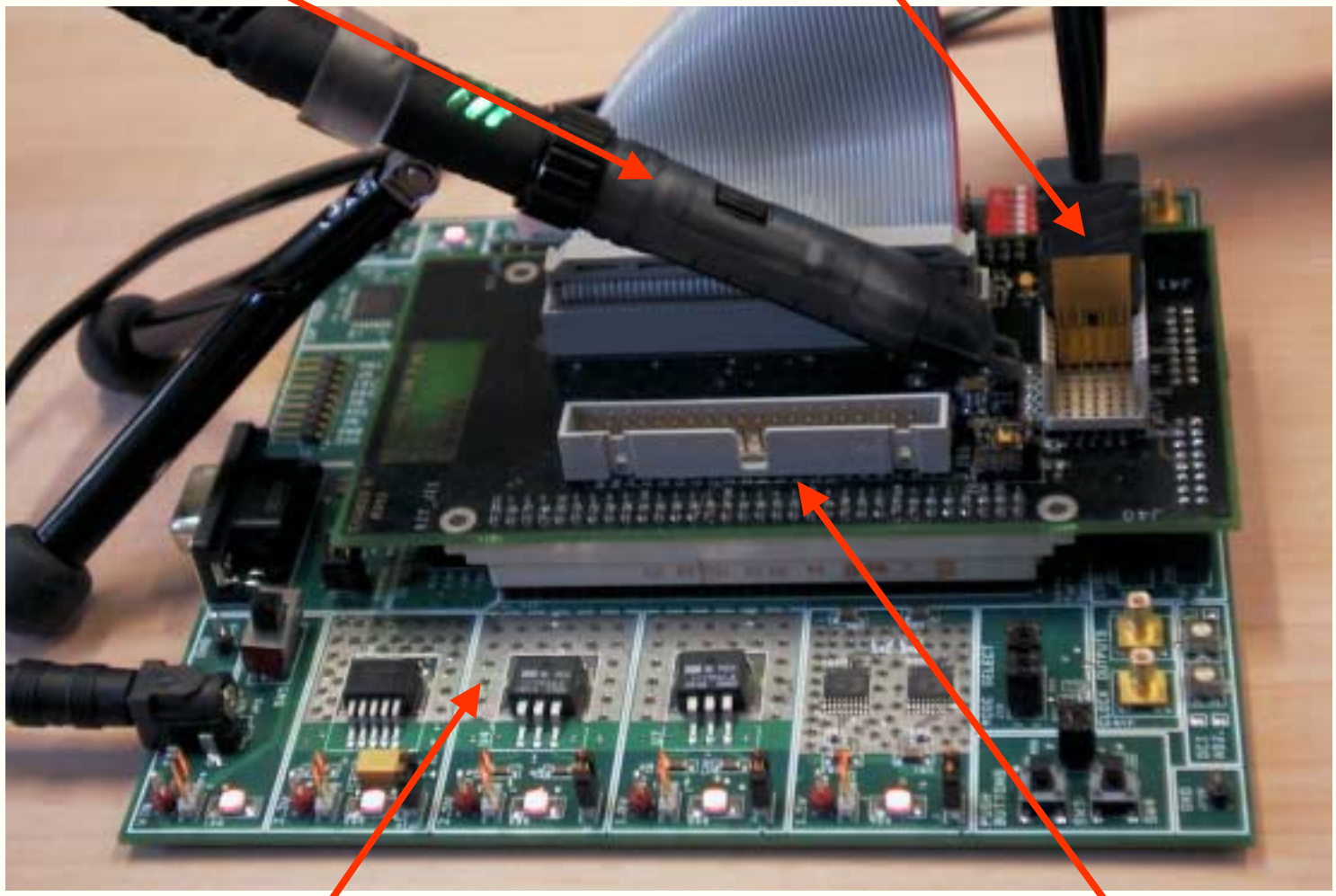

ADF links BER measurement

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- Horizontal eye pattern opening: 70% typical
- No error at 2 Gbit/s during 12 days: BER < 10^{-15} (90% confidence)
- ADF board to TAB connection tested at Fermilab

Analog signal splitter card

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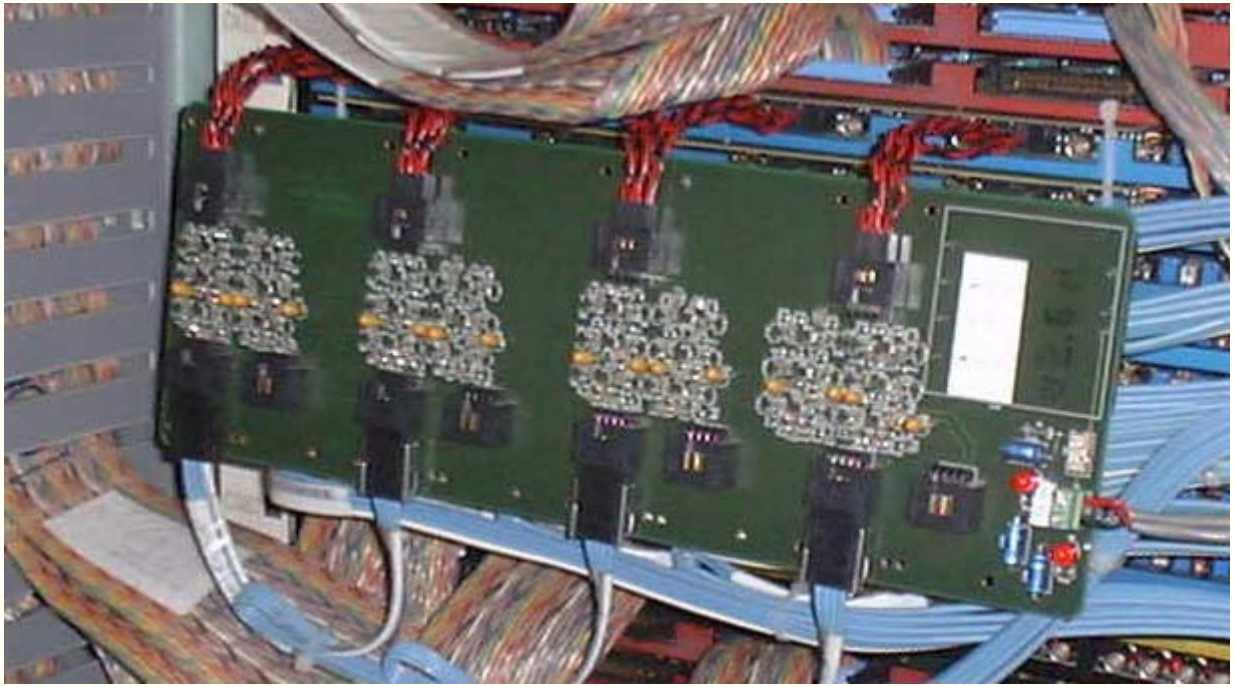
Purpose

Test ADF prototype in D0 without disturbing current data taking



Features

- Active board duplicating differential signals of 8 calorimeter channels
- 4 boards available to split 32 channels
- Insertion of splitter transparent for current system (checked D0 DAQ data)

Serial Command Link Distribution card

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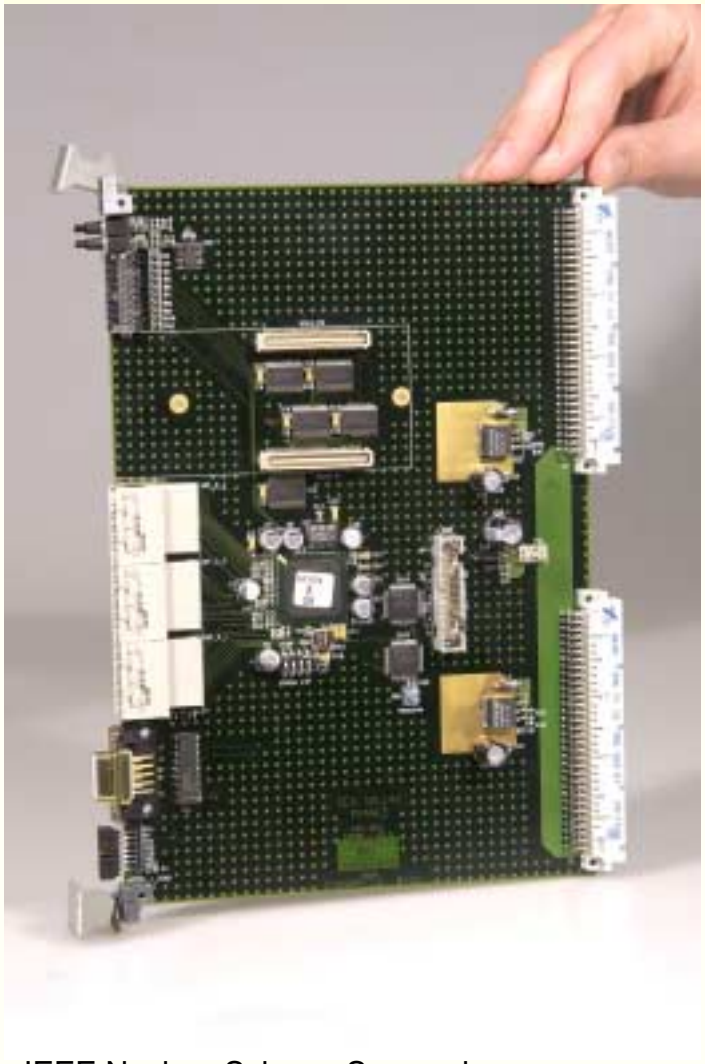
Purpose

Distribute D0 beam crossing clock, synchronous signals to ADF system



Features

- Gets signals from D0 via Fermilab-made SCL Receiver mezzanine card
- Fanout SCL signals to up to 5 crates of ADF boards
- 1 loop-back port for standalone test
- VME mechanics but no VME interface (no need for slow control)

ADF system test setup

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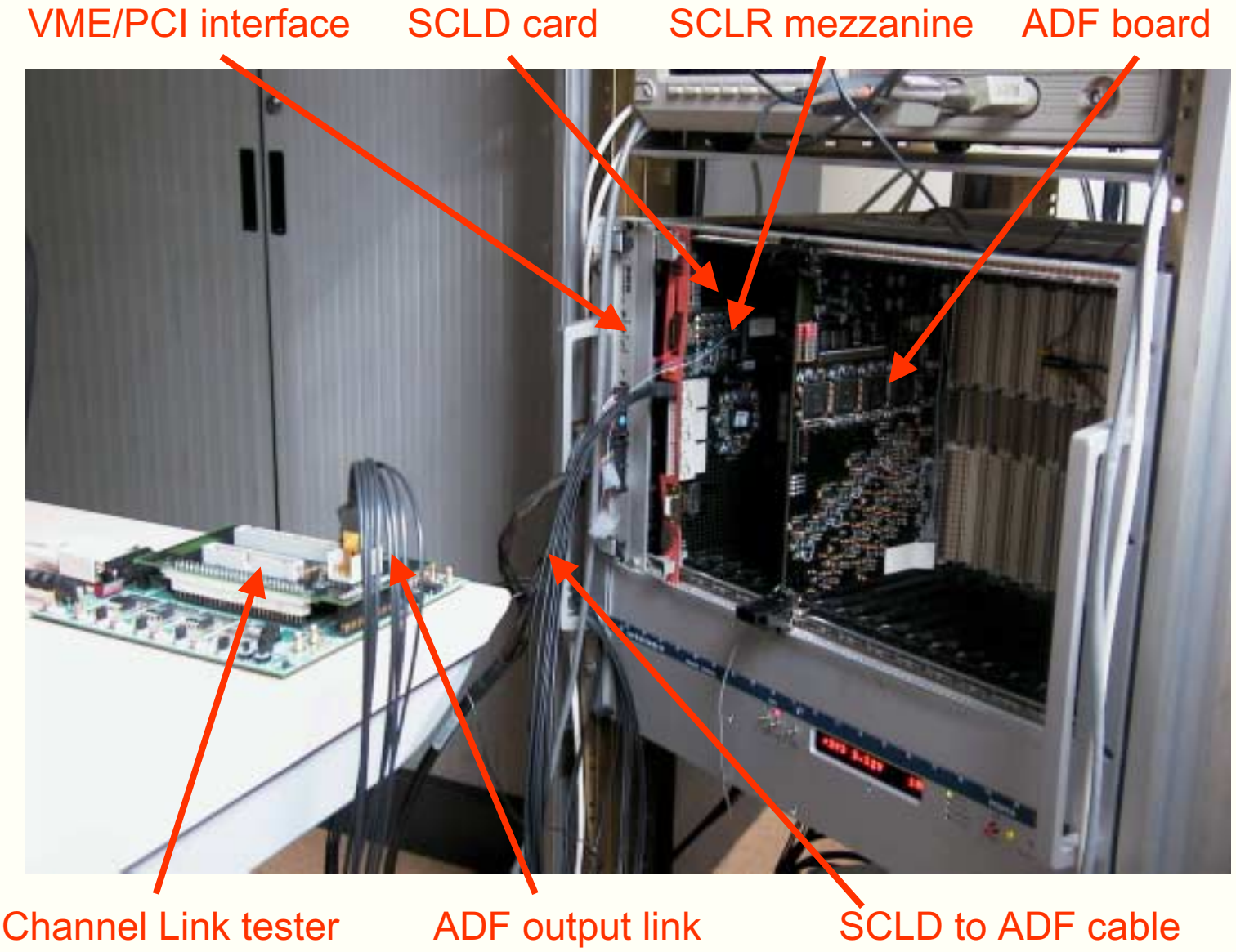

Single channel ADF card

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Purpose

Simple desktop setup to tune analog section; develop firmware/software

Features

- Custom mezzanine card + commercial FPGA evaluation kit
- Analog section: socketed passive components + 1 ADC
- Firmware and software compatible with 32 channel ADF board
- Control via a PC

Single channel SCLD card

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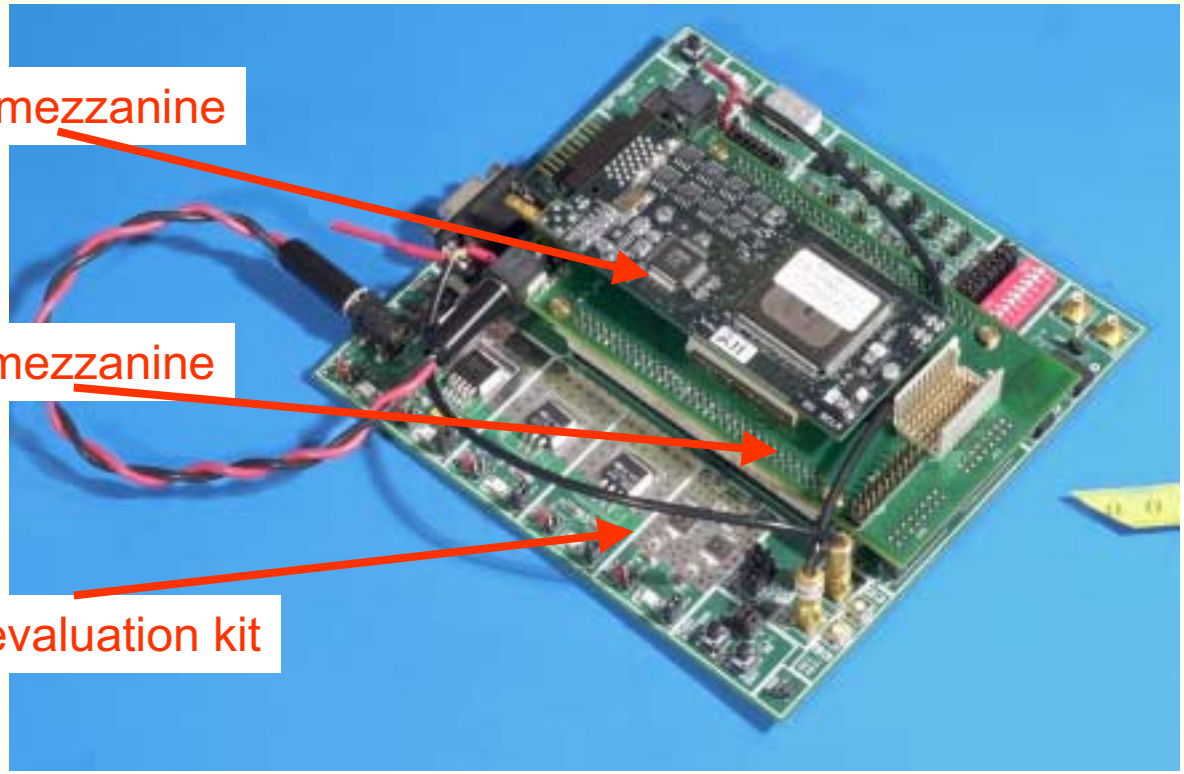
Purpose

Prototype to validate concepts before building full-size SCLD card



Features

Distributes Serial Command Link signals to 1 crate of ADF boards

Tested in-situ at D0 with 1 ADF board and 1 TAB

Firmware and control software

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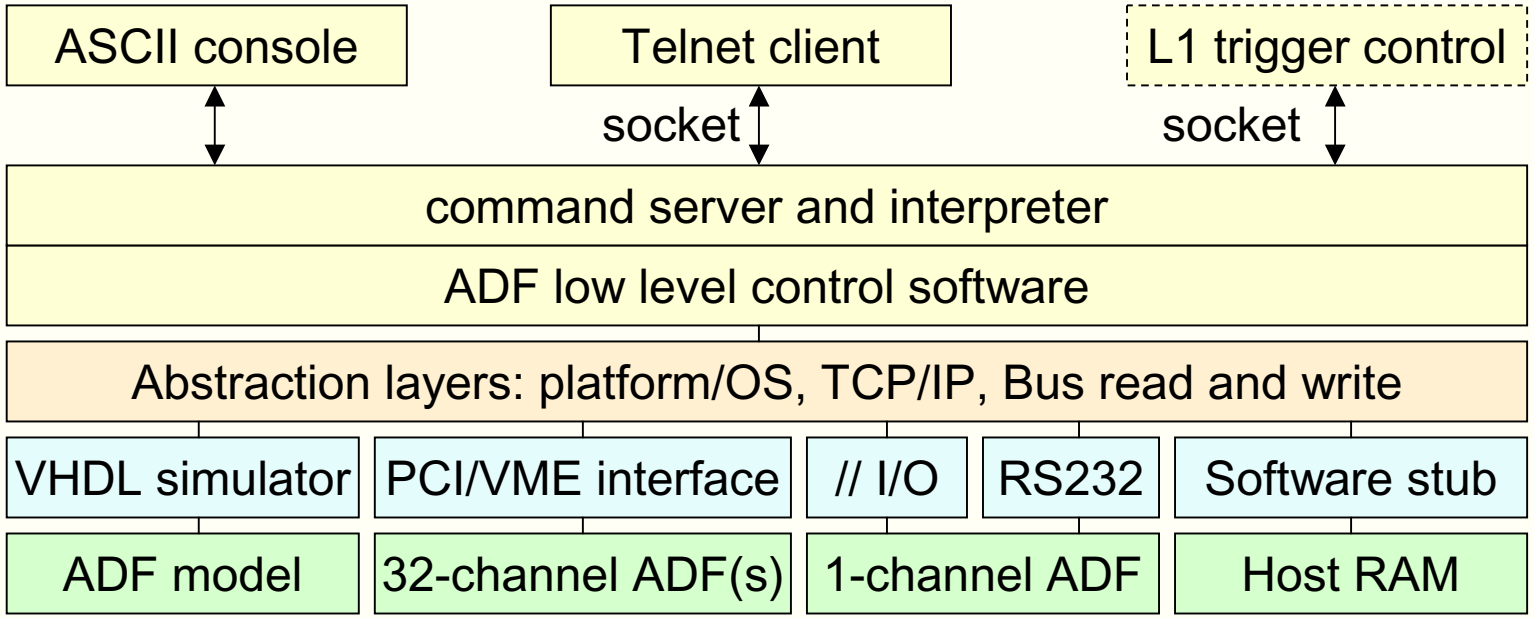
Objectives

Co-simulation of hardware models and control software

Portability (Windows, Linux, LynxOS); various hardware configurations



Implementation

Firmware in VHDL and software in C (~100,000 lines in total)

Layered software with API to access OS and generic control bus

Static link with appropriate library to support OS / hardware variations

ADF project status

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Prototype phase achievements

ADF board: functional and compliant except noise on some channels

SCLD: final board

Analog signal splitter: installed

Channel Link tester: useful tool

Proof of principle of a workable system

Project evolution

Silicon detector upgrade cancelled in 2003: impact on schedule

132 ns bunch spacing at Tevatron not pursued: digital filtering not needed in ADF; operating rate now 1:3 of 7.57 MHz design specification

Production and deployment phase

Transfer of prototypes (Saclay CADENCE) for production (MSU Mentor)

Major changes to ADF board to fulfill updated set of requirements

Production model ADF board

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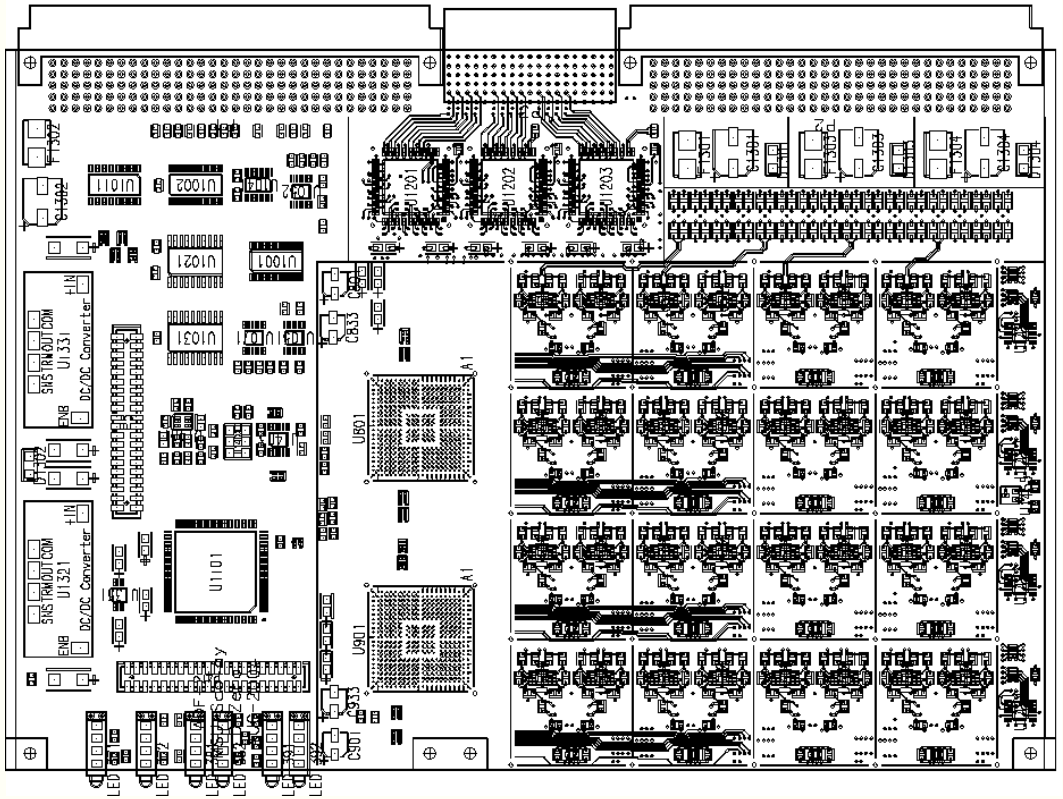

Features

Improved analog section for lower noise; board re-layout

Trimmed logic uses fewer and denser FPGA's

Replaced now obsolete VME bridge by CPLD; reworked clock tree

Pre-production of final ADF board and validation in fall 2004

Summary

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Work completed

- 32-channel ADF board — *Prototype*
- Single channel ADF — *Prototype*
- Single channel SCLD — *Prototype*
- SCLD board — *Final*
- Analog signal splitter — *Support*
- Channel Link Tester — *Support*

Project phase mostly successful

Future work

- Validate production model of ADF board
- Integration with other sub-systems
- Produce and test series of 80 ADF boards (2005); system installation

Upgraded trigger system expected to begin operation in fall 2005