Algorithms and Architecture for the L1 Calorimeter Trigger at D0 Run IIb

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***Abstract*—This paper presents the algorithms and the architecture proposed for the upgrade of the level 1 calorimeter trigger for the D0 experiment. We describe the digital-signal-processing algorithm applied to individual trigger tower signals and the physics algorithms that process the complete array of trigger towers. We investigate the performance of these algorithms and justify our choices. We present the hardware architecture of the system designed to analyze the signals of the 2560 calorimeter trigger tower samples and construct trigger primitives in ~ 3 μs at a rate of 7.57 MHz. We give a detailed description of the two prototype boards that are being built: the analog-to-digital converter and filter board (ADF) that performs the analog conversion and digital processing of 32 calorimeter channels, and the trigger algorithm board (TAB) designed to run the physics selection algorithms on one eighth of the 480 Gbit/s of data produced by the complete set of ADF boards.**

***Index Terms*—Real-time systems, trigger circuits.**

I. Introduction

THE D0 collaboration has proposed an upgrade of the D0 detector operating at the Tevatron, Fermilab, IL, to fulfill ambitious physics goals such as the search for the Higgs boson. The upgrade of D0 for Run IIb consists of the replacement of the silicon tracker and major changes in the trigger systems[1]. The various aspects of the whole project are detailed in [1]. This paper focuses on the upgrade of the Level 1 calorimeter trigger.

II. Motivation for the Upgrade of the Level 1 Calorimeter Trigger

The current L1 calorimeter trigger has been in operation for about 15 years. It applies selection algorithms that are sufficiently simple to fit in the electronic components that were available when it was built. The constant progresses of digital logic circuits give the opportunity to implement more sophisticated selection algorithms that will significantly increase the performance of the system. We anticipate a much sharper turn-on for jet triggers and an improved trigger turn-on for electromagnetic objects. The new system will have the ability to make shape and isolation cuts on electromagnetic triggers, and match tracks to the energy deposition in calorimeter trigger towers. The energy in the intercryostat region will be included when calculating jet energies and missing E_T. Topological triggers will aid in triggering on specific Higgs final states.

The existing Level 1 calorimeter trigger operates with 396 ns bunch spacing and was designed to run with bunch spacing as low as 132 ns. However, critical limitations would appear if the existing system were operated at this rate. For Run IIb, operation at 132 ns was the design requirement. Although bunch spacing at the Tevatron will remain at 396 ns (at least initially), the capability to safely operate with 132 ns bunch spacing is an additional justification for the upgrade. Improved sampling of calorimeter signals and digital filtering will lead to more precise measurements of the energy deposited in each calorimeter trigger tower. Other benefits of the upgrade are a more compact system (three racks instead of 13) and easier maintenance because the components of the current system are now obsolete (1988 design).

III. The Existing Level 1 Calorimeter Trigger

We give a brief summary of the description of the existing D0 Level 1 calorimeter trigger given in [2]. At this level, the whole calorimeter is seen as a cylindrical array of 1280 trigger towers (40×32 in $\eta \times \phi$ space). Analog sums of the calorimeter cells within each trigger tower are made by summers and baseline subtractors (BLSs) to form two differential "trigger pickoff signals": the electromagnetic (EM) and the hadronic (HD) samples. The BLSs deliver the 2560 differential signals to calorimeter trigger front-end cards (CTFEs) that digitize them and compute partial results such as energy sums and counts of trigger towers above a set of thresholds. The final logic stage produces a set of "trigger-terms." These are sent to the "Level-1 trigger framework" that issues trigger decisions.

The proposed upgrade replaces the CTFEs and all the logic that computes the trigger terms; the BLSs and the Level-1 trigger framework are unchanged.

IV. Algorithms for the Upgraded Level 1 Calorimeter Trigger

Two different types of algorithms are deployed in the upgraded Level 1 calorimeter trigger. At first, a digital signal pro-

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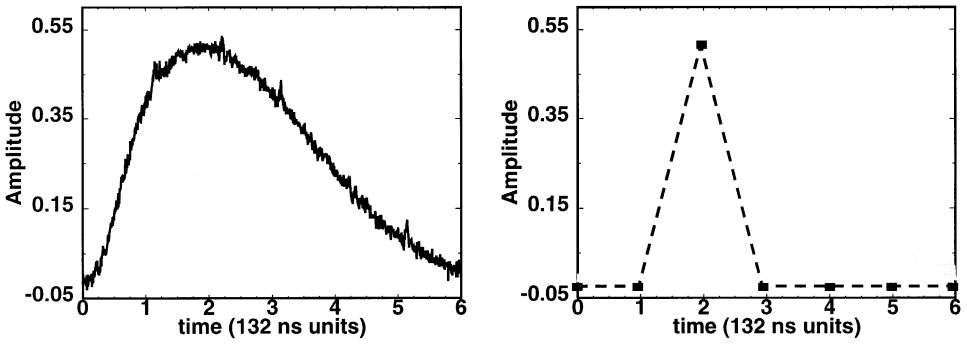
[1]On September 3, 2003, Fermilab's Director made the decision not to include the silicon detector in the continuing upgrade project.



(a) (b)

Fig. 1. (a) Analog trigger pickoff signal and (b) processed pulse after digital processing. Proper scaling is applied on numerical results to make the direct comparison with the original analog amplitude.

cessing algorithm is applied to individual trigger tower signals to produce for each beam crossing a value representative of the transverse energy deposited in that trigger tower. Then, a physics selection algorithm is run on the complete set of 2560 trigger tower energies to construct the trigger terms used by the Level-1 trigger framework.

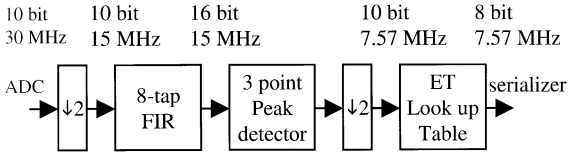


Fig. 2. Digital signal processing algorithm for each trigger tower signal.

A. Signal Processing of Individual Trigger Pickoff Signals

1) Motivation: The shape of a typical trigger pickoff pulse is shown in Fig. 1 (left graph).

The rise time of the signal is ~ 250 ns and the total duration of the pulse is ~ 700 ns. This is a major concern for operation with 132 ns bunch spacing. Assuming that an energy E has been deposited in a trigger tower at a given beam crossing, the energy seen for the previous beam crossing is already $\sim 75\%$ of E. This can be well above the required threshold to fire a trigger for that beam crossing. This premature trigger vetoes several of the following beam crossings, and the event of interest is irretrievably lost. The long tail of the signal produces a series of fake energy values after a real energy deposition ($\sim 80\%$ of E after 132 ns and $\sim 20\%$ of E after 396 ns). This is not an issue in the current system because it operates with 396 ns bunch spacing and because the trigger selection algorithm computes the counts of *individual* trigger towers that are above several given thresholds. However, this is a critical point in the upgraded system for operation with 132 ns bunch spacing, and also because the new selection algorithm acts on sums of energies over a rather large number of trigger towers (16 for jets). In the current system, each trigger pickoff signal is fed to a flash analog-to-digital converter (ADC) that samples the peak value of the signal. Manually adjusted digital delay lines are used to set the sampling time on each trigger tower. Because only one sample is taken per beam crossing, measurements are very sensitive to electronic and pile-up noise as well as signal and clock jitter. The most flexible way to overcome all these limitations is to apply digital processing to trigger pickoff signals. This is described later.

2) Signal Processing Algorithm: Measuring and assigning to the correct beam crossing the energy seen in each channel of a calorimeter is now a well understood problem in high energy physics as reported by SDC [3], ATLAS [4] and CMS [5]. The solution commonly adopted is based on a finite-impulse response (FIR) filter followed by a time filter. In [1], we made a comparative study of several algorithms (linear deconvolution, peak detection and averaging, FIR filter followed by a peak detector) and devised the algorithm shown in Fig. 2.

We refer to the frequency corresponding to 132 ns bunch spacing as $F_{BC} = 7.57\,\mathrm{MHz}$. Analog trigger pickoff signals are converted with 10-bit precision at 30.28 MHz ($F_{BC} \times 4$). This rate was selected as the best tradeoff between short conversion latency and low cost as well as moderate power consumption of the ADCs. The number of samples is then reduced by a factor of two. Selecting which two samples to process among the four that are converted per beam crossing is programmable. Each ADC clock can also be inverted. These features are used to adjust sampling delays from 0 to 49.5 ns in steps of 16.5 ns. This simple scheme allows static per channel delay compensation without the need of programmable digital delay lines. The remaining samples are then fed to a FIR filter running at $F_{BC} \times 2$. The decision to run at twice the minimum required rate was made to cut latency and because of the improved overall quality of the results (precision, assignment to the correct beam crossing, tolerance to clock phase and jitter). Selecting the number of filter taps and coefficient precision was made by simulation. As has been reported for similar applications, we found that 5-taps and 6-bit precision coefficients are adequate but our conservative design supports up to 8-taps. If desired, zeroing some coefficients could make a shorter impulse response. The output of the FIR is fed to a three-point peak detector. This nonlinear operator detects whether the middle input sample is greater than the two adjacent ones. If this condition is satisfied, the middle sample is output; otherwise a null value is output. The result produced by the peak detector is down sampled by a factor 2 (to produce only one result per beam crossing), scaled, and then used as an address for a lookup table that computes the final 8-bit calibrated transverse energy value for that trigger tower.

The same algorithm (with individually tuned parameters) is applied simultaneously to the 2560 trigger tower samples to produce for each beam crossing the map of the transverse energy deposited in the calorimeter.

B. Physics Selection Algorithms

The total L1 accept rate at D0 is limited to approximately 5 kHz because of the structure of the readout system. As the Tevatron luminosity increases in Run IIb to the goal of $2\times10^{32}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$ this limitation will severely constrain the physics reach of the D0 experiment. The current L1 calorimeter trigger is based mainly on counting the number of trigger towers above preset E_T thresholds, although the total scalar sum of E_T deposited in the calorimeter and missing E_T information are also available. Because the spatial extent of D0 trigger towers, 0.2×0.2 in $\eta\times\phi$ space, is significantly smaller than the lateral size of jets in the calorimeter, only a small fraction of a jet's energy is "seen" by a single trigger tower. This results in a very shallow trigger turn-on curve for jet triggers, requiring a trigger tower threshold of only 5 GeV to trigger on 40 GeV jets with 80% efficiency. These low thresholds, coupled with the poor energy resolution of a single trigger tower for jet E_T measurement result in a substantial background in the current high-E_T jet triggers from low-E_T QCD events. This background, which is manageable at the relatively low luminosities of Run IIa, becomes unacceptable in Run IIb, with trigger rates for such important single triggers as those sensitive to events with two high-E_T jets plus missing energy rising to over 2 kHz if thresholds are set such that these triggers have high efficiency for detecting Higgs events.

An obvious solution to this problem is to include more than one trigger tower in the definition of a jet. We have chosen to select these multitower jets using a "sliding windows" algorithm, which is similar to those studied extensively by the ATLAS collaboration [4]. The sliding windows algorithm is simply a search for local maxima of E_T deposition on a grid using a fixed-size "window" made up of a group of contiguous trigger towers in $\eta\times\phi$ space. Local maxima are found by moving the window by fixed steps in η and ϕ (one trigger tower in the D0 case) and searching for a window, the sum of whose trigger tower $E_T s$ is higher than all of its nearest neighbor windows.

After studying several different combinations of sizes and numbers for comparison, we have chosen to define jets in the D0 Run IIb trigger using a window of 2×2 trigger towers in $\eta\times\phi$ space. Local maxima are found by comparing all of the windows whose lower left most trigger tower lies in a 5×5 region about the central window. The central window is a local maximum if its total E_T is greater than that of the neighboring windows above and to the right of it and greater than or equal to that of the windows below and to the left. Finally, a "trigger jet E_T" is defined, for all windows that are found to be local maxima, as the summed E_T of all the trigger towers in the window plus that in a ring of width one trigger tower surrounding it, i.e., a total region of 4×4 trigger towers. The algorithm is shown graphically in Fig. 3. With this definition, 80% of a jet's energy is contained, on average, within the new trigger jet and the ratio of the RMS of the trigger jet E_T distribution to the average is 0.2. This can be compared to the corresponding values of 40% and 0.5 for the current L1 calorimeter jet trigger. Using the new algorithm, background rates for jet triggers are reduced by a factor of 2.5–3 over current triggers with the same efficiency.

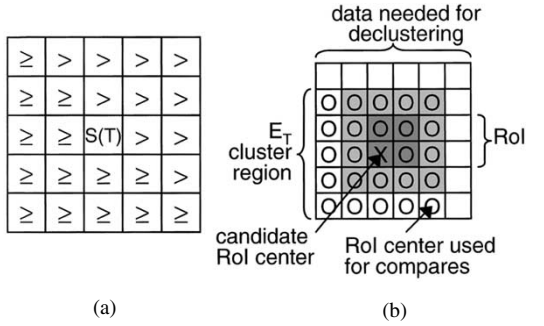


Fig. 3. (a) Windows whose E_T is compared to the central window and (b) a diagram of the various elements of the jet algorithm parameters.

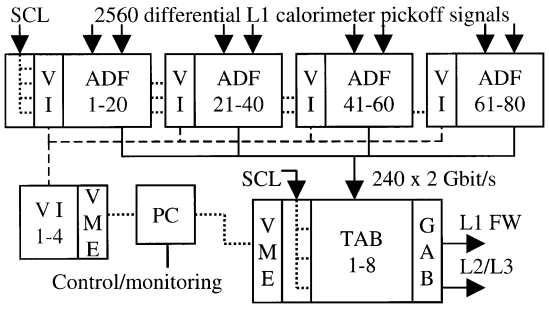


Fig. 4. Architecture of the upgraded D0 L1 calorimeter trigger.

The new L1 calorimeter trigger hardware, described later, also allows the improvement of algorithms used to trigger on electromagnetic objects, such as electrons and photons, and adds the possibility of a new type of trigger on narrow jets caused by the decay of τ leptons. Both the EM and τ algorithms use sliding windows searches to find local maxima of E_T in the calorimeter. The EM algorithm demands that this E_T maximum, found only using energy deposited in the EM part of the calorimeter, has little energy surrounding it and that there is little energy deposited in the hadronic trigger towers directly behind the EM local maximum. The τ algorithm is an extension of the jet algorithm. It selects narrow jets by requiring a large value for the ratio of the E_T in the 2×2 jet window to that in the 4×4 trigger jet E_T region.

Finally, we have also improved the calculation of the scalar sum of E_T over the entire calorimeter as well as the calculation of missing transverse energy and have greatly improved our ability to construct triggers based on specific event topologies in the calorimeter.

V. Architecture of the Upgraded L1 Calorimeter Trigger

The architecture of the upgraded L1 calorimeter trigger is shown in Fig. 4. The system is composed of two major components: the analog-to-digital conversion and filter (ADF) cards and the trigger/global algorithm boards (TABs/GAB). The ADF cards convert to digital format the analog trigger pickoff signals, apply the digital filtering algorithm, and deliver for each beam crossing the value of the transverse energy measured in the 2560 trigger tower channels. The TABs and the GAB apply the physics selection algorithms to construct the trigger terms used

by the Level 1 trigger framework (L1 FW) to produce trigger decisions.

Other elements are used for downloading, monitoring, and global synchronization.

A. ADF System

The ADF system is composed of 4 6U VME64x [6] crates. Each crate houses 20 ADF cards and a VME vertical interconnect (VI) slave module [7]. The four VME vertical interconnect master modules are placed in an additional crate equipped with a VME/PCI interface attached to a desktop PC used for downloading, configuring and monitoring the ADF system. A specific card is used to fanout to each ADF crate the clock and control signals of the general synchronization network of D0, the serial command link (SCL). This card is also used to distribute intra ADF system synchronous signals. Each of the 80 ADF cards receives input from 32 analog channels on rear jack 2 (RJ2), and produces digital streams of filtered energy values on rear jack 0 (RJ0).

Each of the 32 channels of the ADF card comprises a passive termination network followed by a fully differential amplifier, a passive antialiasing filter and a 10-bit ADC. A programmable constant voltage generated by four octal digital-to-analog converters (DACs) is subtracted from each channel before conversion to adjust pedestal values. The digital section of the ADF card comprises field-programmable gate arrays (FPGAs), low-voltage differential signaling (LVDS) serializers, a VME bridge, and a bit of glue logic. In addition to 32 digital filters, the ADF card comprises all the necessary features to help in debugging, calibrating, and monitoring the system. When operating in standalone data acquisition mode, an ADF card can capture the shape of trigger pickoff pulses and deliver this information via VME. These data are exploited off-line to determine the optimal set of filter coefficients for each channel. In test mode, each channel can be loaded with a series of data samples that are then used as inputs to the digital filters. The ADF logic can serialize on its output a serial stream of pseudo-random numbers, a stream of constants, the raw data produced by the ADC or the final output of the digital filter. In normal data taking mode, each ADF card records in 512-word deep history buffers all raw ADC samples as well as the outputs of the FIR and final E_T calibrated results. Upon receipt of a Level 1 trigger accept, the ADF card can optionally send to the TABs the set of nonfiltered ADC values of the event that caused the trigger. This information is useful to check off-line the quality of the digital filter. Once the desired number of raw samples has been sent, the ADF outputs are automatically switched back to filtered data streams. The ADF card can also be programmed to freeze its history buffers on receipt of a L1 trigger accept or a software-generated trigger. History buffers are available for slow control read-out over VME. This mechanism provides a powerful way of debugging and monitoring the ADF system.

B. TAB and GAB System

The architecture of the TABs and GABs is driven by the data-sharing requirements of the sliding windows algorithm. In order to test whether a single 2×2 trigger tower window contains a local maximum or not, using the D0 jet algorithm, data from a 6×6 region of trigger towers are needed. Further constraints also arise from the mapping of calorimeter readout cells to trigger towers in the area between the central and forward calorimeters. Taken together these constraints lead us to a system design with eight TABs, each receiving overlapping data from 30 ADF cards, corresponding to 2×480 trigger tower inputs (EM + HD). The output of the sliding windows algorithms, run in each of the TABs, is sent to a single GAB, which merges the results and creates yes/no decisions for up to 64 separate triggers using the TAB data.

Within the TABs, the sliding windows algorithms and E_T summing are performed in a set of 10 Altera Stratix FPGAs, each responsible for finding local maxima in 16 windows and for sharing data with its neighboring chips. All adds and compares in the chips are performed, with 12-bit precision, bit serially at 90.9 MHz ($F_{BC} \times 12$) and in a fully pipelined manner. This architecture minimizes FPGA resource usage and matches the serial format of data transfer within the system.

Results from each of the ten "sliding windows" chips on a TAB are sent to a "global" chip, also a Stratix, which reformats these data for transmission to the GAB over a serial link similar to that used in ADF-to-TAB transmission, as described below. At this point, positions of jet and EM local maxima are also transmitted to a separate part of the D0 L1 trigger system, the L1 Cal-Track match system, to be matched with tracks from the L1 tracking trigger. Additionally, all trigger tower E_Ts, input to the TAB, are transmitted to the L2 and L3 systems for more sophisticated processing of L1 accepts.

The eight TABs and one GAB are housed in a single crate with the same dimensions as a 9U VME crate but with no backplane aside from a small power bus. Using a standard VME interface for these boards is impossible because connectors for the 30 cables from the ADF cards take up all the space on the back of the TABs. VME communication with the TABs and GAB is accomplished using a custom protocol on separate serial links for each card. The translation of VME read/write requests to this serial protocol is performed by a custom VME/SCL interface card, which also distributes timing and control information to the TABs and GAB from the serial command link. The VME/SCL card is housed in a 9U VME crate along with a VME/PCI interface for communication with a desktop PC.

C. Links and Interfaces

Given the characteristics of the sliding windows algorithm, the data of some trigger towers are used by three different TABs. We investigated several schemes for duplicating data and decided to put the fanout circuitry on the ADF boards. Each ADF card produces three identical copies of its output data stream (32 8-bit energy values per beam crossing). The bandwidth of each of the three ADF output links is $\sim 2\ \mathrm{Gbit/s}$. The total output cross-section bandwidth of the ADF system is 480 Gbit/s. These data are transported from the 80 ADF cards to the eight TABs by 240 hard metric differential cables composed of eight pairs. Connecting FPGA pins on both ends directly using LVDS was considered, but using the Channel Link chipset [8] was preferred because it seemed more robust, imposed no constraints on the choice of FPGAs and description language at both ends, and provided a ready to use interface.

VI. Prototypes

A. ADF Board Prototype

We designed a prototype ADF board using VHDL to describe and simulate its behavior ($\sim$30 000 lines of code). The logic fits in four 500-K gates, 456-pin Xilinx Virtex II FPGAs internally clocked at 60.56 MHz ($F_{BC} \times 8$). We chose the Virtex II family because it includes hardwired multipliers, has large blocks of embedded RAM and offers very compact implementations of small dual-port RAMs and shift registers. The ADF board houses $\sim$1300 components placed on both sides of a 14-layer class six printed circuit board. At the time of writing, the board is under assembly. We designed and installed in the current D0 experiment an active splitter card that duplicates the signals of several trigger towers. The prototype ADF board will be connected in spy-mode to the detector without disturbing Run IIa datataking.

We developed the test and control software for the ADF system. A command-line interpreter supporting multiple clients (via sockets) is provided. We defined a software abstraction layer to interface to the VME bus. Two implementations were made: one for a VME/PCI interface and one to drive the VHDL model of the ADF card. By linking the control software with the appropriate library, the executable code drives transparently the VHDL model of the ADF card or the real hardware. Although the actual card is not yet ready, we wrote and debugged a very large part of the ADF control software ($\sim$16 000 lines of C code) and tested the firmware of the card extensively without the need of writing a complex test bench in VHDL.

B. TAB and GAB Prototypes

Prototypes of the TAB and the VME/SCL interface card have been designed, and the GAB prototype design is well under way. Firmware for all elements of the VME/SCL card and TABs has been written and simulated. This includes data input and output and internal data sharing, jet, EM, and τ sliding windows algorithms, the construction of global sums, data formatting for GAB, Cal-Track, and L2/L3 output, communication with VME and the SCL using our custom serial protocol, and the implementation of extensive test and monitoring capabilities.

At the time of this conference, we have fabricated and assembled one VME/SCL prototype, which is currently under test. The first TAB prototype, a 12-layer board containing the full 11, 768-pin Stratix FPGAs, plus all of the other, final infrastructure, is in fabrication. A GAB prototype will be constructed later this summer.

VII. Summary and Future Work

We have designed a new Level 1 calorimeter trigger for use in the D0 experiment at Run IIb. It performs digital filtering on the signals of 2560 trigger towers and applies physics selections based on sliding windows algorithms. The system is designed to run at a sustained rate of 7.57 MHz and produce results with a fixed $\sim$3 μs latency. The system is composed of 80 ADF cards, eight TABs, one GAB, two custom modules for global synchronization, and a few standard elements for configuration and monitoring. Prototypes of the ADF card, TAB, and GAB have been designed and are being produced. Following tests to be done in 2003, production models will be built and installed in D0 for a scheduled start of operation in 2006.

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