

# **FIC Module Specifications**

## **DRAFT # 2**

This draft is the description of the current design. This design is complete, checked and has been submitted to CAD processing.

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## Introduction

The level2 trigger of the D0 experiment needs a speed adapter for the optical links between the fiber trackers and the central trigger. The level2 trigger is based on “Hot Link” fibers (or coaxial cables) at 160Mbps. The fiber tracker uses the so called “G-Link” connections operating at more than 1Gbps and is incompatible; some conversion is needed.

The links are either transmitting an event or idle between events. The amount of data received for one event on the G-Link is compatible with the bandwidth of the Hot Link. The speed conversion can be done independently for each fiber. The FIC (Fiber Converter) module is designed to perform this conversion.

We will first present some technical information as background; then the external specifications of the FIC module will be discussed. The last part is the precise technical specification of the FIC module.

## Background information

### Serial links primer

The name “serial link” is used for various systems replacing parallel ribbon cables by a single wire (or more precisely by an optical fiber, a coax or a twisted pair). The basic idea is to replace  $x$  bits \*  $y$  MHz by 1 bit \*  $xy$  MHz. In principle, this is very simple: for the transmitter, a PLL (phase locked loop) multiplies the parallel clock and feeds a parallel-in/serial-out shift register. For the receiver, a PLL recovers the clock from the NRZ (non return to zero) serial stream and a clock divider generates the parallel clock to strobe a serial-in/parallel-out shift register.

The first problem is to design the PLL for both a wide operating frequency range and a good stability when the receiver gets noisy signals. The main problem is frame synchronisation in the receiver: where are the boundaries of the parallel words in the serial stream? If the link has a very low bit error rate, it is practical to make an initial synchronisation by some special mean and then to keep that synchronisation for the operation of the link. In case of errors, one has to repeat the initial synchronization. The other option is to use some coding of the data stream both to get good transitions for synchronization and to recover from transmission errors. When one uses optical fibers, there is an additional problem called DC balance. This expression describes the requirement of laser diodes to get an equal number of zeros and ones in the serial data stream.

There are three generations of serial link chipsets.

### First Generation

The first serial chipsets were just implementation of the basic idea. The frame synchronisation in the receiver is done with a special “sync” character, sent when the data link is idle. There is no encoding of the data: the serial stream is identical to the data bits, this has

two major drawbacks: there is no protection against errors on the links. The DC balance is the responsibility of the data provider. In addition, false “sync” characters can appear in the data stream and de-synchronizes the link.

## Second Generation

The next serial chipsets incorporated features that are necessary in any practical set-up, but were missing in the chipsets of the first generation. The first one was simplified interface making the link almost transparent. There is also an extensive set of test configurations to diagnose installed systems without any re-cabling. For optical links, the chipset incorporates the OFC (open fiber control). This is a mandatory safety feature able to switch off the lasers in case of fiber disconnection (and to discover automatically when there is a successful reconnection).

The encoding schemes were converging towards the best solutions in terms of noise tolerance and sync stability. Several standards for optical links have been published, discouraging original implementations. The new chipsets have dropped the features not used in the standards.

## Third Generation

The last serial chipsets are tailored to the standards. They implement completely one and only one standard link (e.g. Sonnet, Fiber Channel, Escon, Fire Wire or Giga Ethernet) including layers above the physical layer. It is not possible to build custom links with such chipsets.

## The Hot Link chipset

The Cypress company manufactures this chipset. It is a typical second-generation chipset. It is designed to operate in the 150-400Mbps range, using the Fiber Channel specification. The chipset normally accepts all the 256 data words of 8 bits and 14 control words; each word is transmitted as 10 serial bits. The chipset uses an encoded version of the data. This encoding will be presented in the error analysis section. Transmission errors are detected and are flagged as encoding “violations”. This encoding guarantees an approximate DC balance for any input sequence while keeping the maximum number of consecutive ones or zeros to less than five.

The chipset can also be configured to transport 10 bits transparently, but without the DC balance property, the detection of errors and with risks of PLL de-synchronisation in case of long sequences of ones or zeros.

When there is no data to transmit, the chipset transmits a special character called fill character to maintain the receiver synchronization. The transmitter chip can also send upon request the “violation” control character which triggers an error in the receiver chip. The chipset is equipped with a comprehensive built-in self-test allowing a complete check of the full link and a measure of the bit error rate.

## The G-Link chipset

The Hewlett Packard company manufactures this chipset. It is also a typical second-generation chipset. It is designed to operate in the 150-1500Mbps range, using a proprietary encoding. This encoding guarantees a transition at a fixed location in the serial segment to ensure synchronisation. The encoding is done by transmitting the input bits accompanied by 4

(for data symbol or 6 for control symbol) bits of framing. The DC balance is achieved by sending the input bits either as presented or complemented; the framing bits being different in the two cases. The chipset can operate in 16 bits mode or in 20 bits mode. In 16 bits mode, the parallel data is 16 or 17 bits; the corresponding serial data contains 20 bits; the chipset accepts also control data of 14 bits. In 20 bits mode, the parallel data is 20 or 21 bits; the control data is 18 bits and the corresponding serial data contains 24 bits. There is no error correction bits in the code, but the chip can detect errors in the framing bits. In 16 or 20 bits mode, there is an extra bit alternating from one word to the next, used to improve error detection and to avoid static patterns on the link. In 17 or 21 bits mode, this extra bit is used as a data bit, but with the loss of the improved error detection.

When there is no data to transmit, the chipset transmits a sequence (a slightly modified symmetric clock at the word frequency) called fill word. The receiver chip can detect invalid patterns which are produced by transmission errors (the transmitter cannot generate them); they are called violation words. In full duplex configuration, the chipset provides an automatic start sequence at power-up and after a reset.

## Environment of the serial links

In this section, we discuss the protocols used on the various serial links. The low-level protocol is implemented in the chipsets and has already been presented. We concentrate on the two next levels: the link level and the transport level.

### The Level 2 data transport protocol

In the Level 2 trigger system of D0, all data must go through the Magic Bus to the main processors. This implies that all event data must be multiple of 128 bits or 16 bytes. The transport protocol is used by all links and is based on a 12 bytes header prefixed and a 4 Bytes trailer appended to a payload data multiple of 16 bytes. The FIC will not raise an error if the event data is not a multiple of 16 bytes.

Each transport entity should add two bytes of physical trailer at the end of the payload. These bytes contains some longitudinal parity, the type of the source and an error indicator.

### The Level 2 data link protocol

This level is responsible for the indication of “Start-event” and “End-of-event” conditions. It is also responsible for link configuration and diagnostics. There are two different link protocols, corresponding to the two chipsets.

The event delimiter function is based on protocol elements identifying the beginning and the end of an event. A trivial FSM (finite state machine) with two states and two transitions is defined.

Condition	From	To
Start-event	Out-of-Event	In-Event
End-of-event	In-Event	Out-of-Event

This FSM is the basis of the data link protocol. This protocol defines the exact implementation of the two conditions (Start-event and End-of-event). It also specifies the treatment of the fill characters (e.g. allowed in the In-Event state) and of unexpected characters (e.g. error characters or data characters in the Out-of-Event state).

### The Hot Link protocols

The Hot links are used everywhere in the Level 2 trigger system. There are many different sources and sinks of Hot Links. There may be many different physical supports for the Hot Links: optical, 75Ω coax and UTP (unshielded twisted pair). Several auxiliary modules (similar to the FIC) are needed to convert between these physical variants. There is a single protocol for all these links with the following features:

- The event delimiter function of the link protocol is based on the use of two control characters (“Start-event” and “End-of-event”).
- The links should transmit only fill characters in the Out-of-Event state; this is an obvious chipset default.
- Fill characters are allowed and ignored in the In-Event state.
- A minimal number (5) of fill characters are required before and after the End-of-event character to allow for link resynchronisation.

Some links use a control character to signal the start of a test sequence (but must use a different method to signal the end of the test sequence).

There is no synchronisation protocol: the Hot Link is said to resynchronize itself on any sequence of two fill characters and such sequences are very common.

### The G-Link protocol

The G-Link is used only from the SVX (Silicon VerteX) systems, namely the CFT, the various PS and the STT. The SVX system is common to CDF and D0, so its specifications should be taken as granted and cannot be modified. The D0 Trigger Level 2 has chosen to use the VTM (VRB Transition Modules) cards to receive the G-Links. These cards have been developed by the SVX group.

The G-Link protocol is implemented in band by using some of the data bits as protocol bits: control characters are not used. Because the 17 and 21 bits modes are not supported by the VTM, it has been decided to use 16 bits data and 2 protocol bits carried in 20 bits mode. One of the extra bit is used as a Start-event indicator, the other one as the End-of-event mark. The limitation to 18 bits follows from the size of the FIFO and from the absence of use for the two extra bits.

The synchronisation protocol is handled completely by the VTM cards.

## Error analysis of the serial links

In this section, the error performances of the serial links are computed taking into account the protocol used. The error performances are computed from the Hamming distances between code words and are not obviously connected to the actual probabilities of bit flip on the serial link. This can be used as an a posteriori control of the validity of the protocols.

### The Hot Link encoding

The Hot Link encoding starts by splitting the input character in a “a” field containing the five lower bits and a “b” field containing the three upper bits. Both fields are independently encoded giving a “a” field of 6 bits and a “b” field of 4 bits. The encoded symbol is the concatenation of the two encoded fields, giving 10 bits.

The Hot Link encoding is characterized by a feature called “running disparity”. The running disparity is a value (either RD+ or RD-) kept between transmitted symbols (more precisely between fields). There is one valid encoding of an input character (or a field) for each running disparity.

The 64 (res. 16) symbols of the encoded “a” (res. “b”) field are separated in 4 groups: type + (T+), type 0 (T0), type – (T-) and invalid (Inv). The T0 set contains symbols with as many ones as zeros. The T+ set contains a majority of symbols with more ones than zeros (plus one balanced value). The T- set is the complement of the T+ one. The Inv set contains the remaining symbols. For the “a” field there are 14 symbols for T+ and T- and 18 symbols for T0 and Inv. For the “b” field, the four types contain 4 symbols each.

The computing of the RD is given by the following rules: a T+ symbols produces RD+, a T- symbols produces RD- and a T0 symbols does not modify RD. For the Inv symbols (the receiver may get some in case of errors) one get RD+ (res. RD-) if the number of ones is larger (res. smaller) than the number of zeros in the symbol. The RD of a character is the initial RD modified by the “a” symbol and then the by the “b” symbol. The RD is computed independently in the transmitter and in the receiver.

The encoding of a field gives a T0 symbol for 50-60% of the configurations, in which case the encoding is independent of RD. In the other cases, the encoding produces a T+ symbol if the disparity is RD-, and the complimentary T- when RD+. The encoding of the data characters is summarised in the following table.

RD in	“a”	RD mid	“b”	RD out	Number
-	T+	+	T-	-	56
-	T+	+	T0	+	56
-	T0	-	T0	-	72
-	T0	-	T+	+	72
+	T0	+	T-	-	72
+	T0	+	T0	+	72
+	T-	-	T0	-	56
+	T-	-	T+	+	56

One can see that RD+ and RD- have the same probability; that a wrong running disparity may sometime produce not a wrong character, but only a violation error.

The encoding of the control characters is outlined in the following table. The “Ctl” symbol is a short hand notation for specific patterns belonging to the invalid type. The fill character belongs to lines 1 and 3.

RD in	“a”	RD mid	“b”	RD out	Number
-	Ctl+	+	T0	+	8
-	T+	+	Ctl-	-	6
+	Ctl-	-	T0	-	8
+	T-	-	Ctl+	+	6

### The Hot Link Error Analysis

For random sequences of bits, out of the  $2^{10}$  (over 1000) possible characters, about 27% are valid (256+14). The others will produce the diagnostic of erroneous character.

A single bit error will transform a T0 symbol to a T+ or a T- symbol with equal probability (~50%); there is also a small probability to go to Inv. A single bit error will transform a T+ (res. T-) symbol in about 60% of the cases to a T0 symbol, >35% to an Inv symbol, the rest being T+ and T-; these probabilities are different for the “a” and the “b” fields. For the time being, the exact computation of the probabilities is replaced by estimations.

For a transmitted data character, a single bit error produces another valid character in about 50% of the cases. The probability that an error converts a data character to a control or fill character is very small (<<1%). A single bit error has a 25% probability to modify the running disparity of the receiver. The two effects should be considered separately.

For a transmitted fill character, a single bit error will be immediately detected in 60% of the cases, will produce a data character in 30% of the cases and another control character in the remaining 10%. In all the cases producing a data character, the running disparity is modified. If the following character is also a fill character, then it will always be in error. If the following character is not a fill character, then one reverts to the case discussed below.

For a transmitted control character, a single bit error will be immediately detected in 70% of the cases, will produce a data character in 20% of the cases and another control character in the remaining 10%. But these figures are means, the exact behaviour for the 14 control characters is given in the following table (here C means control character, X means error, D means data character, F means fill character and [ ] means dependent on RD).

Original Character	The Ten Modified Characters (not in order)									
C0.0	C	C	x	x	x	x	x	x	x	x
C1.0	C	D	D	D	x	x	x	x	x	x
C2.0	C	D	D	D	x	x	x	x	x	x
C3.0	C	x	x	x	x	x	x	x	x	x
C4.0	F	C	C	x	x	x	x	x	x	x
C5.0 (Fill)	C	C	D	D	D	x	x	x	x	x
C6.0	C	C	D	D	D	x	x	x	x	x
C7.0 (Violation)	F	C	x	x	x	x	x	x	x	x
C8.0	D	D	x	x	x	x	x	x	x	x
C9.0	D	D	x	x	x	x	x	x	x	x
C10.0	D	D	x	x	x	x	x	x	x	x
C11.0	D	D	x	x	x	x	x	x	x	x
C0.7	D	D	x	x	x	x	x	x	x	x
C1.7	[C]-	[C]-	D	D	D	[D]+	x	x	x	x
C2.7	[C]+	[C]+	D	D	D	[D]-	x	x	x	x
C4.7	D	D	D	D	D	x	x	x	x	x

Suppose that the transmitter and the receiver have different running disparity before sending a character, the situation after the transmission depends if the transmitter is idle or

sending data characters. When sending fill characters, a change in running disparity is immediately detected (RD alternates between fill characters) and suppressed; a single running disparity discordance produces exactly one error.

When sending data characters, an error is detected in 71% of the cases and the discordance persists in 57% of the cases. This implies that the discordance will disappear without error in 12% of the cases and that a single running disparity discordance produces in average 1.7 errors.

For estimation of the global performances, the hypotheses are:

1. The Hot Link operates with the Level 2 protocol at an activity level of about 20%.
2. The link is subject to random isolated errors of low probability (less than  $10^{-6}$ ).

A single bit error produces in average 1.1 invalid codes. There is a 24% probability that a bit error changes a fill character to a valid data character.

For the protocol, valid character in the Out-of-Event state must be discarded. Erroneous characters in the In-Event state should be kept.

### **The G-Link case**

For random sequences of bits, out of the  $2^{24}$  (over 16 millions) possible words, less than 14% are valid. The others will produce the diagnostic of erroneous word. For error analysis, each word is independent of all the others.

For a transmitted data word, a single bit error produces another valid data word in more than 87% of the cases. Multiple bit errors have also a low probability of generating errors. The probability of transforming a data word to a fill word is negligible; for transforming to a control word the probability is  $\sim 1\%$ . The other cases are flagged as erroneous word.

For a transmitted fill word, a single bit error is detected in more than 93% of the cases. The undetected errors transform the fill word to a data word in 2/3 of the cases.

The control words are somewhere in between (difficult to go to a data word or to a fill word, but easy to go to another control word) but are ignored here because they are not used in the protocols.

For estimation of the global performances, the hypotheses are:

1. The link operates with the Level 2 protocol at an activity level of a few percent (leading to an activity below 20% on the following Hot Link).
2. The link is subject to random isolated errors of low probability (less than  $10^{-6}$ ).

Most (>95%) of the signaled errors occurs on fill words. Less than 2% of the bit errors change a fill word to a valid data word. Most errors modifying event data are undetected.

For the protocol, erroneous words must always be ignored both in and out of events. The error count is a good indicator of the bit error rate. Using some parity control at the transport layer can mitigate the non detection of data errors.



## External specification of the FIC module

In this section, one presents first the protocols used by the FIC on the link and transport layers of the trigger connections. Then, the memory section will discuss the FIFO inside the FIC. The monitoring section will details the options chosen to allow an efficient monitoring with a limited amount of logic and the control section will present the remaining features.

### The G-Link protocol.

The event delimiter function for the G-Link protocol uses an in-band channel of two bits. This in-band channel is built by using the 20 bit mode of the G-Link chipset. This in-band channel is limited to two bits because two bits are enough and because the FIFO are only 18 bits wide. The G-Link control characters are not used. There is no other function in this protocol.

Bit 16 is used to signal the beginning of the event data. It should be present with the first data word of an event. A word with bit 16 on in the In-Event state is ignored, but the “protocol error” flag will be set. A data word without bit 16 in the Off-Event state is interpreted as a “Start-event” indicator, but the “protocol error” flag will be set.

Bit 17 is used to signal the end of the event data. It should be present with the last data word of the current event. As fill words are allowed in the In-Event state, words with missing bit 17 cannot be detected. A data word with bit 17 on in the Off-Event state is interpreted as a “Start-event” indicator, but the “protocol error” flag will be set. It is not allowed to have both bits set on the same word (events should contain at least two words).

Control words and words with Error indicator “ON” are ignored, but the “protocol error” flag will be set.

### The Hot Link Protocol

The Hot Link protocol is built with the control character capability of the Hot Link chipset and with some other techniques. This protocol has several components:

The two characters composing a transmitted word are send with bits 0 to 7 transmitted first, followed by bits 8 to 15. The two characters of a word are never separated by a fill character.

The FIC will append to the event one word (i.e. two characters); the bits 0 to 7 contain the longitudinal parity of the received event, computed on 8 bits characters; bits 8 to 14 are set to zero and bit 15 is an error indicator: it is set if the “protocol error” flag has been set by the G-Link during the reception of this event. The longitudinal parity is the XOR of all the characters in the message; e.g. a message composed only of zeros will have a parity of 0.

The event delimiter function (to identify the first and last character of an event) is based on two control characters (a “Start-event” and an “End-of-event”). The protocol requires that several (at least five) fill characters are present on both sides of the “End-of-event” character. The fill characters inserted between the trailer word of an event and the corresponding “End-of-event” control character are added to improve the probability that the “End-of-event”

character is not received by a de-synchronised receiver. The “Start-event” and “End-of-event” control characters can be defined with on-board jumpers. For the tests in Saclay, we use K28.0 (data = 0) as the “Start-event” control character and K28.3 (data = 3) as the “End-of-event” control character.

The error detection function is used to signal a loss of synchronisation of the G-Link. This is indicated by the absence of the “G-Link ready” signal. This is a major error and deserves an immediate action. One has to disable the triggers, allowing the G-Link to settle down to the idle state. This will allow a spontaneous resynchronisation and the disappearance of the error condition. This function is implemented out of band by a dedicated bus line in the back-plane, **with the JE2-A2 position in the VME connector.**

The test function, used to signal that the transmitter has switched to the BIST (Built In Self Test) mode is implemented as VME instructions.

## The Memory

The FIFO between the G-Link and the Hot Link must accommodate 16 events in the worst case; this translates to a size of 8 Kbytes. The FIFO full condition should never occurs. An error flag is set when this happen. No other action is taken in the FIC. Overflow data is discarded.

## The Monitoring

An external computer monitors the FIC by reading the monitoring data through the VME port at a regular rate (e.g. every 10 seconds). This data must be cleared (by a VME action) after each reading. The FIC contains the needed monitoring data in a set of latches and counters. The monitoring data comprises:

Status of each G-Link. This is the “ready” flag of the G-Link chip.

Latches for the four conditions “FIFO full”, “More than 16 events in a FIFO”, “Error counter overflow” and “Protocol error on G-Link”. These latches are set by the conditions and are reset from VME.

Errors count on each G-Link. These are five bits counters recording the number of invalid cycles (error or control) produced by the G-Link chip. Overflows of these counters are recorded in latches.

Histogram of event counts. This is a set of five counters. Every 2ms one (and only one) of these counters is incremented: the sum of the 5 counters gives the time since the last clear. The counters have 12 bits and should not overflow if the readings are made less than 8s apart (overflow of these counters are recorded in latches). These counters give an idea of the occupancy of the FIFO. There are overflow latches for these counters as for any other counter in the FIC. The latching of an overflow has no side effect on the counters. The rules for incrementing the counters are:

1. Histo0 is incremented if all FIFO are empty.
2. Histo1 is incremented if at least one FIFO has an event and no FIFO have more than one.
3. Histo2 is incremented if at least one FIFO has two events and no FIFO have more than three.
4. Histo4 is incremented if at least one FIFO has four events and no FIFO have more than seven.
5. Histo8 is incremented if at least one FIFO has 8 or more events.

The maximum number of events in the FIFO is computed continuously; the maximum value of this count in the 2ms period is used to increment the histogram.

## The Controls

In addition to the monitoring data, the current status of the FIC can be accessed through the VME port. This comprises, for each link:

1. Current FIFO flags (full and empty).
2. Current events count in FIFO.
3. Current state (idle or processing event) of the input and output link FSM (Finite State Machine).

There is also a one byte field and a trigger bit associated with the slow control of the VTM optical receivers, see below.

The VME port is also used for debugging purpose: the FIFO can be read and written from VME and the automatic forwarding of events can be disabled. This allows for independent testing of the G-Link and Hot Link segments terminating in the FIC.

### Reset

There is a VME reset bit and a front panel push-button allowing resetting the FIC to its power-up state. A reset is also performed when the SYSRST signal from VME is asserted. The reset will empty all the FIFO, clear all the counters and latches, reset the input and output state machines to the Out-of-Event state and abort any ongoing VME transaction.

### The serial control of the VTM

The VTM can be controlled from the FIC, through a serial link. When instructed by the VME, the FIC will transmit one byte of command to the VTM. That command should have been previously deposited in the FIC by a VME write. This command may trigger some answer; in that case the response byte replaces the command and can be read by VME.

The format of the command is

G-Link #	command
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There are 3 bits for the G-Link number and 5 for the command. The channel number recognised are 0, 1, 2 and 3. The valid commands are

Command	Mnemonic	Function	Response
1	Convert	Return optical power	Yes
2	SigDet	Return signal detect indicator	Yes
4	ClkInh	Disable G-Link clock	No
8	ClkEn	Enable G-Link clock	No
16	RstChn	Reset G-Link	No

The values returned by the two first commands are explained in the Finisar documentation. The effect of the last three commands can be found in the HP G-Link specification. It should be noted that writing in the FIFO requests the G-Link clock, even for VME write.

The serial transmission is rather slow (9600 baud). There is always a wait for a response, even with commands without response. The typical time is 3ms. During this time, the trigger bit remains set and can be pooled for operation completion

# FIC Module Specifications

## Inputs and Outputs

There are only four G-Link inputs to the FIC. The inputs to the FIC are through the VTM. Please refer to the VTM reference for details.

There are four Hot Link outputs from the FIC. These outputs are similar to the one proposed by the University of Maryland. The four outputs use four RJ45 connectors.

There is a “Synchronisation Loss” signal. This signal is asserted when at least one of the G-Link receivers is not ready, see the VTM reference for the conditions leading to a drop of the ready state of the HDMP1014. This signal has a TTL level. It is active low and open collector like the bussed VME signals (DTACK, BERR...). **In absence of specification, this signal has been assigned to the JE2-A2 pin.**

## VME Commands

The FIC is an A32, D32 VME slave; it does not implement block transfers and interrupts; it is fully compliant with the VME specs. VME write are always executed as individual bytes; it is possible to write the four bytes of a longword in a single VME cycle. VME read are always executed by longwords. Some exceptions are noted where applicable.

The FIC responds to the following address modifiers:

- 0E -- Extended Supervisor Program Access.
- 0D -- Extended Supervisor Data Access.
- 0A -- Extended Non privileged Program Access.
- 09 -- Extended Non privileged Data Access.

The FIC recognizes addresses of the form XXXXUAYZ where XXXXU are the values on five rotary switches on the FIC board (we use U instead of X for the last one because only 3 bits are used instead of 4), A is the (5 bits) geographic address of the FIC board, Y is 0,1 and 2 and Z is any value from 0 to F. The VME interface can assert BERR in case of illegal address (incompatibility between LWORD and A1).

The 12 longwords are organized in three areas: a control area of five longwords, a monitoring area of also 5 longwords and a debug area of two longwords. These areas are displayed and explained below.

Unless explicitly stated otherwise, the content of all longwords is set to zero during power-on or resets.

	31	23	15	7
ad 00	CTL	Serial	unused	WFx
ad 04	unused	Flags	FSM	FIFOx
ad 08	FIFO0		FIFO1	
ad 0C	FIFO2		FIFO3	
ad 10	Cnt0	Cnt1	Cnt2	Cnt3
ad 14	Flag0	Flag1	Flag2	Flag3
ad 18	Err0	Err1	Err2	Err3
ad 1C	Histo0		Histo1	
ad 20	Histo2		Histo4	
ad 24	Histo8		OvHist	
ad 28	FIFO0		FIFO1	
ad 2C	FIFO2		FIFO3	

## Control area

### Byte at 0: CTL field

This field contains five bits. These are the reset bit, two trigger bits and two control bits. The control bits are normal registers, set and reset only by VME. The trigger bits are bits which can be written to one by VME and are reset to zero by the internal module logic. It is not possible to write these bits to zero from VME once they have been set to one. This kind of bits are used to trigger some action in the module. The reset bit is a kind of trigger bit which is set by the internal logic and can be cleared from VME.

Bit 31 Reset is the bit used for resetting the FIC to its power-up state. Setting this bit has the same effect as a true power-up or a push of the front panel button. The only difference with a true power-up is that this bit will be set after the VME triggered reset while it should be reset after a true power-up (the power-on value of this bit is defined but is currently unknown, it is expected to be zero). Writing this bit while it is already set has no effect. This bit can be cleared by VME without any side effect. This bit is cleared by resets caused by the front panel button or SYSRST.

The VME access to set this bit works normally, but subsequent VME accesses will fail during the reset. The typical duration of the reset is 100ms.

Bit 30 Execute is the trigger bit for sending serial message to the VTM. The content of the byte at address 1 is serially transmitted to the VTM, followed by a long wait for reply (3ms). The bit remains set until the end of the wait. The programmer should poll the content of this bit to check for the completion of the command. If the command produces a response, then the response byte will replace the content of address 1; in the other case, the content of address 1 will not be modified.

Bit 29 Clear is the trigger bit for resetting the monitoring statistics. Setting this bit will clear all the flags and registers in the monitoring area, i.e. long-words from 14 to 24. Bit 25 Inhibit is the control bit used to disable the automatic transmission of events on the Hot Links. The FIC is in normal mode of operation when this bit is reset. When this bit is set, a non empty FIFO will not start an event transmission on the Hot Link. Setting this bit while an event is being emitted has no effect until the end of the event. This bit is set to zero at power up.

Bit 24 Bisten is the control bit used to enable the BIST mode of the Hot Links. When this bit is set, the four Hot Link are in BIST mode. This bit is set to zero at power up.

#### **Byte at 1: Serial field**

This field is a read/write field used to get parameters from and to send control commands to the G-Link receivers. This field is used in conjunction with the execute bit at position 30 in word 0 (CTL field). This field is described in the previous section.

#### **Byte at 2**

This byte is not used. It cannot be accessed alone. Write to this location have no effect and read returns 0.

#### **Byte at 3: WFX field**

This field contains the two extra bits needed to write into the FIFO. They are used when one write in words 28 to 2E.

The bits for FIFO0<17,16> are in bits 7 and 6; those for FIFO1 are in bits 5 and 4; those for FIFO2 are in bits 3 and 2 and those for FIFO3 are in bits 1 and 0.

#### **Byte at 4**

This byte is not used. On read, it contains 0.

Remark that the nine longwords at locations between 4 and 24 included are read-only; write to any of these bytes will cause bus errors.

#### **Byte at 5: Flags field**

This field is a read-only field used to read the status of all the FIFO. Each FIFO has two bits: the FIFO0 flags are in bits 22 and 23; the FIFO1 flags are in bits 20 and 21; the FIFO2 flags are in bits 18 and 19 and the FIFO3 flags are in bits 16 and 17.

The values of these pairs of bits can be:

- 00 empty FIFO.
- 01 FIFO containing data, but not full.
- 10 Illegal, should never occurs.
- 11 full FIFO.

#### **Byte at 6: FSM field**

This field is a read-only field used to read the status of all the FSM. Each channel has two bits: the channel #0 has bits 14 and 15; channel #1 has bits 12 and 13; channel #2 has bits 10 and 11 and channel #3 has bits 8 and 9.

The values of these pairs of bits can be:

- 00 Both FSM in Out-of-Event state.
- 01 G-Link FSM Out-of-Event and Hot Link FSM In-Event.
- 10 This should never occur in normal operation.
- 11 Both FSM in In-Event state.

#### **Byte at 7: FIFOx field**

This read-only field contains two extra bits read from each of the FIFO. The bits from FIFO0 are in bits 6 and 7; the ones from FIFO1 are in 4 and 5; the ones from FIFO2 are in 2 and 3 and the ones from FIFO3 are in 0 and 1. The comments of word 8 can be applied to this byte.

The values of these bits can be:

- 00 Bits 16 and 17 of FIFO reset (it is a normal word in an event).
- 01 Bit 16 set : “Start-event” indicator (it is the first word of an event).
- 10 Bit 17 set : “End-of-event” indicator (it is the last word of an event).
- 11 Both bits set: “End-of-event” for an event where a G-Link error has been detected.

### Word at 8

Read-only word for FIFO0. This word is part of the nine bytes (7 to F) allowing access to the current content of the output lines of the FIFO. This content may change quickly under the action of the Hot Link chipset; so, the value captured by the VME may not be accurate. If one want a precise value, one should disable the Hot Links before reading the value.

### Word at A

Read-only word for FIFO1. Similar to word at 8.

### Word at C

Read-only word for FIFO2. Similar to word at 8.

### Word at E

Read-only word for FIFO3. Similar to word at 8.

### Byte at 10: Cnt0

This read-only byte contains the current number of events in FIFO0. This number includes partial events. The five bits counter is incremented when the G-Link receives the “Start-event” indicator; it decrements when the Hot-Link transmits the “End-of-event” control character. When this counter has a value of 16, an increment request will set the corresponding latch (bit 26 in word 14) and the counter will **!choose between!** stay at 16 until it is decremented **or** go to 17. The counter will count up to 31 before ignoring increments.

This counter will be reset to zero when the corresponding FIFO is empty and the corresponding G-Link FSM is in the Out-of-Event state.

### Byte at 11: Cnt1

This read-only byte contains the current number of events in FIFO1. Similar to Cnt1.

### Byte at 12: Cnt2

This read-only byte contains the current number of events in FIFO2. Similar to Cnt1.

### Byte at 13: Cnt3

This read-only byte contains the current number of events in FIFO3. Similar to Cnt1.

## Monitoring area

### Byte at 14: Flag0

This read-only byte contains the error flags associated to the G-Link # 0. These are one error status and four error latches in this field. This byte can be cleared by using the **clear** trigger in bit 29 of word 0.

- Bit 28 The G-Link is not ready (not clearable from VME).
- Bit 27 The FIFO full latch.
- Bit 26 More than 16 events in FIFO. Set when an event enter the FIFO while Cnt0 has the value 16.

- Bit 25 Protocol error. Set when a protocol error is detected on the incoming G-Link.
- Bit 24 The error overflow latch. Set when the error counter (bits 24-28 in word 18, field Err0) overflows.

**Byte at 15: Flag1**

This read-only byte contains error flags for G-Link # 1. Similar to byte at 14.

**Byte at 16: Flag2**

This read-only byte contains error flags for G-Link # 2. Similar to byte at 14.

**Byte at 17: Flag3**

This read-only byte contains error flags for G-Link # 3. Similar to byte at 14.

**Byte at 18: Err0**

This read-only byte contains the error counter for the G-Link # 0. This byte can be cleared by using the **clear** trigger in bit 29 of word 0.

- Bit 24-28 These contains the error counter. This counter should not overflow if the bit error rate is in the specifications. In case of overflow of this counter, the bit 24 of word 14 (Flag0 field) will be set and the counter will wrap around to zero, continuing the count.

**Byte at 19: Err1**

This read-only byte contains the error counter for the G-Link # 1. Similar to byte at 18.

**Byte at 1A: Err2**

This read-only byte contains the error counter for the G-Link # 2. Similar to byte at 18.

**Byte at 1B: Err3**

This read-only byte contains the error counter for the G-Link # 3. Similar to byte at 18.

**Word at 1C**

This read-only word contains the 12 bits histogram counters Hist0. The meaning of the content of this group of counters was described in the monitoring section of the external specifications. This counter is contained in bits 16 to 27 of the word.

In case of overflow of this counter, the bit 0 of word 29 (OvHist field) will be set and the counter will wrap around to zero, continuing the count. This word can be cleared by using the **clear** trigger in bit 29 of word 0.

Just after a power-up or a reset, this counters contains 0. It should increments continuously at 500Hz when there is no activity on the links.

**Word at 1E**

This read-only word contains the histogram counters Hist1. The counter data is in bits 0-11 and the overflow bit is in bit 1 of word 26. After a reset, the counters in words 1E to 24 should stay at 0 until events start to flow. Otherwise similar to word at 1C.

**Word at 20**

This read-only word contains the histogram counters Hist2. Similar to word at 1C.



**Word at 22**

This read-only word contains the histogram counters Hist4. Similar to word at 1C.

**Word at 24**

This read-only word contains the histogram counters Hist8. Similar to word at 1C.

**Word at 26**

This read-only word contains the overflow bits associated to the five histogram counters. Bit 0 refers to Hist0 in word 1C, bit 1 refers to Hist1 in word 1E, bit 2 refers to Hist2 in word 20, bit 3 refers to Hist4 in word 22 and bit 4 refers to Hist8 in word 24.

This word can be cleared by using the **clear** trigger in bit 29 of word 0.

**Debug area****Word at 28**

Read/write word for FIFO0. Write in byte is not supported: the FIFO is 18 bits wide and cannot be partially written. Any attempt to write only one byte will produce a bus error. The Wfx field (at address 3) supplies the two extra bits needed for a write.

Read are long word operations: FIFO0 and FIFO1 are always read simultaneously (as FIFO2 and FIFO3), independently of the actual size of the VME read operation. When there is a VME read of this longword, there is also an actual read of FIFO0 and FIFO1 (this is the difference with longwords at 8 and C). One should be careful about the side effects on the FIFO content.

There is no protection against simultaneous access to the FIFO from VME and from the link chipsets. It is the responsibility of the programmer to ensure that the G-Link is idle before writing in the FIFO and that the Hot Link is disabled before reading the FIFO. Failure to respect this rule will produce unpredictable effects on the events.

**Word at 2A**

Read/write word for FIFO1. Similar to word at 28.

**Word at 2C**

Read/write word for FIFO2. Similar to word at 28.

**Word at 2E**

Read/write word for FIFO3. Similar to word at 28.

**Mechanical and electrical characteristics****Front panel**

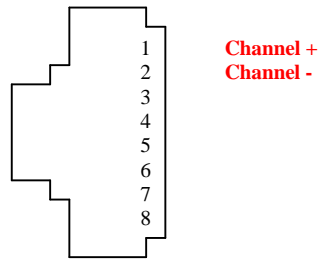
It contains one push-button, four connectors and 26 indicator lights.

**Button**

The push-button is intended to allow a manual reset of the FIC. This reset is identical to the power-up reset (see section on controls).

## Connectors

There are four output connectors for the Hot Links. They are RJ45 connectors. The pins are allocated as shown (seen from front panel):



## Indicators

There are two global indicators and six channel indicators (three red and three green) for each output.

The two global indicators are:

**PwrClk** This red indicator is on when both the +5V and the VME SYSCLK signal are present.

**VME** This green indicator is on when a VME action is in progress.

The three red per channel indicators are:

**Gsyn** This indicator is on when the corresponding G-Link is not ready.

**Fofl** This indicator is on when there is either "FIFO full" or "Event counter overflow".

**Eofl** This indicator is on when there is either "Error counter not zero" or "Error counter overflow".

The three green per channel indicators are:

**Gclk** This indicator is on when the corresponding G-Link clock is present.

**Glon** This indicator is on when an event is being received on the G-Link.

**Hlon** This indicator is on when an event is being transmitted on the Hot Link.

## Electrical consumption

+5V 5 Amp

This power supply is protected by one 5A fuse of type TR5.