FIC for L2 Inputs? With Updates and Decisions from Workshop

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Criteria for Decisions

- Meet Performance Criteria
  - bandwidth, deadtime, acceptance, rejection
    - with adequate margin (for occupancy e.g.)
- Acceptable Schedule Risk
  - (Includes complexity)
  - specification
  - resources
  - prototype and construction
  - commissioning
- Maintenance and Repair
  - resources, complexity, card variants...
- Parts and Engineering Costs
  - within constraints
- Expansion Capability
  - beyond planned scope

New Information from Workshop and Decisions

- New Information at Workshop added in BLUE
- Decisions at Workshop added in RED

Current Input Formats
L2 Baseline

160MHz Cypress Cu Muon
SLIC only 16MB/s

160MHzFiber Global, Cal L2
(protocol subset of Muon)

"1.3 GHz G-link":

- 25 bit frames X 53 MHz = 1.3GHz
- 20 bit L1 CFT 1060MB/s
- 16 bit L1 CPS/FPS 848MB/s
- 16 bit raw (STT, L2PS(?) 848MB/s
  - needs event number tagging
  - not integer multiple of 16 Bytes

1.3 GHZ AMCC (53 MHz X 24 bit)

- SCL mezzanine (CU or Fiber?)
- L1 Mu Cu (not seen by L2)

Workshop Strawman
L2 Inputs

- Cypress 212 everywhere
  - L1 CFT/PS (32b per track)
  - L2 mu
- Serial J2 FIC 53 MHz
  - **A**: G-link in: avoid unless raw data
  - **B**: 16 Cypress Fiber
  - **C**: 16 Cypress Copper
- SCL receiver on each SLIC

MBT

- 16-deep FIFOs all channels
- either G-link or Cypress
- 128b Mbus broadcast
- SCL Mezzanine
  - Send L1 to FIFO
  - Queue L2
  - SCL Initialize
- 2 Cypress Outputs
- Digital I/O (e.g. to Framework)
- VME slave (&Mbus programmed I/O)
  - download
  - control
  - monitor

SLIC

- 16 FIFO's
- either G-link or Cypress inputs
- FPGA routing
- 4 TI C6x Integer DSP's per card
- Master DSP for readout
- 2 Cypress outputs

  hope can send even L3 Unbias data via Cypress outputs

- SCL Mezzanine

  receive SCL Initialize

  send L1 SCL (e.g. Qualifiers) to FIFO

  L2 Accept/Reject?

  - Irrelevant if readout only via Worker Alpha

Serial to Parallel FIC
J2 Backplane Protocol

- 3b Input type
- 64b data
  - G-link: 16b X 4 sources
  - Cypress: 8b X 8 sources
- 1b Cypress_1st_8_Sources
- 8b End_Event
- 8b Data_Strobe

- 84 pins

Question: sure can Mux w/o FIFO?

All FIFOs on FIC (Saclay Proposal)

- VME slave interface
  - monitor (FIFO occupancy scalers)
    - which sources active
    - test data injection
- data pulled across J2 by SLIC/MBT
- data available only when all pieces of event present
- blocks of 8B from a single source

FIFO on FIC
J2 protocol (75 pins)

- 64 b Data (8B) FB
  FIC to board =FB
- 3b Pad_Byte_Count (0-7) FB
- 4b Source_Address FB
  sources in strict geographical order
  skip inactive sources
- Data_Ready FB
  drop at end of event
- Request_Data BF
  request to present data on next clock
  board must drop if no Data_Ready
- Data Clock (40-53 MHz) BF
  any rate board prefers
  board can skip cycles to think
- SCL Initialize
- ?? Link Error??

FIC Power

- Original FIC 22W
  - 4 G-link in, 4 Cypress out
  - 4 FIFO's
  - no VME

  VME is 10 W

  FIFO dominates
    - could use 32 KB FIFO (2 species)?
- Variants with VME interface + FIFO's:

  (Saclay Proposals)

- FIC+ A 34W
  - 4 G-link
- FIC+ B 73 W
  - 16 Fiber Cypress

Move inputs to backplane transition card ("FIC") on J2

+ more real estate on SLIC/MBT
+ protect cables
+ replace/ test SLIC/MBT cards without disturbing cabling
+ money and engineering from Saclay (allows financial contribution)

- MBT, SLIC must negotiate backplane protocol (with Saclay?)
- expense: 2 cards wherever 1 card before (FIC not just for G-link inputs)
- more groups required to

  test prototypes commission maintain

Decision: YES, but not FIC, just inputs

accept engineering risk for cabling ease

Common J2 for MBT, SLIC

+ flexibility
  - choose G-link, Cypress inputs
  - (but Classic FIC allows this too)

- limited number of G-link inputs/card
  - unless do classic FIC
- negotiation time risk

Decision: Yes (Serial J2 simple to negotiate)

Common backplane also for STC (FPGA card)

only works for serial-parallel through J2

implies 212 Cypress Fiber

+ flexibility:

FPGA card more a "component"

e.g. for receiving raw data

could use input section as FIC

if raw data needed for L2PS

- extra layout: VTM uses J3 now, not J2

Decision: Use unaltered VTM

Get rid of Cu Cypress? L2 G, Cal, or L2Mu too?

+ easier to make work than copper
+ uniformity (SLIC, MBT inputs closer)
    single-output FIC?
? better ground isolation
    Cu has transformers
    L2 may be in fixed counting house

- L2 muon already using copper
    change 5 cards or convert 200 cables
- careful handling needed
    1dB loss from fingerprint
- $30/channel more cost
- add to L2 protocol, or lose testing in mu

Decide: 1) Leave muon Cu
2) UMd picks: MBT input Cu or Fiber

Speed up L2 Cypress Fiber 160 MHz to 212 MHz

required for serial-parallel J2 scheme

+ more bandwidth than 160 MHz (+ 1/3)
+ avoid extra clock: multiple of 53 MHz
  (SCL mezzanine, and G-link)

- less noise margin
- mu needs to change to 212

Decide: NO, leave at 160 MHz
(Serial-Parallel J2 protocol dropped)

L1 CFT/PS Output → 212 MHz Cypress Fiber

+ no need for "classic FIC"
  except for raw data
+ system uniformity (fewer input types)

- L1 CFT arrives later at L2STT
  more/earlier buffering?
  8μs to xfr (budget is 10 μs)
  L3 readout harder?? same

- L1 CFT needs output buffer
  complexity behind sheild wall
- cost? own 100 G-links already?

Decision: Keep G-link

Drop 20-bit G-link mode

+ remove one type of input

- transmission 1.6X slower
  - 20 bit to 32 bit
  - probably only affects L2 STT
    - elsewhere in L2 already 32 bit

Decision: Yes, Drop 20 bit mode

Serial Through J2

+ decouples SLIC/MBT from input type
+ most flexibility

- engineering risk, especially at high speeds

  IF tests correct, lose month to decide and cost of custom backplane

- need active extender for J2 Serial?

Decision: Accept backplane inputs,

Serial J2 as best of these protocols

Serial to Parallel thru J2

Decide: NO

STC uses VTM--no economy of scale

- FIFO's on main card
  data push @53 MHz, not data pull
  requires 212 Cypress

+ reduce need for 40MHz clock

+ recoup VTM engineering (esp. Raw)

- SLIC/MBT see multiple input protocols

- 4 G-link max; 16 Cypress is muxed

- negotiation time for details

- event synchronization assumed!

  add event tags?

  - transmission time degraded
    transmit until last source of event?

- thin FIFO's to synch source clocks

  as complex to control as full FIFO's?

  must guarantee can't be overrun

  no problem if out speed >= input

- Clumsy for SLIC

FIFO on FIC
Advantages and not

SEE NEXT SLIDE

+ standard building block
+ no extra FIFO just to shift speed
+ reduce number of MBT's (could raise to 16 inputs each)
+ maximize Saclay contributions
- negotiation time:
  more control required across J2?
- raise number of cards in system (common to all backplane proposals)
- lots of heat on transition card
- extra VME interfaces (management)
- extra VME bus loads (readout speed?)
  MAIN ISSUE IS R/O reliability
  last run: hang/15 min in 20-card crates
  unacceptable: more MB/s, evt loss
- L1 SCL: extra Cypress out on MBT

FIFO on FIC Decision (2)

- not optimal for both SLIC and MBT
  - SLIC: 32-bit wide memory to feed
  - MBT: whole events, 128b Mbus

Notes:

- 1” from bus in VME spec
- beat on Alpha card
- Modify VBD’s to be less sensitive
  - tradeoff readout speed, but do it
- could use 32KB FIFOs on some cards
- Serial VME? Not implemented on Bit3

DECISION

- FIFO on FIC will not be pursued

Classic FIC:
G-link to FIFO to Cypress

+ isolates receiving card from G-link input

+ build only where needed

L1CFT/PS or raw

+ protocol negotiation simple

- extra FIFOs in system to monitor and control
- complex if receiving raw data: event tag

Decision: Retain Classic FIC for G-Link

G-link FIC as standalone card

+ allows > 4 G-link inputs to SLIC or MBT

+ G-links a danger to serial J2 protocol

- extra slot somewhere

for every 4 G-link inputs (6?)

+ room exists in tracking crates 2nd floor

- 20-30 W on transition card is acceptable

so could do as transition card, even with 2-4 Cypress outputs

WILL use VTM in STT input crate

Advice: do as standalone VME card, not transition card to allow flexible # inputs

Event Tagging in FIC
Not Discussed

[requires new FIFO interface for any scheme]

- local clock control
  - + same scheme as muon (and L1 CFT)
  - - new interface not needed by other cards in crate
  - - need VME interface to manage, resynchronize? or self-synch every turn?
- inject L1 SCL into FIFO's as header
  - + need filtered L1 SCL information to process event anyway
  - + automatically arrives before new event and after old one
- critical ONLY for G-link raw data input:
  - L2 PS needs raw
  - STT with SLIC clustering ("Fortner")
- STC card scheme uses Road Card to fan out SCL information?

SCL Fanout to SLIC
Not Discussed

- SCL Initialize

  force clearance of buffers,

  even if partial events

- L1 Qualifiers

  how to process this event

  probably needs to get in FIFO

- L1 Accept number

  enough to be sure event synched

- L2 accept/reject info?

  probably NOT needed if

  - Administrator in full control of L3 readout
  - L3 readout only from alphas, not SLIC

Classic SFO

- Special Card
  - made of blocks from MBT design
  - Fan out via Cypress

+ uses simple interface (Cypress)
+ naturally FIFO'd for processing of event

- extra card to build just for SLIC crates
- cables running across cards
-? if needed to steer processing
  - treat differently from other inputs
  - read first

SFO by backplane bus

- 16b qualifiers
- 1b SCL initialize
- 4b L1 Accept

+ eliminate SFO card

+? Naturally different from other inputs

- more function on MBT
- pins on J2 scarce
- NO bussed pins on J2
  hand-bus on J2
  or front-panel cable bus
- time to negotiate bus protocol

SCL Receiver on SLIC

+ eliminate SFO card

- $500 per SLIC for Mezzanine
- more for extra modules at hub end
- bend SCL protocol even further
- more function on SLIC

Road Card/SFO merge?

+ eliminate SFO card
+ share function with L1 CFT Fanout?

- Conflicts with Mbus on J3
  - if road fanout in STT crate on J3

STT Baseline

- L1 CFT input on G-link via J3 (as in VTM card)
- Fiber road card fans out to STC's on J2 road bus
- STC FPGAs perform cluster and road match
- clusters to fitter card on 40 MHz J3 output (cluster) bus
- fitter card track output:
- Cypress hotlink (160 MHz) to L2CFT for L2 data
- VME accessible output memory for L3 readout of full data set
- Storage of input data on Unbiased Event Qualifier for VME readout.
- VBD for readout; fiber road card as controller

STT Baseline + L1CFT on Cypress

- STC receives SMT data through J2 from a FIC.
- 16-deep input fifos for each input channel (location moved)
- L1CFT information arrives 212 MHz fiber instead of G-link
- Output Cypress hotlink now 212 MHz fiber

STT with SLIC clustering ("Fortner Proposal")

- G-link FIC for SLIC
- need event tagging on FIC (or SLIC)
- fan-out of L1 CFT information to SLIC
- complexity rises if limited to 4 G-link inputs per SLIC
- SLIC does clustering
- Fitting done in Alpha
- Bit3 + Alpha Administrator for download/monitoring/readout

STT with Fitting in SLIC (Strawman)

- STC as with L1 CFT on Cypress
- Clusters to SLIC via Cypress Fiber 212
- crate = 9 STC 2 SLIC 1 fiber road card
- Fitting in SLIC
- issues:
  - transfer times in and out of STC
  - passive fanout enough for L1 CFT?
  - connectivity of SLIC:
    - assignment of DSPs to tracks
  - timing and number of DSP's per card
- download/control/monitoring/readout:
- Fiber Road card vs Bit3/Alpha Admin

Other L2-STT Commonality

- similarity of road card and SCL Fanout?
- if raw input needed for preshower:

  G-link FIC (as SLIC clustering)?

  STC with Fiber output as G-link FIC?