Inputs to L2 Global

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December 19, 1996

Choosing a Physical Input

- Already picked a variable-length data format
- Now wish to choose a common physical layer for all L2 preprocessors to feed L2 Global
- Prefer a physical layer used by one or more L2 preprocessors for input as well
  - avoid multiplying protocols
- see

  http://www.pa.msu.edu:80/hep/d0/ftp/l2/data_transfer/
  Global Data Input Links.ps Global Data Format.doc

I/O Requirements

- Global:
  - 10 KHz x .5 KB/event = 5MB/sec/10 links
    =.5 MB/sec per link
- Hope to use for input to L2 Cal Preprocessor
  - 10KHz x 3-12 KB/event / 10 links = 12 MB/sec
- What does mu preprocessor need?
  - 1/3 MB/sec (2% X 16MB/sec = slow “Hot Links”)
- Suggest design for 30 MB/sec per link
  = backplane speed divided by 10 links

Control Issues

- Simple control protocol:
  - use event terminator
  - wait fixed time after terminator

    then send next event
  - no per-event handshake
  - event length used only to cross-check

Driver (Commercial?)

- Speed of physical link?
- VME Format?
  - more likely to find commercial card
  - 20-60 B/μsec (32 vs 64 b)
  - contention? (e.g. with L3 readout)
- PCI Format?
  - 50-150 B/ μsec (32 b)
  - more likely to have to build?
  - 90 degree connectors??

D0-built Receiver

- need compatible chip-set available
- Multiple sources on 128 bit “Magic Bus”
  - 320 B/ μsec on “VME for Physics” crate P3 bus
  - fast bus arbitration
  - single event on bus at a time
- perhaps 8 inputs per VME card
- 16 input buffers per card
- on-board arbitration among 8 sources

CDF inputs vs D0 plans (Not sharable?)

- smaller events, 50 KHz
- Central control of buffers
- N=4 buffers vs 16
- sources serialized
  - central source control?
  - event-synchronous preprocessors?
  - control link back to sources?
- each source: full bandwidth of “Magic Bus”

Some Simulation Issues

- The input buffering means extra transfer time:
  - input to receiver buffers
  - transfer into Global buffers across “Magic Bus”
- How many Cal Preprocessor output links?
  - 1 natural if VME

    extra overhead, synchronization to combine results
  - 3 natural if PCI

    probably does not inflate slot count