L2 Fast Monitoring

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Goals of Fast Monitoring

- Understand (for normal operation)
  - sources of deadtime
    - processing time for each element
    - loading of each of buffers within system
    - interaction of trigger setup and performance
  - where to expend tuning effort to improve performance
- Assist in debugging in case of problems

Buffer Occupancy

- To track deadtime need to know where events pile up
- Must monitor every (set of) input FIFO's
- This is the truth
  - knowing processing time is not enough
- Fast monitoring = scaler gate
  - sample say 100 ns, no correlation with event flow
- fraction of time with 0,1,2,….16 events

Proposal

- At least 1 set of scalers per board
  - on-board scalers, readout by VME

    scalers for each channel, 0….16 events (17 n scalers)

    perfect precision of latch not required

    if fuzzy, keep separate scaler for total cycles

    need clear command
  - in L2 HWFW, send gate by differential ECL
- Contents: Select among
  - Channel *m*
  - worst channel on card
  - present to logic analyzer even if onboard scalers

Other thoughts

- Onboard or off-board scalers required for non-CPU boards (e.g. MBT, FIC)
- CPU boards MAY choose to give equivalent information by recording fraction of time with 0,1,2….16 events by CPU timer
  - circular buffer of times at transitions
  - if this doesn't interfere with processing too much
  - still should present current count to logic analyzer
  - probably only one "channel": event-synch input