L2 Protocol: Decisions at Last?

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L2 Hardware Issues after Workshop

- L2 Header, Trailer — finally?
- FIFO sizes — OK
- 2 state vs stateless inputs — 2(optional)
- re-framing protocol for G-link, Cypress — OK
- G-link control characters? — OK
- VTM vs Finnisar (FIC) — VTM
- VME decisions: FIC? Other issues — VME
- shortened Mbus? — yes
- Revised GS (L2) Definition — check/propose
- Purchasing, spares, part counts — tomorrow

Current situation

- All items for L1CFT, MBT are agreed to
- for FIC, some items being looked into
  - if it changes from this, I will notify

In Other News

- Prototype Alphas at U Mich
  - first problems found and fixed
  - have talked with debugger, PCI
- Draft 4 MBT spec/TDR
  - heavy iteration with JTL
  - some holes shaken out of specs
  - Arbitrary Data Download by separate card
- Draft 2 FIC spec soon
  - successful iteration with JTL
    - all concerns fixed, or at least agreed to try in January

Standard Crate VME Slot Assignments

- 1: Bit3 (Crate Controller) no J3
- 2: VBD (2 signals from J3 to Admin)
  - through connector (or hole in blank MBus)
- 3-6 J3 connector for VTM
  - up to 4 FIC's, or any non-MBus cards (SLIC/SFO)
- 7-21 J3 Magic Bus:
  - 21 Pilot MBT (preproc. : 1MBT for 2 Workers)
  - 20 [Assistant MBT]
  - 18-19 Administrator
  - 16-17 Worker [need MBT/2 Workers]
  - 7-15 +4 Workers or non-MBus cards

VME

- A32/D32 slave for MBT, FIC (SLIC A24/D16)
  - able to read back whatever is settable status
  - registers (L1_busy for FIC, state, error, …)
  - Geo Address: J1 5th row for setup: G*step+addr
- Hope: Bit3 MPM optical 618 instead of 412
  - prototype in January; have PCI Extender Crate
  - direct view of full crate address space from TCC
    - requires PCI extender crate

L2 Maximum Event Sizes

- Length = 16B(min) … 4KB (max) X 16 events
  - includes 12B header and 4B trailer
  - source pads to multiples of 16B with zeros after trailer
  - VRB: 32KB or 64KB, but currently no raw data to L2!
  - 5 KHz max (Cypress) is 16B/μs X 200 μs =3.2KB
    - clearly issue of max, not mean!
- Actual Max Event / FIFO "event" total

	Actual Max Event	FIFO "event"	total
FIC/CFT/PS	272B	.5KB	8KB
Cal/MBT	304B	4KB	64KB
Mu/SLIC	.3 to 3KB	.5KB	8KB
Global/MBT	2.3KB	4KB	64KB

=255 tracks*8B

(255*16B = 4KB = STT?)

G-Link to FIC: L1 CFT/PS, L1 Cal

- Little Endian [Alpha] (b0 is LSb, b15 is MSb)
  - send B0 = b0-7 first on FIC
- 2*16 bit frames Glink (B0-1, then B2-3)
  - 16b data in 20b frames; **b16=BEGIN, b17=END**
- 12B header, 4B trailer, then 0 pads [to 16B]
  - last 0 pad or last trailer frame tagged with End
  - 2 B long parity in trailer
  - Use Standard L2 Header/Trailer format
    - as adjusted to address L1CFT concerns
- Timing may force fewer than 47 tracks max

L2 Header REARRANGED!

B0	# objects (NOT IN HEADER)	[note 255 max!]
B1	Header Length in 4B words (1B)	[=3 for default]
B2	Object Length in 4B words (1B)	[ALL same size!]
B3	Header/Trailer Format # (hi 3 bits)	[ONLY changes if new format]
	Object Format # (lo 5 bits)	[ONLY changes if new format]
B4	Data Type # (1B)	[unique in all L2 MBT inputs]
B5	Bunch # (1B)	
B6-7	Rotation# (2B)	[B6 is LSB of rotation]
B8	Algorithm Major Version (1 B)	[e.g. 7 from Version 7.1]
B9	Algorithm Minor Version (1B)	[e.g. 1 from 7.1]
	or Processor Specific Bits (1B)	[esp. if hardware data source]
B10	Processor Specific Bits (1B)	
B11	Error Bits	[b7 on means some error]
		[some standard for L2 Proc]

Standard Status Bits
b7, b1 for all; others if L2proc

7 **error on event (any kind): use at own risk**

6 no processing attempted (none required)

5 object list truncated (any reason)

4 Receiver error on some input physical trailer

3

2

1

0 0 for real data, 1 for MC data

L2 Trailer REARRANGED!

B0 Bunch # (1B) = B5 of Header

B1 Data Type # (1B) = B4 of Header

(Swapped even/odd from Header)

B2 Longitudinal Parity of even Bytes

B3 Longitudinal Parity of odd Bytes

or--if parity too slow to calculate, Turn # (B6-7 of Header)

MBT Out, SLIC, FIC will append physical trailer with 8-bit hardware-generated longitudinal parity

Zero padding to 16 B group FOLLOWS trailer, before End of Event

L2 Physical Trailer

- FIC, SLIC, MBT Out: add a physical 2B trailer
  - after logical trailer, before End Event
    - This BREAKS 16B boundary, but handled by MBT
  - B0 8 bit longitudinal parity of received data
  - B1 Status Bits [b7 on if any receive error]
    - not included longitudinal parity!
    - b0, b1 are type ID: 0 = FIC, 1 = SLIC, 2 = MBT
- MBT inputs place this in B0, B1 of 16B physical trailer
  - adds B14, its own longitudinal parity of everything received
  - B15 its own Error Bits [b7 on if any receive error]
  - reserves 4B for incoming, may give error locations in B4-13
  - MBT Outs produce 2B physical trailer like FIC

L1 CFT/PS Headers

- Standard, Except:
  - L2CFT input has header length = 4
    - 4B extra to pass track counts in each bin
  - FPS has object length = 2
    - 6B per cluster min needed, so send 8B per cluster
- Pt organized like a signed byte:
  - MBS: sign next Pt Bin
  - next extended pt or cluster
- Q for Rob'n'Roger:
  - fmt numbering by source, not system-wide?

L2G Header/Trailer

- Mu raw data from SLIC after trailer
  - Unbiased Sample and Forced Write events
  - doesn’t really fit single-object-size format
  - tagged in processor-specific bits

Endian-ness and Unpacking

- So Far, spec covers only getting into Alpha memory
- Work has started on understanding how this propagates to L3 and offline

FIC

- Construction based on VTM
  - requires modified Magic Bus backplanes
- VME for monitoring, control, testing
- L1 Busy hand-wired “bus”
  - open collector to pilot MBT (also for SLIC?)
  - allows simple reframing of G-link
- Cypress End Event = 2 (5?) Pad, then END?
- FIFOs smaller: 8KB
- Use FIC’s for L2CAL as well!
- 1st early Feb; 2-3 at FNAL April/early May

G-link for FIC

- L1CFT and L1Cal
- FF0/FF1 alternating at 5ms during idles?
  - Would be ideal for re-synch of G-link
  - probably just sending FF1
- For Error analysis:
  - few or no pads in transmission

Cypress Control Chars: What is 1 bit away? (Renardy)

- 1 control char: K28.3
  - *PROPOSE: Use as END instead of K23.7?*
  - *Discuss with ECB?*
- 2C: K28.0 [BEGIN], K28.7
- 3C: K28.4
- 2Data: K23.7 [END], K27.7, K29.7, K30.7
- 3D, 1C: K28.1, K28.2
- 3D, 2C: K28.5 [PAD!], K28.6

other 1-bit errors generate violations

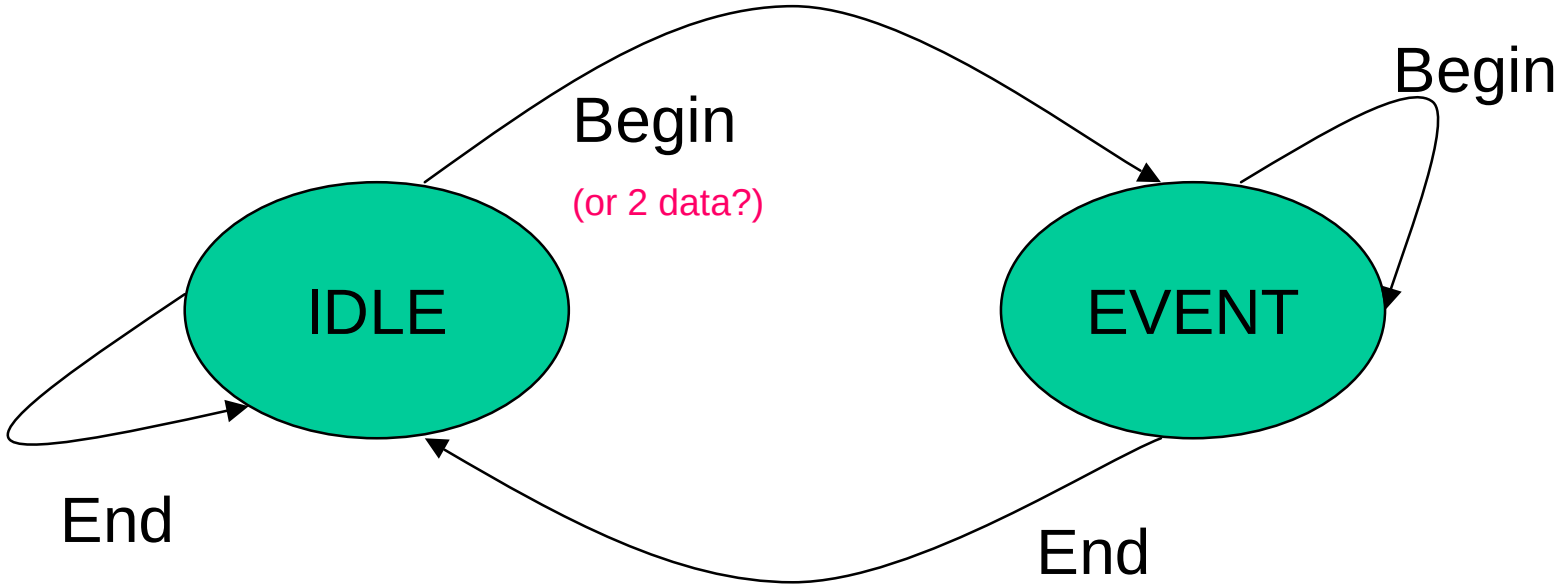
Cypress Assumptions

- enough time to send/decode 2 special chars
- good error detection (74% of states are invalid)
  - adapt recovery to this
- Reframe in ~ 5 characters (.3 μsec)
  - fast enough for between events
- Reframe if 2 consecutive errors
  - rather than always reframing

Reframing Cypress: On Provocation model

- During Reframing:
  - no data into FIFO
  - stays in reframe until successful (identifies Pad)
    - any benefit of timeout?
  - upstream buffers may fill, generating L1 Busy
  - LED to indicate reframing? Counter/flipflop?
    - How to identify channel? Rotary: channel n or ALL?
- Causes of reframing:
  - Powerup
  - n consecutive bad or unknown control char
  - front panel (flipflop?)
  - VME (SLIC, MBT): part of SCL Initialize handling
    - Admin. will hold off clear of L1 Busy: read status

Input state machine



State bit (IDLE/EVENT) is input to FIFO handling logic

Begin Event

- Be sure input fifo correctly aligned
- ready to resume inserting data into FIFO

End Event

- Close up FIFO: stop inserting data
- Mark FIFO with end of event tag
- pad FIFO to 16B? (in case of errors)
  - probably handled by reset on Begin Event
- Add physical trailer recording errors
  - On readout of FIFO

Input during IDLE

- FIFO DISABLED
  - data format insensitive to errors in PAD's
- Pad Ignore (even tho clocked)
- Data count (IDLE errors)
  - 2 consecutive DATA = BEGIN? Probably not...
- Error count
- Special Character:
  - Begin normal start of EVENT (align FIFO)
  - End assume missed Begin
  - any other: count

Input during EVENT

- FIFO ENABLED
  - sensitive to errors in PADS
  - try to preserve data format
- Pad Ignore (even tho clocked)
- Data insert into FIFO
- Error insert into FIFO, tag ERROR
- Special Character:
  - End: tag End, normal start of IDLE
  - Begin: assume missed End
  - other: insert into FIFO, tag ERROR (?)

Event Synch Error Handling

- Mismatch of event tags between channels
- Only SLIC or Alpha can notice
  - irrelevant for MBT, FIC
- Only Administrator Alpha Handles:
  - requests Pilot MBT to set ERROR1 in SCL
  - This will provoke SCL_INITIALIZE
    - kills which buffers: 1 kills FE L2 decision, 2 kills L3 R/O?
- How does SLIC notify Administrator Alpha?
  - L2 Header status bit is sufficient
    - no gain for “immediate” notify via say special character
    - no guarantee it’s going to Pilot MBT anyway

Error Handling Strategy

- Confine errors to single event, single channel
  - missing an event boundary: event synch error
    - only SCL_INITIALIZE will clear this
- count errors as detected; VME readback
  - FIC can't do this if no VME
  - 1 B lasts 60 ns: no ECL scaler gate w/o stretching
- no elaborate recovery or detection
  - unless can be FIXED locally
    - and faster, more reliably than operator intervention
  - else: support diagnosis, save evidence
    - data flow hang can usually localize problem

Cypress Self Test

- Excellent for debugging, Bit Error Rate testing
  - transmitter: send sequence of ALL symbols
  - receiver: verify got sequence in order
  - SLIC, MBT: both Xmit and Rcv on board
- Start/stop can’t be special characters!
  - All: VME (or Mbus for MBT)
    - and a front panel flipflop?
  - test point(s) on front panel?
    - Should see a pulse every cycle through test sequence
    - or just an error counter for VME reading

L2-style Geographic Section

- Will propose modification to GS protocols
  - VBD initialization with crate info
    - maybe re-initialize by computer
  - time-stamped record of L1, L2 error declarations
    - handled by “Dallas Chip” in FE sections
    - TCC must be involved for L2
  - L1 busy handling rationale differs
    - busy not guaranteed to halt event flow
    - emphasis on diagnosis, since prevention not guaranteed