#### L2 I/O Transfer

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## L2 Messages (Cypress)

- Length: min = 16B to 4KB max per event
  - includes 12B header and 4B trailer
  - source responsible for padding to multiples of 16B
    - source padding occurs after trailer
      - zeros? Some other pattern?
- FIC and MBT must pass through all events
  - no decisions on event header or tags

#### Cypress special characters

- Start Event is K28.0 (00 Hex)
- Pad characters K28.5 (05 Hex) are ignored
  - except for reframing, see below
  - may occur at any time
  - do NOT appear in FIFO's
- End Event is character K23.7 (08 Hex)
  - PRECEEDED BY 2 Pad Characters
- Fewer the merrier?
  - But it is a communication path, esp. for FIC, SLIC

#### Start Event

- Be sure input fifo correctly aligned
- ready to resume inserting data into FIFO

#### **End Event**

- Close up FIFO: stop inserting data
- Mark FIFO with end of event tag
- pad FIFO to 16B? (in case of errors)
  - Or pad on FIFO read without eating part of next event
- Add 16 B transport trailer recording errors?
  - Or prepare trailer and save it?
  - See later discussion about transport trailer

## Error Handling Strategy

- Confine errors to single event, single channel
  - missing an event boundary: event synch error
    - only SCL\_INITIALIZE will clear this
- count errors as detected; VME readback
  - FIC can't do this: no VME
  - 1 B lasts 60 ns: no ECL scaler gate w/o stretching
- no elaborate recovery or detection
  - unless can be FIXED locally
    - and faster, more reliably than operator intervention
  - else: support diagnosis, save evidence
    - data flow hang can usually localize problem

## Cypress Tramsission Error Detection

- Cypress detects illegal special character
  - almost 3/4 of all possible 10bit frames are invalid
    - 8b data in 10b frame; only a few VALID special chars
- Cypress indicates valid special character
  - receiver must decode them and decide action
    - decoder for each special character defined: minimize
    - usually skip data insertion, kick a state machine
  - What about valid but undefined special character
    - same as illegal special character (but not seen as fast)?
    - or ignore (treat like pad character)
      - fairly rare, since few valid special characters?

#### Action on Transmision Error

- insert 'data' byte in FIFO on first error
  - usually keeps input FIFO correctly aligned
  - fails if pad character is mangled during an event
- Increment channel's error counter (LED?)
- prepare to notify receiver
  - Record in transport trailer? Or just remember?
- begin reframe on second consecutive error?
  - Only in "reframe on provocation" model
  - trash # of bytes of data, misalign input FIFO
  - {pad, pad, end\_event}:
- keep event boundary, avoid SCL\_INITIALIZE
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### Reframing Cypress: On Provocation model

#### • During Reframing:

- no data into FIFO
- stays in reframe until successful (identifies Pad)
  - any benefit of timeout?
- upstream buffers may fill, generating L1 Busy
- LED to indicate reframing? Counter/scaler?
  - How to identify channel? Rotary: channel n or ALL?

#### Causes of reframing:

- Powerup
- 2 consecutive bad or unknown control char
- front panel (flipflop)
- VME (SLIC, MBT): part of SCL Initialize handling
  - Admin. will hold off clear of L1 Busy: read status

#### Reframing Cypress: Continuous model

- ALWAYS in reframe mode
  - after powerup (2048B = 128  $\mu$ sec) requires 2 pads in 5 B
  - Is this secure enough?
- LED to indicate reframe occurred?
   Counter/scaler?
  - How to identify channel? Rotary: channel n or ALL?
- NO control is required: self-correcting
  - no need to count consecutive transmission errors
  - reframes before END\_EVENT
  - reframes between events
  - reframes during SCL\_INIT (link carries pads only)
- IF reframe mid-event, what happens to data?

## Transmission Error Notification: Options

- Don't bother to tell receiver (ugh)
- Status register for each FIFO (queue by event)
  - SLIC DSP can read registers
  - set Bit in output Header for Alpha
- Private line to receiving Alpha (MBT only)
  - wire-or MBUS line, remembered until this event
  - extra PCI read during interrupt routine
  - lose info on which channel had error?
- Transport trailer (16B) on event? (each FIFO)
  - works for ANY of SLIC, FIC, or MBT

#### Transport Trailer?

- Propose reserve sufficient resources
  - Decide if insert in input FIFO or tack onto transfer
- Defer implementation?

### Event Synch Error Handling

- Mismatch of event tags between channels
- Only SLIC or Alpha can notice
  - irrelevant for MBT, FIC
- Only Administrator Alpha Handles:
  - requests Pilot MBT to set ERROR1/2 in SCL
  - This will provoke SCL\_INITIALIZE
    - kills which buffers: 1 kills FE L2 decision, 2 kills L3 R/O?
- How does SLIC notify Administrator Alpha?
  - L2 Header status bit is sufficient
    - no gain for "immediate" notify via say special character
    - no guarantee it's going to Pilot MBT anyway

### Cypress Self Test

- Excellent for debugging, Bit Error Rate testing
  - transmitter: send sequence of all symbols
  - receiver: verify got sequence in order
  - SLIC, MBT: both Xmit and Rcv on board
- No special character in data stream?
  - All: front panel flipflop? (especially FIC: no VME)
  - SLIC: VME
  - MBT: VME/Mbus
  - test point(s) on front panel?
    - Should see a pulse every cycle through test sequence

## Initialization special Character?

- Proposed: Initialization Complete
  - K29.7 (0A Hex)
  - FIC to SLIC, possibly SLIC to MBT
    - channel by channel? What will receiver do with it?
    - FIC is special problem w/o VME interface
    - use one ECL out line to signal this as scaler gate?
  - Is it sufficient to wait, then see event flow hang or provoke SCL Initialize if receivers not ready?
  - Information flow the wrong way?
    - VME register reporting frames all locked
      - let Alpha/TCC read?

# Special Characters for Busy/Free?

- Buffer Busy/ Buffer Free
  - K28.1/K27.7 (01, 09 Hex)
- + try to prevent overflow of input FIFO
  - FIC, SLIC, MBT?
- more characters to recognize
- does it ever get there fast enough?
  - If so, often enough to reduce event synch errors?
  - No guarantee gets to Pilot MBT anyway (2 MBTs)
- new failure modes (noise -> busy)
  - add buffer free to end event sequence?

#### L2G Header/trailer

- 12B Header, 4B Trailer
- Tradeoff:
  - 4B Header word fixed vs.
  - 4B Trailer = one 4B Header word
- Opinions?

#### L2G Header, Trailer Matched

- H1: Length (1B), Format # (2B), Object Length(1B)
- H2: Source(1B), Rotation(2B), Bunch(1B)
- H3: Status(1B), Version(1B), Switches(1B), Nobj(1B)
- Trailer = H2

#### L2G Header, Fixed Word

- H1: Length (1B), Format # (2B), Object Length(1B)
- H2: Nobj(1B), Rotation(2B), Bunch(1B)
- H3: Source(1B),Status(1B),Version(1B),Switches(1B)
- Trailer:Source(1B),Rotation(2B), Bunch(1B)