FIC Monitoring

R. Bernard & J.F.Renardy
CEA/DSM/DAPNIA/SPP

Monitoring Proposal

- Monitoring done in VME
  - periodic read-out of monitoring information from VME.
  - Counter/Latches reset from VME after reading.
- For each input/output channel
  - Error Latches and Error counter
  - Histogram of event number

Error latches

- Latches
  - FIFO full
  - Error counter overflow
  - >16 events in FIFO
  - Protocol error
- Error counter
  - 4 bits counter

Event Number Histogram

- Histogram max event number amongst channels.
- Histogram max event number for sampling period of 2 ms.

Event Number Histogram (2)

- 5 entries
  - 0 event in all channels.
  - 1 event in some channels and 0 event in the others.
  - Less than 3 events in all channels; at least one channel with 2 or more events.
  - Less than 7 events in all channels; at least one channel with 4 or more events.
  - one channel with 8 or more events.

Event Number Histogram (3)

- Updates @ 500Hz
- 12 bits counters.
- Overflow after 8 seconds.
- One overflow latch for each histogram bin.